

## 2N7002KDW-AU

### 60V N-Channel Enhancement Mode MOSFET – ESD Protected

**Voltage**

**60 V**

**Current**

**250mA**

#### Features

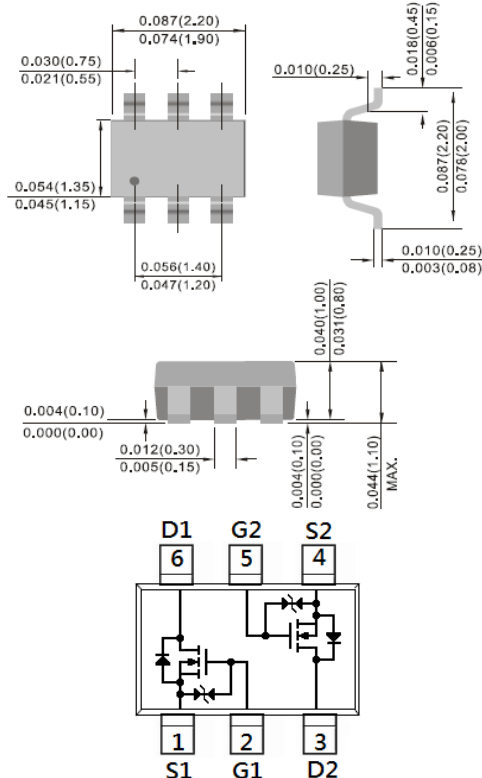
- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@500mA < 3\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@200mA < 4\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc
- ESD Protected 2KV HBM
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

#### Mechanical Data

- Case : SOT-363 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0002 ounces, 0.006 grams

**SOT-363**

**Unit: inch(mm)**



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V <sub>DS</sub>	60	V
Gate-Source Voltage		V <sub>GS</sub>	±20	
Continuous Drain Current		I <sub>D</sub>	250	mA
Pulsed Drain Current		I <sub>DM</sub>	1000	
Power Dissipation	T <sub>A</sub> =25°C	P <sub>D</sub>	350	mW
	Derate above 25°C		4	mW/°C
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55~150	°C
Typical Thermal Resistance		R <sub>θJA</sub>	357	°C/W
- Junction to Ambient <sup>(Note 3)</sup>				



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### Electrical Characteristics ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =10uA	60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA	-	-	3	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =200mA	-	-	4	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =250mA	100	-	-	mS
Dynamic <sup>(Note 5)</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =250mA, V <sub>GS</sub> =5V <sup>(Note 1,2)</sup>	-	0.8	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.35	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.2	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	-	35	-	pF
Output Capacitance	C <sub>oss</sub>		-	13	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	8	-	
Turn-On Delay Time	td <sub>(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =200mA, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω <sup>(Note 1,2)</sup>	-	2.7	-	ns
Turn-On Rise Time	tr		-	19	-	
Turn-Off Delay Time	td <sub>(off)</sub>		-	15	-	
Turn-Off Fall Time	tf		-	23	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>	---	-	-	250	mA
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =200mA, V <sub>GS</sub> =0V	-	0.82	1.3	V

#### NOTES :

- Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .
- Essentially independent of operating temperature typical characteristics.
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
- The maximum current rating is package limited.
- Guaranteed by design, not subject to production testing.

## 2N7002KDW-AU

### TYPICAL CHARACTERISTIC CURVES

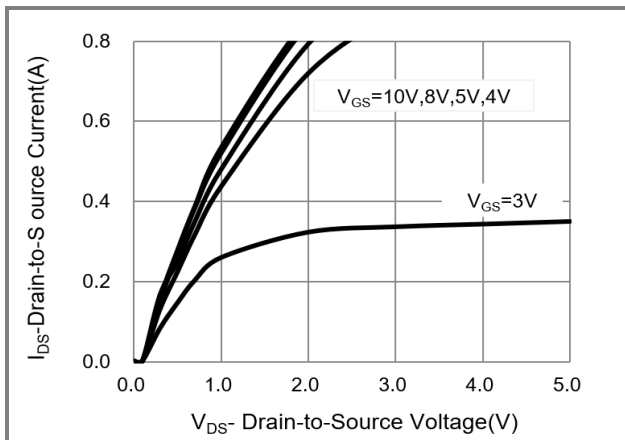


Fig.1 On-Region Characteristics

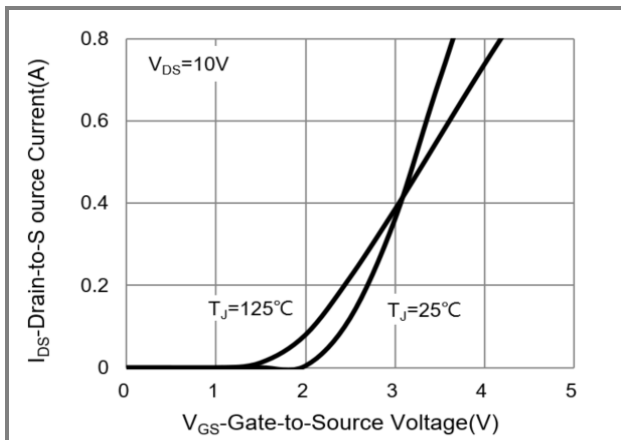


Fig.2 Transfer Characteristics

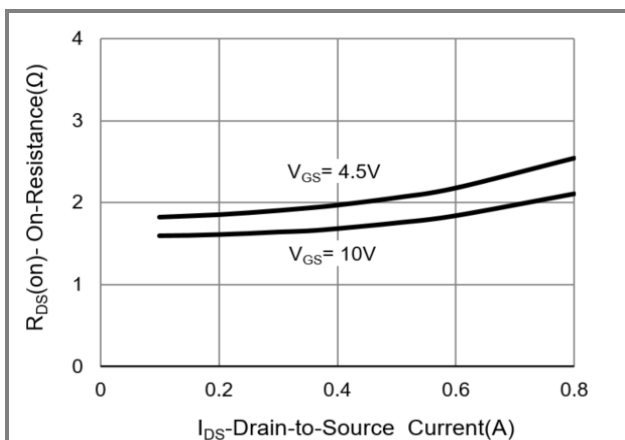


Fig.3 On-Resistance vs. Drain Current

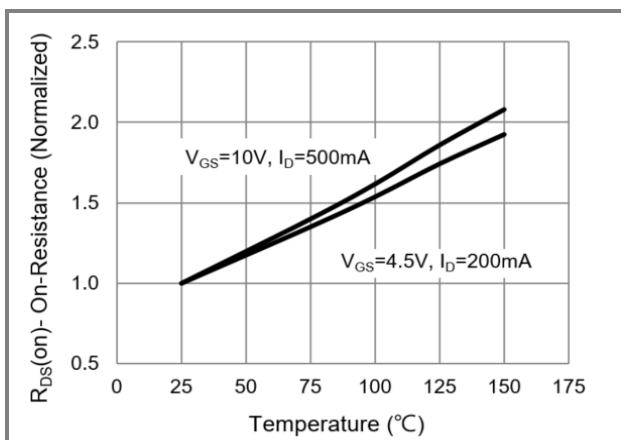


Fig.4 On-Resistance vs. Junction temperature

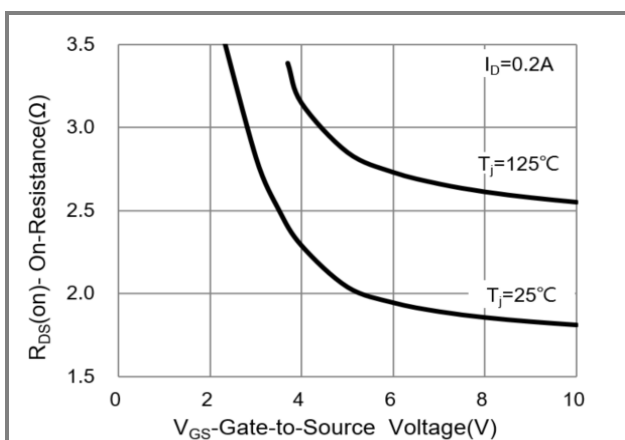


Fig.5 On-Resistance Variation with  $V_{GS}$

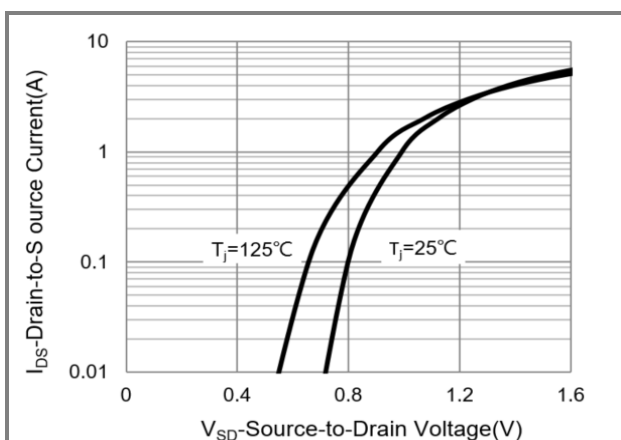


Fig.6 Body Diode Characteristics

## 2N7002KDW-AU

### TYPICAL CHARACTERISTIC CURVES

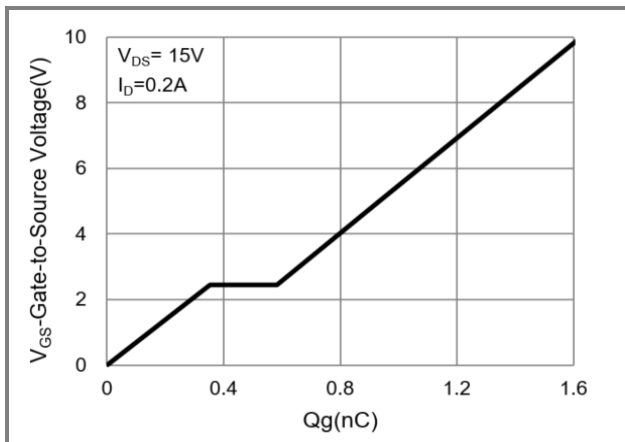


Fig.7 Gate-Charge Characteristics

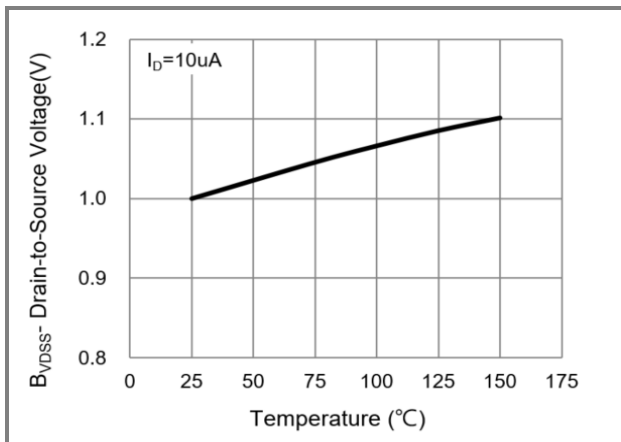


Fig.8 Breakdown Voltage Variation vs. Temperature

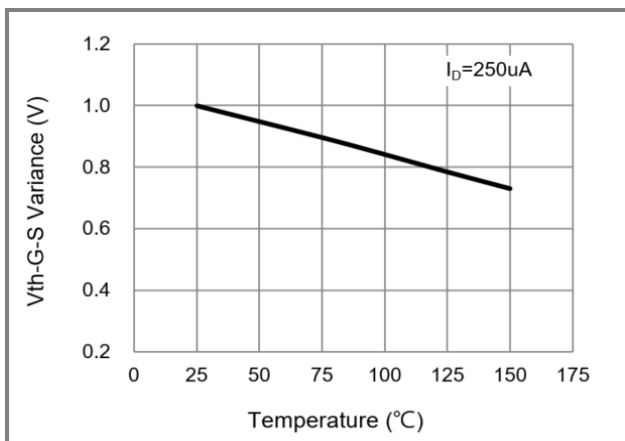


Fig.9 Threshold Voltage Variation with Temperature

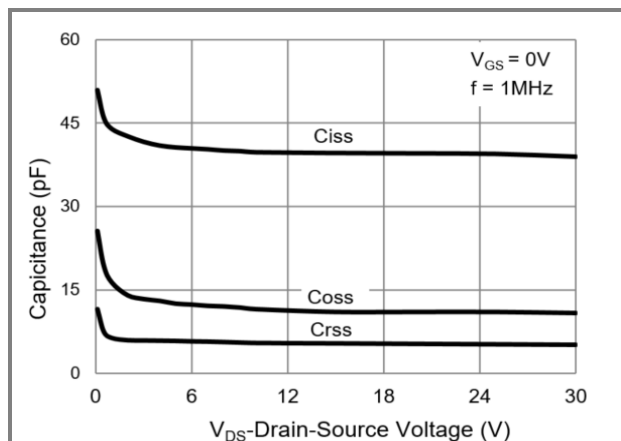


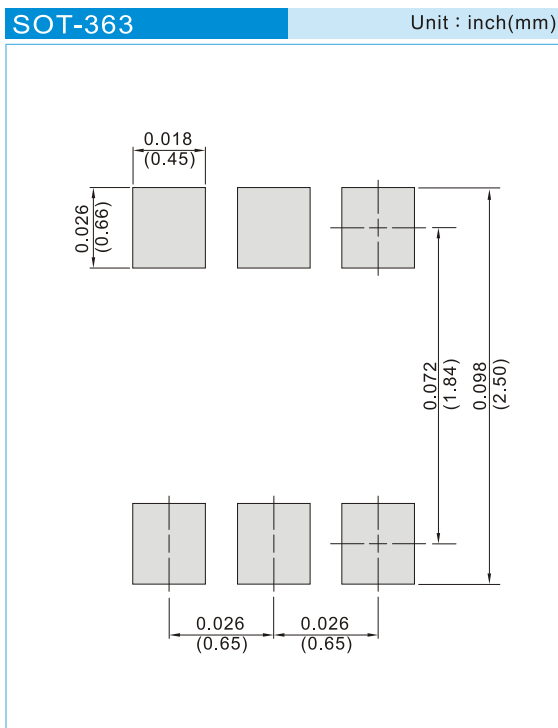
Fig.10 Capacitance vs. Drain-Source Voltage

## 2N7002KDW-AU

### Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
2N7002KDW-AU_R1_000A1	SOT-363	3K pcs / 7" reel	K27	Halogen free

### Mounting Pad Layout





## 2N7002KDW-AU

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