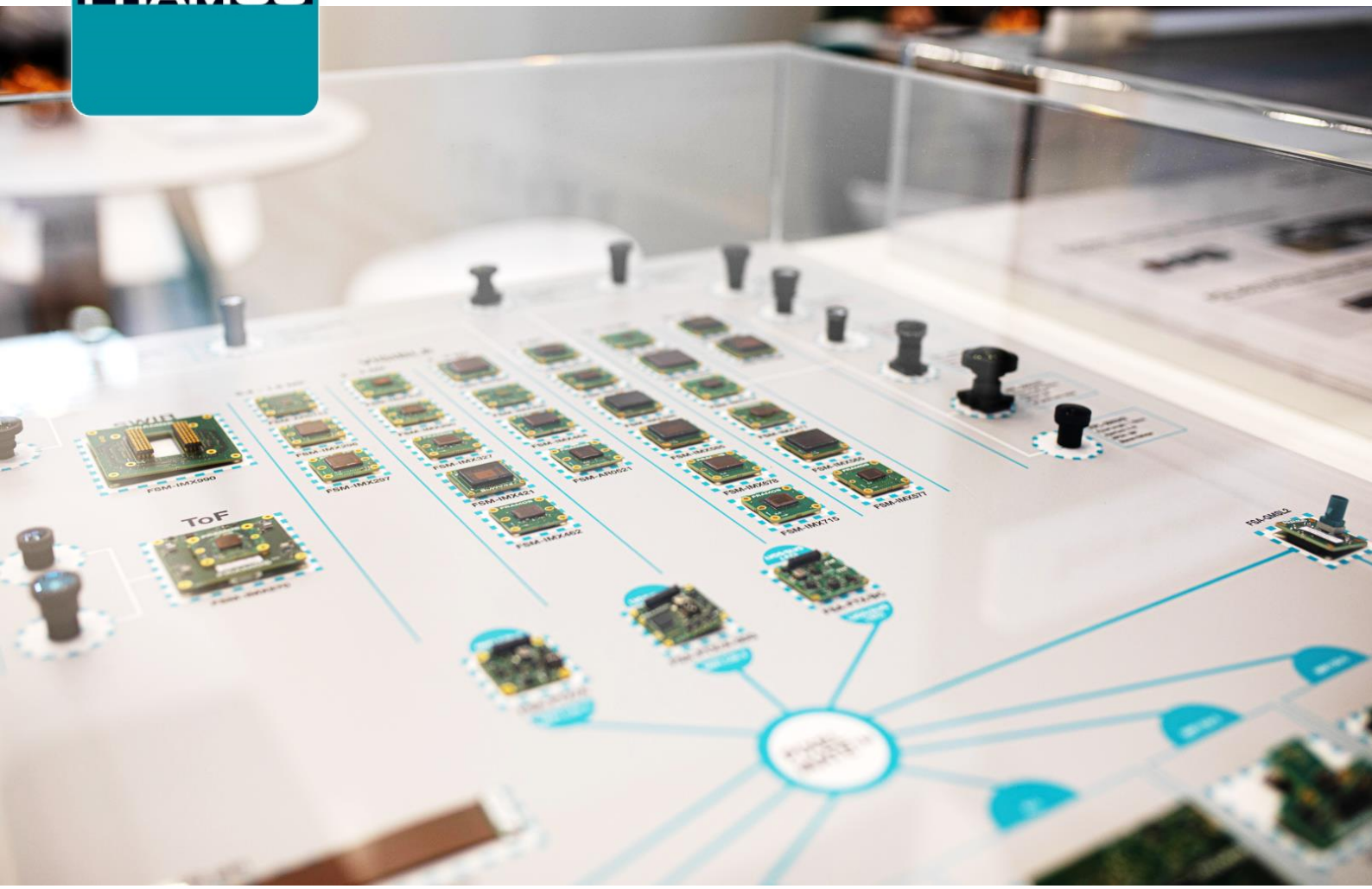

User Manual

Includes the components: FSM* (Generic), FSA*, FFA*, FPA*, FMA*

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Certification and Standards

The equipment described in this document is designed for evaluation and laboratory use, as well as for the integration into electronic devices. The customer is responsible to take all necessary precautions to fulfill regulations and laws of end-customer and target-market applications and to abide to all applicable export control laws.

Non-arms use

FRAMOS is strictly committed to the policy of non-arms use. These products are not designed for military use and it is strictly prohibited to use them in any transaction involving arms. This may include, but is not limited to, using, reselling or otherwise transferring any FRAMOS products to design, develop, manufacture, customize arms, or for use or storage them in military purposes.

Technical Support

The technical equipment described in this document, be it hardware or software, is delivered as-is and does not include any obligations from FRAMOS to provide technical customer support. Technical support is granted on a per-project basis at the discretion of FRAMOS.

ATTENTION
Electrostatic sensitive devices!
Observe precautions for handling!

Handling ESD Sensitive Components

The electronic components like Printed Circuit Boards (PCB) described in this document are sensitive to Electrostatic Discharge (ESD) and need to be handled with high care in static controlled environments. It is strongly recommended to follow the general handling practices for ESD sensitive parts, that include, but are not limited to, the following points:

- Treat all PCBs and components as ESD sensitive.
- Assume that you will damage the PCB or component if you are not ESD conscious
- Handling areas must be equipped with a grounded table, floor mats and wrist strap
- A relative humidity level must be maintained between 20% and 80% non-condensing
- PCBs should not be removed from their protective package, except in a static controlled location
- PCBs must be handled only after personnel have grounded themselves via wrist straps and mats
- PCBs or components should never come in contact with clothing
- Try to handle all PCBs only by their edges, preventing contact with any components.

FRAMOS is not responsible for any damages caused by ESD on customer side.

Optical Sensor Modules and FSM:GO

To safeguard your optical sensor module performance and durability, exercise caution against abrupt changes in temperature or humidity. Condensation risks arise during such fluctuations and may impact the sensor module functionality. Adhering to this advice helps maintain optimal conditions, particularly when using lenses, ensuring a prolonged and reliable sensor module experience.

The FSM:GO optical sensor modules are precision-engineered products, requiring meticulous handling to maintain their high-quality performance. To ensure the integrity of these finely-tuned components, the following handling guidelines must be strictly adhered to:

- Always operate in an Electrostatic Discharge (ESD) safe environment. Personnel should be equipped with ESD-compliant clothing and, when feasible, wear protective gloves to minimize the risk of electrostatic damage to the module.
- Exercise extreme caution when handling the optical module. These are not merely inert objects but sophisticated optical instruments that demand careful and considered treatment.
- When picking up the module, do so by grasping the lens holder or the printed circuit board (PCB). Avoid contact with the lens itself to prevent damage.
- Refrain from exerting any rotational or undue force on the lens. Such actions can misalign the optical elements, compromising the module's performance.
- The front lens element should remain untouched. Contact with the lens surface can lead to contamination or scratches, which could significantly degrade image quality.

Cleaning the Lens Cover

To remove dust from the lens cover, use a pressurized air duster. The air must be free of oil, moisture or other contaminants that could remain on the lens cover. To clean the plastic window of the lens cover, use a small amount of isopropyl alcohol on a cleaning cloth. Do not scratch the plastic window. Do not pour the alcohol directly on the plastic window.

Cleaning the module

To clean the outside of the reader housing, use a small amount of isopropyl alcohol on a cleaning cloth. Do not pour the cleaner directly onto the module.
CAUTION: Do not attempt to clean any products with harsh or corrosive solvents, including lye, methyl ethyl ketone (MEK) or gasoline.

By following these handling instructions, you will preserve the functional integrity and optical clarity of your FSM:GO module, ensuring optimal performance in your vision applications.

Life support applications

These products are not designed for use in life support systems, appliances or devices where malfunction of the products can reasonably be expected to result in personal injury. Customers, Integrators and End Users using or selling these products for use in such applications do so at their own risk and agree to fully indemnify FRAMOS for any damages resulting from any improper use or sale.

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Contents

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1 Introduction

FSM Ecosystem

The FSM Ecosystem consists of FRAMOS Sensor Modules, Adapters, Software and Sources, and provides one coherent solution supporting the whole process of integrating image sensors into embedded vision products.

During the evaluation and proof-of-concept phase, off-the-shelf sensor modules with a versatile adapter framework allow the connection of latest image sensor technology to open processing platforms, like the NVIDIA Jetson Family or the 96boards.org standard. Reference drivers and sample applications deliver images immediately after installation, supporting V4L2 and an optional derivate API providing comfortable integration. Within the development phase, electrical design references and driver sources guide with a solid and proven baseline to quickly port into individual system designs and extend scope, while decreasing risk and efforts.

FSM:GO

The introduction of the FSM:GO series further enhances the FSM Ecosystem by offering an optimized, ready-to-use solution for volume production. The FSM:GO series comprises compact, integrated single-board sensor modules that deliver superior image quality and are meticulously engineered for high-volume deployment. These modules are designed to meet the industry's growing demand for efficient, high-performance imaging systems that can be easily integrated into a wide range of applications.

Off-the-Shelf Hardware

- **FRAMOS Sensor Modules (FSM)** from stock, ready for evaluation and prototyping
- Versatile adapter framework, allowing flexible testing of different modules, on different processing boards.
- **FRAMOS Sensor Adapter (FSA):** Everything needed for specific sensor operation
- **FRAMOS Sensor Modules:GO (FSM:GO**) Offers integrated single-board design, tailored for volume production, removing the need for FSA, and streamlined for easy evaluation, prototyping, and sensor integration and deployment in embedded vision applications.
- **FRAMOS Processor Adapter (FPA):** Connect up to four FSM + FSA or FSM:GO to a specific processor board
- From lenses, mechanics and cables, all necessary imaging accessories are available from a single source

Kickstart Software Package

- Drivers with basic sensor integration
- V4L2 drivers for specific image sensors
- Platform specific device tree overlays
- Streamlined V4L2 library (LibSV) with comfortable and generic C/C++ API
- Example applications demonstrating initialization, configuration and image acquisition

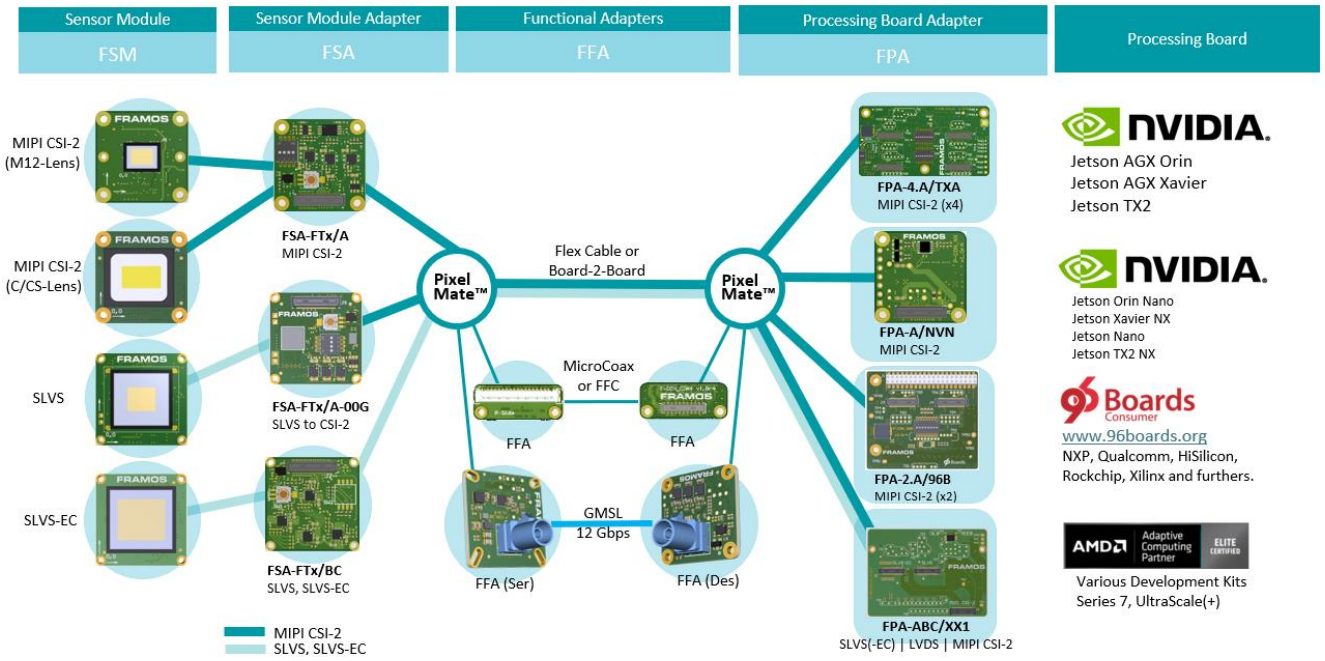
Further to the off-the-shelf hardware and software, the Ecosystem supports you on a project basis with:

- Driver sources, allowing the focus on application specific scope and sensor features
- Electrical references for FSA and FPA, supporting quick and optimized embedding of FSMs
- Engineering services via FRAMOS and its partners, allowing you to focus on your product’s unique value

1.1 Ecosystem Overview

FSM Ecosystem

The figure below shows a map of compatibility with all components inside the Ecosystem. Every element (or hardware) and connection displayed in **Blue** operates with native MIPI CSI-2 (D-PHY) data.



Every component and connection displayed in Teal operates with proprietary (SLVS) or standardized (SLVS-EC) LVDS data, that requires further attention to the physical processing of the image data by either data conversion or specific FPGA IP. Users of MIPI CSI-2 based processing systems are supported by FSM specific data conversion located on dedicated FRAMOS Sensor Adapters (FSAs).

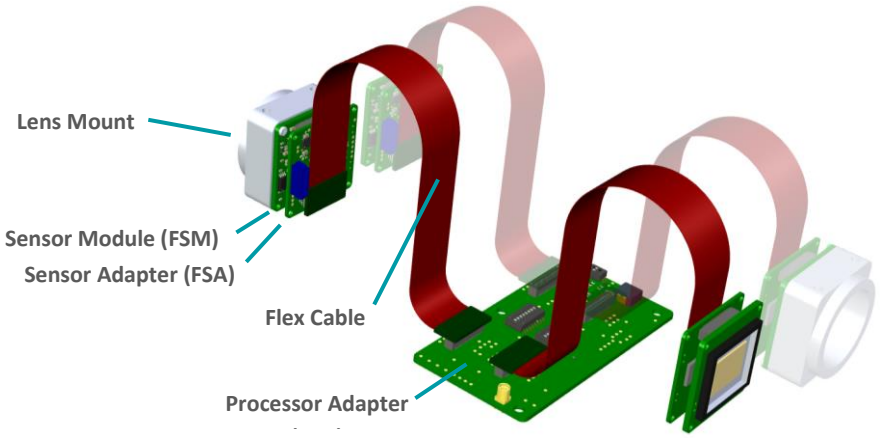
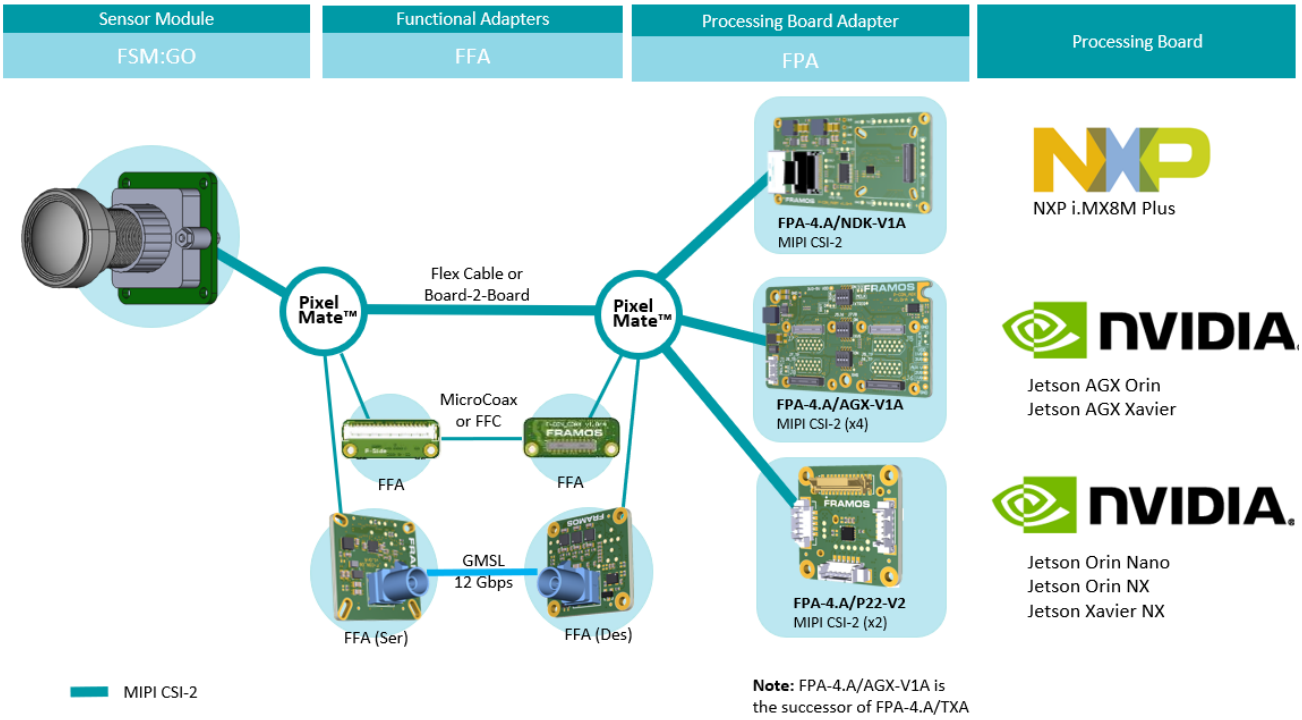


Figure 1: Assembly of a typical Sensor Module Development Kit

Specification and compatibility of all individual components are listed in the appropriate chapter of this User Manual. Access to software and drivers is only granted with the purchase of the appropriate development kit. Electrical design sources, support and services are provided on an individual basis, they are not part of the development kit or a standard component purchase.

FSM:GO

The figure presented illustrates the compatibility landscape within the Ecosystem, highlighting all the components designed to interface with the FSM:GO series. Each element and interconnection depicted in blue is configured to operate using the native MIPI CSI-2 (D-PHY) data.



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1.2 Compliances

CE Declaration

This equipment is in compliance with the essential requirements and other relevant provisions of the following RoHS Directives: Directive 2011/65/EU and (EU) 2015/863.

RoHS

The RoHS Directive (RoHS = Restriction of Hazardous Substances) complements the WEEE Directive by severely restricting the presence of specific toxic substances in electronic equipment at the design phase, thereby reducing the environmental impact of discarding such products at the end of their useful life. FRAMOS is committed to complying with this Directive and has worked in collaboration with its suppliers to evaluate the new restrictions, to identify relevant exemptions, and to substitute environmentally benign, compliant alternative materials in its product components and manufacturing processes. Subject to the available exemptions, FRAMOS. products were compliant with the RoHS Directive for its products.

Materials declarations comply with EN 63000:2018 requirements for RoHS Technical Documentation.

EU Declaration of conformity according to RoHS are issued on customer demand.

REACH

FRAMOS does neither manufacture nor import chemical substances. FRAMOS is well aware of:

- the requirements of REACH regulation of the European Council (EC) No. 1907/2006.,
- the SVHC Candidate List,
- our obligations concerning safety data sheets as well as informing customers.

WEEE

The WEEE Directive obliges manufacturers, importers, and/or distributors of electronic equipment to label the equipment for recycling and to provide for recycling of the electronic equipment at the end of its useful life. FRAMOS is committed to complying with the WEEE Directive (as implemented in each EU member state). In accordance with the requirements of the WEEE Directive, FRAMOS has labelled its electronic products that are shipped. The WEEE label and instructions for disposal are as follows:

Instructions for disposal of waste equipment by users in the European Union

This symbol on the product or its packaging indicates that this product must not be disposed of with other waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of electrical waste and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your consumer waste equipment for recycling, please contact your local city recycling office or the dealer from whom you originally purchased the product.

Electro Magnetic Compliance (EMC)

The FRAMOS Sensor Module Ecosystem are OEM components / devices and provided board level. Electrical components with no or open housings do not comply with standards for electromagnetic compatibility (EMC), as the unshielded circuitry enables electromagnetic interference with other electronic devices.

Users who integrate components of the FRAMOS Sensor Module Ecosystem into their systems are obliged to perform appropriate testing regarding electromagnetic interference and apply CE conformity.

2 Start-Up Instructions

This chapter provides a general example of the hardware assembly procedure. Note that the actual setup may differ in appearance depending on the components used. However, the primary steps, rules, and cautions apply to every system.

2.1 Hardware Assembly

All development kits (Devkits) come pre-assembled.

FSM Ecosystem
It is only necessary to connect the FSM, FSA, and Flex Cable assembly to the FPA and attach it to the appropriate Processor Board.

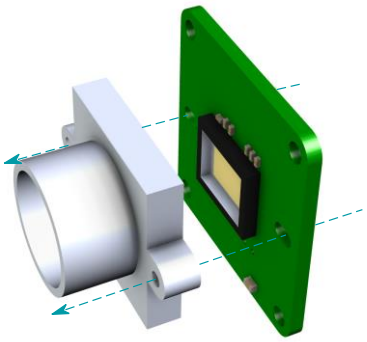
FSM:GO
It is only necessary to connect the FSM assembly to the FPA and attach it to the appropriate Processor Board.

Required Materials
FRAMOS Sensor Module Development Kit or individual components. Note that '**X**' represents a placeholder value for the specific product code you may be using:

- FSM-IMX**XXX**
- FSM:GO-IMX**XXX**
- FSA-FT**XX**/A
- FPA-**XXXXXX**
- FMA-FC-150/60-**XXXX**
- M12 lens mount (optional)

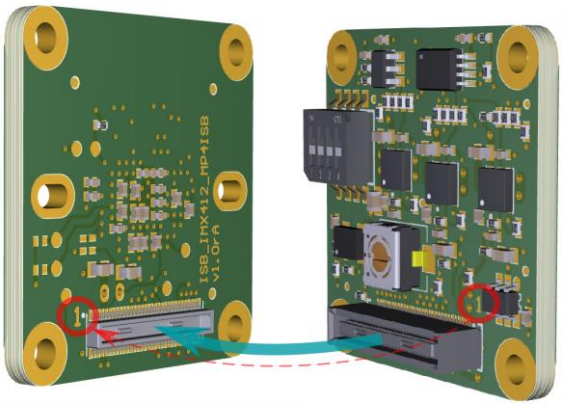
Note: Due to manual alignment requirements for back focal distance and position, C/CS-mounts are frequently shipped already attached to the FSM.

1. Add M12 lens mount (optional)
Prior to assembling the FSM to the FSA, screw an optional M12 lens mount to the FSM.



Fitting screws are provided with the lens mount. If assembling a third-party mount, refer to the technical drawings for the specific module to confirm the hole diameters and select the appropriate fitting screws.

2. Connect FSM and FSA
Connect the FSM to the FSA by pressing the two 60 pin connectors together. Watch carefully for the correct connector orientation and the match of both "Pin1" to "Pin1".



Fix the mechanical connection by using the provided screws with distance holders and nuts between both boards. In the case of a C/CS-mount, screw the board stack into the lens mount mechanics instead of using the nuts.

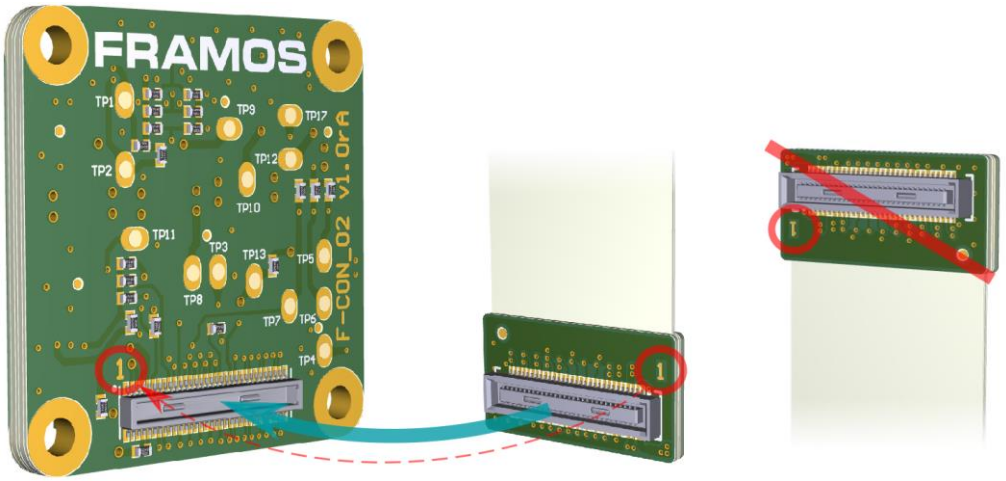
Note: Skip this step if you are working with FSM:GO sensor module as it doesn't require to be connected to FSA.

3. Add Flex Cable

FSM Ecosystem

Connect the FSM, FSA stack via the connector on the rear side of the FSA to the appropriate side of the FMA-FC-150/60 flex cable.

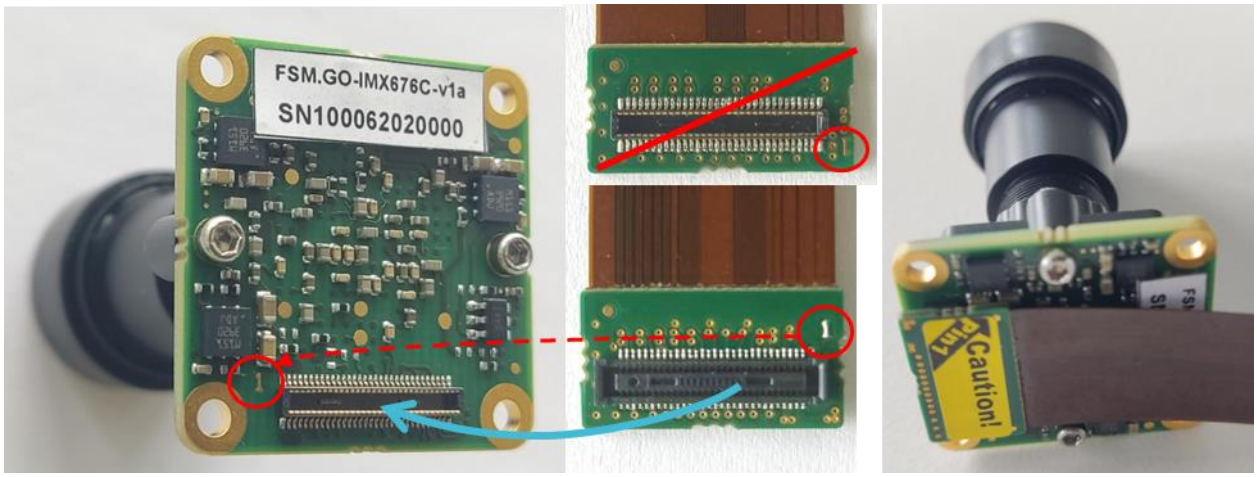
Note: Skip this step if you are going to connect a "piggy-back" FPA like the FPA-A/NVN.



Warning: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of the FSM, Adapters or the Processor Board.

FSM:GO

Connect the rear side of the FSM:GO module to the appropriate side of the FMA-FC-150/60 flex cable by pressing the two 60-pin pixelmate connectors together. Ensure the correct orientation by matching pin-1 on both connectors before securing the connection.



4. Connect to FPA and Processor Board

Proceed according to the Devkit type you purchased:

- 4.1 FSM- **XXXXXXX** **/NVN-Devkit**
- 4.2 Others – Example: FSM-**XXXXXXX**/**TXA-Devkit**
- 4.3 FSM:GO – **XXXXXX**/P22-Devkit

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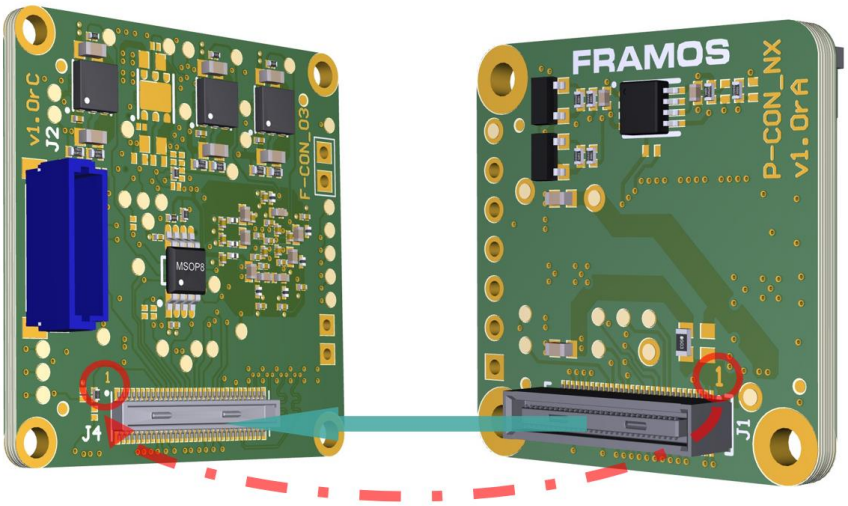
4.1 FSM-xxxxxxx/NVN-Devkit (FPA-A/NVN)

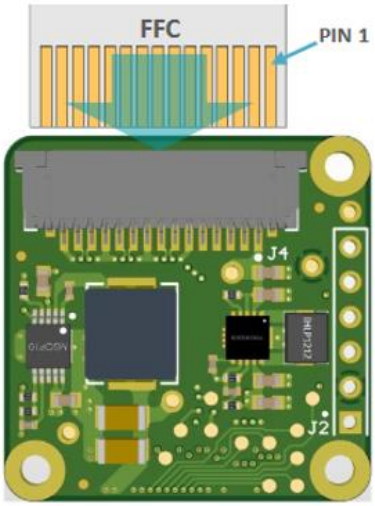
a) Connect FSA to FPA

Connect the FSA to the FPA by pressing the two 60 pin connectors together. Watch carefully for the correct connector orientation and the match of both "Pin1" to “Pin1”.



b) Add Flex Cable

Add the cable to the FSM-FSA-FPA stack. Make sure to set the cable in the connector with the proper orientation.

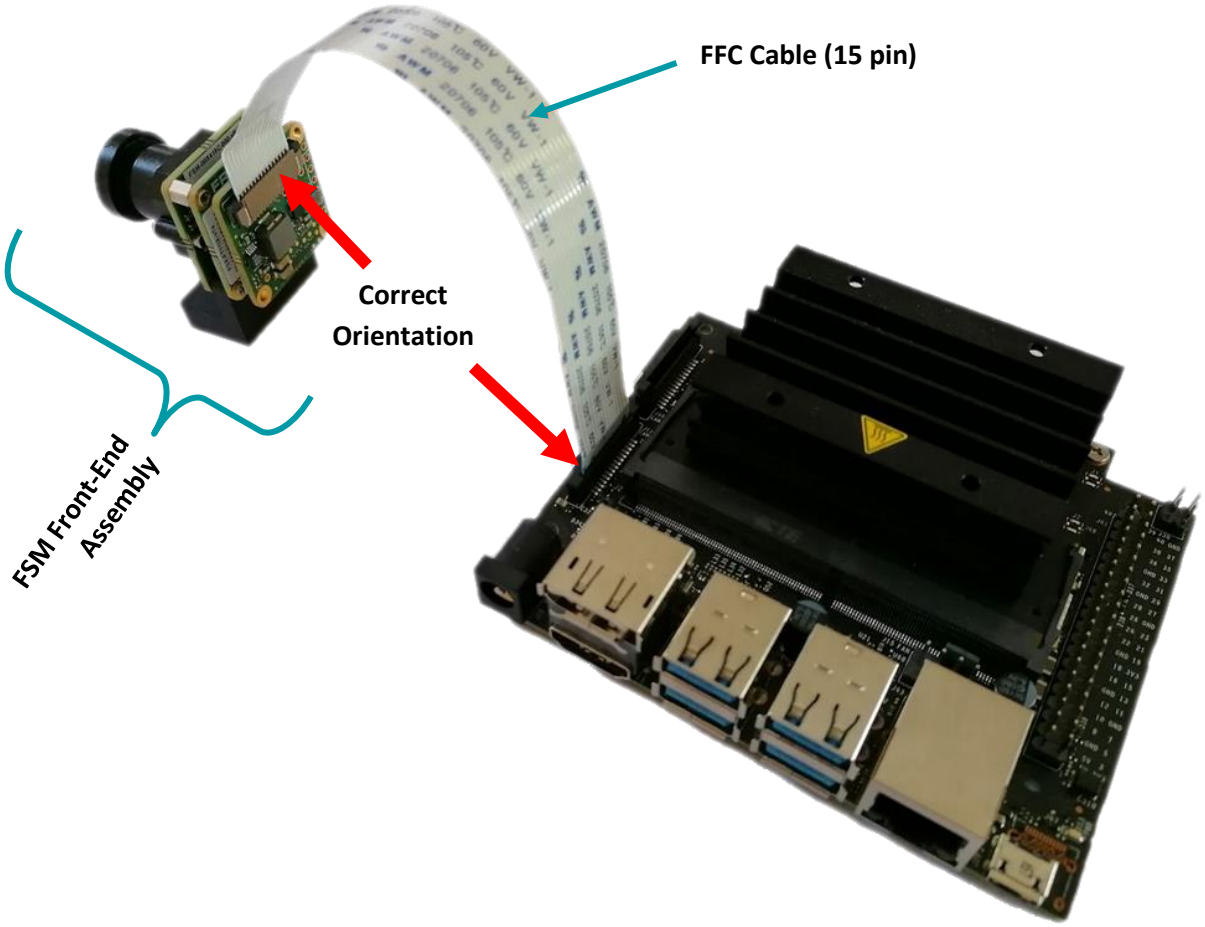


Connect the FSM, FSA and FPA stack via flex cable to the appropriate connector of the Jetson Nano/Xavier NX.

Warning: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board.

c) Final Assembly

Remove the power supply of the carrier board and connect the complete assembly. Power up the processing board and start the software setup.



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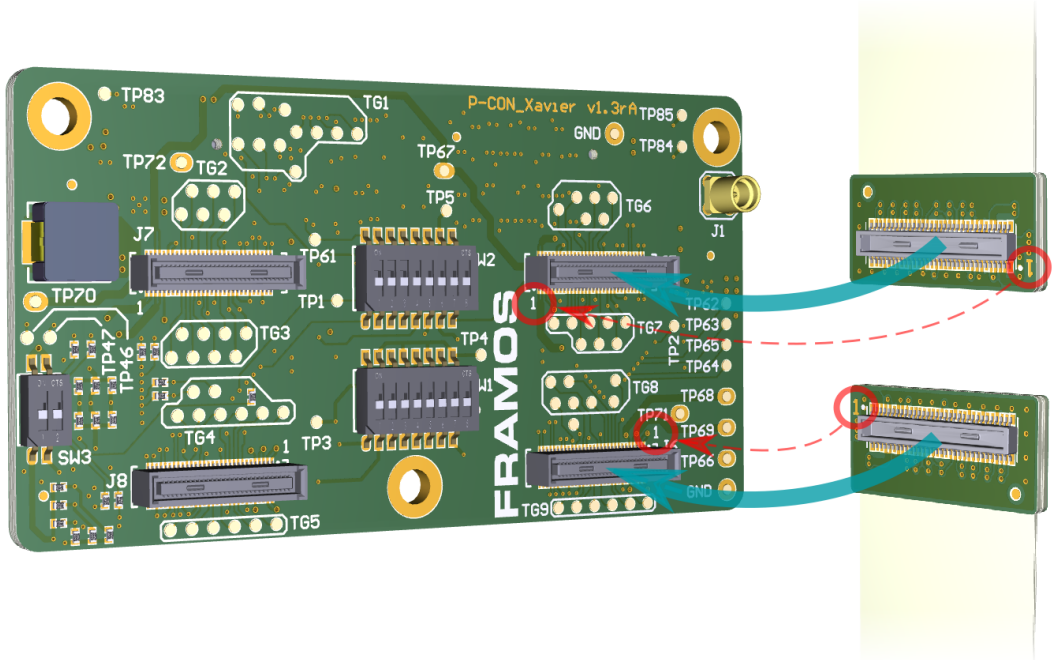
4.2 Other Devkits – Example: FSM- XXXXXXX /TXA Devkit (FPA-4.A/TXA)

a) Connect FSA to FPA

Connect the other side of the flex cable to a sensor connector on the FPA. According to the available sensor interface count, multiple FSM+FSA assemblies can be connected.



With processor boards like the NVIDIA Jetson TX2 Development Kit, the FPA provides access to only two MIPI CSI-2 lanes on FSM3 (J7) and FSM4 (J8). This might lead to restrictions in combination with some FSMs. For compatibility, please review the connector description of the specific FPA.

Warning: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board.

b) Finalize Assembly

Remove the power supply of the processor board and connect the complete assembly to the processor board. Follow the guidelines of the processor board manufacturer for the appropriate camera connector.

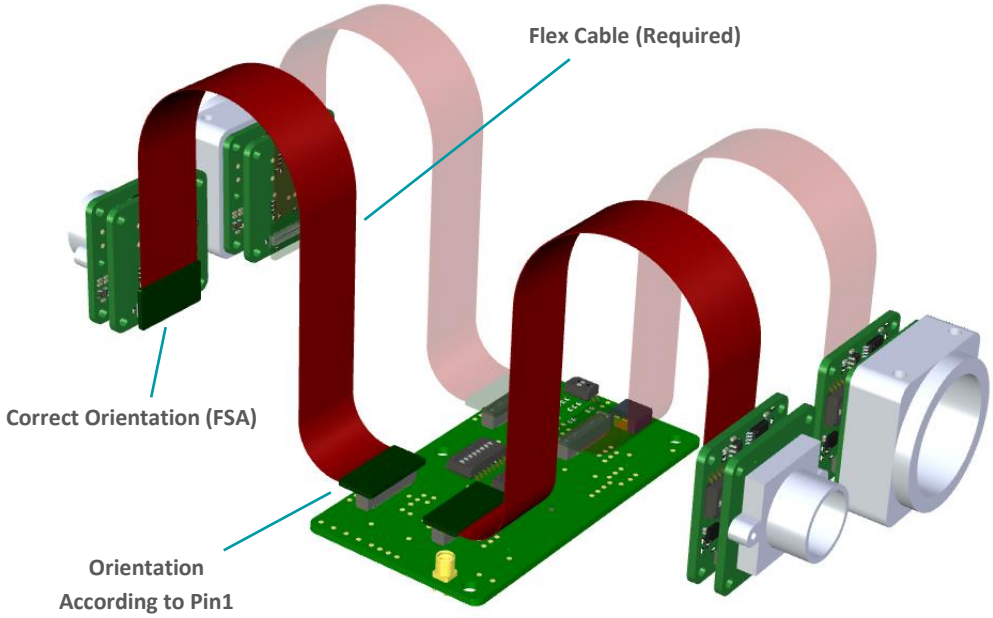


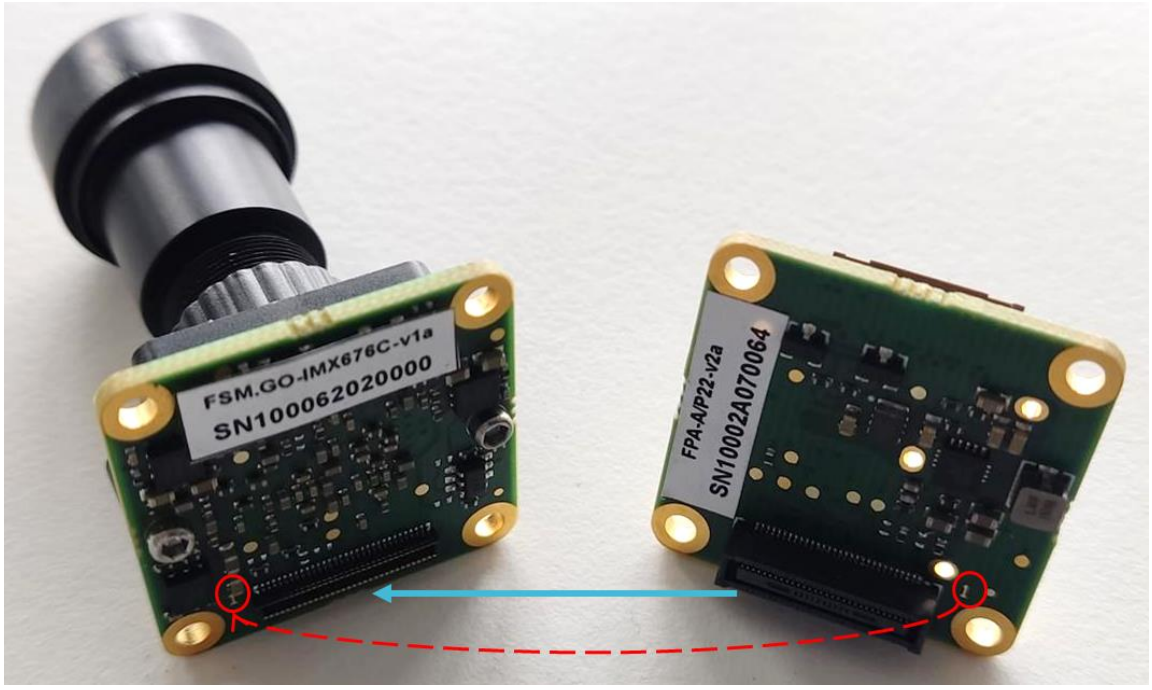
Figure 2: Correct orientation of Flex Cable in an example Multi-Sensor Setup (NVIDIA Jetson)

Power up the processing board and start the software setup.

4.3 FSM:GO – XXXXXX/P22-Devkit (FPA-A/P22-V2A)

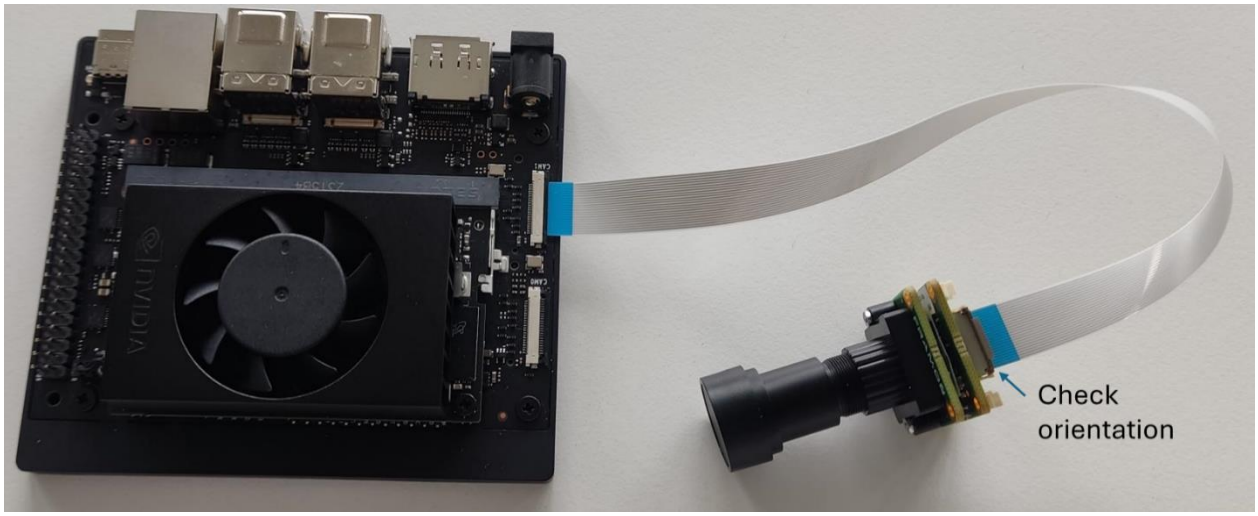
a) Connect FSM:GO to FPA-A/P22-V2A

Connect the rear side of the FSM:GO module to the FPA-A/P22-V2A, by pressing the two 60-pin pixelmate connectors together. Check the connector orientation and match pin-1 of both connectors.



b) Connect FPA-A/P22-V2A to sensor connectors

Connect the FPA-A/P22-V2A to the sensor connectors CAM0/1 of Nvidia Jetson Orin Nano/NX DevKit using FMA-CBL-FFC22.



Warning: Incorrect connector orientation will lead to permanent damage of the FSM:GO module or the processor board

2.2 Software Setup

For instructions on the setup of the target processor board and driver installation procedure, please refer to the "User Guide" included in the appropriate installation package.

The link to the software downloads is part of the development kit package.

3 FRAMOS Sensor Modules (FSM)

The FRAMOS Sensor Modules (FSM) encompass a broad range of high-performance imaging solutions including the FSM+FSA and the for volume optimized FSM:GO series. These modules are engineered to facilitate seamless integration of advanced image sensors into a variety of embedded vision systems. By offering standardized connectivity features such as connector types, pinouts, mechanical formats, and compatible accessories, the FSM Ecosystem delivers unparalleled versatility and ease of use. Whether for initial evaluation, proof-of-concept phases, or scaling up to mass production, FSM provides a flexible and reliable foundation for your imaging requirements. This section delves into the overarching characteristics of the FSM ecosystem and explores the specifics of each module, complemented by detailed datasheets for individual models.

3.1 FSM:GO

The FSM:GO series of optical sensor modules represents a specialized subset within the FRAMOS Sensor Ecosystem, designed to accelerate the deployment of vision systems with an emphasis on ease of use and rapid integration. Built around cutting-edge image sensor technology, FSM:GO modules are preconfigured with optimal lens pairings and precision focus options to cater to specific application demands. The plug-and-play nature of these modules, combined with FRAMOS's quality calibration, ensures that they are not only ready for immediate deployment but also finely tuned for exceptional performance in a wide array of vision applications. The ensuing subsection provides an introduction to the unique attributes and capabilities of the FSM:GO modules, guiding users toward selecting the perfect vision solution.

3.2 FSM+FSA

The FRAMOS Sensor Modules are printed circuit boards, interfacing various types of image sensors with standardized connectivity like connector type, pinout, mechanical format and compatible accessories. The goal of this is to provide various sensor boards that can be used “off the shelf” to connect a variety of image sensors to a host system. Starting from evaluation and proof-of-concept, but also in mass production where adjustments to actual needs are easily possible.

The following chapter provides information on the generic attributes as well as the individual modules, in addition to the individual FSM datasheets.

Common Specification
In general, FSMs are differentiated by two main attributes:

- Image sensor size dependent mechanical footprint (26.5 mm, 28 mm)
- Data interface type specific pinout (MIPI CSI-2, LVDS)

All image sensor signals are routed directly from sensor to the 60-pin connector. All passives visible on the PCB decouple the various power loads of the image sensor. Please refer to the appropriate image sensor documentation for further information.

3.2.1 Portfolio Overview of Sensor Modules

The portfolio of sensor modules includes several FSMs, which are listed with their main attributes on the following pages:

- Native MIPI CSI-2 Modules – Global Shutters
- Native MIPI CSI-2 Modules – Rolling Shutters
- Sub-LVDS, SLVS and SLVS-EC Modules

These attributes describe the individual FSMs without any additional hardware like FSA or FPA. They are defined by the integration of the bare image sensor and are not manipulated or preprocessed in any way.

3.2.1.1 Native MIPI CSI-2 Modules

Global Shutters

Model Name	FSM-IMX297	FSM-AR0144	FSM-IMX296	FSM-HDP230	FSM-IMX568	FSM-IMX565
Shutter Type	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter
Technology	Pregius (Gen2)(Bin)	-	Pregius (Gen2)	-	Pregius S (Gen4)	Pregius S (Gen4)
Resolution [MP]	0.4	1	1.6	2.3	5.1	12.3
Resolution [HxV]	728 x 544	1280 x 800	1456 x 1088	1944 x 1204	2472 x 2064	4128 x 3008
Max. Framerate [FPS]	120.9 FPS (1-Lane)	60.3 FPS (2-Lane)	60.4 FPS (1-Lane)	59.9 FPS (4-Lane) 59.9 FPS (2-Lane)	96.2 FPS (4-Lane) 51.7 FPS (2-Lane)	42.6 FPS (4-Lane) 22.3 FPS (2-Lane)
Mono / Color	Mono	Color / Mono	Mono	Color / Mono	Color / Mono	Color / Mono
Sensor Manufacturer	Sony	onsemi	Sony	Pyxalis	Sony	Sony
Sensor Name	IMX297LLR / IMX297LQR	AR0144CSSM / AR0144CSSC	IMX296LLR / IMX296LQR	HDPYX 230-G Mono / HDPYX 230-G RGB	IMX568AAMJ-M / IMX568AAQJ-C	IMX565AAMJ-C / IMX565AAQJ-C
Application / Grade	Sensing	Industrial	Sensing	Automotive	Industrial	Industrial
Optical Format [inch]	1/2.9	1/4	1/2.9	1/2.5	1/1.8	1/1.1
Pixel Size [µm]	6.9 x 6.9	3 x 3	3.45 x 3.45	3.2 x 3.2	2.74 x 2.74	2.74 x 2.74
Pixel Bitdepth [bit]	10 bit	10 / 12 bit	10 bit	8 / 10 / 12 / 14 / 16 bit	8 / 10 / 12 bit	8 / 10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	1	1 / 2	1	2 / 4	2 / 4	2 / 4
Communication Interface	I²C (4-wire serial)	I²C	I²C (4-wire serial)	I²C	I²C	I²C
Drive Frequency [MHz]	37.125 / 74.25 / 54	6 to 48	37.125 / 74.25 / 54	6 to 27	37.125 / 54 / 74.25 MHz	37.125 / 54 / 74.25 MHz
Input Voltages	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 2.8V	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 2.8V	1.1V, 1.8V, 2.9V, 3.3V	1.1V, 1.8V, 2.9V, 3.3V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	C/CS-Mount option
Board Dimensions [mm²]	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm	26.5 mm x 26.5 mm

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Rolling Shutters (Part 1/4) – up to 5 MP

Model Name	FSM-IMX290	FSM-IMX327	FSM-IMX462	FSM-IMX662
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Technology	Starvis	Starvis	Starvis + NIR	Starvis2
Resolution [MP]	2.1	2.1	2.1	2.1
Resolution [HxV]	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080
Max. Framerate [FPS]	120 FPS (4-Lane) 60 FPS (2-Lane)	60 FPS (4-Lane) 60 FPS (2-Lane)	120 FPS (4-Lane) 60 FPS (2-Lane)	97.8 FPS (4-Lane) 97.8 FPS (2-Lane)
Mono / Color	Color	Color	Mono	Color
Sensor Manufacturer	Sony	Sony	Sony	Sony
Sensor Name	IMX290LLR / IMX290LQR	IMX327LQR1	IMX462LQR-C	IMX662AAQR-C
Application / Grade	Security	Security	Security	Security
Optical Format [inch]	1/2.8	1/2.8	1/2.8	1/2.8
Pixel Size [µm]	2.9 x 2.9	2.9 x 2.9	2.9 x 2.9	2.9 x 2.9
Pixel Bitdepth [bit]	10 / 12 bit	10 / 12 bit	10 / 12 bit	10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	2 / 4	2 / 4	2 / 4	2 / 4
Communication Interface	I^2C	I^2C	I^2C	I^2C
Drive Frequency [MHz]	37.125 / 74.25	37.125 / 74.25	37.125 / 74.25	24 / 27 / 37.125 / 74.25
Input Voltages	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.1V, 1.8V, 3.3V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options
Board Dimensions [mm²]	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5

Version 1.5.0 from 2024-05-23

Rolling Shutters (Part 2/4) – up to 5 MP

Model Name	FSM-IMX464	FSM-IMX335	FSM-AR0521	FSM-IMX675
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Technology	Starvis + NIR	Starvis	-	Starvis2
Resolution [MP]	4.2	5	5	5
Resolution [HxV]	2712 x 1538	2616 x 1964	2592 FSM x 1944	2592 FSM x 1944
Max. Framerate [FPS]	90 FPS (4-Lane) 30 FPS (2-Lane)	60 FPS (4-Lane) 30 FPS (2-Lane)	69 FPS (4-Lane) 34 FPS (2-Lane)	80 FPS (4-Lane) 60 FPS (2-Lane)
Mono / Color	Color / Mono	Color / Mono	Color / Mono	Color
Sensor Manufacturer	Sony	Sony	onsemi	Sony
Sensor Name	IMX464LQR-C	IMX335LLN / IMX335LQN	AR0521SR2M / AR0521SR2C	IMX675AAQR
Application / Grade	Security	Security		Security
Optical Format [inch]	1/1.8	1/2.8	1/2.5	1/2.8
Pixel Size [µm]	2.9 x 2.9	2 x 2	2.2 x 2.2	2 x 2
Pixel Bitdepth [bit]	10 / 12 bit	10 / 12 bit	8 / 10 / 12 bit	10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	2 / 4	2 / 4	2 / 4	2 / 4
Communication Interface	I^2C	I^2C	I^2C	I^2C
Drive Frequency [MHz]	6 to 27 / 37.125 / 74.25	6 - 27 / 37.125 / 74.25	10 to 48	24 / 27 / 37.125 / 72 / 74.25
Input Voltages	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.7V	1.1V, 1.8V, 3.3V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options
Board Dimensions [mm²]	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5

Version 1.5.0 from 2024-05-23

Rolling Shutters (Part 3/4) – 8 MP

Model Name	FSM-IMX334	FSM-IMX485	FSM-IMX585	FSM-IMX678	FSM-IMX415	FSM-IMX715
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Technology	Starvis	Starvis + NIR	Starvis2	Starvis2	Starvis + NIR	Starvis + NIR
Resolution [MP]	8.3	8.3	8.3	8.3	8.4	8.4
Resolution [HxV]	3864 x 2180	3864 x 2180	3856 x 2180	3856 x 2180	3864 x 2192	3864 x 2192
Max. Framerate [FPS]	60 FPS (4-Lane)	72 FPS (4-Lane) 38 FPS (2-Lane)	90.1 FPS (4-Lane) 30 FPS (2-Lane)	72 FPS (4-Lane) 30 FPS (2-Lane)	90 FPS (4-Lane) 44 FPS (2-Lane)	90 FPS (4-Lane) 44 FPS (2-Lane)
Mono / Color	Color / Mono	Color	Color	Color / Mono	Color	Color
Sensor Manufacturer	Sony	Sony	Sony	Sony	Sony	Sony
Sensor Name	IMX334LLR / IMX334LQR	IMX485LQJ	IMX585AAQJ1-C	IMX678AAQR1	IMX415-AAQR	IMX715AAQR1
Application / Grade	Security	Security	Security	Security	Security	Security
Optical Format [inch]	1/1.8	1/1.2	1/1.2	1/1.8	1/2.8	1/2.8
Pixel Size [µm]	2 x 2	2.9 x 2.9	2.9 x 2.9	2 x 2	1.45 x 1.45	1.45 x 1.45
Pixel Bitdepth [bit]	10 / 12 bit	10 / 12 bit	10 / 12 bit	10 / 12 bit	10 / 12 bit	10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	4	2 / 4	2 / 4	2 / 4	2 / 4	2 / 4
Communication Interface	I^2C	I^2C	I^2C	I^2C	I^2C	I^2C
Drive Frequency [MHz]	6 - 27 / 37.125 / 74.25	6 to 27 / 37.125 / 74.25	6 to 27 / 37.125 / 72 / 74.25	6 - 27 / 37.125 / 74.25	24 / 27 / 37.125 / 72 / 74.25	24 / 27 / 37.125 / 72 / 74.25
Input Voltages	1.2V, 1.8V, 2.9V	1.2V, 1.8V, 2.9V	1.1V, 1.8V, 3.3V	1.1V, 1.8V, 3.3V	1.1V, 1.8V, 2.9V	1.1V, 1.8V, 2.9V
Supported Lens Mounts	M12 or C/CS-Mount options	C/CS-Mount option	C/CS-Mount option	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options
Board Dimensions [mm²]	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5

Version 1.5.0 from 2024-05-23

Rolling Shutters (Part 4/4) – equal or higher than 12 MP

Model Name	FSM-IMX412	FSM-IMX577	FSM-IMX477	FSM-AR1335	FSM-IMX283
Shutter Type	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter	CMOS Rolling Shutter
Technology	Starvis	Starvis	Starvis	-	Starvis
Resolution [MP]	12.3	12.3	12.3	13.1	20.2
Resolution [HxV]	4056 x 3040	4056 x 3040	4056 x 3040	4208 x 3120	5496 x 3694
Max. Framerate [FPS]	59.9 FPS (4-Lane) 30 FPS (2-Lane)	59.9 FPS (4-Lane) 30 FPS (2-Lane)	59.9 FPS (4-Lane) 30 FPS (2-Lane)	27.2 FPS (4-Lane) 13 FPS (2-Lane)	24.7 FPS (4-Lane)
Mono / Color	Color	Color	Color	Color	Color
Sensor Manufacturer	Sony	Sony	Sony	onsemi	Sony
Sensor Name	IMX412-AACK	IMX477-AAPK	IMX577-AACK	AR1335CSSM / AR1335CSSC	IMX283CQJ
Application / Grade	Security	Security	Security	Industrial	Audio/Video
Optical Format [inch]	1/2.3	1/2.3	1/2.3	1/3.2	1
Pixel Size [µm]	1.55 x 1.55	1.55 x 1.55	1.55 x 1.55	1.1 x 1.1	2.4 x 2.4
Pixel Bitdepth [bit]	10 / 12 bit	8 / 10 / 12 bit	8 / 10 / 12 bit	8 / 10 bit	10 / 12 bit
Data Interface [Type]	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2	MIPI CSI-2
Data Interface [# Lanes]	2 / 4	2 / 4	2 / 4	2 / 4	4
Communication Interface	I^2C (CCI)	I^2C (CCI)	I^2C (CCI)	I^2C	I^2C
Drive Frequency [MHz]	6 / 12 / 18 / 27	6 to 27	6 to 27	6 to 48	6 to 27
Input Voltages	1.05V, 1.8V, 2.75V	1.05V, 1.8V, 2.8V	1.05V, 1.8V, 2.8V	1.2V, 1.8V, 2.7V	1.2V, 1.8V, 2.9V
Supported Lens Mounts	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	M12 or C/CS-Mount options	C/CS-Mount option
Board Dimensions [mm²]	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5	26.5 x 26.5

Version 1.5.0 from 2024-05-23

3.2.1.2 Sub-LVDS, SLVS and SLVS-EC Modules

Model Name	FSM-IMX264	FSM-IMX304	FSM-IMX530
Shutter Type	CMOS Global Shutter	CMOS Global Shutter	CMOS Global Shutter
Technology	Pregius (Gen2)	Pregius (Gen2)	Pregius S (Gen4)
Resolution [MP]	5.1	12.4	24.5
Resolution [HxV]	2464 x 2056	4112 x 3008	5328 x 4608
Max. Framerate [FPS]	CSI-2: 35.7 FPS (4-Lane)	CSI-2: 23.4 FPS (4-Lane)	SLVS-EC: 106.9 FPS (8-Lane) CSI-2: 30 FPS (4-Lane)
Mono / Color	Color / Mono	Color / Mono	Color / Mono
Sensor Manufacturer	Sony	Sony	Sony
Sensor Name	IMX264LLR / IMX264LQR	IMX304LLR / IMX304LQR	IMX530-AAMJ / IMX530-AAQJ
Application / Grade	Industrial	Industrial	Industrial
Optical Format [inch]	2/3	1.1	1.2
Pixel Size [µm]	3.45 x 3.45	3.45 x 3.45	2.74 x 2.74
Pixel Bitdepth [bit]	12 bit	12 bit	8 / 10 / 12 bit
Data Interface [Type]	SubLVDS	SubLVDS	SLVS, SLVS-EC
Data Interface [# Lanes]	4	4 / 8	1 / 2 / 4 / 8
Communication Interface	I^2C (4-wire serial)	I^2C (4-wire serial)	I^2C (4-wire serial)
Drive Frequency [MHz]	37.125 / 54 / 74.25	37.125 / 54 / 74.25	37.125 / 54 / 74.25
Input Voltages	1.2V, 1.8V, 3.3V	1.2V, 1.8V, 3.3V	1.1V, 1.8V, 2.9V, 3.3V
Supported Lens Mounts	C/CS-Mount option	C/CS-Mount option	C/CS-Mount option
Board Dimensions [mm²]	28 x 28	28 x 28	28 x 28

3.3 The Standard

3.3.1 Mechanical

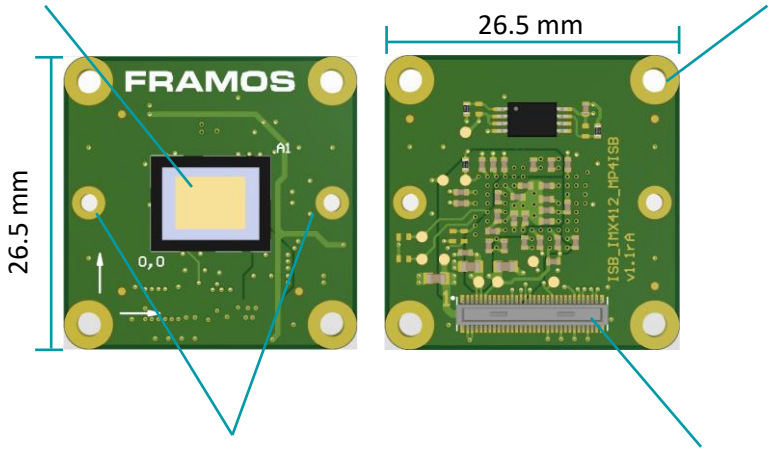
3.3.1.1 Generic 26.5 mm footprint

Various Image Sensors

- Global & Rolling Shutters
- Optically centered to square PCB

4 Mounting Holes

- Reliable mechanical fixing
- C/CS-Mount options



M12 Lens Options

- Default usage of standard mounts
- Customer Specific lens assembly and focusing

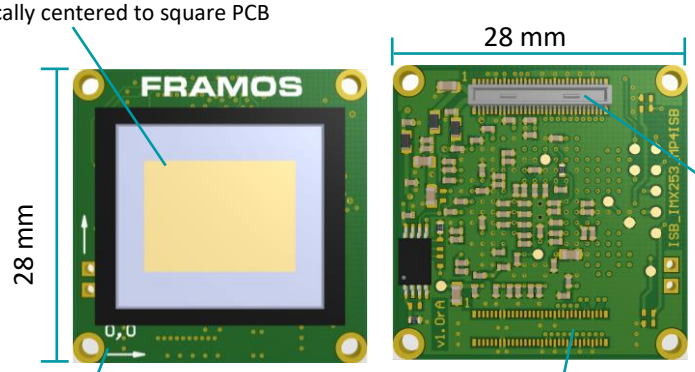
FRAMOS PixelMate™ (C)

- Standardized 60 pin connector and layout
- 4-Lane MIPI CSI-2, D-PHY
- Hirose DF40C-60DP-0.4V(51)
- Bottom position

3.3.1.2 Generic 28 mm footprint

Various Image Sensors ≥2/3”

- Focus on industrial Global Shutters
- Optically centered to square PCB



FRAMOS PixelMate™ (S)

- Standardized 60 pin connector and layout
- Up to 8-Lane sub-LVDS output
- Hirose DF40C-60DP-0.4V(51)
- MIPI CSI-2 converter options
- Top position

4 Mounting Holes

- Reliable fixing
- C/CS-Mount options

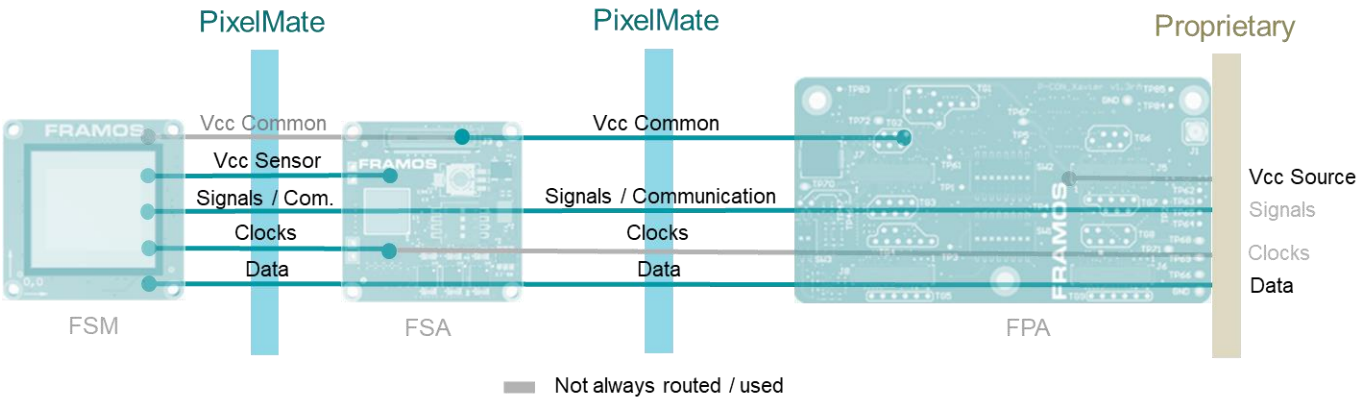
Second Connector Optional

- Hirose DF40C-60DP-0.4V(51)
- Support for 16 Lane LVDS (8+8 Lanes)
- Bottom position

3.3.2 PixelMate™ - Connector Pinouts

The FSM Ecosystem adopts a standard Hirose 60 pin board to board connector supporting 5Gbps and beyond, to connect to all relevant signals from the image sensor.

- Connector Type (All FSM): Hirose DF40C-60DP-0.4V
- Number of Pins: 60 (2 rows á 30 pins)
- Locking: No
- Cable Shielding: Yes
- Connector Shielding: No
- Pinning Layouts:
  - ***PixelMate™ (C)***: MIPI CSI-2
  - ***PixelMate™ (S)***: LVDS, SLVS, SLVS-EC



Actual signals used by the individual FSM is image sensor dependent and may vary.

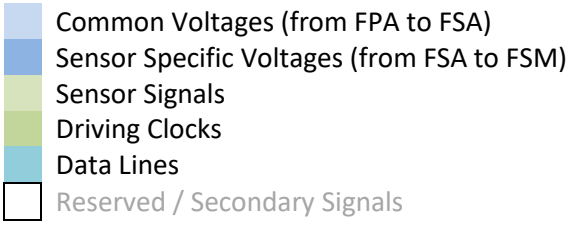
Version 1.5.0 from 2024-05-23

3.3.2.1 PixelMate™ (C) - MIPI CSI-2 Pinout (4-Lane)

This pinout scheme applies to all sensors that natively output image data according to the MIPI CSI-2 standard. As by the definition in the MIPI standard, this layout provides 1x4 or 2x2 data lanes on the connector.

Pin#	Signal	Pin#	Signal
1	3V8	2	1V8
3	3V8	4	1V8
5	V_ANA	6	V_DIG
7	V_ANA	8	V_DIG
9	V_IF	10	V_AUX
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	SPI_MISO	18	SPI_MOSI
19	XMASTER0	20	XMASTER1
21	I2C_0_SCL	22	I2C_1_SCL
23	SPI_CS	24	SPI_SCK
25	XVS0	26	XVS1
27	I2C_0_SDA	28	I2C_1_SDA
29	XHS0	30	XHS1
31	XTRIG0	32	XTRIG1 / FSTROBE
33	PW_EN_0	34	PW_EN_1
35	SLAMODE1	36	SLAMODE2
37	GND	38	GND
39	INCK	40	GPIO4 (MCLK2)
41	MCLK_1	42	GPIO5 (MCLK3)
43	GND	44	GND
45	D_CLK_1_P	46	D_DATA_3_P
47	D_CLK_1_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

Table 1: Standard Pinout of MIPI CSI-2 (4-Lane) interface



The table above shows the position of each signal on the 60-pin connector in case the image sensor provides it. For further details, please refer to the image sensor Datasheet.

Note: The table shows the general signal assignment that applies to all connections using PixelMate™ (C). The signals that are eventually available depend on image sensor and adapter configuration. Please use the *FSM Connector Pinout* from the individual FSM datasheet as reference for the available signals.

3.3.2.2 PixelMate™ (S) - Sub-LVDS, SLVS and SLVS-EC Pinout (8-Lane)

This pinout scheme applies to all sensors that natively output image data using signals according to Sub-LVDS, SLVS or SLVS-EC specification. This layout provides eight data lanes on the connector. Devices with SLVS and SLVS-EC share the same sensor package pins therefore share the same connector pins.

Note: Lane number assignment is applied according to SLVS numbering, which differs in most cases from the SLVS-EC lane numbering. Please refer to image sensor datasheet for correct SLVS-EC numbering.

Pin#	Signal	Pin#	Signal
1	3V8	2	1V8
3	3V8	4	1V8
5	V_ANA	6	V_DIG
7	V_ANA	8	V_DIG
9	V_IF	10	V_AUX
11	GND	12	GND
13	GND	14	GND
15	SDA	16	SCL
17	SDO	18	XCE
19	TOUT0	20	SLAMODE
21	TOUT1	22	XMASTER
23	TOUT2	24	NC
25	NC	26	XTRIG
27	NC	28	XHS
29	NC	30	XVS
31	GND	32	GND
33	RST	34	D_DATA_7_P
35	MCLK	36	D_DATA_7_N
37	GND	38	GND
39	D_DATA_6_P	40	D_DATA_5_P
41	D_DATA_6_N	42	D_DATA_5_N
43	GND	44	GND
45	D_DATA_4_P	46	D_DATA_3_P
47	D_DATA_4_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_2_P	52	D_DATA_1_P
53	D_DATA_2_N	54	D_DATA_1_N
55	GND	56	GND
57	D_DATA_0_P	58	D_CLK_0_P
59	D_DATA_0_N	60	D_CLK_0_N

Table 2: Standard Pinout of LVDS (8-Lane) interface

Common Voltages (from FPA to FSA)
Sensor Specific Voltages (from FSA to FSM)
Sensor Signals
Driving Clock
Data Lines

The table above shows the position of each signal on the 60-pin connector in case the image sensor provides it. For further details, please refer to the image sensor Datasheet.

Note: The table shows the general signal assignment that applies to all connections using PixelMate™ (S). The signals that are eventually available depend on image sensor and adapter configuration. Please use the *FSM Connector Pinout* from the individual FSM datasheet as reference for the available signals.

4 Ecosystem for Native MIPI CSI-2 Image Sensors

The following chapters provide the relevant technical information for sensor modules (FSM) with native MIPI CSI-2 data output.

A setup with single or multiple sensor modules consists of one to four FSMs, each with an appropriate sensor specific FSA, and one FPA for the target processor board. Only FSA and FPA designs shown in this chapter are compatible to each other.

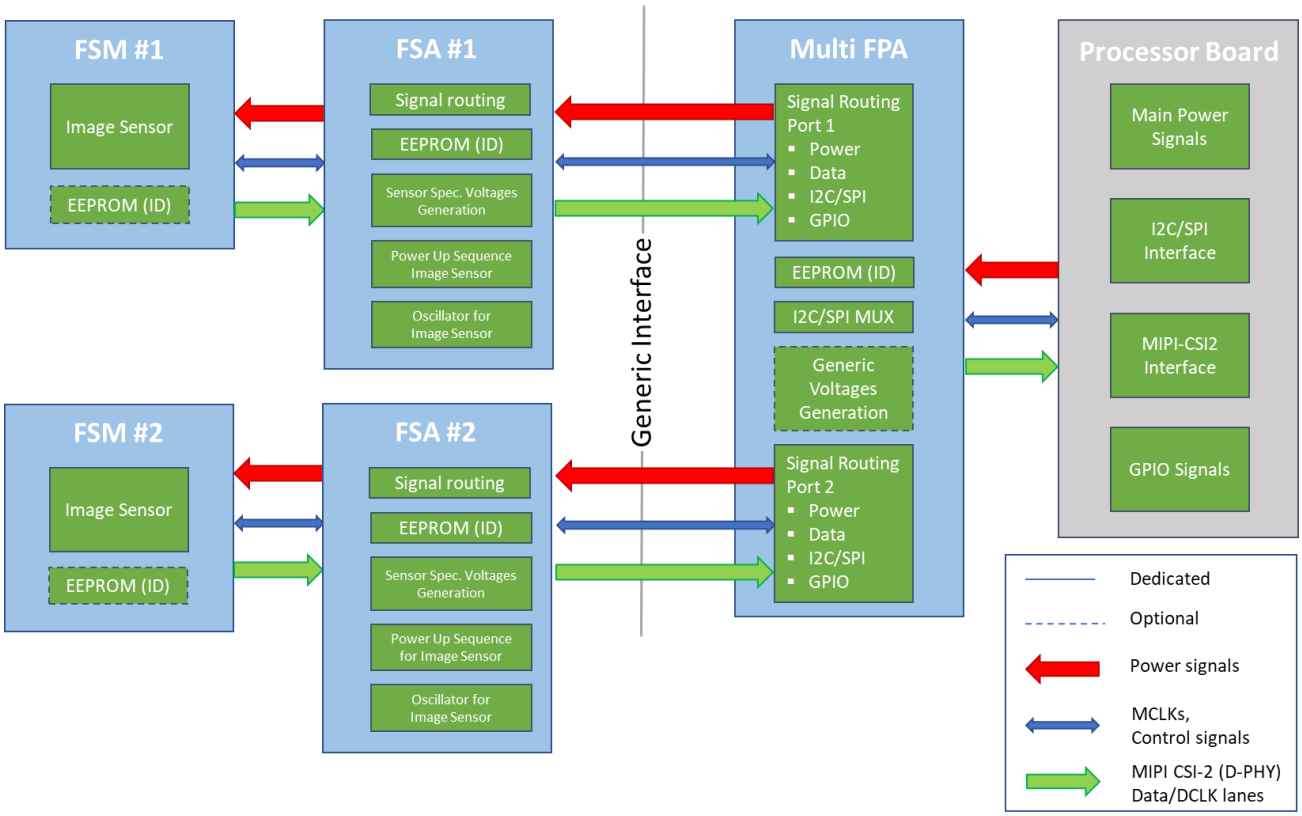


Figure 3: Block Diagram of Components in Multi Sensor Setup

While the FRAMOS Sensor Modules (FSM) are targeting at the most efficient design, the FRAMOS Sensor Adapters (FSA) support all present sensors and their individual electronic requirements from voltage rails to reference clock generation. The goal is to reduce noise and heat generation on image sensor board by moving this to the FSA. Further, it leaves the choice to the user to integrate this circuitry into their own processor board designs with the target to also reduce size and redundancy. All electrical references are created and available on a per project basis.

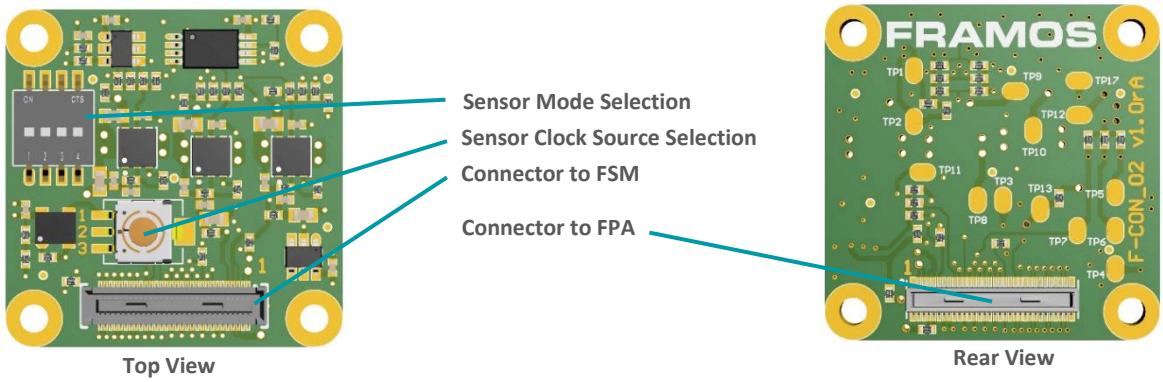
5 FSA-FTx/A: FRAMOS Sensor Adapter for MIPI CSI-2

- Connects FSM with MIPI CSI-2 Output to FPA
- Each FSM has a specific FSA

Functional Blocks:

- Signal routing
- Voltage generation for image sensor
- Power up sequence for image sensor
- Driving frequency generation (oscillator)
- EEPROM (config / ID)

5.1 Interface Description



5.1.1 Sensor Mode Selection

Pos.	Select	State	Description
1	ON OFF	Enabled Disabled	Enable / Disable EEPROM on FSA. Note: It is recommended to be disabled, if FSM is equipped with EEPROM.
2	ON OFF	High Low	Select I2C address of sensor, signal depending on sensor type: SLAMODE, SLASEL or SLAMODE1. Please refer to sensor documentation for available signals.
3	ON OFF	High Low	Select I2C address of sensor, signal availability depending on sensor type: SLAMODE2. Please refer to sensor documentation for available signals.
4	ON OFF	High Low	Drive XMASTER pin of FSM (see sensor documentation for details).

Table 3: Selection of Sensor Mode on FSA-FTx/A-V1

5.1.2 Sensor Clock Source Selection

Pos.	Description
1	Clock Provided from FSA **(Default)**
2	External Clock 1 (MCLK0)
3	External Clock 2 (MCLK1)

Table 4: Selection of Sensor Clock Source on FSA-FTx/A-V1

5.1.3 Test Points

Name	Signal
TP1	I2C_0_SCL (SPI_SCK)
TP2	I2C_0_SDA (SPI_MOSI)
TP3	IS_MCLK_0
TP4	IS_RST_0
TP5	SLAMODE1
TP6	SLAMODE2
TP7	IS_GPIO0 (XMASTER0)
TP8	GND
TP9	3V8_VDD
TP10	1V8_VDD
TP11	V_ANA
TP12	V_IF
TP13	V_DIG
TP17	GND

Table 5: Test Points on FSA-FTx/A-V1

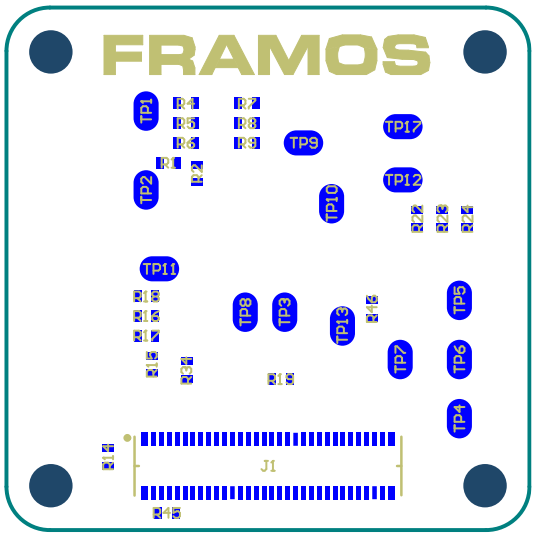


Figure 4: Test Points on FSA-FTx/A-V1

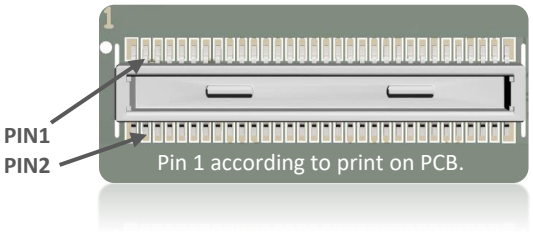
5.1.4 Connector to FPA

Type: Hirose DF40C-60DP-0.4V

Name: J1

Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	AUX_ANA	6	AUX_DIG
7	AUX_ANA	8	AUX_DIG
9	AUX_IF	10	AUX_V
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	GPIO14	18	GPIO15(SPI_MISO)
19	GPIO0(XMASTER0)	20	GPIO8
21	I2C_0_SCL(SPI_SCK)	22	I2C_1_SCL
23	GPIO17(SPI_CS)	24	GPIO16(SYS_PW_EN)
25	GPIO1(XVS0)	26	GPIO9
27	I2C_0_SDA(SPI_MOSI)	28	I2C_1_SDA
29	GPIO2(XHS0)	30	GPIO10
31	GPIO3(XTRIG0)	32	GPIO11(FSTROBE)
33	PW_EN_0	34	PW_EN_1
35	GPIO6	36	GPIO7
37	GND	38	GND
39	MCLK_0	40	GPIO4(MCLK2)
41	MCLK_1	42	GPIO5(MCLK3)
43	GND	44	GND
45	D_CLK_1_P	46	D_DATA_3_P
47	D_CLK_1_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

Table 6: Pinout of FSA-FTx/A-V1, connector to FRAMOS Processor Adapter (FPA)



Note: Colored signals are not routed directly to FSM and might be modified by FSA. All **other signals** are unmodified and passed through right from the image sensor.

Version 1.5.0 from 2024-05-23

J1: Signal Description to FPA (Part 1/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
1	3V8_VDD	Power	3.8V Power Supply (Triggers FSA/FSM power-up)	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
2	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
3	3V8_VDD	Power	3.8V Power Supply (Triggers FSA/FSM power-up)	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
4	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
5	AUX_ANA	Power	Not Connected	(FSM)			
6	AUX_DIG	Power	Not Connected	(FSM)			
7	AUX_ANA	Power	Not Connected	(FSM)			
8	AUX_DIG	Power	Not Connected	(FSM)			
9	AUX_IF	Power	Not Connected	(FSM)			
10	AUX_V	Power	Not Connected	(FSM)			
11	GND	GND	Common Ground				
12	GND	GND	Common Ground				
13	GND	GND	Common Ground				
14	GND	GND	Common Ground				
15	RST_0	IN	General reset for FSM, resets images sensor (XCLR).	Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
16	RST_1	IN		(Reset_IC)	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
17	GPIO14	IN/OUT		FSM			
18	GPIO15(SPI_MISO)	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
19	GPIO0(XMASTER0)	IN		(FSM)	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
20	GPIO8	IN/OUT		FSM			
21	I2C_0_SCL(SPI_SCK)	IN	I2C SCL for EEPROM and FSM	EEPROM, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V
22	I2C_1_SCL	IN	Additional I2C SCL for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V
23	GPIO17(SPI_CS)	IN		FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
24	GPIO16(SYS_PW_EN)	IN/OUT		FSM			
25	GPIO1(XVS0)	IN/OUT	XVS from/to FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V, VOLmax=0.2V,VOHmin=1.6V
26	GPIO9	IN/OUT		FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
27	I2C_0_SDA(SPI_MOSI)	IN/OUT	I2C SDA for EEPROM and FSM	EEPROM, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V, VOLmax=0.36V,VOHmin=1.44V
28	I2C_1_SDA	IN/OUT	Additional I2C SDA for FSM	FSM			
29	GPIO2(XHS0)	IN/OUT	XHS from/to FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V, VOLmax=0.2V,VOHmin=1.6V
30	GPIO10	IN/OUT		FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
31	GPIO3(XTRIG0)	IN	XTRIG for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
32	GPIO11(FSTROBE)	OUT	FSTROBE from FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
33	PW_EN_0	IN	PW_EN for FSM	FSM	LVCMOS18 (1.8V)	Normal: High, Pwr Down: Low	VILmax=0.36V,VIHmin=1.44V

J1: Signal Description to FPA (Part 2/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
34	PW_EN_1	IN	Additional PW_EN for FSM	FSM	LVCMOS18 (1.8V)	Normal: High, Pwr Down: Low	VILmax=0.36V,VIHmin=1.44V
35	GPIO6	IN		(FSM)	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
36	GPIO7	IN		(FSM)	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
37	GND	GND	Common Ground				
38	GND	GND	Common Ground				
39	MCLK_0	IN CLK	Master clock 0 (FSM input clock when SW1 in position 2)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
40	GPIO4(MCLK2)	IN/OUT		FSM			
41	MCLK_1	IN CLK	Master clock 1 (FSM input clock when SW1 in position 3)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
42	GPIO5(MCLK3)	IN/OUT		FSM			
43	GND	GND	Common Ground				
44	GND	GND	Common Ground				
45	D_CLK_1_P	OUT	MIPI-CSI2 output clock (1, P)	FSM	MIPI D-PHY		
46	D_DATA_3_P	OUT	MIPI-CSI2 output data (3, P)	FSM	MIPI D-PHY		
47	D_CLK_1_N	OUT	MIPI-CSI2 output clock (1, N)	FSM	MIPI D-PHY		
48	D_DATA_3_N	OUT	MIPI-CSI2 output data (3, N)	FSM	MIPI D-PHY		
49	GND	GND	Common Ground				
50	GND	GND	Common Ground				
51	D_DATA_0_N	OUT	MIPI-CSI2 output data (0, N)	FSM	MIPI D-PHY		
52	D_DATA_1_N	OUT	MIPI-CSI2 output data (1, N)	FSM	MIPI D-PHY		
53	D_DATA_0_P	OUT	MIPI-CSI2 output data (0, P)	FSM	MIPI D-PHY		
54	D_DATA_1_P	OUT	MIPI-CSI2 output data (1, P)	FSM	MIPI D-PHY		
55	GND	GND	Common Ground				
56	GND	GND	Common Ground	FSM			
57	D_DATA_2_P	OUT	MIPI-CSI2 output data (2, P)	FSM	MIPI D-PHY		
58	D_CLK_0_P	OUT CLK	MIPI-CSI2 output clock (0, P)	FSM	MIPI D-PHY		
59	D_DATA_2_N	OUT	MIPI-CSI2 output data (2, N)	FSM	MIPI D-PHY		
60	D_CLK_0_N	OUT CLK	MIPI-CSI2 output clock (0, N)	FSM	MIPI D-PHY		

5.2 Technical Drawing

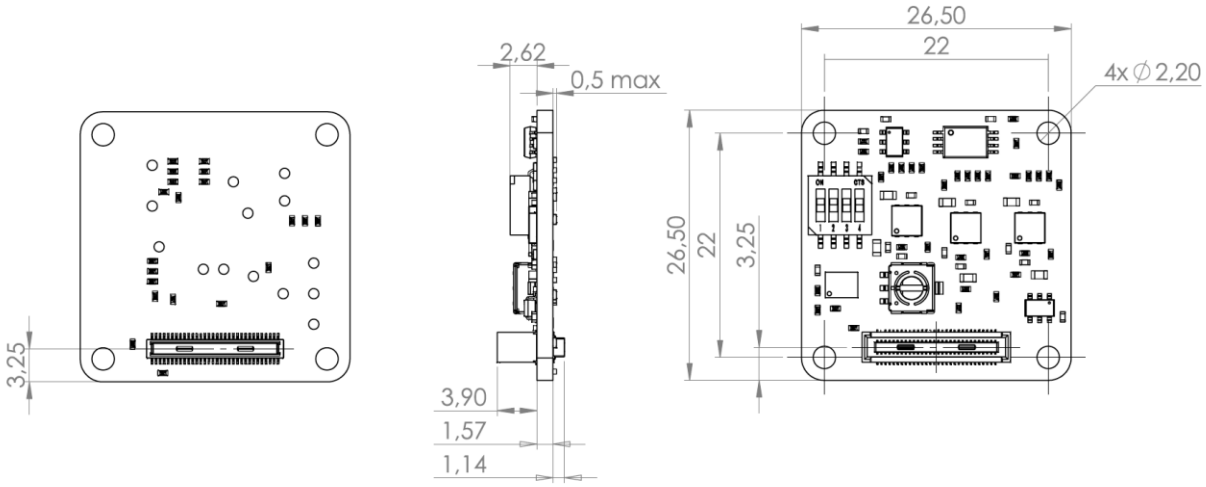


Figure 5: Technical Drawing of FSA-FTx/A-V1

6 Ecosystem for Sub-LVDS, SLVS and SLVS-EC Image Sensors

The following chapters provide the relevant technical information for Sub-LVDS, SLVS and SLVS-EC sensor modules (FSM), according to the two supported data chains:

- Data conversion to MIPI CSI-2 (D-PHY)
- Native data streaming

6.1 Sub-LVDS and SLVS Sensors on MIPI CSI-2

The Sub-LVDS and SLVS sensor setup with MIPI CSI-2 conversion hardware configuration consists of one or multiple FSMs with Sub-LVDS or SLVS output, each with an appropriate sensor specific FSA and one FPA for the target processor board. The MIPI CSI-2 conversion takes place on the FSA. Only FSA and FPA designs shown in this chapter are compatible to each other. The FPA defines the maximum number of sensor modules that can be operated per processor board.

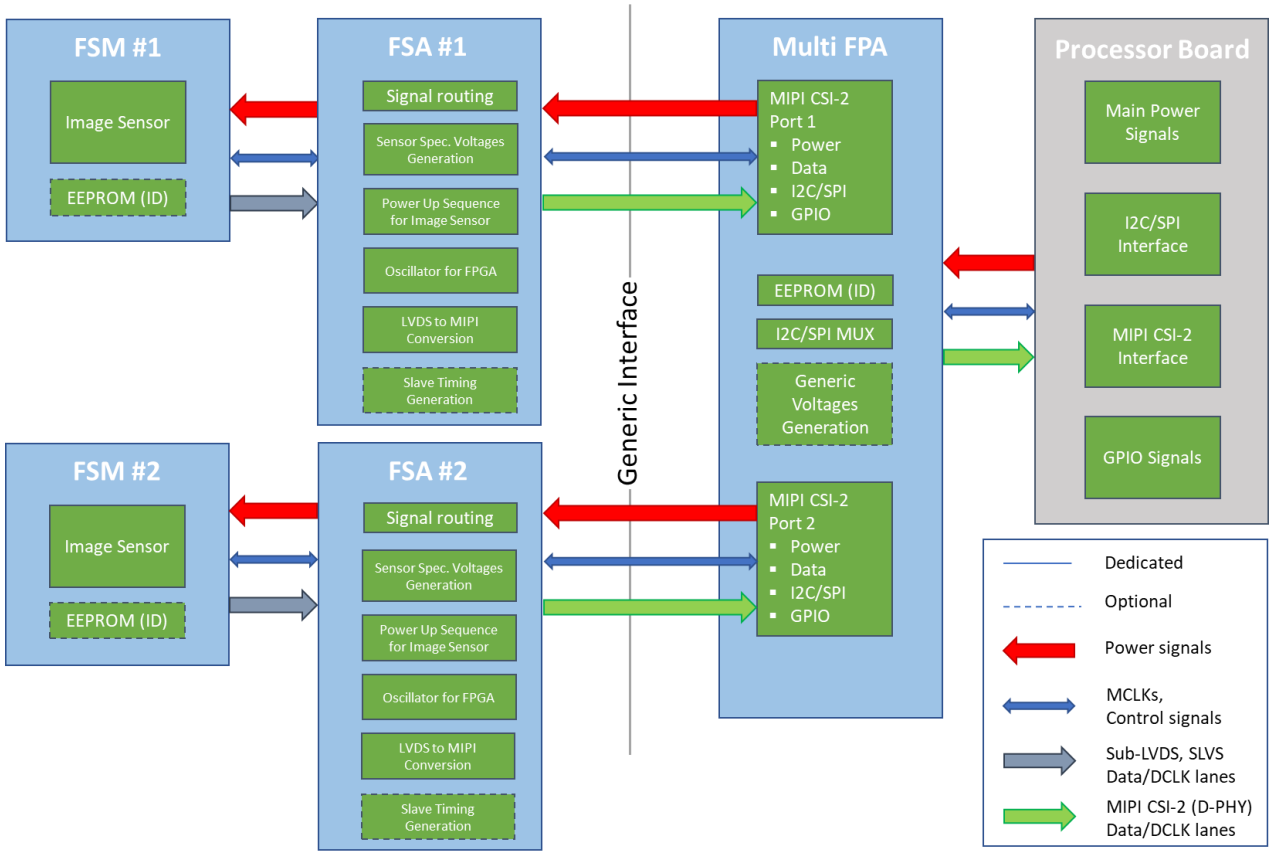


Figure 6: Block Diagram of components in Sub-LVDS / SLVS to MIPI CSI-2 Sensor Setup

6.2 Pure Sub-LVDS, SLVS or SLVS-EC Chain

The pure Sub-LVDS, SLVS and SLVS-EC sensor setup consists of one or multiple FSMs with Sub-LVDS or SLVS output, each with an appropriate sensor specific FSA and one FPA for the target processor board. No data signal conversion takes place. Only FSA and FPA designs shown in this chapter are compatible to each other. The FPA defines the maximum number of sensor modules that can be operated per processor board.

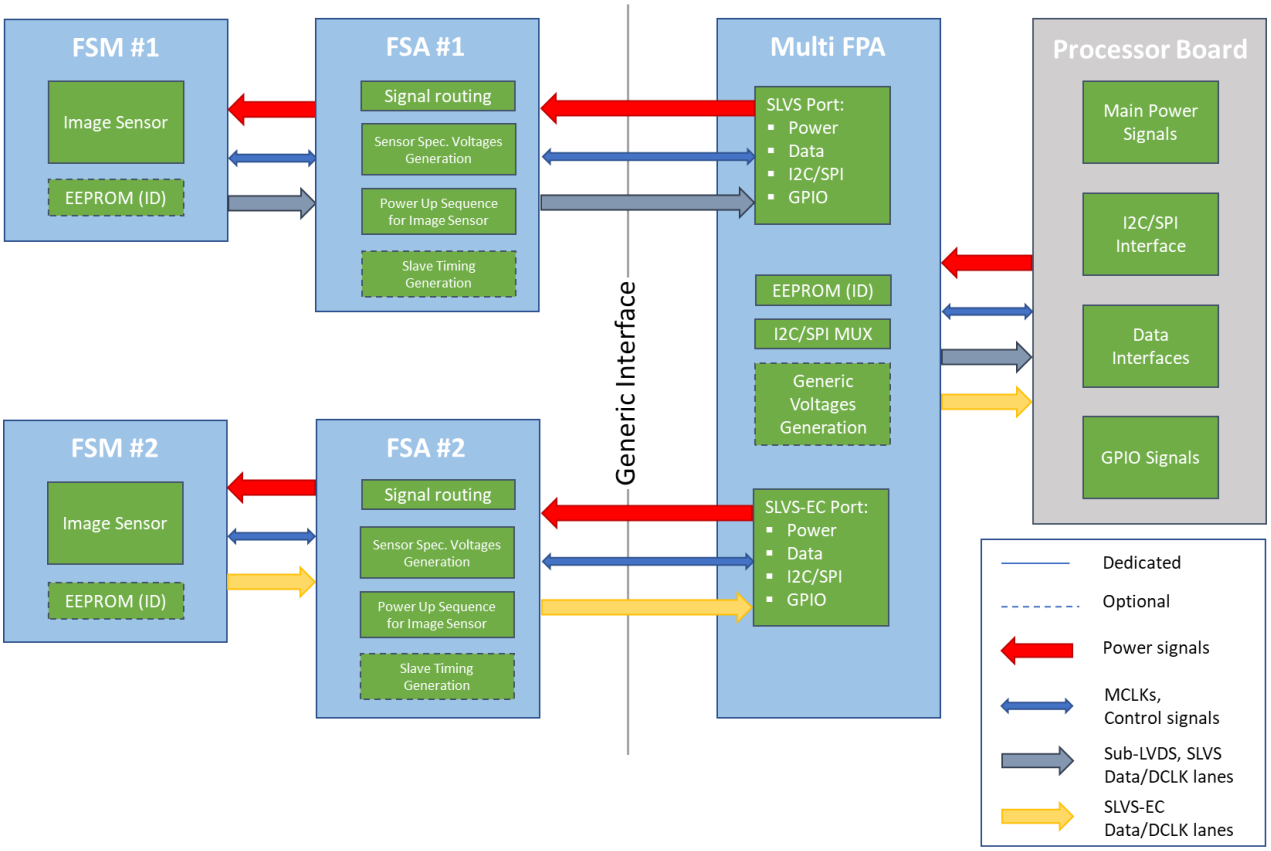
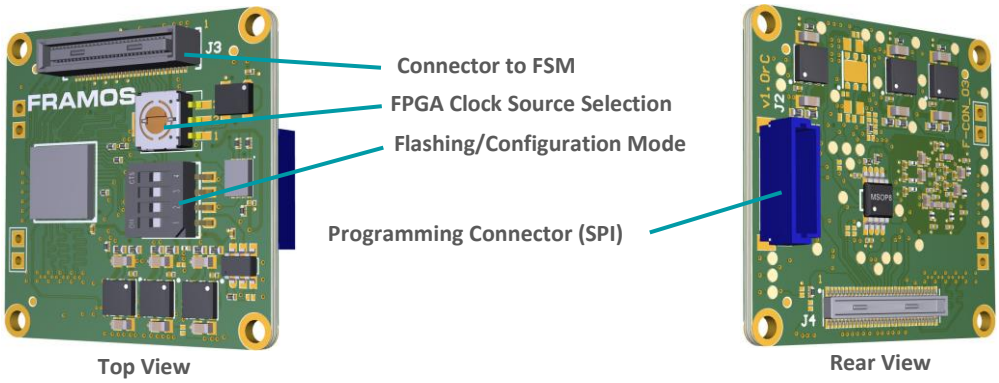


Figure 7: Block Diagram of components in Sub-LVDS, SLVS and SLVS-EC Sensor Setup

7 FSA-FTx/A-00G-V1: FRAMOS Sensor Adapter with LVDS to CSI-2 Conversion

Connects FSM with Sub-LVDS or SLVS data output to FPA with MIPI CSI-2 input
Performs image data conversion to MIPI CSI-2 (D-PHY)
Each FSA variant ("x") might be FSM specific



Functional Blocks:

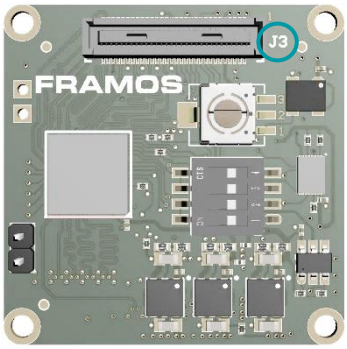
- Signal routing
- Voltage generation and power up sequence for image sensor
- Master clock and slave timing generation
- Image data conversion to MIPI CSI-2

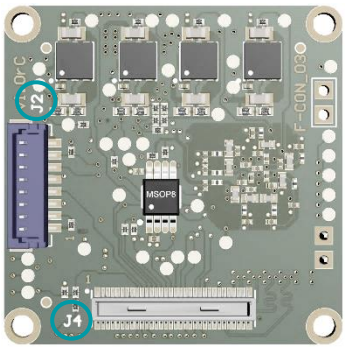
7.1 Functional Specification

Item	FSA-FT14/A-00G	FSA-FT15/A-00G	FSA-FT18/A-00G
Supported FSM	FSM-IMX264	FSM-IMX304	FSM-IMX530
Color / Mono	Both		
Resolution & Framerate	**2448 x 2048 @ 35FPS** 2048 x 1536 @ 47FPS 1920 x 1080 @ 60FPS	**4096 x 3000 @ 23FPS** 4096 x 2160 @ 30FPS 3840 x 2160 @ 30FPS	**5320 x 4600 @ 15FPS** 4512 x 4512 @ 18FPS 5328 x 3040 @ 22FPS 4064 x 3008 @ 27FPS 2660 x 2300 @ 54FPS
Bit Depth[1]	10, 12 bit (RAW)		
Input Data Format	4-Lane, Sub-LVDS	8-Lane, Sub-LVDS	8-Lane, SLVS
Output Data Format	4-Lane, MIPI CSI-2 (D-PHY) @ 594 Mbps	4-Lane, MIPI CSI-2 (D-PHY) @ 1188 Mbps	4-Lane, MIPI CSI-2 (D-PHY) @ 1188 Mbps
Operating Mode	Master, Slave		
Clock Source	Internal (37.125MHz), or extern via processor board		
FW Change/Update[1]	I2C (int), SPI (ext)		
Driver	NVIDIA Jetson TX2, AGX Xavier (LibSV and Libargus)		

[1] Firmware updates are applied via the processor board over the I2C bus, or using the external SPI interface attaching an appropiate programmer (Lattice HW-USBN-2B). Updates to the onboard flash are permanent and can only be applied via SPI. Updates via I2C will be lost when powercycling the FSA.

7.2 Interface Description



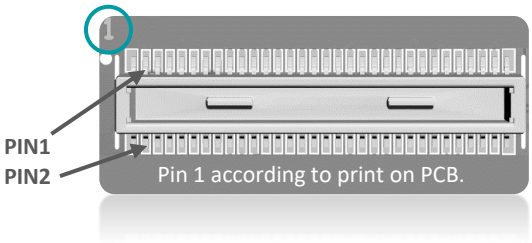


7.2.1 J3: Connector to FSM

Label: J3
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSM

7.2.2 J4: Connector to FPA

Label: J4
Type: DF40C-60DP-0.4V
Pinout:



Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	EE_MISO	18	GPIO15(SPI_MISO)
19	GPIO0(XMASTER0)	20	EE_MOSI
21	I2C_0_SCL(SPI_SCK)	22	NC
23	GPIO17(SPI_CS)	24	GPIO16(SYS_PW_EN)
25	GPIO1(XVS0)	26	EE_SCK
27	I2C_0_SDA(SPI_MOSI)	28	NC
29	GPIO2(XHS0)	30	EE_SS
31	GPIO3(XTRIG0)	32	GPIO11
33	PW_EN	34	CRESET_B
35	GPIO6	36	GPIO7
37	GND	38	GND
39	MCLK_0	40	GPIO4(MCLK2)
41	MCLK_1	42	GPIO5(MCLK3)
43	GND	44	GND
45	NC	46	D_DATA_3_P
47	NC	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

Table 7: Pinout of FSA-FTx/A-00G-V1, connector to FRAMOS Processor Adapter (FPA)

Version 1.5.0 from 2024-05-23

J4: Signal Description (Part 1/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
1	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
2	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
3	3V8_VDD	Power	3.8V Power Supply	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
4	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
5	NC	-	Not Connected				
6	NC	-	Not Connected				
7	NC	-	Not Connected				
8	NC	-	Not Connected				
9	NC	-	Not Connected				
10	NC	-	Not Connected				
11	GND	GND	Common Ground				
12	GND	GND	Common Ground				
13	GND	GND	Common Ground				
14	GND	GND	Common Ground				
15	RST_0	IN	General reset for FSA and FSM, resets Crosslink logic and image sensor (XCLR).	Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
16	RST_1	IN		Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
17	EE_MISO	OUT	4-wire SPI MISO for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
18	GPIO15(SPI_MISO)	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
19	GPIO0(XMASTER0)	IN/OUT	Connected to Test Point (TP22)	Test point			
20	EE_MOSI	IN	4-wire SPI MOSI for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
21	I2C_0_SCL(SPI_SCK)	IN	I2C SCL for Crosslink user interface and FSM	CrossLink, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V
22	NC	-	Not Connected				
23	GPIO17(SPI_CS)	IN		FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
24	GPIO16(SYS_PW_EN)	IN/OUT	Connected to Test Point (TP34)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
25	GPIO1(XVS0)	IN/OUT	Multiple FSM synchronization	CrossLink	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V VOLmax=0.2V,VOHmin=1.6V
26	EE_SCK	IN	4-wire SPI SCK for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
27	I2C_0_SDA (SPI_MOSI)	IN/OUT	I2C SDA for Crosslink user interface and FSM	CrossLink, FSM	LVCMOS18 (1.8V)		VILmax=0.54V,VIHmin=1.26V VOLmax=0.36V,VOHmin=1.44V
28	NC	-	Not Connected				
29	GPIO2(XHS0)	IN/OUT	Connected to Test Point (TP23)	Test point			
30	EE_SS	IN	4-wire SPI CS for Crosslink and Flash programming	CrossLink, Flash	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
31	GPIO3(XTRIG0)	IN/OUT	Connected to Test Point (TP24)	Test point			
32	GPIO11	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.2V,VOHmin=1.6V
33	PW_EN	IN	FSA Power Enable (Crosslink and FSM)	LDO_ICs	LVCMOS18 (1.8V)	Normal: High, Pwr Down: Low	VILmax=0.36V,VIHmin=1.44V

J4: Signal Description (Part 2/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
34	CRESET_B	IN	Reset Crosslink Configuration	CrossLink	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.36V,VIHmin=1.44V
35	GPIO6	IN/OUT	Connected to Test Point (TP21)	Test point, (FSM)	LVCMOS18 (1.8V)	1A: High, 10: Low	VILmax=0.36V,VIHmin=1.44V
36	GPIO7	IN/OUT	Connected to Test Point (TP33)	Test point			
37	GND	GND	Common Ground				
38	GND	GND	Common Ground				
39	MCLK_0	IN CLK	Master clock 0 (Crosslink input clock when SW2 in position 2)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
40	GPIO4(MCLK2)	IN/OUT	Connected to Test Point (TP32)	Test point			
41	MCLK_1	IN CLK	Master clock 1 (Crosslink input clock when SW2 in position 3)	Rotary Switch	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin=1.44V
42	GPIO5(MCLK3)	IN/OUT	Connected to Test Point (TP31)	Test point			
43	GND	GND	Common Ground				
44	GND	GND	Common Ground				
45	NC	-	Not Connected				
46	D_DATA_3_P	OUT	MIPI-CSI2 output data (3, P)	CrossLink	MIPI D-PHY		
47	NC	-	Not Connected				
48	D_DATA_3_N	OUT	MIPI-CSI2 output data (3, N)	CrossLink	MIPI D-PHY		
49	GND	GND	Common Ground				
50	GND	GND	Common Ground				
51	D_DATA_0_N	OUT	MIPI-CSI2 output data (0, N)	CrossLink	MIPI D-PHY		
52	D_DATA_1_N	OUT	MIPI-CSI2 output data (1, N)	CrossLink	MIPI D-PHY		
53	D_DATA_0_P	OUT	MIPI-CSI2 output data (0, P)	CrossLink	MIPI D-PHY		
54	D_DATA_1_P	OUT	MIPI-CSI2 output data (1, P)	CrossLink	MIPI D-PHY		
55	GND	GND	Common Ground				
56	GND	GND	Common Ground				
57	D_DATA_2_P	OUT	MIPI-CSI2 output data (2, P)	CrossLink	MIPI D-PHY		
58	D_CLK_0_P	OUT CLK	MIPI-CSI2 output clock (0, P)	CrossLink	MIPI D-PHY		
59	D_DATA_2_N	OUT	MIPI-CSI2 output data (2, N)	CrossLink	MIPI D-PHY		
60	D_CLK_0_N	OUT CLK	MIPI-CSI2 output clock (0, N)	CrossLink	MIPI D-PHY		

7.2.3 Firmware Flashing/Configuration

Options \ Switch Pattern	1	2	3	4
Boot configuration from flash, configuration and flash update via SPI enabled **(Default)**	**Off**	**On**	**Off**	**On**
Configuration from host via I2C	**On**	**Off**	**On**	**Off**

Table 8: Selection of Sensor Mode on FSA-FTx/A-00G-V1

7.2.4 FPGA Clock Source Selection

Pos.	Description
1	Clock provided from FSA **(Default)**
2	External clock 1 (MCLK0)
3	External clock 2 (MCLK1)

Table 9: Selection of Sensor Clock Source on FSA-FTx/A-00G-V1

7.2.5 Test Points

Name	Signal	Name	Signal	Name	Signal
TP1	PW_EN1	**TP13**	IS_MCLK	**TP25**	XTRIG2
TP2	V_ANA	**TP14**	GND	**TP26**	GPIO11(TOUT0)
TP3	GND	**TP15**	XHS	**TP27**	GPIO8(TOUT1)
TP4	PW_EN2	**TP16**	IS_RST	**TP28**	GPIO9(TOUT2)
TP5	AUX_V	**TP17**	GND	**TP29**	GPIO16
TP6	GND	**TP18**	XMASTER	**TP30**	GND
TP7	PW_EN3	**TP19**	XVS	**TP31**	GPIO5(MCLK3)
TP8	V_DIG	**TP20**	GND	**TP32**	GPIO4(MCLK2)
TP9	PW_EN4	**TP21**	GPIO6	**TP33**	GPIO7
TP10	V_IF	**TP22**	GPIO0(XMASTER0)	**TP34**	GPIO16(SYS_PW_EN)
TP11	GPIO1(XVS0)	**TP23**	GPIO2(XHS0)		
TP12	XTRIG	**TP24**	GPIO3(XTRIG)		

Table 10: Test Points on FSA-FTx/A-00G-V1

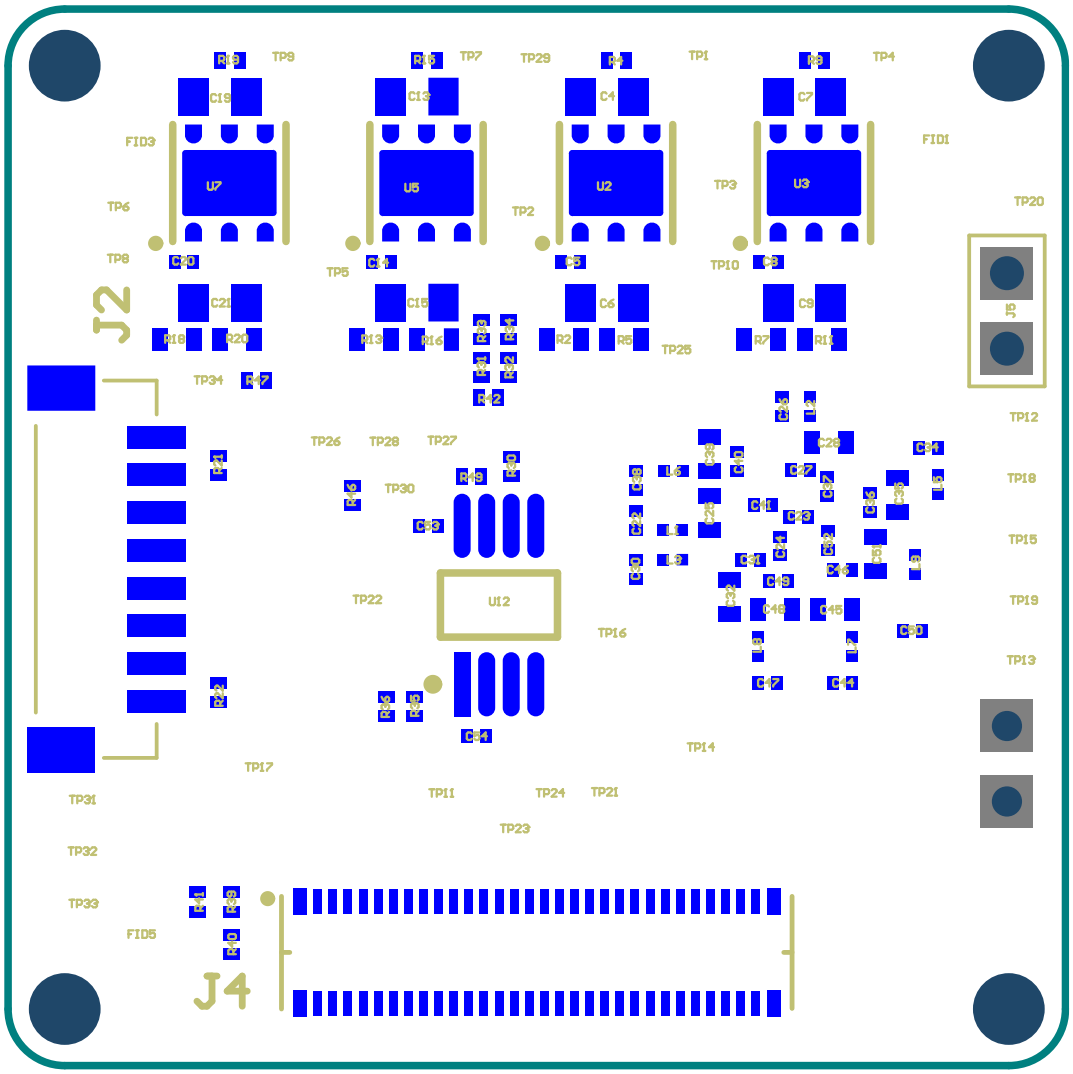
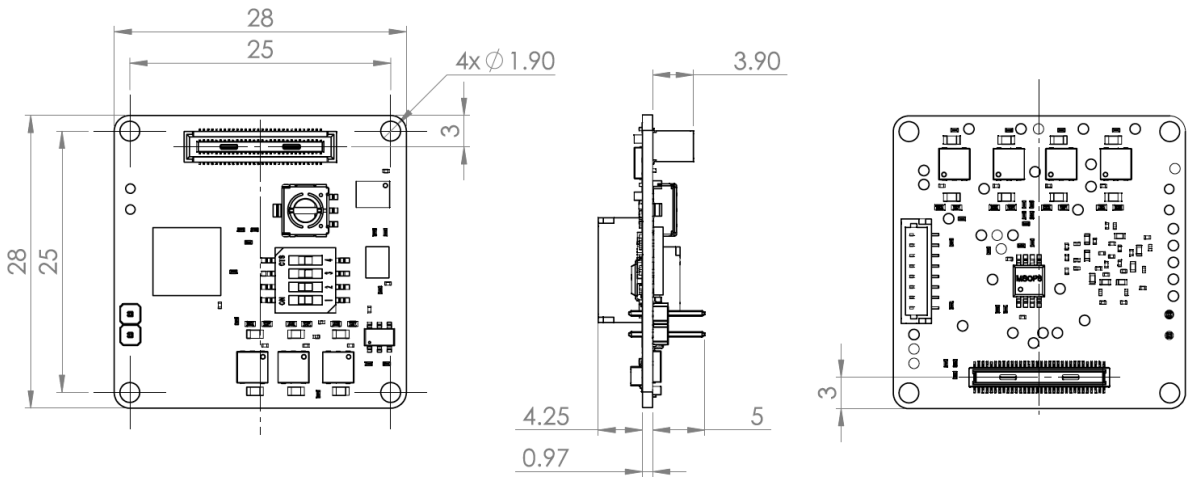


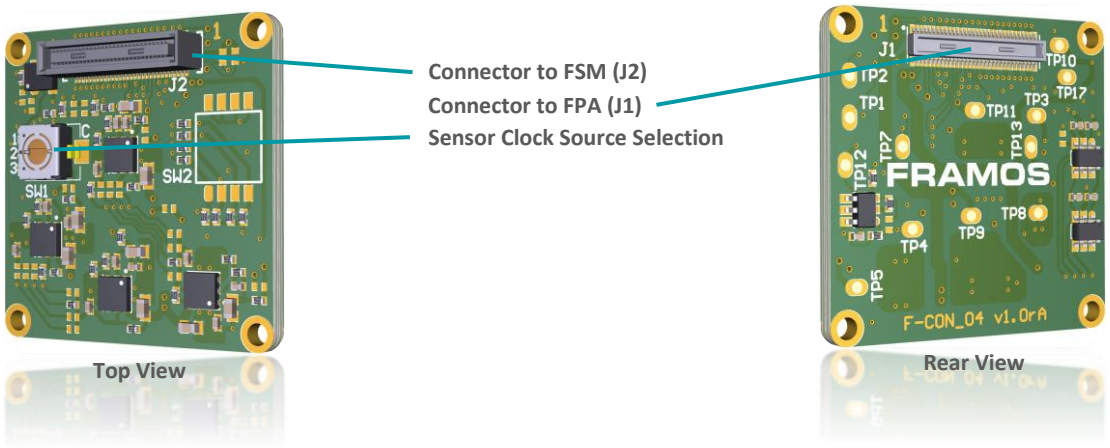
Figure 8: Test Points on FSA-FTx/A-00G-V1

7.3 Technical Drawing



8 FSA-FTx/BC-V1: FRAMOS Sensor Adapter for Sub-LVDS, SLVS and SLVS-ECC

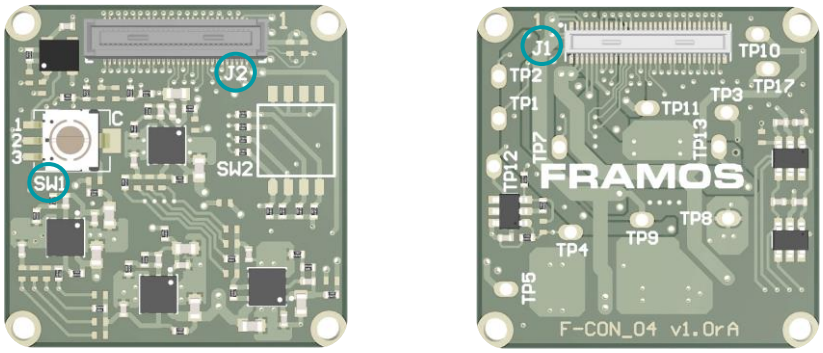
- Connects FSM with Sub-LVDS, SLVS or SLVS-EC output to FPA
- Each FSA variant (“x”) might be FSM specific



Functional Blocks:

- Signal routing
- Voltage generation for image sensor
- Power up sequence for image sensor

8.1 Interface Description



8.1.1 SW1: Sensor Clock Source Selection

Pos.	Description
1	Clock Provided from FSA **(Default)**
2	External Clock 1 (MCLK0)
3	External Clock 2 (MCLK1)

Table 11: Selection of Sensor Clock Source on FSA-FTx/A-V1

8.1.2 J2: Connector to FSM

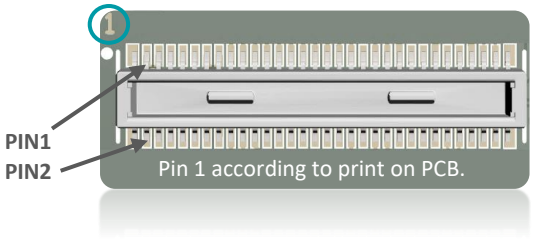
Label: J2
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSM

8.1.3 J1: Connector to FPA

Label: J1

Type: Hirose DF40C-60DP-0.4V

Pinout:



Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	AUX_ANA	6	AUX_DIG
7	AUX_ANA	8	AUX_DIG
9	AUX_IF	10	AUX_V
11	GND	12	GND
13	GND	14	GND
15	I2C_0_SDA(SPI_MOSI)	16	I2C_0_SCL(SPI_SCK)
17	SDO	18	XCE
19	TOUT0	20	GPIO6
21	TOUT1	22	GPIO0(XMASTER)
23	TOUT2	24	GPIO7
25	GPIO16	26	XTRIG1
27	GPIO14	28	XHS
29	GPIO10	30	XVS
31	GND	32	GND
33	RST_0	34	D_DATA_7_P
35	MCLK_0	36	D_DATA_7_N
37	GND	38	GND
39	D_DATA_6_P	40	D_DATA_5_P
41	D_DATA_6_N	42	D_DATA_5_N
43	GND	44	GND
45	D_DATA_4_P	46	D_DATA_3_P
47	D_DATA_4_N	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_2_P	52	D_DATA_1_P
53	D_DATA_2_N	54	D_DATA_1_N
55	GND	56	GND
57	D_DATA_0_P	58	D_CLK_0_P
59	D_DATA_0_N	60	D_CLK_0_N

Table 12: Pinout of FSA-FTx/BC-V1, connector to FRAMOS Processor Adapter (FPA) with Sub-LVDS, SLVS or SLVS-EC input

J1: Signal Description (Part 1/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
1	3V8_VDD	Power	3.8V Power Supply (Triggers FSA/FSM power-up)	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
2	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
3	3V8_VDD	Power	3.8V Power Supply (Triggers FSA/FSM power-up)	LDO_ICs, FSM			3V8_VDD=3.7V-5.1V, max. 0.3A
4	1V8_VDD	Power	1.8V Power Supply	LDO_ICs, FSM			1V8_VDD=1.7V-1.9V, max. 0.3A
5	AUX_ANA	Power	Not Connected	(FSM)			
6	AUX_DIG	Power	Not Connected	(FSM)			
7	AUX_ANA	Power	Not Connected	(FSM)			
8	AUX_DIG	Power	Not Connected	(FSM)			
9	AUX_IF	Power	Not Connected	(FSM)			
10	AUX_V	Power	Not Connected	(FSM)			
11	GND	GND	Common Ground				
12	GND	GND	Common Ground				
13	GND	GND	Common Ground				
14	GND	GND	Common Ground				
15	I2C_0_SDA(SPI_MOSI)	IN/OUT	I2C SDA for FSM. Connected to Test Point (TP1)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V
16	I2C_0_SCL(SPI_SCK)	IN	I2C SCL for FSM. Connected to Test Point (TP2)	Test point, FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
17	SDO	OUT		FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
18	XCE	IN		FSM	LVCMOS18 (1.8V)	I2C: High, 4-wire: Low	VILmax=0.36V, VIHmin= 1.44V
19	TOUT0	OUT	TOUT0 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
20	GPIO6	IN	Slave address select for FSM (SLAMODE0)	FSM	LVCMOS18 (1.8V)	1A: High, 10: Low	VILmax=0.36V,VIHmin= 1.44V
21	TOUT1	OUT	TOUT1 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
22	GPIO0(XMASTER)	IN	XMASTER for FSM. Connected to Test Point (TP7)	Test point, FSM	LVCMOS18 (1.8V)	Slave: High, Master: Low	VILmax=0.36V, VIHmin= 1.44V
23	TOUT2	OUT	TOUT2 from FSM	FSM	LVCMOS18 (1.8V)		VOLmax=0.4V, VOHmin=1.4V
24	GPIO7	IN	XTRIG2 for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
25	GPIO16	IN	Slave address select for FSM (SLAMODE1)	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
26	XTRIG1	IN	XTRIG1 for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
27	GPIO14	IN	Slave address select for FSM (SLAMODE2)	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V
28	XHS	IN/OUT	XHS for FSM	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V
29	GPIO10	IN	OMODE for FSM	FSM, (Power Sequencer)	LVCMOS18 (1.8V)	SLVS-EC: High, SLVS: Low	VILmax=0.36V, VIHmin= 1.44V
30	XVS	IN/OUT	Multiple FSM synchronization	FSM	LVCMOS18 (1.8V)		VILmax=0.36V,VIHmin= 1.44V, VOLmax=0.4V, VOHmin=1.4V

Version 1.5.0 from 2024-05-23

J1: Signal Description (Part 2/2)

Pin	Net name	I/O	Primary function description	Connected to	I/O Standard	I/O State	I/O DC Characteristic
31	GND	GND	Common Ground				
32	GND	GND	Common Ground				
33	RST_0	IN	General reset for FSM	Reset_IC	LVCMOS18 (1.8V)	Normal: High, Reset: Low	VILmax=0.54V, VIHmin= 1.26V
34	D_DATA_7_P	OUT	LVDS output data (7, P)	FSM	LVDS/SLVS/SLVS-EC		
35	MCLK_0	IN CLK	Master clock 0 (SW1 in pos 2 or 3)	Rotary switch	LVCMOS18 (1.8V)		VILmax=0.36V, VIHmin= 1.44V
36	D_DATA_7_N	OUT	LVDS output data (7, N)	FSM	LVDS/SLVS/SLVS-EC		
37	GND	GND	Common Ground				
38	GND	GND	Common Ground				
39	D_DATA_6_P	OUT	LVDS output data (6, P)	FSM	LVDS/SLVS/SLVS-EC		
40	D_DATA_5_P	OUT	LVDS output data (5, P)	FSM	LVDS/SLVS/SLVS-EC		
41	D_DATA_6_N	OUT	LVDS output data (6, N)	FSM	LVDS/SLVS/SLVS-EC		
42	D_DATA_5_N	OUT	LVDS output data (5, N)	FSM	LVDS/SLVS/SLVS-EC		
43	GND	GND	Common Ground				
44	GND	GND	Common Ground				
45	D_DATA_4_P	OUT	LVDS output data (4, P)	FSM	LVDS/SLVS/SLVS-EC		
46	D_DATA_3_P	OUT	LVDS output data (3, P)	FSM	LVDS/SLVS/SLVS-EC		
47	D_DATA_4_N	OUT	LVDS output data (4, N)	FSM	LVDS/SLVS/SLVS-EC		
48	D_DATA_3_N	OUT	LVDS output data (3, N)	FSM	LVDS/SLVS/SLVS-EC		
49	GND	GND	Common Ground				
50	GND	GND	Common Ground				
51	D_DATA_2_P	OUT	LVDS output data (2, P)	FSM	LVDS/SLVS/SLVS-EC		
52	D_DATA_1_P	OUT	LVDS output data (1, P)	FSM	LVDS/SLVS/SLVS-EC		
53	D_DATA_2_N	OUT	LVDS output data (2, N)	FSM	LVDS/SLVS/SLVS-EC		
54	D_DATA_1_N	OUT	LVDS output data (1, N)	FSM	LVDS/SLVS/SLVS-EC		
55	GND	GND	Common Ground				
56	GND	GND	Common Ground				
57	D_DATA_0_P	OUT	LVDS output data (0, P)	FSM	LVDS/SLVS/SLVS-EC		
58	D_CLK_0_P	OUT	LVDS output clock (0, P)	FSM	LVDS/SLVS/SLVS-EC		
59	D_DATA_0_N	OUT	LVDS output data (0, N)	FSM	LVDS/SLVS/SLVS-EC		
60	D_CLK_0_N	OUT	LVDS output clock (0, N)	FSM	LVDS/SLVS/SLVS-EC		

8.1.4 TPx: Test Points

Name	Signal	Name	Signal	Name	Signal
TP1	I2C_0_SDA (SPI_MOSI)	**TP7**	IS_GPIO0 (XMASTER0)	**TP12**	V_IF
TP2	I2C_0_SCL (SPI_SCK)	**TP8**	GND	**TP13**	V_DIG
TP3	IS_MCLK_0	**TP9**	3V8_VDD	**TP17**	GND
TP4	IS_RST_0	**TP10**	1V8_VDD		
TP5	V_ANA-1	**TP11**	V_ANA		

Table 13: Test Points on FSA-FTx/BC-V1

8.2 Technical Drawing

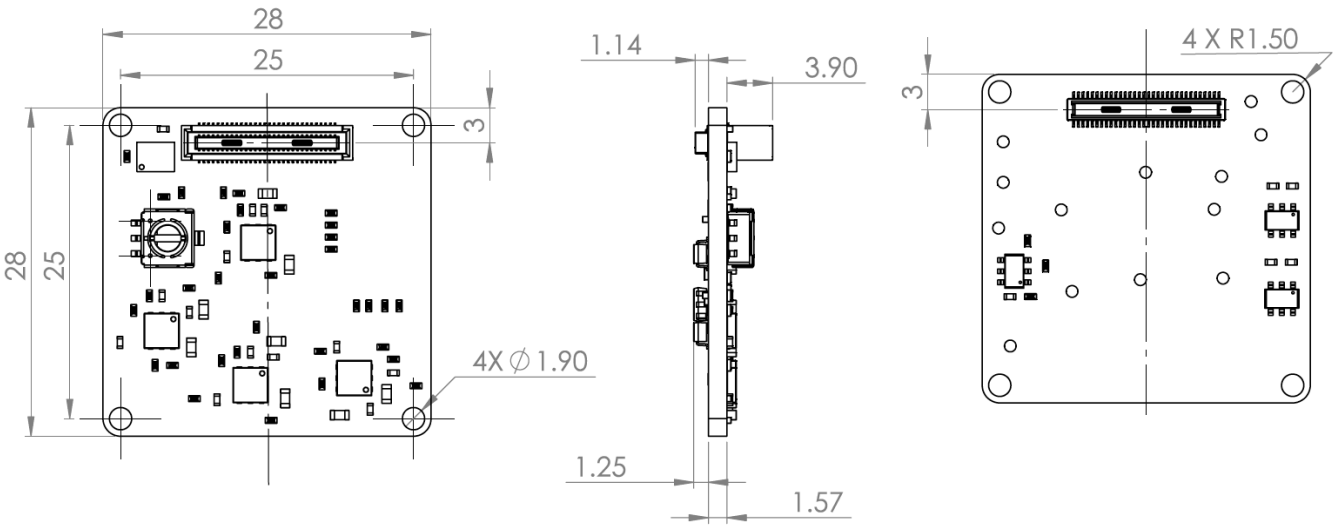


Figure 9: Technical Drawing of FSA-FTx/BC-V1

9 FRAMOS Functional Adapter (FFA)

The FRAMOS Functional Adapters (FFA) add device specific functionality to the FSM Ecosystem. They are optional to use and provide PixelMate™ interfaces on in- and output. This way they integrate seamlessly into an existing chain that consists of all components required to connect an FSM to a processor board.

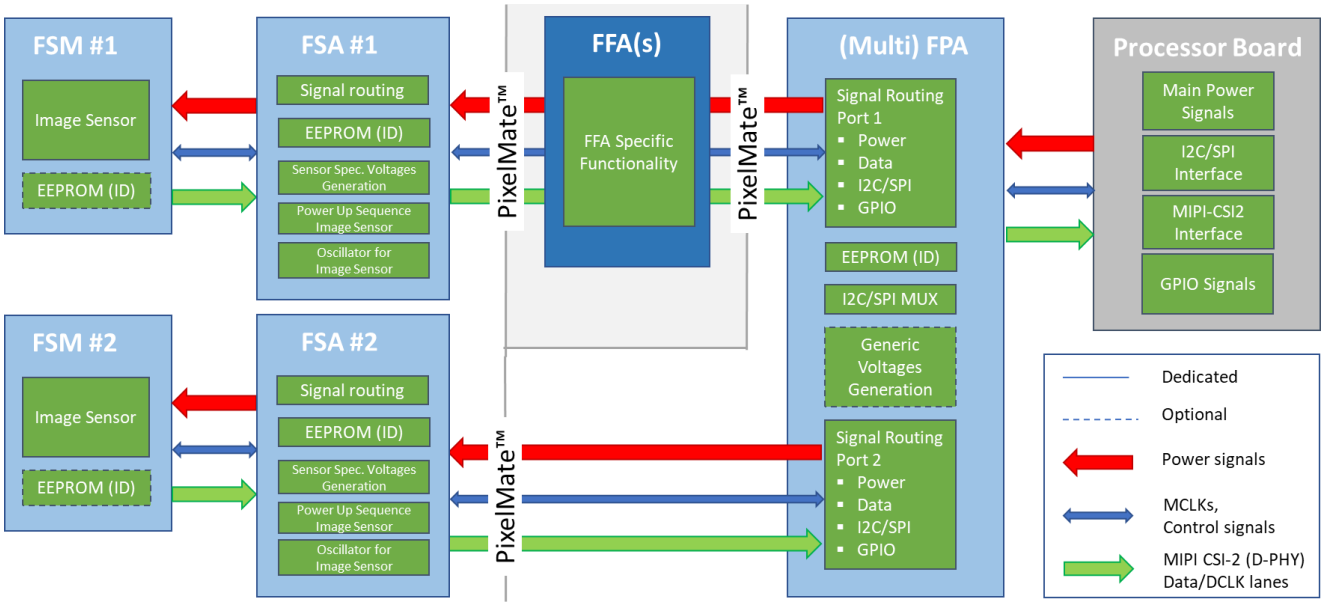


Figure 10: Block Diagram of components in MIPI CSI-2 chain with optional FFA on top FSM chain.

As an example, Figure 10 shows the block diagram of two FSMs connected to a processor board with their appropriate adapters (FSA, FPA). In the lower chain (#2), the FSM+FSA combination is directly connected to the FPA via the generalized PixelMate™ connector. In the upper chain (#1) contains an FFA (pair) with PixelMate™ in- and output. This FFA can be a single PCB performing i.e. image pre-processing, as well as a pair of boards acting as interface adapters, converting the interface completely (SerDes) or partially (connector/cable type) back and forth.

9.1 FFA-GMSL-SerDes

On the FRAMOS Functional Adapters (FFA) for GMSL, Maxim's "Gigabit Multimedia Serial Link" is utilized to transfer up to 12 Gbps of uncompressed video data, I2C communication, GPIOs and Power via a single coax wire with automotive grade Fakra connectors.

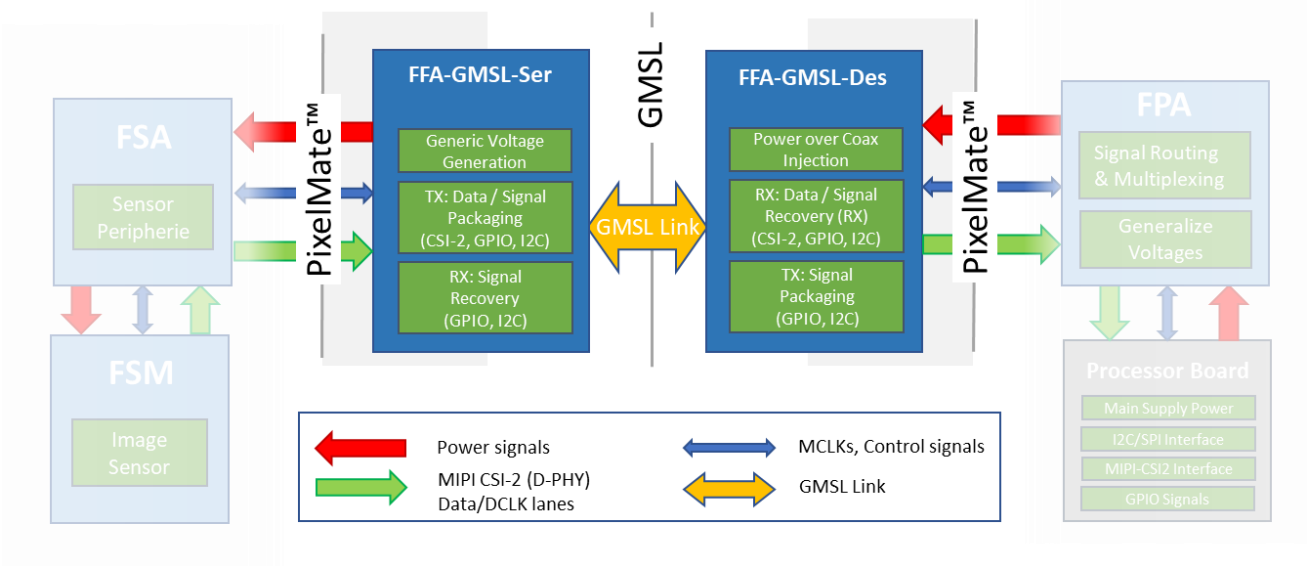


Figure 11: Block Diagram of FFA-GMSL-Ser and FFA-GMSL-Des inside the FSM Ecosystem.

As shown in Figure 11, the integration takes place in form of a serializer- (FFA-GMSL-Ser) and deserializer- (FFA-GMSL-Des) board, that create the appropriate GMSL line between each other and providing PixelMate™ conform MIPI CSI-2 connectivity on in- / output to FSA / FPA. This way they are physically compatible to all FSMs of the Ecosystem with this interface.

Note: Due to high power requirements of specific sensors, even if physically interface compatible, operation might not be possible due to lack of power over coax. Please check the Table 14 for an overview about tested and confirmed setups.

			Driver Implemented Modes [Full Resolution / max. FPS]	
Modules	**Physically Compatible**	**Reference Drivers (NVIDIA Jetson)**	**6 Gbps**	**12 Gbps**
FSM-AR0144	Yes	On Request.	Driver support on request, physically supported.	-
FSM-AR0521	Yes	On Request.		-
FSM-AR1335	Yes	On Request.		-
FSM-HDP230	Yes	On Request.		-
FSM-IMX264	Yes	On Request.		-
FSM-IMX283	Yes	On Request.		-
FSM-IMX290	Yes	Yes		1920 x 1080 / 120
FSM-IMX327	Yes	On Request.		-
FSM-IMX296	Yes	Yes		1456 x 1088 / 60
FSM-IMX297	Yes	On Request.		-
FSM-IMX304	Yes[2]	Yes		4112 x 3008 / 24
FSM-IMX334	Yes	On Request.		-
FSM-IMX335	Yes	On Request.		-
FSM-IMX412	Yes	Yes		4056 x 3040 / 60
FSM-IMX477	Yes	On Request.		-
FSM-IMX577	Yes	Yes		4056 x 3040 / 60
FSM-IMX415, 715	Yes	Yes		3864 x 2192 / 90
FSM-IMX462	Yes	Yes		1920 x 1080 / 120
FSM-IMX662	Yes	Yes		1920 x 1080 / 98
FSM-IMX464	Yes	Yes		2712 x 1538 / 90
FSM-IMX485	Yes	On Request.		-
FSM-IMX568	Yes	Yes		2472 x 2064 / 96
FSM-IMX585	Yes	Yes		3856 x 2180 / 90
FSM-IMX530	Yes[2]	Yes		5328 x 4608 / 15
FSM-IMX565	Yes	Yes		4128 x 3008 / 43
FSM-IMX675	Yes	Yes		2608 x 1964 / 81
FSM-IMX678	Yes	Yes		3856 x 2180 / 72
FSM-IMX990	Yes	Yes		1296 x 1032 / 125

Table 14: FRAMOS Sensor Module Compatibility and Support by FFA-GMSL-SerDes

Note: With the revision **V1A** of the FFA-GMSL-Des (Deserializer), ***only one GMSL line is supported per carrier board***. The power supplied from the carriers is not sufficient to source multiple or demanding image sensors. The **V2A** variant supports more power demanding image sensors with an external 12V power supply.

[2] High sensor power consumption. Requires Deserializer V2A for operation.

Latency

The latency added by GMSL conversion is related to the data rate and image width. It is 1 video line + 128 x T_{PCLK} where T_{PCLK} is the pixel clock of the sensor. As the actual delay depends on the operation mode, you can find a few examples for orientation below.

Modules	Resolution [V x H]	Framerate [fps / Hz]	Latency [µs]
FSM-IMX462	1920 x 1080	60 120	7,76 8,26
FSM-IMX415	3864 x 2192	45 90	23,55 10,15
FSM-IMX283	5496 x 3694	12 25	47,21 31,58

The values needed for calculation can be found in the corresponding sensor datasheet.

Sensor Communication and General Purpose Input- / Outputs (GPIO)

The SerDes chain embeds several (sensor) signals as well as communication into the GMSL stream. It is differentiated between 10 available multi-functional pins (MFP), providing latency optimized signals, and slower signals available by an IO extender communicating via I2C:

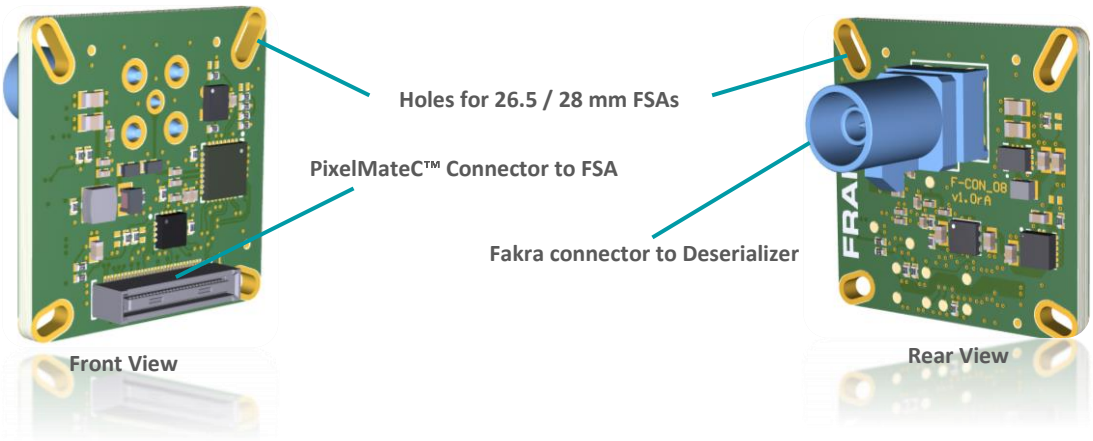
- GPIO Extender:
  - SLAMODE0, SLAMODE1, SLAMODE2, XMASTER, TOUT0, TOUT1, TOUT2
- Multi-Functional Pins
  - MFP0: SCK
  - MFP1: XCE
  - MFP2: XCLR
  - MFP3: XVS
  - MFP4: INCK (MFP4 is output of PLL, can generate a 1-75 MHz clock)
  - MFP5: XHS (OD out)
  - MFP6: XTRIG1 (OD out)
  - MFP7: SDI or I2C SDA (configurable)
  - MFP8: SDO or I2C SCL (configurable)
  - MFP9: XTRIG2 (OD out)
  - MFP10: NC

For details on the specific signals, check the documentation of your image sensor and FSA type.

9.1.1 **FFA-GMSL-Ser-V1A** (Serializer, Sensor Side)

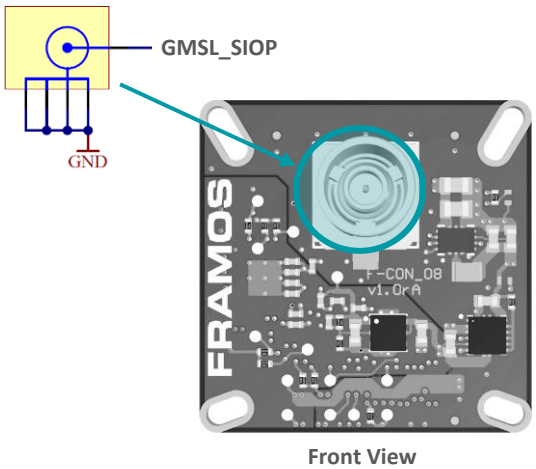
Serializer board acting as transmitter (TX), connecting to FSM+FSA stack serializing image data, embedding of bidirectional communication and sensor GPIOs. Connects to PixelMateC and outputs GMSL on Fakra type connector.

- 4-Lane MIPI CSI-2 Input
- Supporting 6 / 12 Gbps output modes
- Generic supply voltage (3V8, 1V8) recovery from PoC
- GPIOs and I2C Communication via MFP/ I2C Extender
- Testpoints to important signals
- Compatible to GMSL 6 / 12 Gbps compliant receivers.



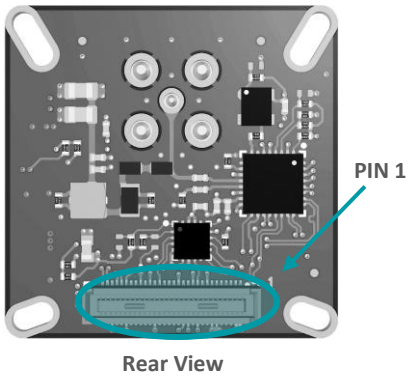
Fakra / GMSL Connector

Lable: J2
Type: 2FA1-NZSP-PCBB6
Pinout:



PixelMateC Connector

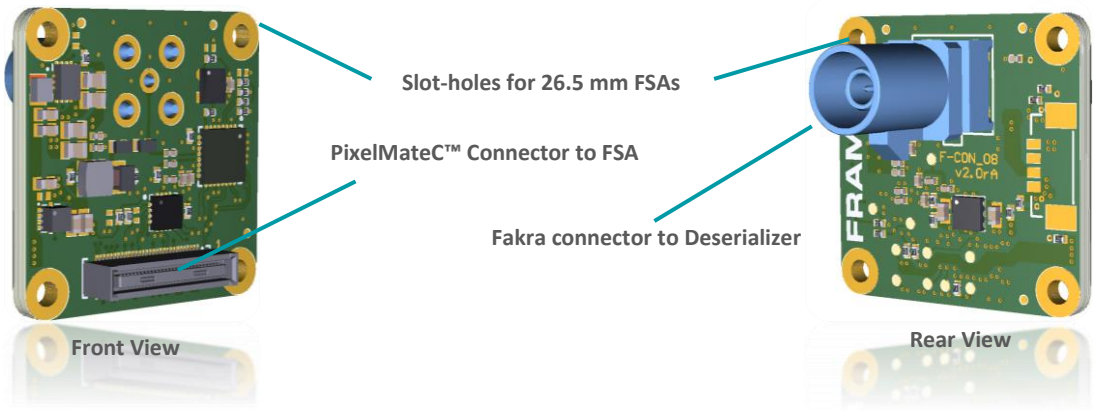
Lable: J1
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSA
Compatibility: FSA-FTx/A



9.1.2 **FFA-GMSL-Ser-V2A** (Serializer, Sensor Side)

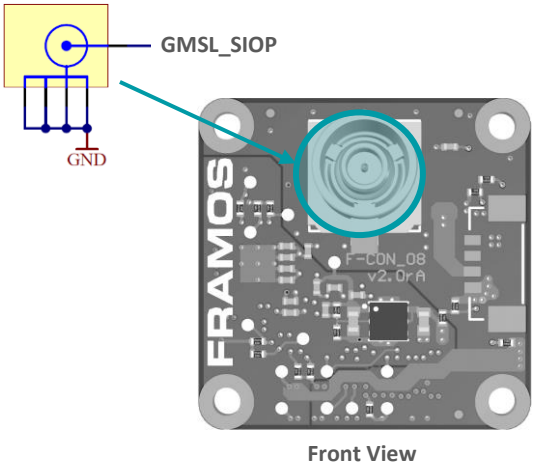
Serializer board acting as transmitter (TX), connecting to FSM+FSA stack serializing image data, embedding of bidirectional communication and sensor GPIOs. Connects to PixelMateC and outputs GMSL on Fakra type connector.

- 4-Lane MIPI CSI-2 Input
- Supporting 6 / 12 Gbps output modes
- Generic supply voltage (3V8, 1V8) recovery from PoC
- **V2A**: 26.5 mm footprint[3]
- GPIOs and I2C Communication via MFP/ I2C Extender
- Testpoints to important signals
- Compatible to GMSL 6 / 12 Gbps compliant receivers.



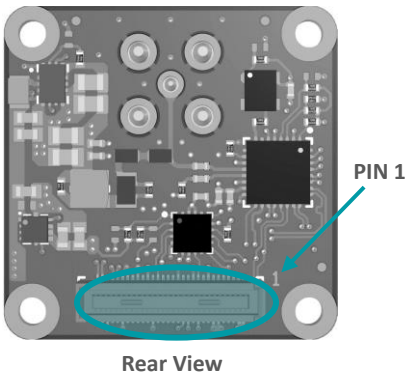
Fakra / GMSL Connector

Lable: J2
Type: 2FA1-NZSP-PCBB6
Pinout:



PixelMateC Connector

Lable: J1
Type: DF40HC(4.0)-60DS-0.4V
Pinout: According to FSA
Compatibility: FSA-FTx/A

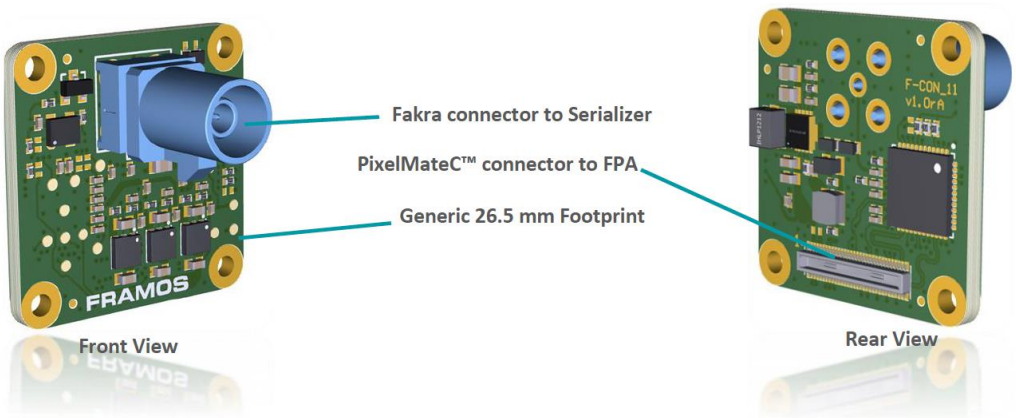


[3] Supports piggyback / board-to-board stacking only with 26.5 mm boards. Compatible to 28 mm footprint using PixelMateC Flex Cable.

9.1.3 **FFA-GMSL-Des-V1A** (Deserializer, Processor Side)

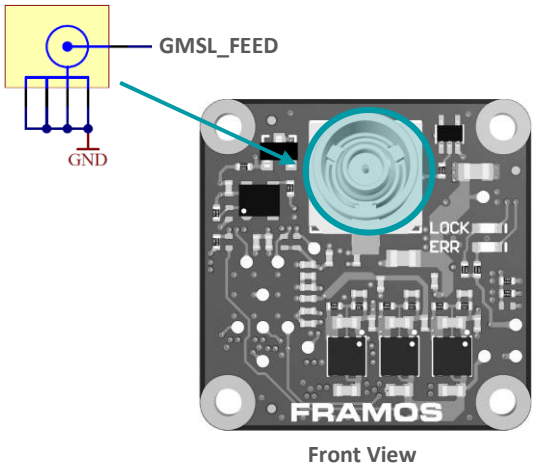
The deserializer board acts as a receiver (RX) by converting GMSL data (on the input) to FPA or Carrier boards using the PixelMateC interface. This board comes in two variants, namely **FFA-GMSL-Des-V1A** and **FFS-GMSL-Des-V2A**, both of which are responsible for deserializing image data, embedding bidirectional communication, and sensor GPIOs. They connect to the PixelMateC interface and output GMSL through a Fakra-type connector. The key features of the deserializer board are listed below, along with the differences between the V1A and V2A variants.

- Supporting 6 / 12 Gbps input modes
- 4-Lane MIPI CSI-2 Output
- Maximum one GMSL chain supported per FPA/Carrier
- GPIOs and I2C Communication via MFP / I2C Extender
- Testpoints to important signals
- Power over Coax (PoC) Injection



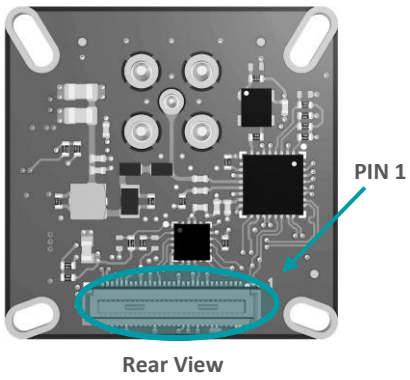
Fakra / GMSL Connector

Lable: J2
Type: 2FA1-NZSP-PCBB6
Pinout:



PixelMateC Connector

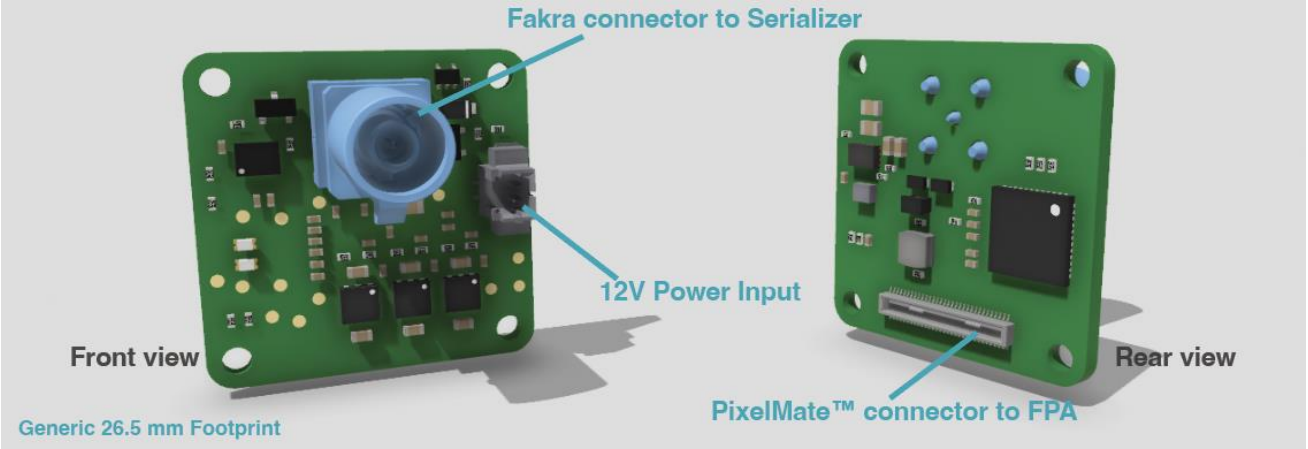
Lable: J1
Type: DF40C-60DP-0.4V
Pinout: Refer to Table 15
Compatibility: FSA-FTx/A



9.1.4 **FFA-GMSL-Des-V2A** (Deserializer, Processor Side)

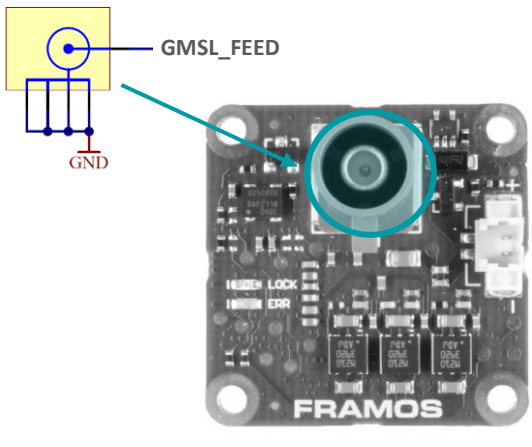
The deserializer board acts as a receiver (RX) by converting GMSL data (on the input) to FPA or Carrier boards using the PixelMateC interface. This board comes in two variants, namely **FFA-GMSL-Des-V1A** and **FFS-GMSL-Des-V2A**, both of which are responsible for deserializing image data, embedding bidirectional communication, and sensor GPIOs. They connect to the PixelMateC interface and output GMSL through a Fakra-type connector. The key features of the deserializer board are listed below, along with the differences between the V1A and V2A variants.

- Supporting 6 / 12 Gbps input modes
- 4-Lane MIPI CSI-2 Output
- Power over Coax (PoC) Injection
- V2A variant allows a separate, carrier independent power input
- GPIOs and I2C Communication via MFP / I2C Extender
- Testpoints to important signals
- Supports multi-sensor operation on the FPA/Carrier



Fakra / GMSL Connector

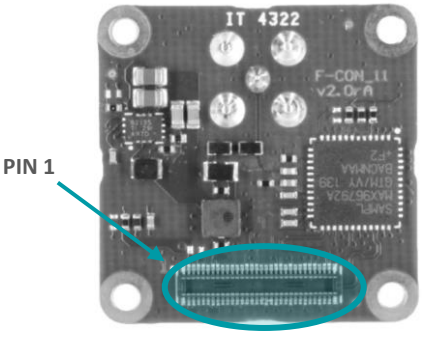
Lable: J2
Type: 2FA1-NZSP-PCBB6
Pinout:



Front View

PixelMateC Connector

Lable: J1
Type: DF40C-60DP-0.4V
Pinout: Refer to Table 15
Compatibility: FSA-FTx/A



Rear View

Pinout: J1 (PixelMateC)

Pin #	Name	Pin #	Name
1	3V8_VDD	2	1V8_VDD
3	3V8_VDD	4	1V8_VDD
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	GND	12	GND
13	GND	14	GND
15	RST_0	16	RST_1
17	NC	18	NC
19	NC	20	NC
21	I2C_0_SCL(SPI_SCK)	22	NC
23	NC	24	NC
25	GPIO1(XVS0)	26	NC
27	I2C_0_SDA(SPI_MOSI)	28	NC
29	GPIO2(XHS0)	30	GPIO10(XTRIG1)
31	GPIO3(XTRIG0)	32	NC
33	PW_EN_0	34	PW_EN_1
35	NC	36	NC
37	GND	38	GND
39	MCLK_0	40	NC
41	NC	42	NC
43	GND	44	GND
45	NC	46	D_DATA_3_P
47	NC	48	D_DATA_3_N
49	GND	50	GND
51	D_DATA_0_N	52	D_DATA_1_N
53	D_DATA_0_P	54	D_DATA_1_P
55	GND	56	GND
57	D_DATA_2_P	58	D_CLK_0_P
59	D_DATA_2_N	60	D_CLK_0_N

*Table 15: Pinout of FFA-GMSL-Des-V**X**A, connector to FRAMOS Processor Adapter (FPA)*

Device Details:

The FFA-GMSL-Des-V2A deserializer is similar to the V1A variant. However, it moves the PoC power source to an external power supply, making it independent of power limitations imposed by the FPA or carrier board. As a result, it can support demanding sensors as well as multi-sensor operation on the FPA/Carrier, whereas the V1A variant only supports one sensor. One GMSL deserializer physically supports 6 or 12 Gbps GMSL input, and one MIPI CSI-2 output via PixelMate™. The **V2A** deserializer receives power from a **required** external 12V power supply before being converted down by a switching buck converter to 8V, which is then available through Power over Coax (PoC):

Note: To provide power to the V2A deserializer, an external 12 V power supply is required. A power rating of 12 VDC, 1 A is recommended.

It is important to note that though 6 Gbps is physically supported in the V2A variant of the deserializer, NVIDIA Jetpack JP5.1 only supports the 12 Gbps speed.

9.2 FFA-FFC – PixelMateC to FFC Adapters

Two small format boards (FFA-A/FFC and FFA-FFC/A) are available which adapt the PixelMateC MIPI CSI-2 connector to an unshielded Flat Flexible Cable (FFC) and back. This allows the connection of affordable and highly available FFC cabling in different lengths between the front-end and the receiver for evaluation purposes and as reference for integrated solutions on custom basis.

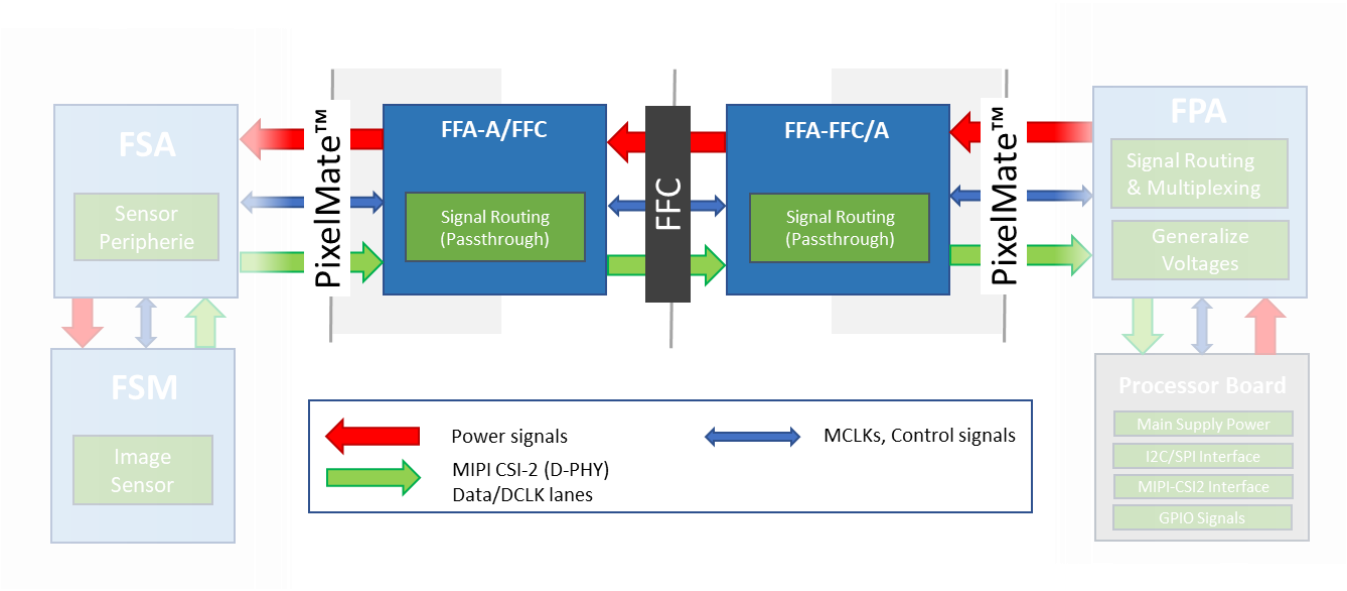
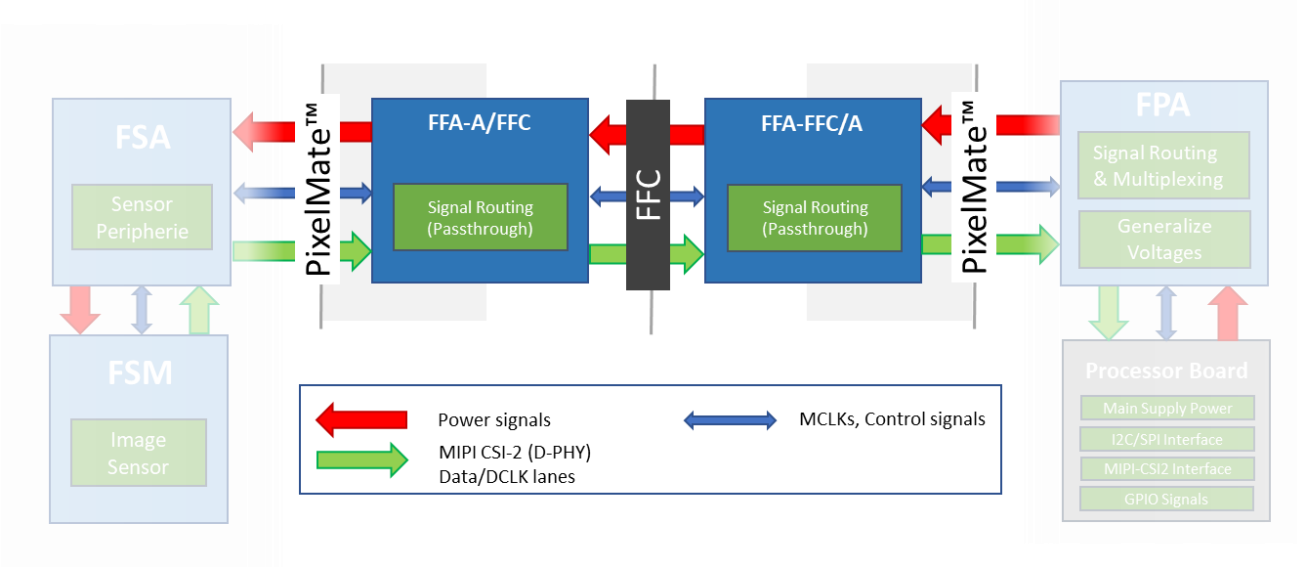


Figure 12: System Diagram of FFA-A/FFC and FFA-FFC/A inside the FSM Ecosystem.



As shown in figure 12, the integration takes place in form of two FFAs, adapting from PixelMateC to FFC and back. The boards only take care about signal routing from one to the other connector, signals pass through and stay unaltered.

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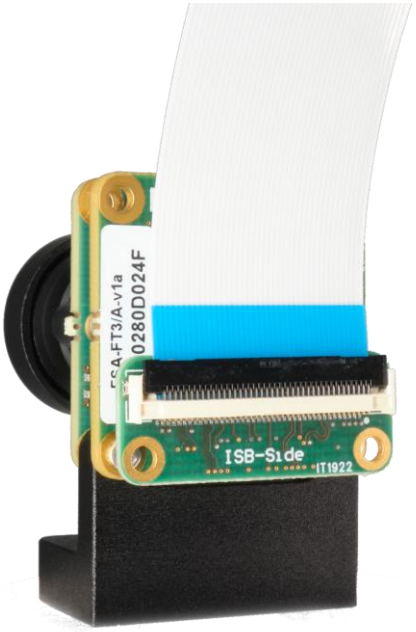


Figure 13: FFA-A/FFC Connected to FSM+FSA Stack (Front-End)

Cabling

For the cabling, an unshielded standard 40 pin FFC cable with 0.5 mm pitch is required. For signal matching, a TOP to BOTTOM cable (like the Molex 0150200440 or 0150200446) must be used in-between both adapters.

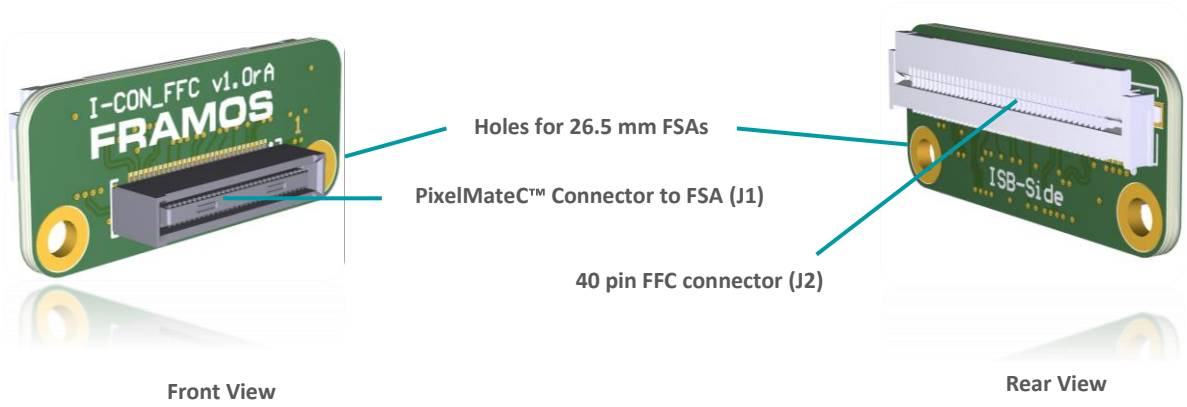
Due to the reduction from 60 pins to 40 pins, a couple of signals were dropped from the PixelMateC layout. The following signals are not available when using the FFC cable:

- RST1 (1)
- Second I2C (2)
- MCLK 1, 2, 3 (3)
- GPIOs: 14, 15, 8, 17, 9, 10, 11 (7)
- SLAMODE 1, 2, 3 (3)
- Second MIPI CLK (2)
- GND (2)

Regular single sensor setups in the FSM Ecosystem (native CSI-2 or converted from SLVS) do not use these signals and are not affected by missing signals. The complete pinout can be found in the following adapter-specific chapters.

9.2.1 **FFA-A/FFC40-V1A** (PixelMateC to 40 pin FFC, Sensor / FSA Side)

The FFA-A/FFC40 board adapts the output of the front-end (FSM+FSA stack) to utilize an appropriate FFC cable. The pin count is reduced from 60 pins to 40 pins; signals stay untouched.



FFC Connector

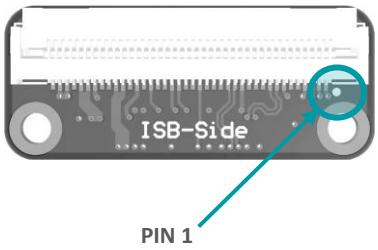
Lable: J2 Type: Molex 5051104091 Pin Count: 40 pin Pitch: 0.5 mm Shielding Connector / Cable: No / No	**Pinout**			
	1	GND	21	GPIO3(XTRIG0)
	2	D_CLK_0_N	22	GPIO2(XHS0)
	3	D_CLK_0_P	23	GPIO1(XVS0)
	4	GND	24	I2C_0_SDA(SPI_MOSI)
	5	D_DATA_2_N	25	I2C_0_SCL(SPI_SCK)
	6	D_DATA_2_P	26	GPIO0(XMASTER0)
	7	GND	27	RST_0
	8	D_DATA_1_P	28	AUX_V
	9	D_DATA_1_N	29	AUX_IF
	10	GND	30	AUX_DIG
	11	D_DATA_0_P	31	AUX_DIG
	12	D_DATA_0_N	32	AUX_ANA
	13	GND	33	AUX_ANA
	14	D_DATA_3_N	34	GND
	15	D_DATA_3_P	35	1V8_VDD
	16	GND	36	1V8_VDD
	17	MCLK_0	37	GND
	18	GND	38	3V8_VDD
	19	PW_EN_1	39	3V8_VDD
	20	PW_EN_0	40	GND

Table 16: FFC Connector on FFA-A/FFC40

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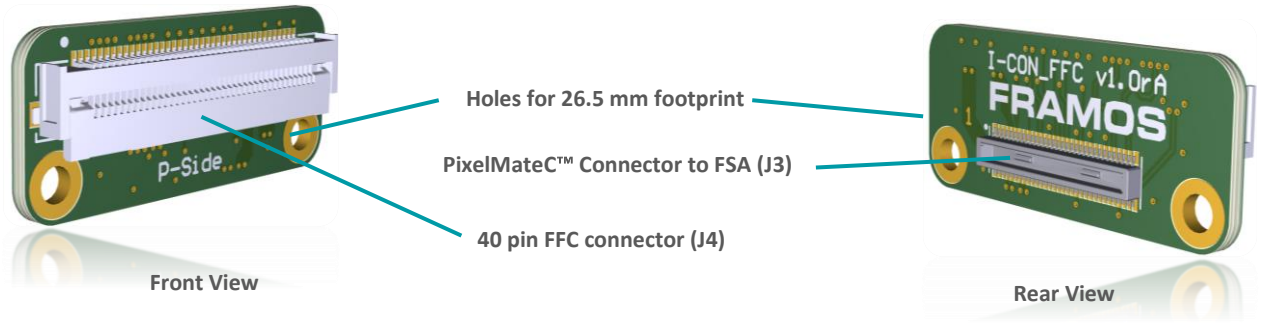
9.2.2 **FFA-FFC40/A-V1A** (40 pin FFC to PixelMateC, Processor Side)

Adapting the FFC cable coming from a front-end with FFA-A/FFC back to PixelMateC.



FFC Connector

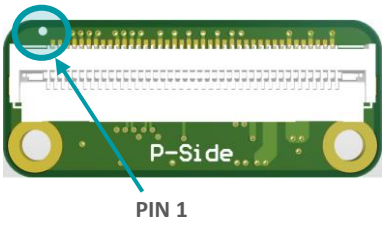
Lable: J4 Type: Molex 5051104091 Pin Count: 40 pin Pitch: 0.5 mm Shielding Connector / Cable: No / No	**Pinout**			
	1	GND	21	GPIO3(XTRIG0)
	2	D_CLK_0_N	22	GPIO2(XHS0)
	3	D_CLK_0_P	23	GPIO1(XVS0)
	4	GND	24	I2C_0_SDA(SPI_MOSI)
	5	D_DATA_2_N	25	I2C_0_SCL(SPI_SCK)
	6	D_DATA_2_P	26	GPIO0(XMASTER0)
	7	GND	27	RST_0
	8	D_DATA_1_P	28	AUX_V
	9	D_DATA_1_N	29	AUX_IF
	10	GND	30	AUX_DIG
	11	D_DATA_0_P	31	AUX_DIG
	12	D_DATA_0_N	32	AUX_ANA
	13	GND	33	AUX_ANA
	14	D_DATA_3_N	34	GND
	15	D_DATA_3_P	35	1V8_VDD
	16	GND	36	1V8_VDD
	17	MCLK_0	37	GND
	18	GND	38	3V8_VDD
	19	PW_EN_1	39	3V8_VDD
	20	PW_EN_0	40	GND

Table 17: FFC Connector on FFA-FFC40/A

9.3 FFA-MC – PixelMateC to Micro Coax Adapters

Small format boards adapting from the sophisticated PixelMateC MIPI CSI-2 connector to a shielded micro coaxial cable and back. Allowing the connection of special customized, flexible and round cabling made for cable routing through challenging and winding enclosures at great environmental robustness. As a component of the FSM Ecosystem, they aim for evaluation purpose and are a reference to be integrated into custom solutions.

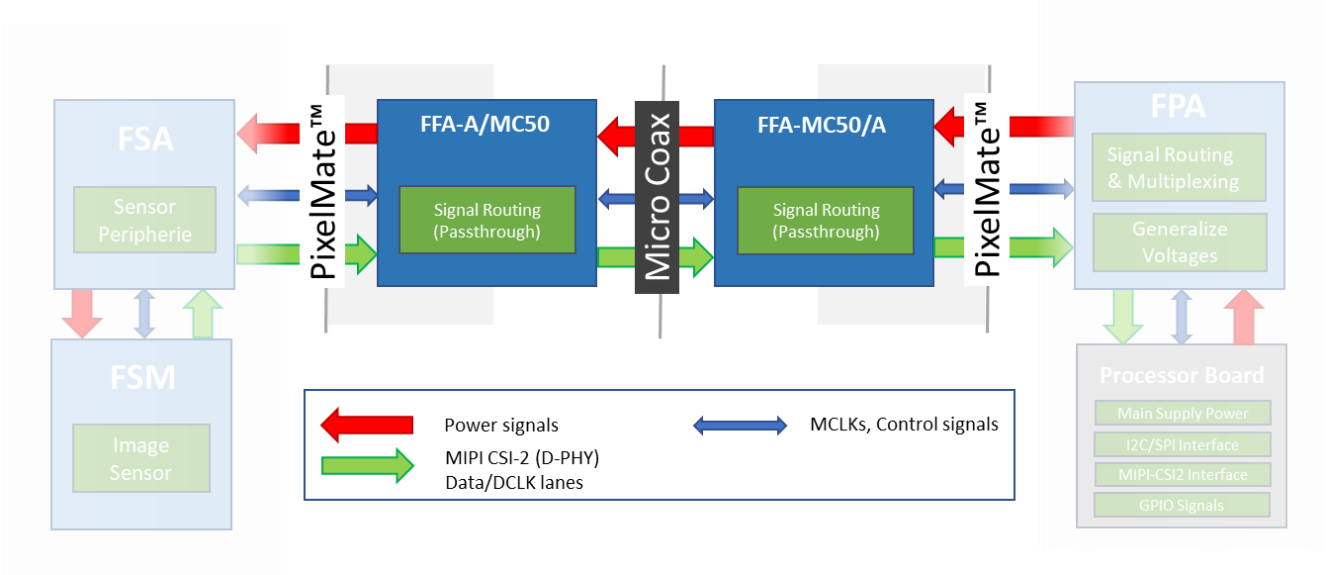


Figure 14: System Diagram of FFA-A/MC50 and FFA-MC50/A inside the FSM Ecosystem.

As shown in Figure 11, the integration takes place in form of two FFAs, adapting from PixelMateC to micro coax and back. The boards only take care about signal routing from one to the other connector, signals pass through and stay unaltered.

Figure 15: FFA-A/MC50 Connected to FSM+FSA Stack (Front-End)

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Cabling

For the cabling, a shielded, 50 pin micro coaxial cable with 0.4 mm pitch and 1:1 pin assignment on both ends is required. Please refer to Chapter 9.3.3 – “FMA-CBL-MC50-0.3m-V1A – Micro Coax Cable” for a recommended reference assembly.

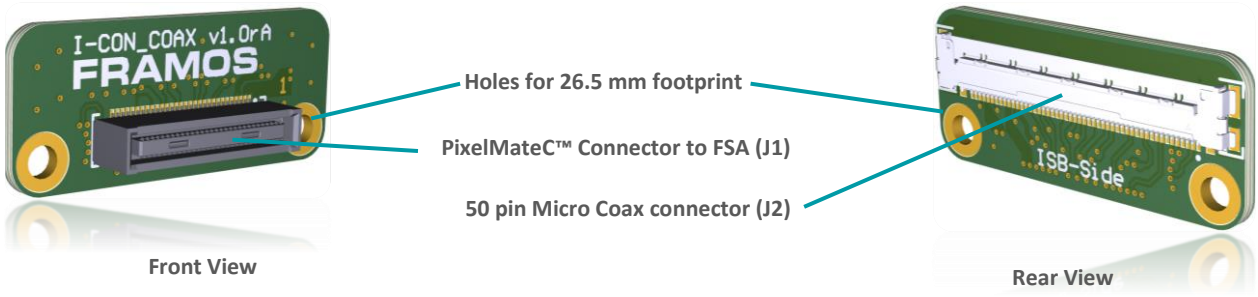
Due to the reduction from 60 to 50 pins, a couple of signals are dropped from the PixelMateC layout. The following signals are not available:

- Second I2C (2)
- MCLK 1, 2, 3 (3)
- Second MIPI CLK (2)
- GND (3)

Regular single sensor setups in the FSM Ecosystem (native CSI-2 or converted from SLVS) do not use these signals and are not affected by missing signals. The complete pinout can be found in the following, adapter specific, chapters.

9.3.1 **FFA-A/MC50-V1A** (PixelMateC to 50 pin Micro Coax, Sensor / FSA Side)

Adapting the output of the front-end (FSM+FSA stack) to utilize an appropriate Micro Coax cable. Pin count is reduced from 60 pins to 50 pins, signals stay untouched.



Micro Coax Connector

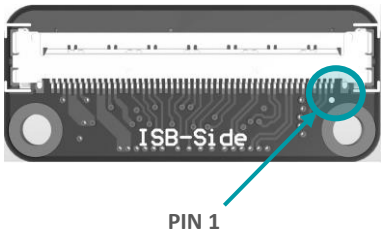
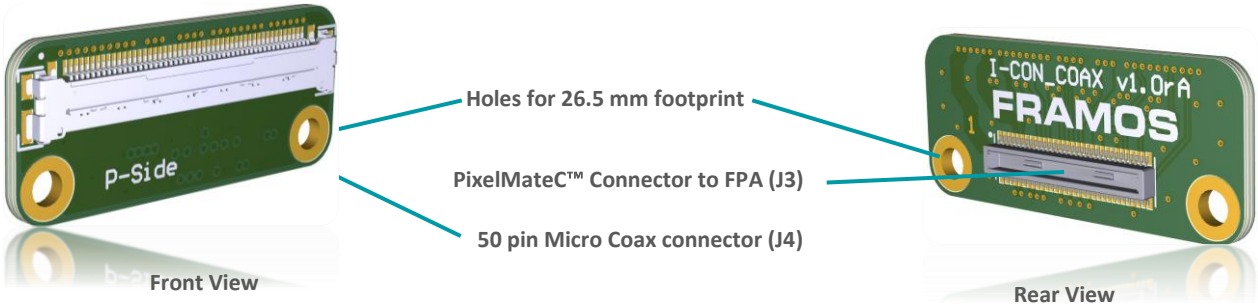
Lable: J2 Type: I-PEX 20525-050E-02 Pin Count: 50 pin Pitch: 0.4 mm Shielding: Yes	**Pinout**			
	1	GND	26	I2C_0_SDA(SPI_MOSI)
	2	D_CLK_0_N	27	GPIO9
	3	D_CLK_0_P	28	GPIO1(XVS0)
	4	GND	29	GPIO16(SYS_PW_EN)
	5	D_DATA_2_N	30	GPIO17(SPI_CS)
	6	D_DATA_2_P	31	I2C_0_SCL(SPI_SCK)
	7	GND	32	GPIO8
	8	D_DATA_1_P	33	GPIO0(XMASTER0)
	9	D_DATA_1_N	34	GPIO15(SPI_MISO)
	10	GND	35	GPIO14
	11	D_DATA_0_P	36	RST_1
	12	D_DATA_0_N	37	RST_0
	13	GND	38	GND
	14	D_DATA_3_N	39	AUX_V
	15	D_DATA_3_P	40	AUX_IF
	16	GND	41	AUX_DIG
	17	MCLK_0	42	AUX_DIG
	18	GPIO7	43	AUX_ANA
	19	GPIO6	44	AUX_ANA
	20	PW_EN_1	45	GND
	21	PW_EN_0	46	1V8_VDD
	22	GPIO11	47	1V8_VDD
	23	GPIO3(XTRIG0)	48	GND
	24	GPIO10	49	3V8_VDD
	25	GPIO2(XHS0)	50	3V8_VDD

Table 18: FFC Connector on FFA-A/MC50

9.3.2 **FFA-MC50/A-V1A** (50 pin FFC to PixelMateC, Processor Side)

Adapting the output of the front-end (FSM+FSA stack) to utilize an appropriate Micro Coax cable. Pin count is reduced from 60 pins to 50 pins, signals stay untouched.



FFC Connector

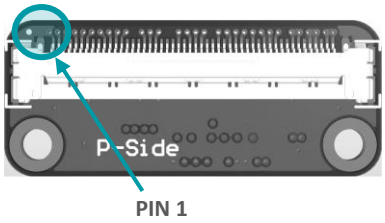
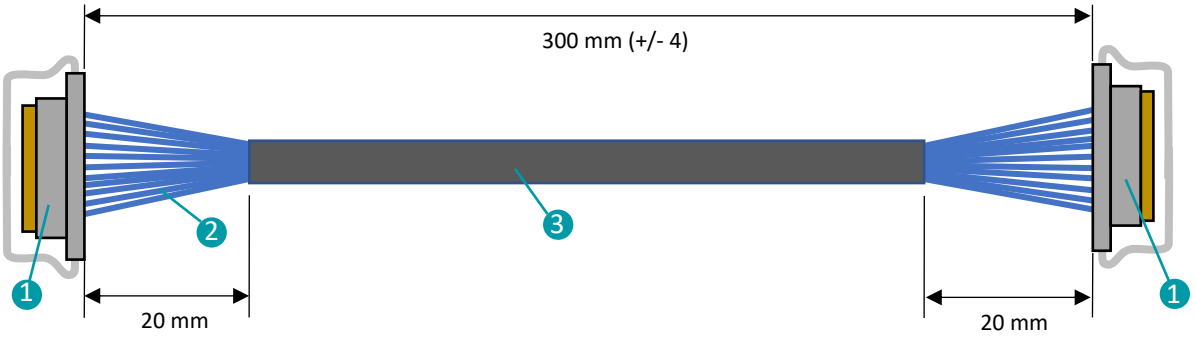
Lable: J4 Type: I-PEX 20525-050E-02 Pin Count: 50 pin Pitch: 0.4 mm Shielding: Yes	**Pinout**			
	1	GND	26	I2C_0_SDA(SPI_MOSI)
	2	D_CLK_0_N	27	GPIO9
	3	D_CLK_0_P	28	GPIO1(XVS0)
	4	GND	29	GPIO16(SYS_PW_EN)
	5	D_DATA_2_N	30	GPIO17(SPI_CS)
	6	D_DATA_2_P	31	I2C_0_SCL(SPI_SCK)
	7	GND	32	GPIO8
	8	D_DATA_1_P	33	GPIO0(XMASTER0)
	9	D_DATA_1_N	34	GPIO15(SPI_MISO)
	10	GND	35	GPIO14
	11	D_DATA_0_P	36	RST_1
	12	D_DATA_0_N	37	RST_0
	13	GND	38	GND
	14	D_DATA_3_N	39	AUX_V
	15	D_DATA_3_P	40	AUX_IF
	16	GND	41	AUX_DIG
	17	MCLK_0	42	AUX_DIG
	18	GPIO7	43	AUX_ANA
	19	GPIO6	44	AUX_ANA
	20	PW_EN_1	45	GND
	21	PW_EN_0	46	1V8_VDD
	22	GPIO11	47	1V8_VDD
	23	GPIO3(XTRIG0)	48	GND
	24	GPIO10	49	3V8_VDD
	25	GPIO2(XHS0)	50	3V8_VDD

Table 19: FFC Connector on FFA-FFC40/A

9.3.3 FMA-CBL-MC50-0.3m-V1A – Micro Coax Cable

Cable assembly of I-PEX connectors with micro coaxial cable. CE and RoHS compliant, various lengths are available on request. Pin assignment is 1:1.



(1) Connector: I-PEX CABLINE® -CA

- Housing: 20634-150T-02
- Shell: 2764-0501-002
- P-Bar: 2766-0501
- Shielded: Yes
- Contact Pitch (mm): 0.400
- Height: 1.10 Max (1.00 Nom.)
- Pin Count: 50
- Mating Direction: Horizontal

(2) Cable: Micro Coaxial

- Type: MCX AWG40 UL1354
- Length: 300 mm
- Color: Black

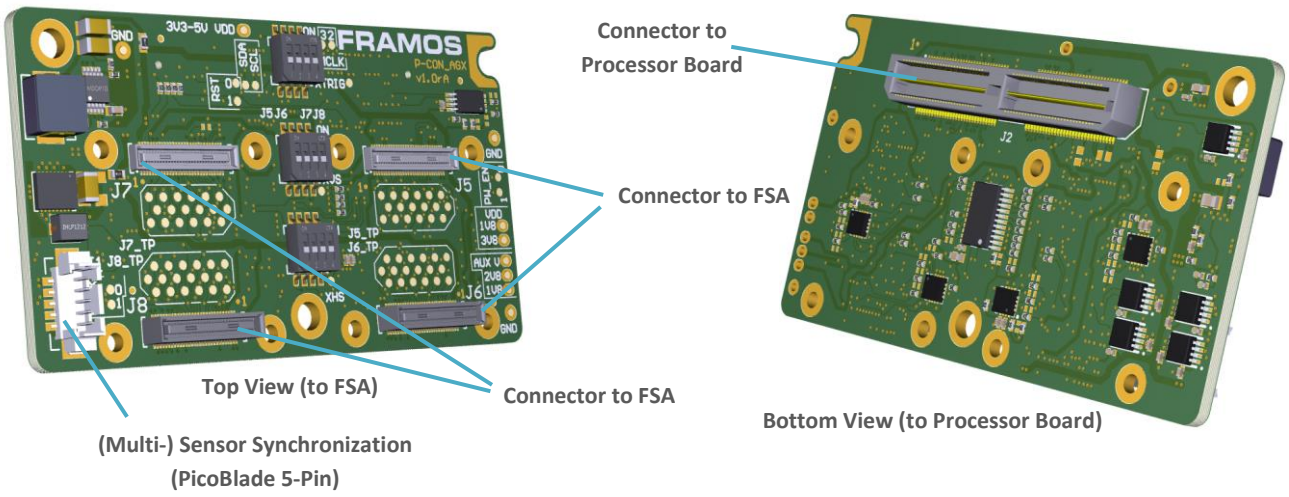
(3) Insulation Tape

10 FRAMOS Processor Adapter (FPA)

- Connects multiple FSAs to one processor board
- Processor board specific
- Differentiates two input interface types:
  - **A:** MIPI CSI-2
  - **BC:** Sub-LVDS / SLVS (**B**) and SLVS-EC (**C**)

10.1 FPA-4.A/AGX-V1A: Quad FPA to NVIDIA Jetson AGX Orin and AGX Xavier

- Adapting from PixelMate to NVIDIA Jetson AGX Developer Kit Connector
- Four 4-Lane MIPI CSI-2
- Generation of standard PixelMate power rails
- Testpoints to important sensor signals
- Enhanced sensor control signal access via I2C extender
- Synchronization and timing signal access via Molex Picoblade connector
- **Compatible Processor Boards:**
  - NVIDIA Jetson Orin AGX Development Kit
  - NVIDIA Jetson Xavier AGX Development Kit



10.1.1 Description of Connectors and Interfaces

Name	Description	Connector Type	Orientation
J1	XVS, XHS and XTRIG Signals	Molex PicoBlade, 5-Pin (53398-0571)	Pin 1 marked on PCB
J2	PixelMate to Processor Board	Samtec QTH-060-01-L-D-A	Pin 1 marked on PCB
J5	PixelMate to FSA (4x MIPI CSI-2 lanes)	Hirose DF40C-60DS-0.4V(51)	Pin 1 Printed on PCB next to each connector.
J6		Hirose DF40HC(4.0)-60DS-0.4V(51)	
J7		Hirose DF40C-60DS-0.4V(51)	
J8		Hirose DF40HC(4.0)-60DS-0.4V(51)	

Table 20: Connectors on FPA-4.A/AGX-V1A

The Pin 1 markings can be found in the following chapters along with the Pinout, as well as on the PCB in copper or silkscreen layer next to the connector.

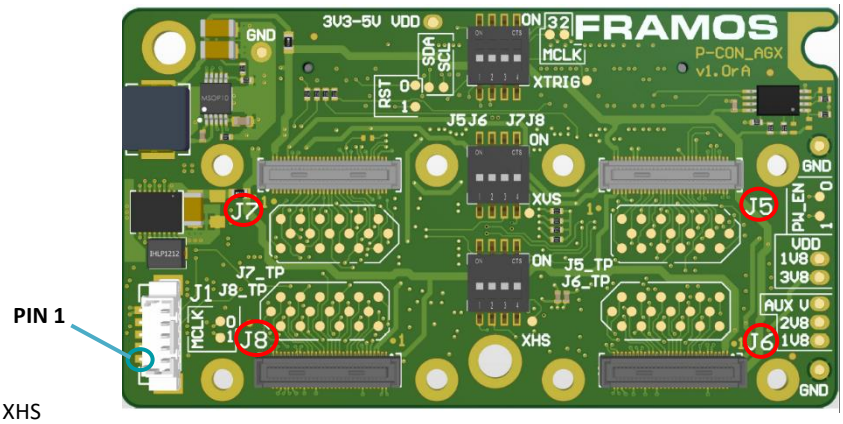
Note: All signals are routed from J5, J6, J7, J8 (to FSA) to J2 (to processor), test points and pin row. They follow the signal specification according to the FSA output interface. Control signals going to J1 (I2C, clock, GPIO) are buffered to allow voltage translation.

J1 – XVS, XHS and XTRIG Signals

Type: Molex PicoBlade, 53398-0571

Pinout:

Pin #	Name
1	1V8_VDD
2	XVS0
3	XHS0
4	XTRIG0
6	GND



Note: Switches SW1, SW2 and SW3 refer to XVS, XHS and XTRIG signals respectively. When SW1, SW2 and SW3 are off, the corresponding signals XVS0, XHS0 and XTRIG0 are not connected.

J5, J6, J7, J8 - Connectors to Sensor Adapters (FSA)

Connectors	Type
J5, J7	Hirose DF40C-60DS-0.4V(51)
J6, J8	Hirose DF40HC(4.0)-60DS-0.4V(51)

Note: The two PixelMate connectors, J5 and J7, feature a compact 1.5 mm height, enabling direct connection of 26.5x26.5mm FSM:GO or classic FSA modules onto the board through J6 and J8.

Pinout:

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	3V8_VDD	16	RST_1	31	GPIO3(XTRIG0)	46	D_DATA_D_P
2	1V8_VDD	17	NC	32	NC	47	D_CLK_B_N
3	3V8_VDD	18	NC	33	PW_EN_0	48	D_DATA_D_N
4	1V8_VDD	19	GPIO0(XMASTER0)	34	PW_EN_1	49	GND
5	2V8_AUX	20	NC	35	GPIO6(SLAMODE0)	50	GND
6	NC	21	I2C_X_SCL	36	GPIO7(SLAMODE1)	51	D_DATA_A_N
7	2V8_AUX	22	I2C_Y_SCL	37	GND	52	D_DATA_B_N
8	NC	23	NC	38	GND	53	D_DATA_A_P
9	1V8_AUX	24	GPIO16(SLAMODE2)	39	MCLK_0	54	D_DATA_B_P
10	NC	25	GPIO1(XVS0)	40	GPIO4(MCLK2)	55	GND
11	GND	26	NC	41	MCLK_1	56	GND
12	GND	27	I2C_X_SDA	42	GPIO5(MCLK3)	57	D_DATA_C_P
13	GND	28	I2C_Y_SDA	43	GND	58	D_CLK_A_P
14	GND	29	GPIO2(XHS0)	44	GND	59	D_DATA_C_N
15	RST_0	30	GPIO10(TENABLE)	45	D_CLK_B_P	60	D_CLK_A_N

Connector I2C Mapping

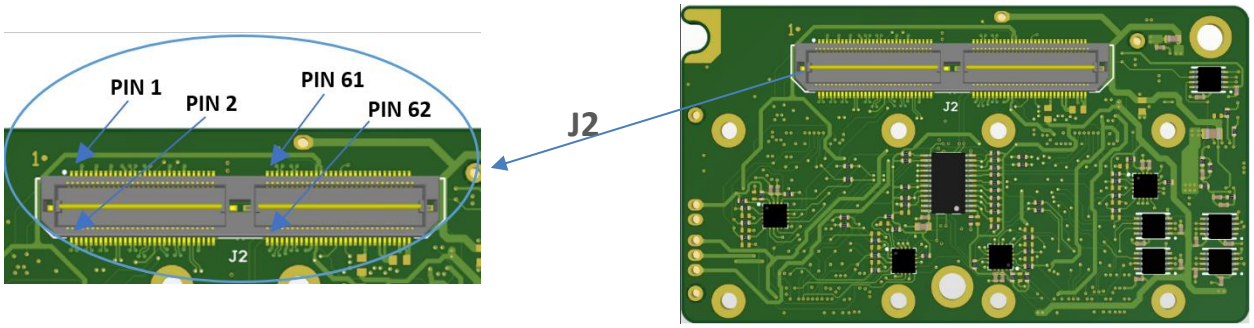
The connectors are mapped to specific ports on the I2C multiplexer. Each PixelMate is associated with two I2C lines: the primary line (I2C_X) and the auxiliary line (I2C_Y)

Connector	I2C_X	I2C_Y
J5	I2C_0	I2C_1
J6	I2C_2	I2C_3
J7	I2C_4	I2C_5
J8	I2C_6	I2C_7

MIPI CSI-2 Signal Mapping for PixelMate Connectors

PixelMate Pin	Signal Name	Signal Name on J5	Signal Name on J6	Signal Name on J7	Signal Name on J8
P:58 N:60	D_CLK_A	D_CLK_0	D_CLK_2	D_CLK_4	D_CLK_6
P:45 N:47	D_CLK_B	D_CLK_1	D_CLK_3	D_CLK_5	D_CLK_7
P:53 N:51	D_DATA_A	D_DATA_0	D_DATA_4	D_DATA_8	D_DATA_12
P:54 N:52	D_DATA_B	D_DATA_1	D_DATA_5	D_DATA_9	D_DATA_13
P:57 N:59	D_DATA_C	D_DATA_2	D_DATA_6	D_DATA_10	D_DATA_14
P:46 N:48	D_DATA_D	D_DATA_3	D_DATA_7	D_DATA_11	D_DATA_15

J2: Connector to Processor Board



Label: J2

Type: Samtec QTH-060-01-L-D-A

Pinout:

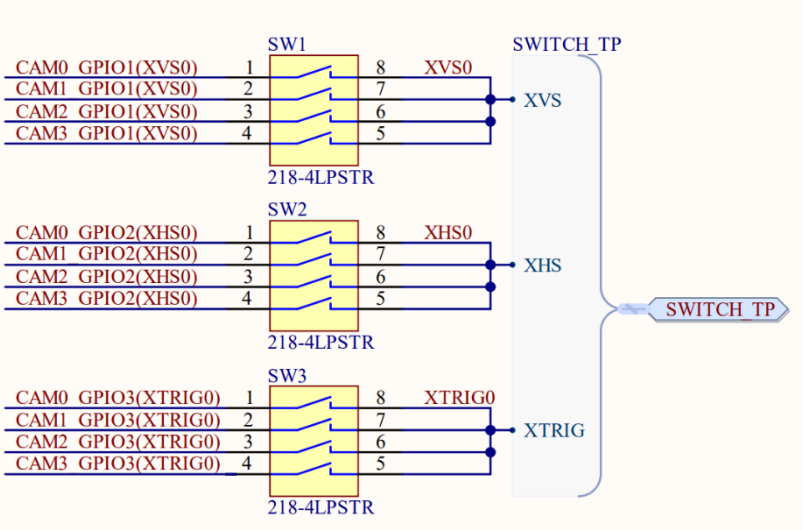
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	D_DATA_0_P	2	D_DATA_2_P	61	D_DATA_10_N	62	D_DATA_14_N
3	D_DATA_0_N	4	D_DATA_2_N	63	GND	64	GND
5	GND	6	GND	65	D_CLK_5_P	66	D_CLK_7_P
7	D_CLK_0_P	8	D_CLK_1_P	67	D_CLK_5_N	68	D_CLK_7_N
9	D_CLK_0_N	10	D_CLK_1_N	69	GND	70	GND
11	GND	12	GND	71	D_DATA_11_P	72	D_DATA_15_P
13	D_DATA_1_P	14	D_DATA_3_P	73	D_DATA_11_N	74	D_DATA_15_N
15	D_DATA_1_N	16	D_DATA_3_N	75	I2C_SCL	76	NC
17	GND	18	GND	77	I2C_SDA	78	NC
19	D_DATA_4_P	20	D_DATA_6_P	79	GND	80	GND
21	D_DATA_4_N	22	D_DATA_6_N	81	2V8_AUX	82	2V8_AUX
23	GND	24	GND	83	2V8_AUX	84	NC
25	D_CLK_2_P	26	D_CLK_3_P	85	NC	86	NC
27	D_CLK_2_N	28	D_CLK_3_N	87	NC	88	MCLK_1
29	GND	30	GND	89	NC	90	PW_EN_1
31	D_DATA_5_P	32	D_DATA_7_P	91	MCLK_0	92	RST_1
33	D_DATA_5_N	34	D_DATA_7_N	93	PW_EN_0	94	MCLK_2
35	GND	36	GND	95	RST_0	96	NC
37	D_DATA_8_P	38	D_DATA_12_P	97	NC	98	NC
39	D_DATA_8_N	40	D_DATA_12_N	99	GND	100	GND
41	GND	42	GND	101	NC	102	1V8_AUX
43	D_CLK_4_P	44	D_CLK_6_P	103	NC	104	NC
45	D_CLK_4_N	46	D_CLK_6_N	105	NC	106	NC
47	GND	48	GND	107	NC	108	3V3_VDD
49	D_DATA_9_P	50	D_DATA_13_P	109	NC	110	3V3_VDD
51	D_DATA_9_N	52	D_DATA_13_N	111	NC	112	NC
53	GND	54	GND	113	NC	114	NC
55	NC	56	NC	115	GND	116	GND
57	NC	58	NC	117	NC	118	3V3-5V_VDD
59	D_DATA_10_P	60	D_DATA_14_P	119	NC	120	3V3-5V_VDD

Table 21: Pinout of FPA-4.A/AGX-V1A connector to NVIDIA Jetson AGX Xavier and AGX Orin

10.1.2 SW1, SW2, SW3: Configuration Switches

DIP switches SW1, SW2 and SW3 are mainly for interconnecting FSA's triggering signals (XVS, XHS and XTRIG).

DIP switch SW1 is designated to interconnect XVS pins, DIP switch SW2 is designated to interconnect XHS pins and DIP switch SW3 is designated to interconnect XTRIG pins.



Default state of DIP switches

SW1 – all positions OFF (XVS pins are NOT interconnected)
SW2 – all positions OFF (XHS pins are NOT interconnected)
SW3 – all positions OFF (XTRIG pins are NOT interconnected)

I2C: Access to further Signals

The FPA contains an I2C GPIO extender (TCA6408). It allows the control of further timing uncritical signals through the I2C bus. Each connector is paired with its own dedicated I2C GPIO expander, connected to the I2C_X line. The mapping for I2C_X is as follows:

Connector	I2C_X
J5	I2C_0
J6	I2C_2
J7	I2C_4
J8	I2C_6

While all GPIO expanders share a common address (0x20), they are accessed through different I2C clock and data lines, and the specific I2C line for each connector is identified by the corresponding I2C_X value.

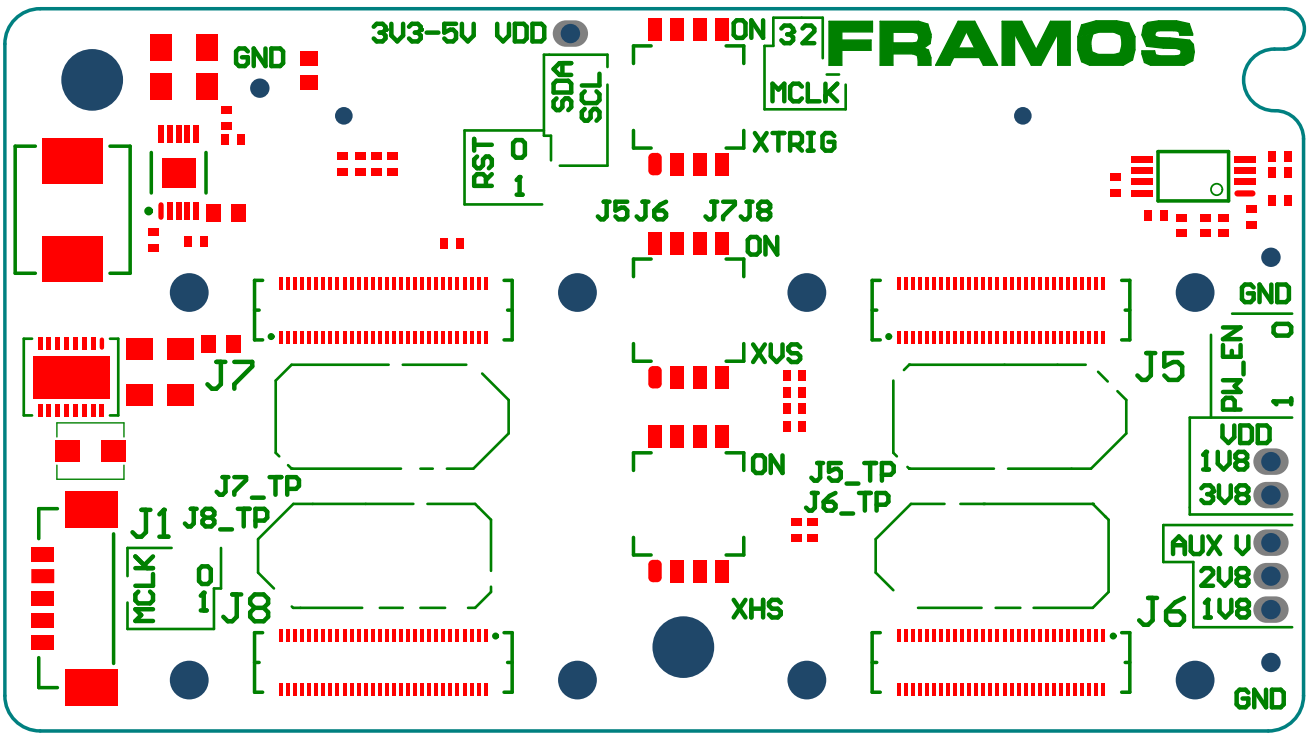
I2C Address[4]: 0x20

Pinout:

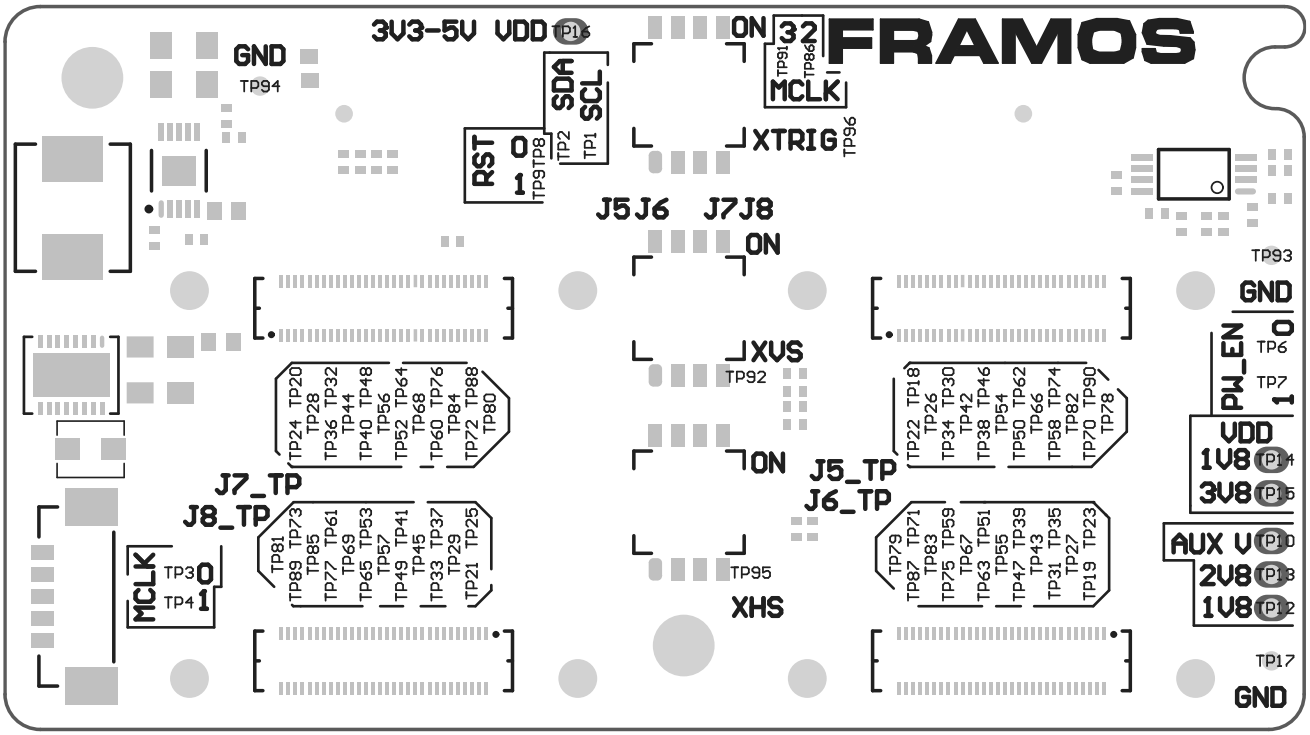
[4] Earlier revisions will listen to the I2C address: 0x21

Pin #	Name	Pixelmate PIN
P0	PW_EN_0	33
P1	PW_EN_1	34
P2	RST_0	15
P3	GPIO0(XMASTER0)	19
P4	GPIO6(SLAMODE0)	35
P5	GPIO7(SLAMODE1)	36
P6	GPIO16(SLAMODE2)	24
P7	GPIO10(TENABLE)	30

10.1.3 External Signals & Test Points



Version 1.5.0 from 2024-05-23



Connector J5: J5_TP and Ungrouped Test Points

Label	Signal	Label		Signal
TP18	CAM0_RST_0	TP62		CAM0_GPIO3(XTRIG0)
TP22	CAM0_RST_1	TP66		CAM0_PW_EN_0
TP26	CAM0_GPIO0(XMASTER0)	TP70		CAM0_PW_EN_1
TP30	I2C_0_SCL(SPI_SCK)	TP74		CAM0_GPIO6
TP34	I2C_1_SCL	TP78		CAM0_GPIO7
TP38	CAM0_GPIO16(SYS_PW_EN)	TP82		CAM0_MCLK_0
TP42	CAM0_GPIO1(XVS0)	TP86		GPIO4(MCLK2)
TP46	I2C_0_SDA(SPI_MOSI)	TP90		CAM0_MCLK_1
TP50	I2C_1_SDA	TP91		GPIO5(MCLK3)_TP
TP54	CAM0_GPIO2(XHS0)			
TP58	CAM0_GPIO10			

Connector J6: J6_TP Test Points

Label	Signal	Label	Signal
TP19	CAM1_RST_0_TP	TP63	CAM1_GPIO3(XTRIG0)_TP
TP23	CAM1_RST_1_TP	TP67	CAM1_PW_EN_0_TP
TP27	CAM1_GPIO0(XMASTER0)_TP	TP71	CAM1_PW_EN_1_TP
TP31	I2C_2_SCL(SPI_SCK)_TP	TP75	CAM1_GPIO6_TP
TP35	I2C_3_SCL_TP	TP79	CAM1_GPIO7_TP
TP39	CAM1_GPIO16(SYS_PW_EN)_TP	TP83	CAM1_MCLK_0_TP
TP43	CAM1_GPIO1(XVS0)_TP	TP87	CAM1_MCLK1_TP
TP47	I2C_2_SDA(SPI_MOSI)_TP		
TP51	I2C_3_SDA_TP		
TP55	CAM1_GPIO2(XHS0)_TP		
TP59	CAM1_GPIO10_TP		

Connector J7: J7_TP Test Points

Label	Signal	Label	Signal
TP20	CAM2_RST_0_TP	**TP64**	CAM2_GPIO3(XTRIG0)_TP
TP24	CAM2_RST_1_TP	**TP68**	CAM2_PW_EN_0_TP
TP28	CAM2_GPIO0(XMASTER0)_TP	**TP72**	CAM2_PW_EN_1_TP
TP32	I2C_4_SCL(SPI_SCK)_TP	**TP76**	CAM2_GPIO6_TP
TP36	I2C_5_SCL_TP	**TP80**	CAM2_GPIO7_TP
TP40	CAM2_GPIO16(SYS_PW_EN)_TP	**TP84**	CAM2_MCLK_0_TP
TP44	CAM2_GPIO1(XVS0)_TP	**TP88**	CAM2_MCLK1_TP
TP48	I2C_4_SDA(SPI_MOSI)_TP		
TP52	I2C_5_SDA_TP		
TP56	CAM2_GPIO2(XHS0)_TP		
TP60	CAM2_GPIO10_TP		

Connector J8: J8_TP Test Points

Label	Signal	Label	Signal
TP21	CAM3_RST_0_TP	**TP65**	CAM3_GPIO3(XTRIG0)_TP
TP25	CAM3_RST_1_TP	**TP69**	CAM3_PW_EN_0_TP
TP29	CAM3_GPIO0(XMASTER0)_TP	**TP73**	CAM3_PW_EN_1_TP
TP33	I2C_6_SCL(SPI_SCK)_TP	**TP77**	CAM3_GPIO6_TP
TP37	I2C_7_SCL_TP	**TP81**	CAM3_GPIO7_TP
TP41	CAM3_GPIO16(SYS_PW_EN)_TP	**TP85**	CAM3_MCLK_0_TP
TP45	CAM3_GPIO1(XVS0)_TP	**TP89**	CAM3_MCLK1_TP
TP49	I2C_6_SDA(SPI_MOSI)_TP		
TP53	I2C_7_SDA_TP		
TP57	CAM3_GPIO2(XHS0)_TP		
TP61	CAM3_GPIO10_TP		

Other Test Points (Ungrouped)

Label	Signal
TP92	XVS0_TP
TP93	GND
TP94	GND
TP95	XHS0_TP
TP96	XTRIG0_TP

10.1.4 Technical Drawing

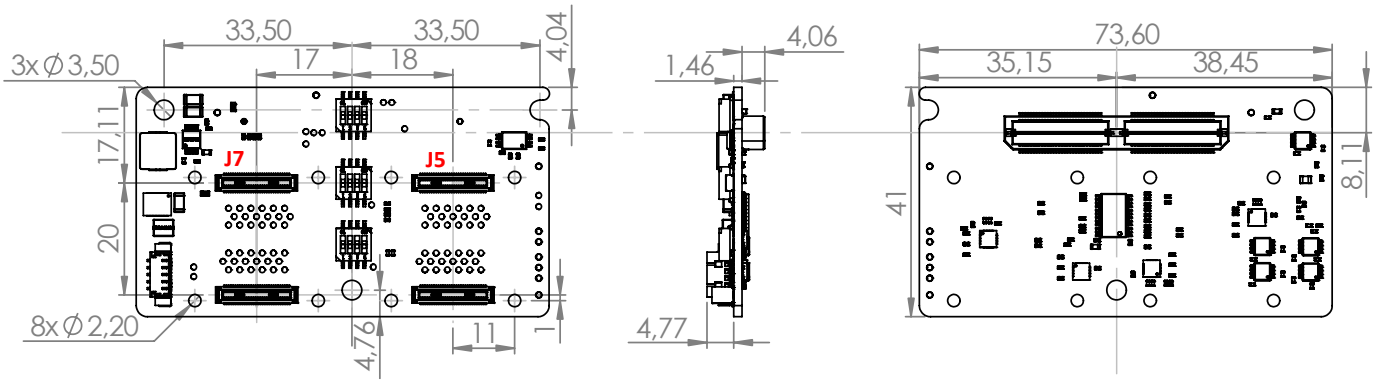
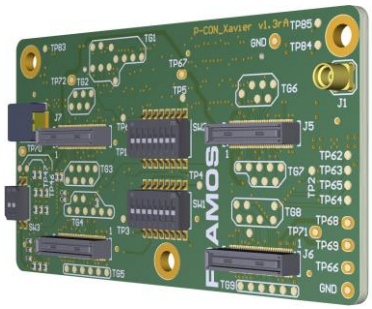


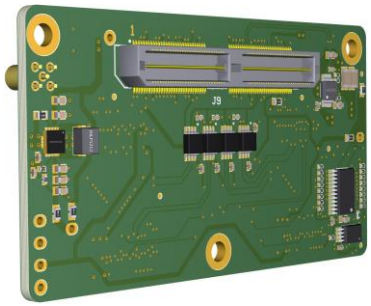
Figure 16: Technical Drawing of FPA-4.A/AGX-V1A

Note: The two PixelMate connectors, J5 and J7, feature a compact 1.5 mm height.

10.2 FPA-4.A/TXA-V1: Quad FPA to NVIDIA Jetson TX2 and AGX Xavier, AGX Orin

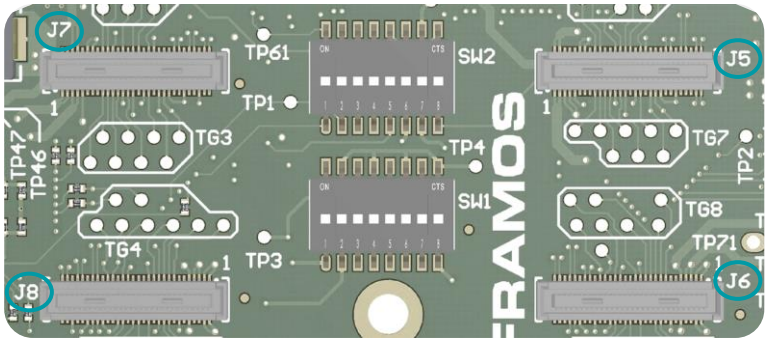
- Four 4-Lane MIPI CSI-2 Inputs
- Signal routing and I2C multiplexing
- Testpoints to important sensor signals
- Dynamic device tree management (EEPROM)
- Configuration of trigger routing
- Compatible Processor Boards:
  - NVIDIA Jetson TX2, AGX Xavier, **AGX Orin Development Kits
  - CTI Rogue (AGX101, AGX111)





**Note: The FPA-4.A/TXA V1 comes in two variants, V1B and V1C. The V1C redesign mounts to the NVIDIA® AGX Orin™ natively. The V1B requires removing a plastic cover on the NVIDIA® AGX Orin™. For more information, see 10.1.6 Technical Drawing, page 63.

10.2.1 J5, J6, J7, J8: Connectors to Sensor Adapters (FSA)



Name	Description	Connector Type	Orientation
J5	Port 1, 4-Lanes CSI-2, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	Pin 1 Printed on PCB next to each connector.
J6	Port 2, 4-Lanes CSI-2, to FSA		
J7	Port 3, 4-Lanes CSI-2 (TX2: 2-Lanes), to FSA		
J8	Port 4, 4-Lanes CSI-2 (TX2: 2-Lanes), to FSA		

Table 22: Image Sensor Connectors on FPA-4.A/TXA-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Further notes for signals on FSA connectors J5, J6, J7, J8:

CAM0_MCLK and CAM1_MCLK are routed through four bus transceivers for better integrity of the signal

CAM0_PWDN and CAM0_RST signals are routed in parallel to all connectors

I2C_GP3_CLK and I2C_GP3_DATA are routed parallel to EEPROM and I2C multiplexer (8 channels)

EEPROM functionality is primarily used to utilize functionality of L4T Plugin manager (deprecated with JetPack 4.6+ drivers) and offers additional user space for configuration etc.

Each FSA connector is connected to two multiplexer channels:

- MUX-ch0/ch1 are connected to J5
- MUX-ch2/ch3 are connected to J6
- MUX-ch4/ch5 are connected to J7
- MUX-ch6/ch7 are connected to J8

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

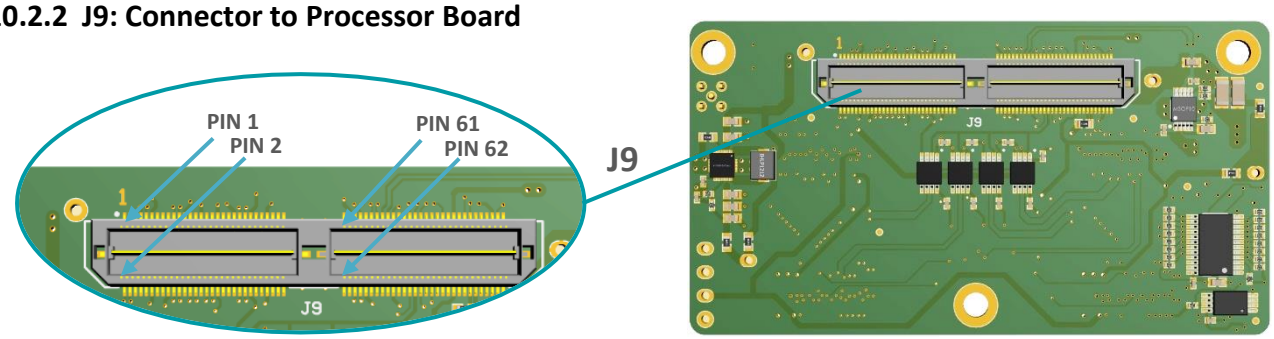
Image Sensor CSI-2 lane Support per Port

The table below shows the possible MIPI CSI-2 lane configurations per FSM / Processor Board combination, that are supported in HW using the FPA-4.A/TXA-V1.

	NVIDIA Jetson TX2				NVIDIA AGX Xavier and AGX Orin			
FSM with FSA-FTx/A (all)	**J5**	**J6**	**J7**	**J8**	**J5**	**J6**	**J7**	**J8**
FSM-AR0144	2	2	2	2	2	2	2	2
FSM-AR0521	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-AR1335	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-HDP230	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX264	4	4	-	-	4	4	4	4
FSM-IMX283	4	4	-	-	4	4	4	4
FSM-IMX290, 327	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX296, 297	1	1	1	1	1	1	1	1
FSM-IMX304	4	4	-	-	4	4	4	4
FSM-IMX334	4	4	-	-	4	4	4	4
FSM-IMX335	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX412, 477, 577	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX415, 715	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX462, 662	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX464	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX485, 585	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX530	4	4	-	-	4	4	4	4
FSM-IMX565, 568	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX675	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4
FSM-IMX678	2 / 4	2 / 4	2	2	2 / 4	2 / 4	2 / 4	2 / 4

Table 23: Image Sensor Support per Port with FPA-4.A/TXA-V1

10.2.2 J9: Connector to Processor Board



Label: J9

Type: QTH-060-01-L-D-A

Pinout:

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	D_DATA_0_P	2	D_DATA_2_P	61	D_DATA_10_N	62	D_DATA_14_N
3	D_DATA_0_N	4	D_DATA_2_N	63	GND	64	GND
5	GND	6	GND	65	D_CLK_5_P	66	D_CLK_7_P
7	D_CLK_0_P	8	D_CLK_1_P	67	D_CLK_5_N	68	D_CLK_7_N
9	D_CLK_0_N	10	D_CLK_1_N	69	GND	70	GND
11	GND	12	GND	71	D_DATA_11_P	72	D_DATA_15_P
13	D_DATA_1_P	14	D_DATA_3_P	73	D_DATA_11_N	74	D_DATA_15_N
15	D_DATA_1_N	16	D_DATA_3_N	75	I2C_SCL	76	NC
17	GND	18	GND	77	I2C_SDA	78	NC
19	D_DATA_4_P	20	D_DATA_6_P	79	GND	80	GND
21	D_DATA_4_N	22	D_DATA_6_N	81	2V8_AUX	82	2V8_AUX
23	GND	24	GND	83	2V8_AUX	84	NC
25	D_CLK_2_P	26	D_CLK_3_P	85	TP_85	86	XVS0
27	D_CLK_2_N	28	D_CLK_3_N	87	TP_87	88	MCLK_1
29	GND	30	GND	89	TP_89	90	PW_EN_1
31	D_DATA_5_P	32	D_DATA_7_P	91	MCLK_0	92	RST_1
33	D_DATA_5_N	34	D_DATA_7_N	93	PW_EN_0	94	MCLK_2
35	GND	36	GND	95	RST_0	96	NC
37	D_DATA_8_P	38	D_DATA_12_P	97	TP_97	98	NC
39	D_DATA_8_N	40	D_DATA_12_N	99	GND	100	GND
41	GND	42	GND	101	1V2_AUX	102	1V8_AUX
43	D_CLK_4_P	44	D_CLK_6_P	103	TP_103	104	TP_104
45	D_CLK_4_N	46	D_CLK_6_N	105	TP_105	106	TP_106
47	GND	48	GND	107	TP_107	108	3V3_VDD
49	D_DATA_9_P	50	D_DATA_13_P	109	NC	110	3V3_VDD
51	D_DATA_9_N	52	D_DATA_13_N	111	NC	112	TP_112
53	GND	54	GND	113	NC	114	NC
55	NC	56	NC	115	GND	116	GND
57	NC	58	NC	117	TP_117	118	3V3-5V_VDD
59	D_DATA_10_P	60	D_DATA_14_P	119	SYS_PW_EN	120	3V3-5V_VDD

Table 24: Pinout of FPA-4.A/TXA-V1 connector to NVIDIA Jetson TX2 and AGX Xavier and AGX Orin

10.2.3 SW1, SW2: Configuration Switches

DIP switches SW1 and SW2 are mainly for interconnecting FSA's triggering signals (XVS, XHS and XTRIG).

DIP switch SW1 is designated to interconnect XVS/XHS pins while DIP switch SW2 is designated to interconnect XTRIG pins and aggregate CAM2_MCLK04(MCLK2) and GPIO25_VDD_SYS_EN(SYS_PW_EN) from FPA in parallel to all FSA connectors.

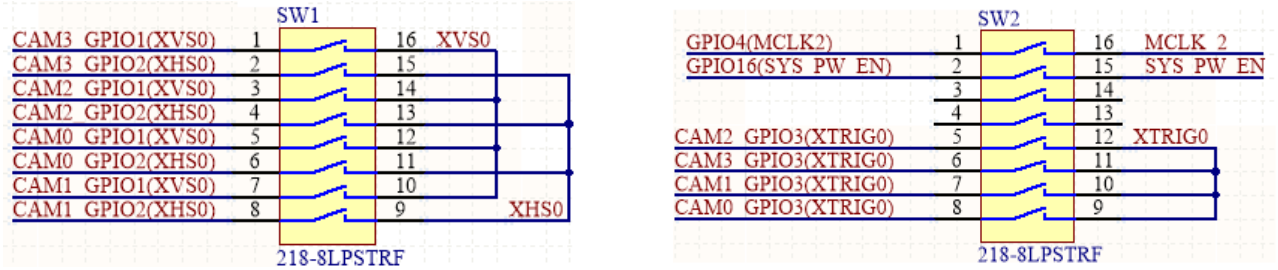


Table 25: Configuration of SW1 and SW2 on FPA-4.A/TXA-V1

10.2.4 SW3: Configuration Switches

DIP switch SW3 is designated to enable/disable FPA EEPROM and it's write protection.

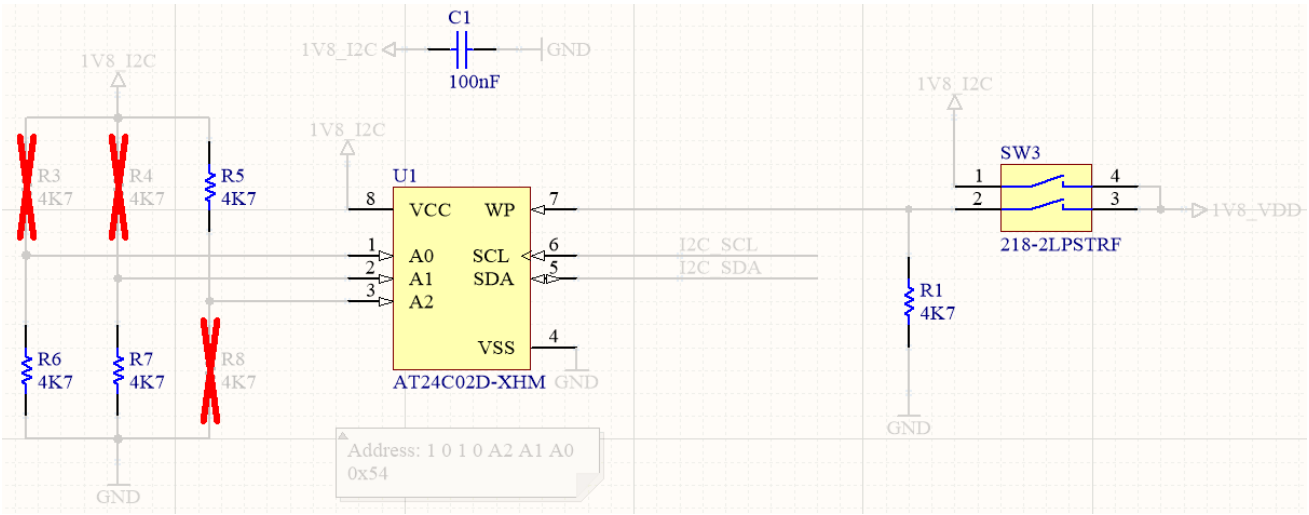


Table 26: Configuration of SW3 on FPA-4.A/TXA-V1

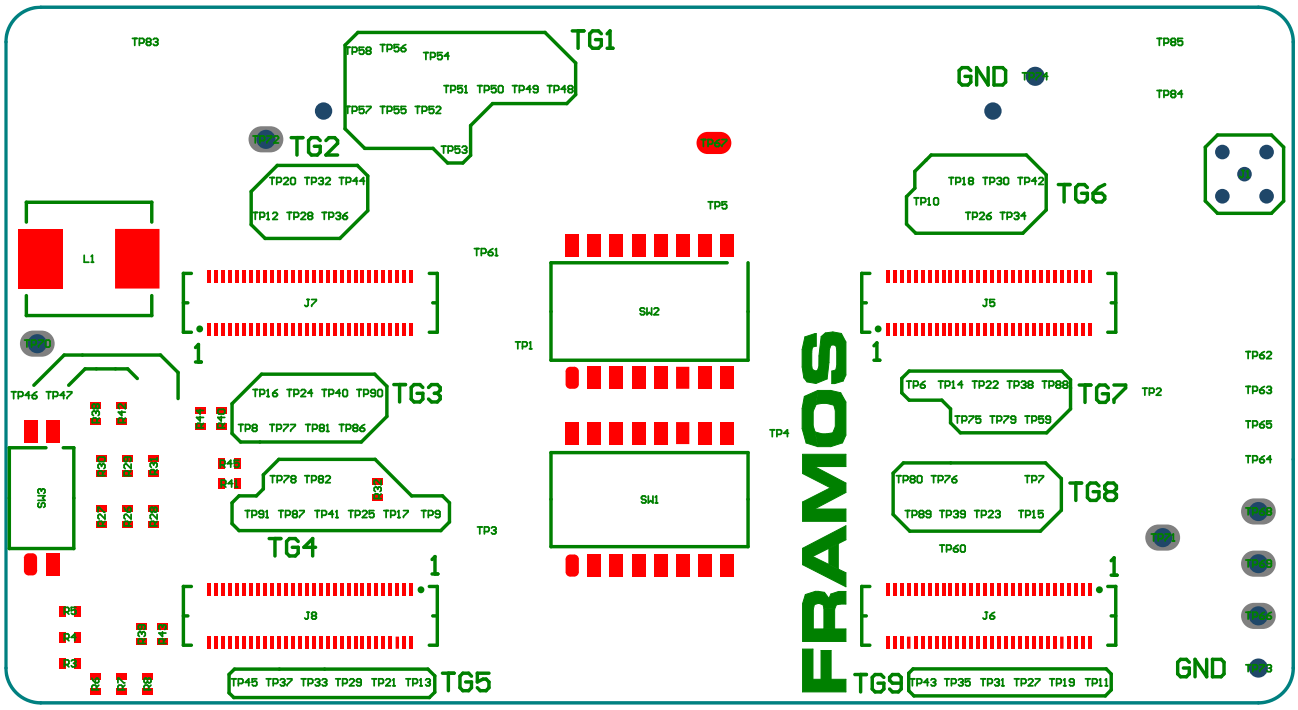
Default state of DIP switches

SW1 – all positions OFF (XVS/XHS pins are NOT interconnected)

SW2 – all positions OFF (XTRIG pins are NOT interconnected, MCLK2 and SYS_PW_EN are NOT aggregate)

SW3 – positions-1 ON, position-2 OFF (EEPROM is ENABLED without write protection)

10.2.5 TGx, TPx: Test Groups and Test Points



Connector J9: TG1 and Ungrouped Test Points

Label	Signal (TG1)	Label	Signal
TP48	TP_85	**TP46**	I2C_SCL
TP49	TP_87	**TP47**	I2C_SDA
TP50	TP_89	**TP61**	MCLK_2
TP51	TP_97	**TP62**	PW_EN_0
TP52	TP_103	**TP63**	PW_EN_1
TP53	TP_104	**TP64**	RST_0
TP54	TP_105	**TP65**	RST_1
TP55	TP_106		
TP56	TP_107		
TP57	TP_112		
TP58	TP_117		

Connector J5 (TG6, TG7) and J6 (TG8, TG9)

Label (J5)	Signal (TG6, TG7)	Label (J6)	Signal (TG8, TG9)
TP59	CAM0_MCLK_0	**TP60**	CAM1_MCLK_0
TP88	CAM0_MCLK_1	**TP89**	CAM1_MCLK_1
TP6	CAM0_GPIO14	**TP7**	CAM1_GPIO14
TP10	CAM0_GPIO15(SPI_MISO)	**TP11**	CAM1_GPIO15(SPI_MISO)
TP14	CAM0_GPIO0(XMASTER0)	**TP15**	CAM1_GPIO0(XMASTER0)
TP18	CAM0_GPIO8	**TP19**	CAM1_GPIO8
TP22	CAM0_GPIO17(SPI_CS)	**TP23**	CAM1_GPIO17(SPI_CS)
TP26	CAM0_GPIO9	**TP27**	CAM1_GPIO9
TP30	CAM0_GPIO10	**TP31**	CAM1_GPIO10
TP34	CAM0_GPIO11	**TP35**	CAM1_GPIO11
TP38	CAM0_GPIO6	**TP39**	CAM1_GPIO6
TP42	CAM0_GPIO7	**TP43**	CAM1_GPIO7
TP75	I2C_0_SCL(SPI_SCK)	**TP76**	I2C_2_SCL(SPI_SCK)
TP79	I2C_0_SDA(SPI_MOSI)	**TP80**	I2C_2_SDA(SPI_MOSI)

Version 1.5.0 from 2024-05-23

Connector J7 (TG2, TG3) and J8 (TG4, TG5)

Label (J5)	Signal (TG6, TG7)	Label (J6)	Signal (TG8, TG9)
TP86	CAM2_MCLK_0	**TP87**	CAM3_MCLK_0
TP90	CAM2_MCLK_1	**TP91**	CAM3_MCLK_1
TP8	CAM2_GPIO14	**TP9**	CAM3_GPIO14
TP12	CAM2_GPIO15(SPI_MISO)	**TP13**	CAM3_GPIO15(SPI_MISO)
TP16	CAM2_GPIO0(XMASTER0)	**TP17**	CAM3_GPIO0(XMASTER0)
TP20	CAM2_GPIO8	**TP21**	CAM3_GPIO8
TP24	CAM2_GPIO17(SPI_CS)	**TP25**	CAM3_GPIO17(SPI_CS)
TP28	CAM2_GPIO9	**TP29**	CAM3_GPIO9
TP32	CAM2_GPIO10	**TP33**	CAM3_GPIO10
TP36	CAM2_GPIO11	**TP37**	CAM3_GPIO11
TP40	CAM2_GPIO6	**TP41**	CAM3_GPIO6
TP44	CAM2_GPIO7	**TP45**	CAM3_GPIO7
TP77	I2C_4_SCL(SPI_SCK)	**TP78**	I2C_6_SCL(SPI_SCK)
TP81	I2C_4_SDA(SPI_MOSI)	**TP82**	I2C_6_SDA(SPI_MOSI)

Other Test Points (Ungrouped)

Label	Signal
TP1	GPIO16(SYS_PW_EN)
TP2	GPIO5(MCLK3)
TP3	XVS0
TP4	XHS0
TP74	GND
TP5	XTRIG0
TP83	GPIO4(MCLK2)
TP84	CAM0_GPIO2(XHS0)
TP85	CAM0_GPIO3(XTRIG0)

10.2.6 Technical Drawing

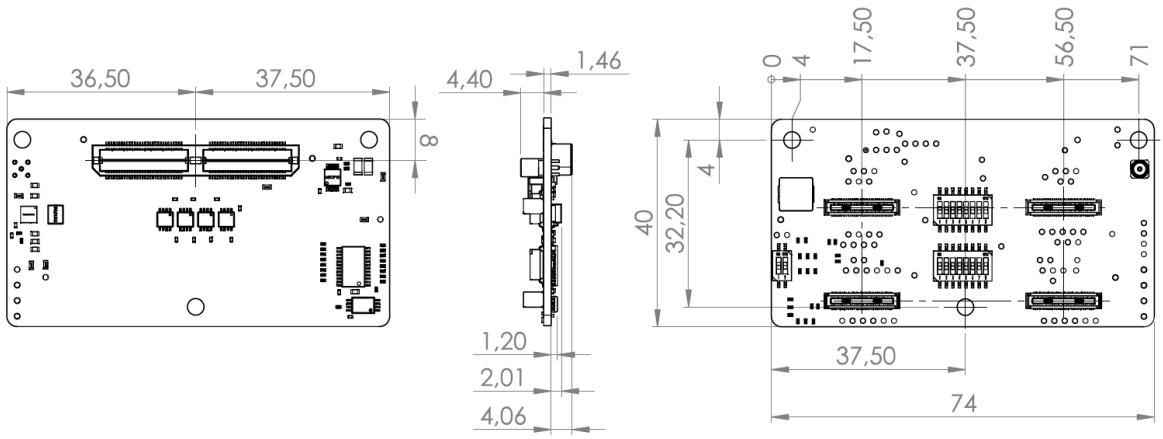
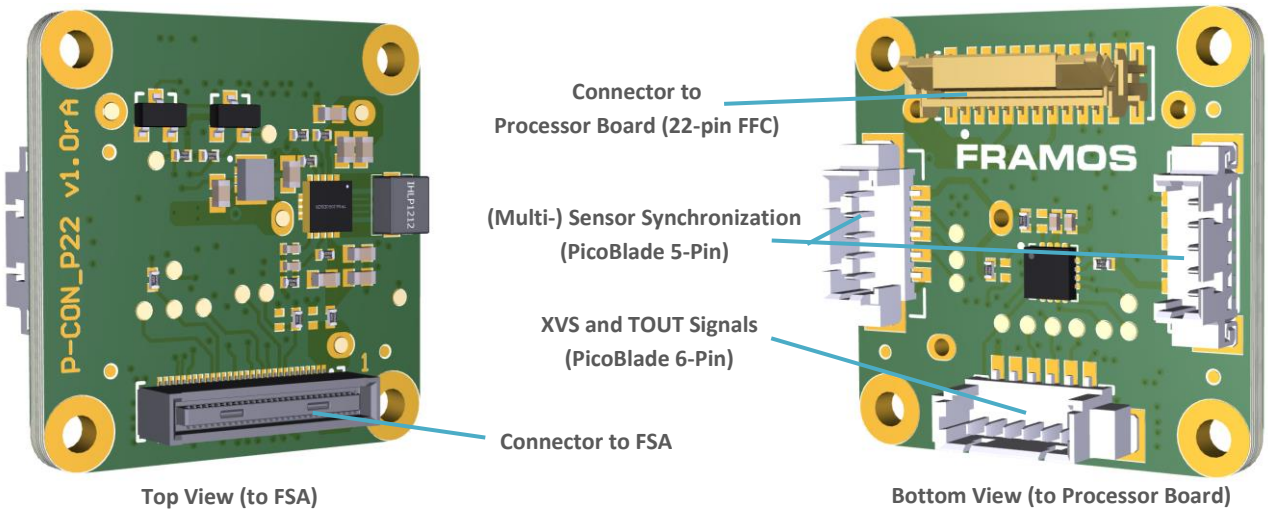


Figure 17: Technical Drawing of FPA-4.A/TXA-V1

Note: The FPA-4.A/TXA-V1 comes in two variants, V1B and V1C. Mechanical dimensions may alter slightly. The V1C is redesigned to accommodate mounting to the NVIDIA® AGX Orin™ whereas the V1B, pictured above, requires removing a plastic cover on the NVIDIA® AGX Orin™ to mount.

10.3 FPA-A/P22-V2: Piggyback FPA to NVIDIA Jetson Orin Nano/NX and Xavier NX Developer Kits

- Adapting from PixelMate to 22-Pin FFC Cable
- 4-Lane MIPI CSI-2
- Generation of standard PixelMate power rails from 3V3 input voltage
- Signal level translation for logic
- Enhanced sensor control signal access via I2C extender
- Synchronization and timing signal access via Molex Picoblade connectors
- **Compatible Processor Boards:**
  - NVIDIA Jetson Orin Nano Development Kit
  - Orin NX SoM on the Orin Nano carrier



10.3.1 Description of Connectors and Interfaces

Name	Description	Connector Type
J1	PixelMateC to FSA (4x MIPI CSI-2 lanes)	Hirose DF40HC(4.0)-60DS-0.4V
J2	22-Pin FFC to Processor Board	Hirose FH12-22S-0.5SVA(54)
J3	XVS and TOUT Signals	Molex PicoBlade, 6-Pin (53398-0671)
J4	(Multi-) Sensor Synchronization	Molex PicoBlade, 5-Pin (53398-0571)
J5	(Multi-) Sensor Synchronization	Molex PicoBlade, 5-Pin (53398-0571)

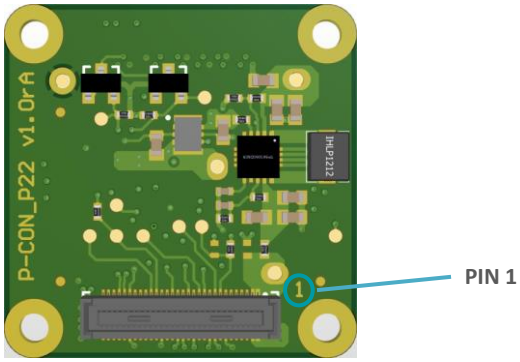
Table 27: Connectors on FPA-A/P22-V2

The Pin 1 markings can be found in the following chapters along with the Pinout, as well as on the PCB in copper or silkscreen layer next to the connector.

Version 1.5.0 from 2024-05-23

J1: PixelMateC to FSA

PixelMate MIPI CSI-2 type connector to FSA. The pin assignment of J1 is versatile and aligns with FSA pinouts.



Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters, or the Processor Board. Using flex cable (FMA-FC-150/60-V1) between FSA and FPA is optional. It is only compatible to FSAs with MIPI CSI-2 output.

J2: Connector to Processor Board

Type: Hirose FH12-22S-0.5SVA(54)

Pinout:

Pin #	Name	Pin #	Name
1	GND	12	D_DATA_2_P
2	D_DATA_0_N	13	GND
3	D_DATA_0_P	14	D_DATA_3_N
4	GND	15	D_DATA_3_P
5	D_DATA_1_N	16	GND
6	D_DATA_1_P	17	IS_RST_IN
7	GND	18	MCLK_IN
8	D_CLK_0_N	19	GND
9	D_CLK_0_P	20	I2C_SCL_IN
10	GND	21	I2C_SDA_IN
11	D_DATA_2_N	22	3V3_VDD

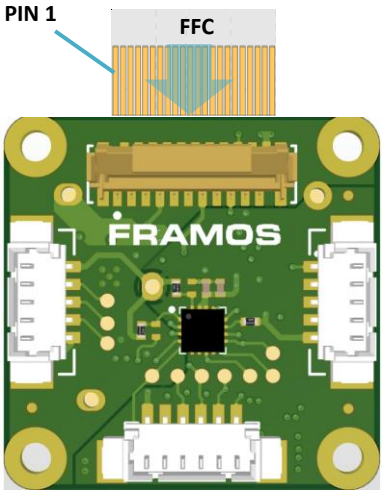


Table 28: Pinout of FPA-A/P22-V2 connector to NVIDIA Jetson Orin Nano Development Kit / Orin NX SoM

Almost all signals coming from the FSA through J1 are directly routed to J2 and follow accordingly the signal specification in the section of the corresponding FSA within “Signal Description to FPA”.

The following signals are converted on the FPA and are to be treated with **LVCMOS33 (3.3V)** logic level:

- I2C_SCL_IN
- I2C_SDA_IN

Caution: Use only FFC with same-side contacts, as i.e. Molex 0151660241.

J3 – XVS, TOUT Signals

Type: Molex PicoBlade, 53398-0671
Pinout:

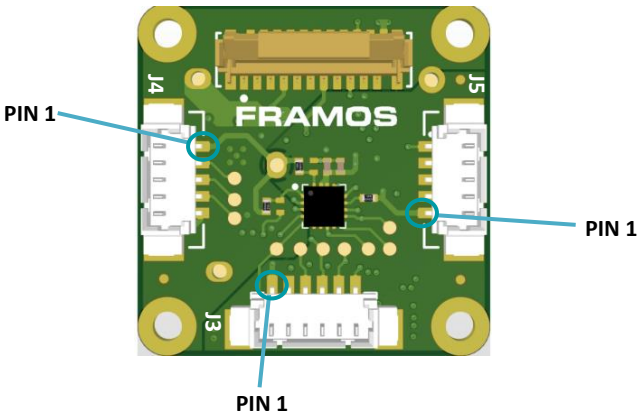
Pin #	Name
1	1V8_VDD
2	GPIO1(XVS0)
3	GPIO11(TOUT0)
4	GPIO8(TOUT1)
5	GPIO9(TOUT2)
6	GND

J4 / J5 – (Multi-) Sensor Synchronization Signals

Type: Molex PicoBlade, 53398-0571
Pinout:

Pin #	Name
1	1V8_VDD
2	GPIO1(XVS0)
3	GPIO2(XHS0)
4	GPIO3(XTRIG0)
5	GND

Note: This pinout applies to both Connectors J4 and J5 and allows interconnection across multiple boards for the synchronization of multiple sensors.



10.3.2 I2C: Access to further Signals

As the GPIO capabilities are limited by the low pin-count of the 22-pin FFC interface connector, the FPA contains an I2C GPIO extender (TCA6408). It allows the control of further timing uncritical signals through the I2C bus.

I2C Address[5]: 0x20

Pinout:

Pin #	Name
P0	PW_EN_0
P1	PW_EN_1
P2	RST_0
P3	GPIO0(XMASTER0)
P4	GPIO6(SLAMODE0)
P5	GPIO7(SLAMODE1)
P6	GPIO16(SLAMODE2)
P7	GPIO10(TENABLE)

[5] Earlier revisions will listen to the I2C address 0x21, which may conflict with the FFA-GMSL-Ser (if applied).

10.3.3 External Signals & Test Points

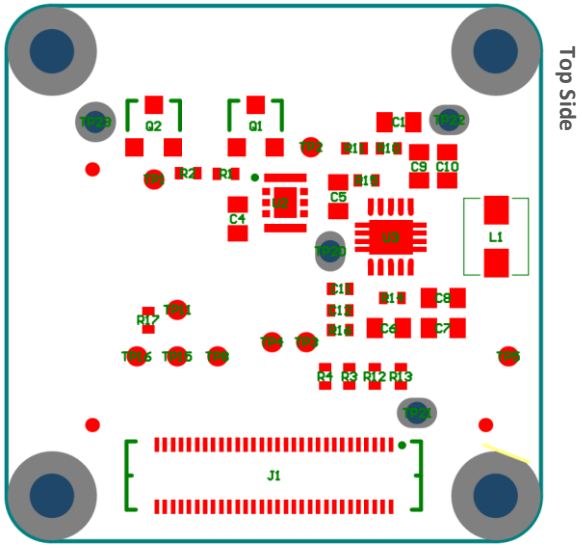
Test Points

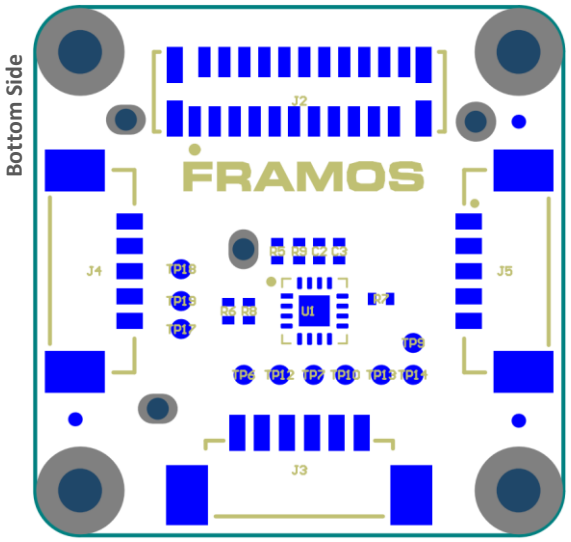
Top Side (heading to FSA):

Label	Signal
TP1	I2C_0_SCL(SPI_SCK)
TP2	I2C_0_SDA(SPI_MOSI)
TP3	CAM_RST_0
TP4	GPIO14
TP5	GPIO15(SPI_MISO)
TP8	GPIO17(SPI_CS)
TP11	GPIO10(TENABLE)
TP15	CAM_MCLK_0
TP16	CAM_MCLK_1
TP20	1V8_VDD
TP21	3V8_VDD
TP22	3V3_VDD
TP23	GND

Bottom Side (heading to Processor Board):

Label	Signal
TP6	GPIO0(XMASTER0)
TP7	GPIO8(TOUT1)
TP9	GPIO16(SLAMODE2)
TP10	GPIO9(TOUT2)
TP12	GPIO11(TOUT0)
TP13	GPIO6(SLAMODE0)
TP14	GPIO7(SLAMODE1)
TP17	GPIO3(XTRIG0)
TP18	GPIO1(XVS0)
TP19	GPIO2(XHS0)





10.3.4 Technical Drawing

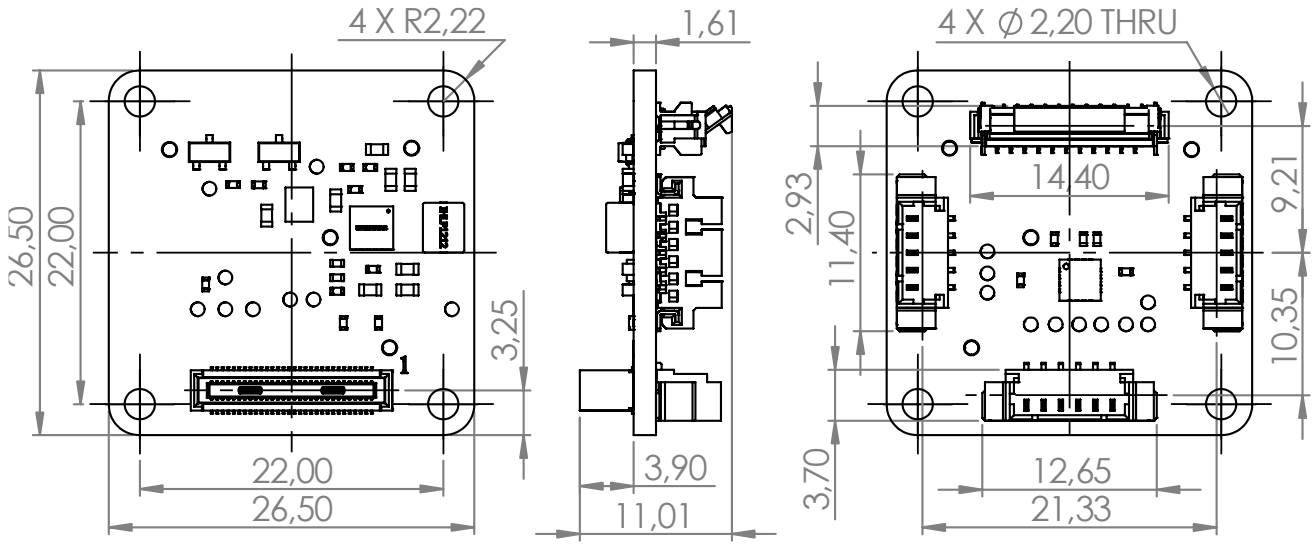
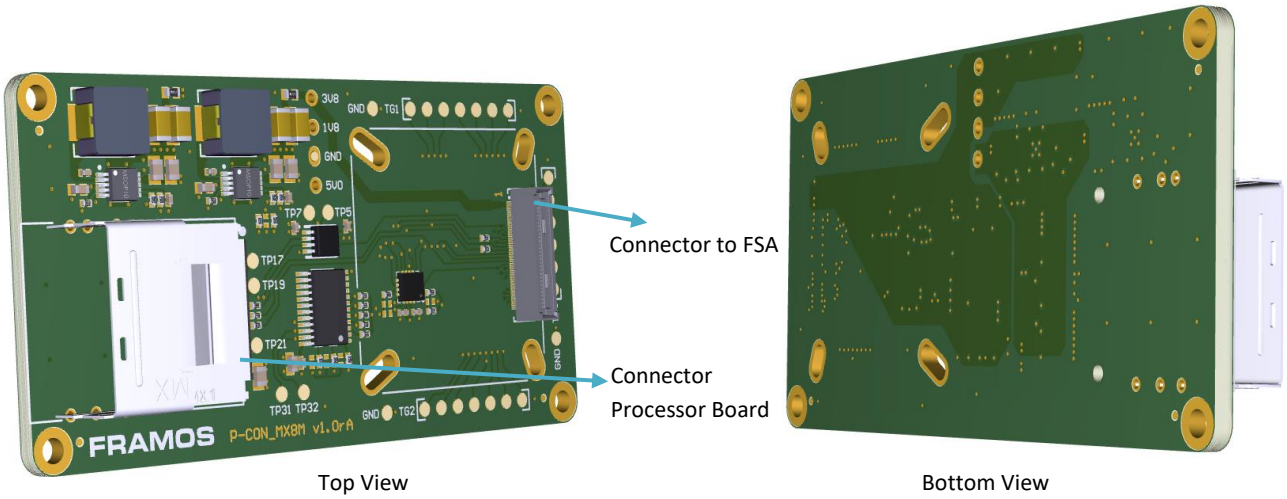


Figure 18: Technical Drawing of FPA-A/P22-V2

10.4 FPA-A/NDK-V1A: Piggyback FPA to NXP i.MX Developer Kit

- Adapting from PixelMate to miniSAS Cable
- 4-Lane MIPI CSI-2
- Generation of standard PixelMate power rails from 3V3 and 5V0 input voltage
- Signal level translation for logic
- Enhanced sensor control signal access via I2C GPIO Expander
- **Compatible Processor Boards:**
  - NXP i.MX8MP development kit



10.4.1 Description of Connectors and Interfaces

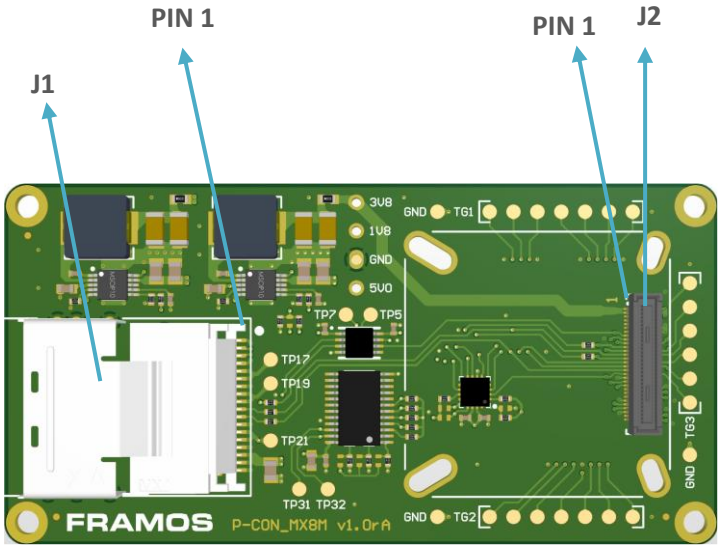
Name	Description	Connector Type	Orientation
J1	PixelMate to Processor Board	Molex 757830132	**Pin 1 marked on PCB**
J2	PixelMateC to FSA (4x MIPI CSI-2 lanes)	**Hirose DF40HC(4.0)-60DS-0.4V**	**Pin 1 marked on PCB**

Table 29: Connectors on FPA-A/NDK-V1A

Note: The Pin 1 markings can be found in the following chapters along with the Pinout, as well as on the PCB in copper or silkscreen layer next to the connector.

J1: Connector to Processor Board

Label: J1
Type: 757830132
Cable: miniSAS cable (e.g. Molex 79576-2107)



Pinout:

Pin #	Name	Pin #	Name
A1	GND	**B1**	GND
A2	D_DATA_0_N	**B2**	D_CLK_0_N
A3	D_DATA_0_P	**B3**	D_CLK_0_P
A4	GND	**B4**	GND
A5	D_DATA_1_N	**B5**	TP_1V8
A6	D_DATA_1_P	**B6**	TP_1V8
A7	GND	**B7**	GND
A8	MCLK_IN	**B8**	TP_12V
A9	RST_R	**B9**	TP_12V
A10	I2C_SDA	**B10**	SYNC_R
A11	I2C_SCL	**B11**	PWDN_R
A12	GND	**B12**	GND
A13	D_DATA_2_N	**B13**	3V3_VIN
A14	D_DATA_2_P	**B14**	3V3_VIN
A15	GND	**B15**	GND
A16	D_DATA_3_N	**B16**	5V0_VIN
A17	D_DATA_3_P	**B17**	5V0_VIN
A18	GND	**B18**	GND

Table 30: Pinout of FPA-4.A/NDK-V1A connector to NXP i.MX

Note : Component Connections

1. **MCLK_IN:** Connected to CAM0_MCLK_0 through buffer for stable clock signal transmission.
2. **RST_R:** Linked to RST_0 via buffer for controlled and reliable reset mechanism.
3. **SYNC_R:** Connected to CAM0_GPIO1 (XVS0) for synchronization between components.
4. **PWDN_R:** Direct connection to PW_EN_0 for effective power state management.

J2: Connector to Sensor Adapter (FSA)

Label: J2

Type: **Hirose DF40HC(4.0)-60DS-0.4V**

Pinout:

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	3V8_VDD	16	RST_1	31	CAM0_GPIO3(XTRIG0)	46	D_DATA_3_P
2	1V8_VDD	17	CAM0_GPIO14(LDD_ERR)	32	CAM0_GPIO11(TOUT)	47	NC
3	3V8_VDD	18	CAM0_GPIO15(SPI_MISO)	33	PW_EN_0	48	D_DATA_3_N
4	1V8_VDD	19	CAM0_GPIO0(XMASTER0)	34	PW_EN_1	49	GND
5	NC	20	CAM0_GPIO8	35	CAM0_GPIO6(SLAMODE0)	50	GND
6	NC	21	I2C_0_SCL(SPI_SCK)	36	CAM0_GPIO7	51	D_DATA_0_N
7	NC	22	I2C_1_SCL	37	GND	52	D_DATA_1_N
8	NC	23	CAM0_GPIO17(SPI_CS)	38	GND	53	D_DATA_0_P
9	NC	24	GPIO16(SYS_PW_EN)	39	CAM0_MCLK_0	54	D_DATA_1_P
10	NC	25	CAM0_GPIO1(XVS0)	40	NC	55	GND
11	GND	26	CAM0_GPIO9	41	CAM0_MCLK_1	56	GND
12	GND	27	I2C_0_SDA(SPI_MOSI)	42	NC	57	D_DATA_2_P
13	GND	28	I2C_1_SDA	43	GND	58	D_CLK_0_P
14	GND	29	CAM0_GPIO2(XHS0)	44	GND	59	D_DATA_2_N
15	RST_0	30	CAM0_GPIO10	45	NC	60	D_CLK_0_N

Table 31: Pinout of FPA-4.A/NDK-V1A connector to FSA

10.4.2 I2C: Access to further Signals

The FPA contains an I2C GPIO expander. It allows the control of further timing uncritical signals through the I2C bus.

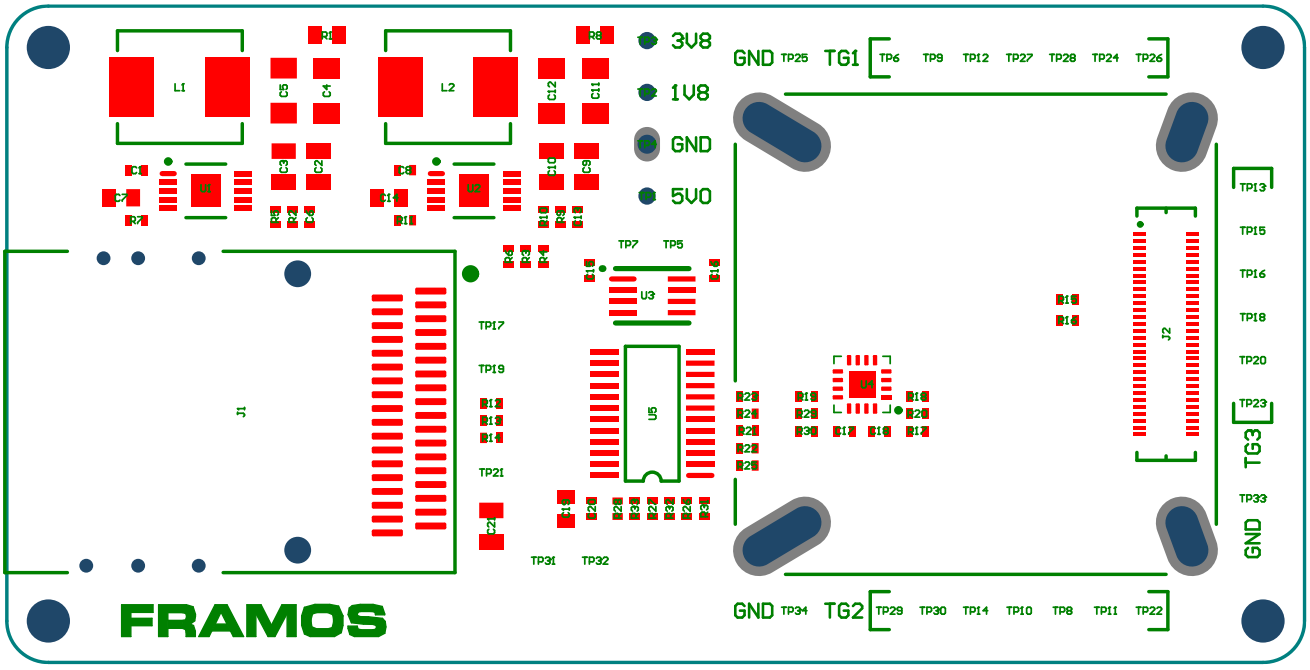
I2C Address[6]: 0x20

Pinout:

Pin #	Name
P0	CAM0_GPIO6(SLAMODE0)
P1	CAM0_GPIO0(XMASTER0)
P2	CAM0_GPIO14(LDD_ERR)
P3	CAM0_GPIO11(TOUT)
P4	RST_1
P5	PW_EN_1
P6	CAM0_GPIO8
P7	GPIO16(SYS_PW_EN)

[6] Earlier revisions will listen to the I2C address 0x21, which may conflict with the FFA-GMSL-Ser (if applied).

10.4.3 TGx, TPx: Test Groups and Test Points



Ungrouped Test Points

Label	Signal	Label	Signal
TP1	5V0_VIN	**TP19**	TP_12V
TP2	1V8_VDD	**TP21**	3V3_VIN
TP3	3V8_VDD	**TP25**	GND
TP4	GND	**TP31**	I2C_SCL
TP5	CAM0_MCLK_0	**TP32**	I2C_SDA
TP7	CAM0_MCLK_1	**TP33**	GND
TP17	TP_1V8	**TP34**	GND

TG1: Synchronisation Signals

Label	Signal	Label	Signal
TP6	CAM0_GPIO1(XVS0)	**TP26**	PW_EN_1
TP9	CAM0_GPIO2(XHS0)	**TP27**	RST_0
TP12	CAM0_GPIO3(XTRIG0)	**TP28**	RST_1
TP24	PW_EN_0		

TG2: Control Signals and GPIOs

Label	Signal	Label	Signal
TP8	CAM0_GPIO14(LDD_ERR)	**TP22**	CAM0_GPIO6(SLAMODE0)
TP10	CAM0_GPIO15(SPI_MISO)	**TP29**	I2C_0_SCL
TP11	CAM0_GPIO0(XMASTER0)	**TP30**	I2C_0_SDA
TP14	CAM0_GPIO17(SPI_CS)		

TG3: Control Signals and GPIOs

Label	Signal	Label	Signal
TP13	CAM0_GPIO8	**TP18**	CAM0_GPIO10
TP15	GPIO16(SYS_PW_EN)	**TP20**	CAM0_GPIO11(TOUT)
TP16	CAM0_GPIO9	**TP23**	CAM0_GPIO7

10.4.4 Technical Drawing

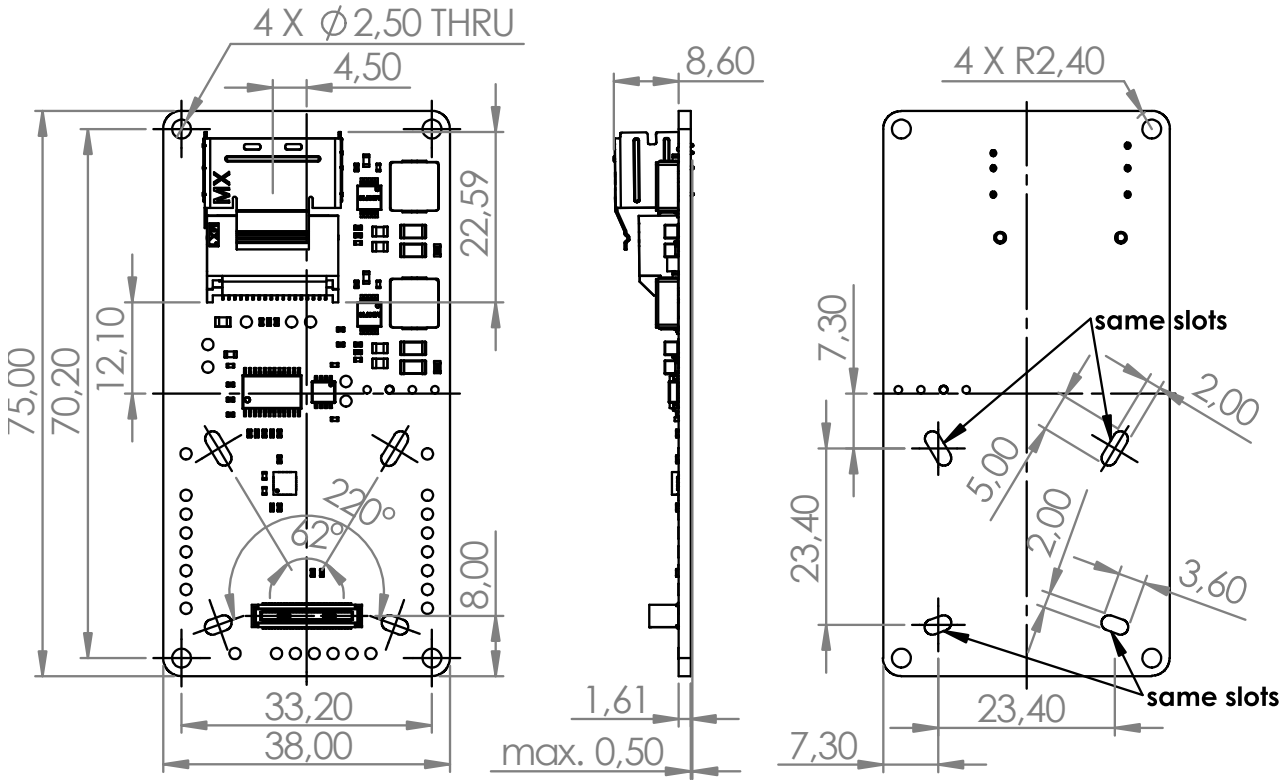
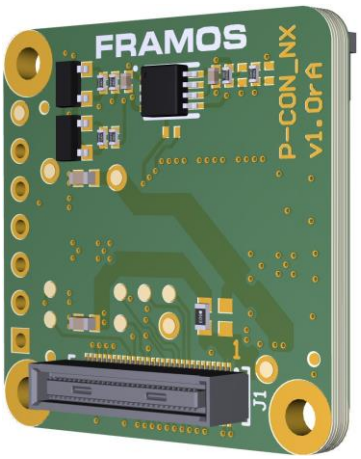


Figure 19: Technical Drawing of FPA-A/NDK-V1A

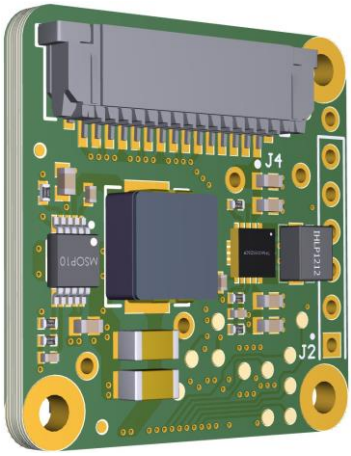
10.5 FPA-A/NVN-V1: Piggyback FPA to NVIDIA Jetson Nano and TX2 NX

- One 2-Lane MIPI CSI-2 Input
- Signal routing and power conversion
- Voltage level translation for control signals
- Testpoints to important sensor signals
- Board-to-board stacking to FSA

- Compatible Processor Boards:
  - NVIDIA Jetson Nano Development Kit
  - NVIDIA Jetson TX2 NX Developer Kit
  - NVIDIA Xavier NX Development Kit



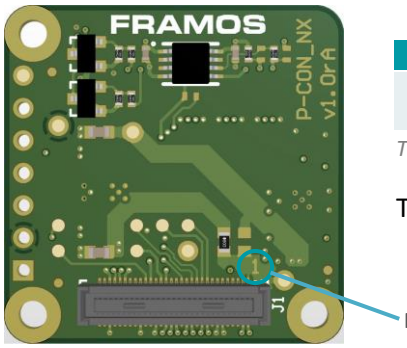
Top View (to FSA)



Bottom View (to Processor Board)

Note: All signals are routed from J1 (to FSA) to J4 (to processor), test points and pin row. They follow the signal specification according to the FSA output interface. Control signals going to J4 (I2C, clock, GPIO) are buffered to allow voltage translation.

10.5.1 J1: Connector to Sensor Adapters (FSA)



Name	Description	Connector Type	Orientation
J1	2-Lanes CSI-2, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	Pin 1 marking in copper on PCB, next to connector.

Table 32: Image Sensor Connector on FPA-A/NVN-V1

The pin assignment of J1 is according to the corresponding FSA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters, or the Processor Board. Using flex cable (FMA-FC-150/60-V1) between FSA and FPA is optional.

Image Sensor CSI-2 lane Support per Port

The table below shows the possible MIPI CSI-2 lane configurations per FSM / Processor Board combination, that are supported in HW using the FPA-A/NVN-V1.

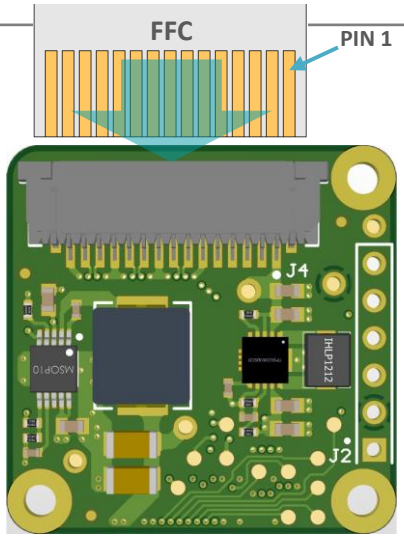
	NVIDIA Jetson Nano / TX2 NX / Xavier NX
FSM with FSA-FTx/A	**J4 [# Lanes]**
FSM-AR0144	2
FSM-AR0521	2
FSM-AR1335	2
FSM-HDP230	2
FSM-IMX264	Not Supported[7]
FSM-IMX283	Not Supported[7]
FSM-IMX290, 327	2
FSM-IMX296, 297	1
FSM-IMX304	Not Supported[7]
FSM-IMX334	Not Supported[7]
FSM-IMX335	2
FSM-IMX412, 477, 577	2
FSM-IMX415, 715	2
FSM-IMX462, 662	2
FSM-IMX464	2
FSM-IMX485, 585	2
FSM-IMX530	Not Supported[7]
FSM-IMX565	2
FSM-IMX675	2
FSM-IMX678	2

Table 33: Image Sensor Support per Port with FPA-A/NVN-V1

Note: Due to different interface routing and thus Device Tree configuration, the provided drivers only support NVIDIAs official Development Kits of the revision B01.

[7] NVIDIA Jetson Nano, Xavier NX and TX2 NX Development Kits only provide 2-lanes MIPI CSI-2, sensor requires 4-lanes.

10.5.2 J4: Connector to Processor Board



Label: J4

Type: Amphenol SFW15R-2STE1LF

Pinout:

Pin #	Name	Pin #	Name
1	3V3_VDD	9	GND
2	I2C_SDA_IN	10	CSI0_D1_P
3	I2C_SCL_IN	11	CSI0_D1_N
4	MCLK_0	12	GND
5	CAM_PWDN	13	CSI0_D0_P
6	GND	14	CSI0_D0_N
7	CSI0_CLK_P	15	GND
8	CSI0_CLK_N		

Table 34: Pinout of FPA-A/NVN-V1 connector to NVIDIA Jetson Nano / TX2 NX / Xavier NX Development Kits

Caution: Use only FFC with opposing contacts (TOP-BOT), like Würth 686715200001.

10.5.3 External Signals & Test Points

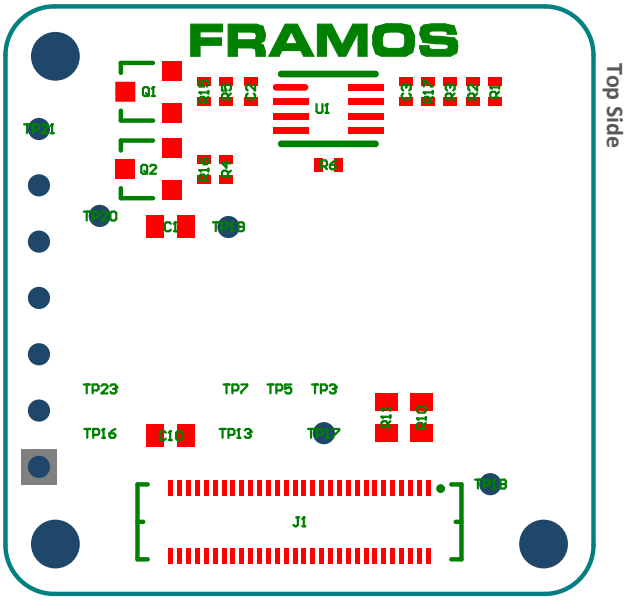
Test Points

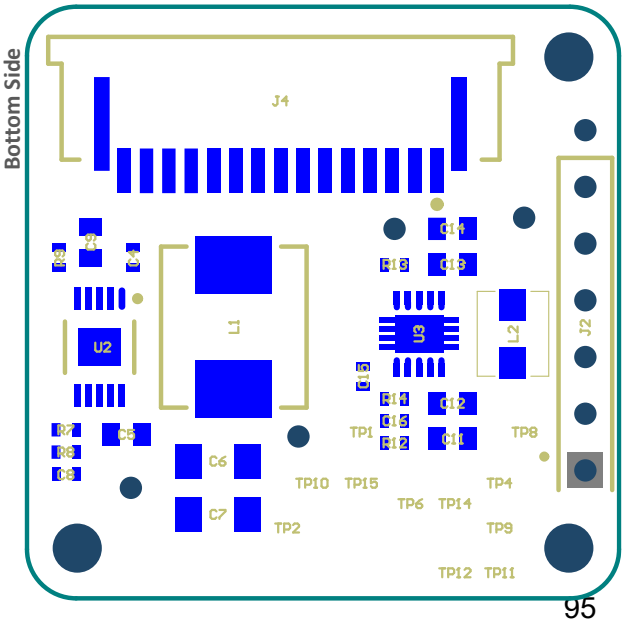
Top Side (heading to FSA):

Label	Signal
TP3	CAM0_GPIO14
TP5	CAM0_GPIO0 (XMASTER0)
TP7	CAM0_GPIO17 (SPI_CS)
TP13	CAM0_GPIO6
TP16	CAM0_MCLK1
TP17	1V8_VDD
TP18	3V8_VDD
TP19	3V3_VDD
TP20	GND
TP21	CAM0_PW_EN0
TP23	CAM0_GPIO3 (XTRIG0)

Bottom Side (heading to Processor Board):

Label	Signal
TP1	I2C_0_SDA (SPI_SCK)
TP2	CAM0_RST_0
TP4	CAM0_GPIO15(SPI_MISO)
TP6	CAM0_GPIO8
TP8	CAM0_SYS_PW_EN)
TP9	CAM0_GPIO9
TP10	I2C_0_SDA (SPI_MOSI)
TP11	CAM0_GPIO10
TP12	CAM0_GPIO11 (FSTROBE)
TP14	CAM0_GPIO7
TP15	CAM0_MCLK0





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Pin Rail J2 (not assembled[8])

Pin	Signal
1	1V8_VDD
2	GND
3	CAM0_GPIO1 (XVS0)
4	CAM0_GPIO2 (XHS0)
5	CAM0_GPIO11 (FSTROBE)
6	CAM0_PW_EN1

Note: All signals on Test Points and Pin Rail are LVCMOS18 (1.8V) logic, according to image sensor specification.

10.5.4 Technical Drawing

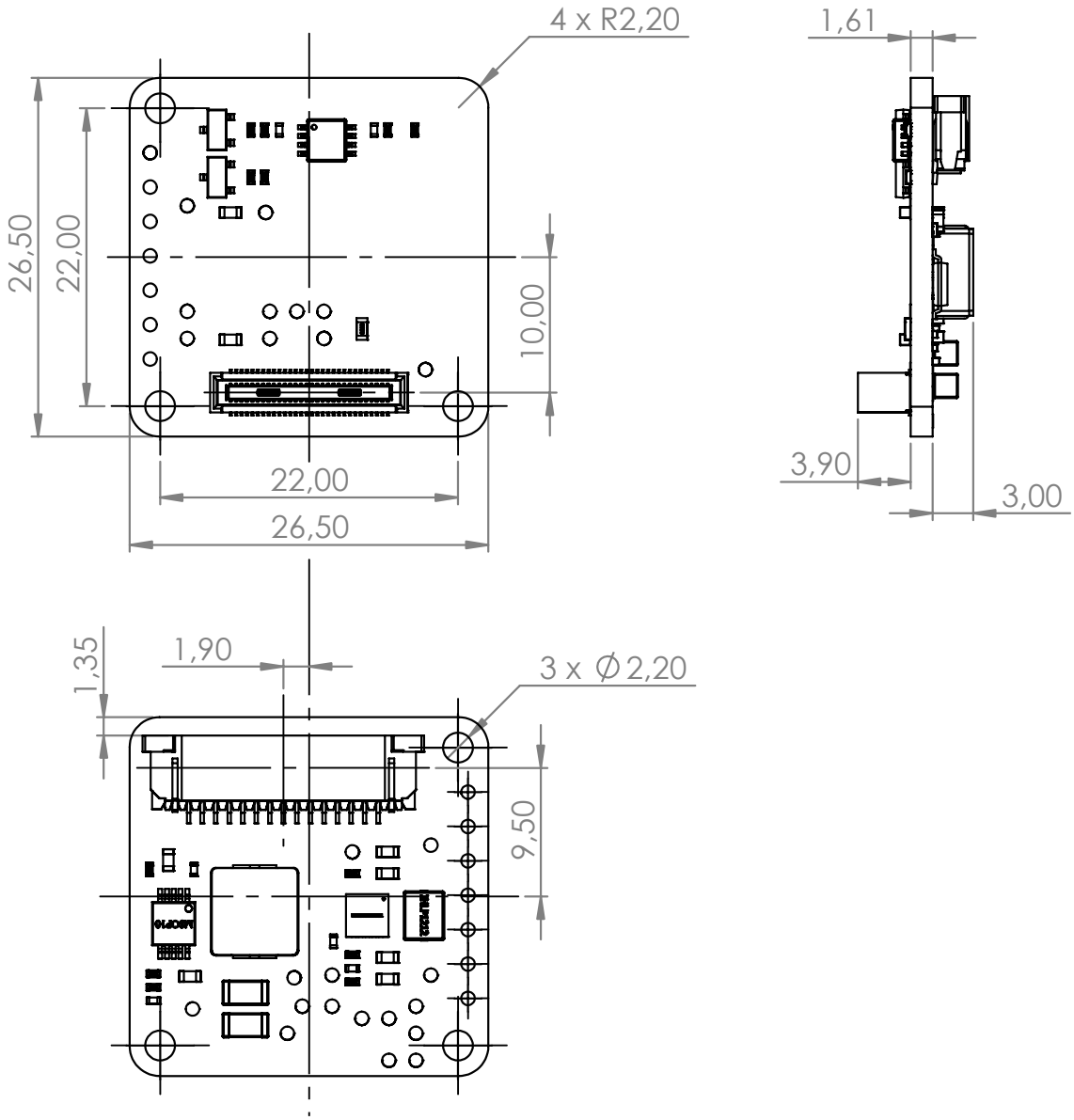

Figure 20: Technical Drawing of FPA-A/NVN-V1

[8] By default, J2 is not assembled. Soldering a regular 1x6 pin stripe with 2.54 pitch is recommended for usage.

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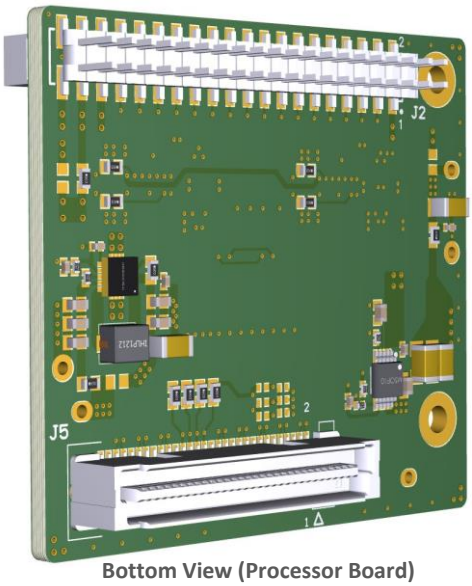
10.6 FPA-2.A/96B-V1: Dual FPA to 96Boards.org Consumer Edition

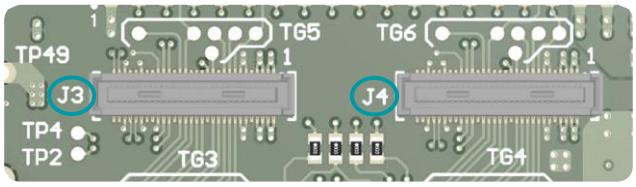
- Two MIPI CSI-2 Inputs with 4- and 2-Lanes
- Signal routing and I2C multiplexing
- EEPROM for dynamic device tree management
- Testpoints to important sensor signals
- Configuration of trigger routing
- Compatible Processor Boards:
  - 96boards Consumer Edition (CE)
    https://www.96boards.org/products/ce/

Top View



Bottom View (Processor Board)

J3, J4: Image Sensor Connectors



Name	Description	Connector Type	Orientation
J3	Port 1, 4-Lanes CSI-2, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	Pin 1 Printed on PCB next to each connector.
J4	Port 2, 4-Lanes CSI-2, to FSA[9]		

Table 35: Image Sensor Connectors on FPA-2.A/A-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

[9] The usage of the second port might require a minor hardware modification by the user. Further details are described in the “User Guide” in the platform specific software package.

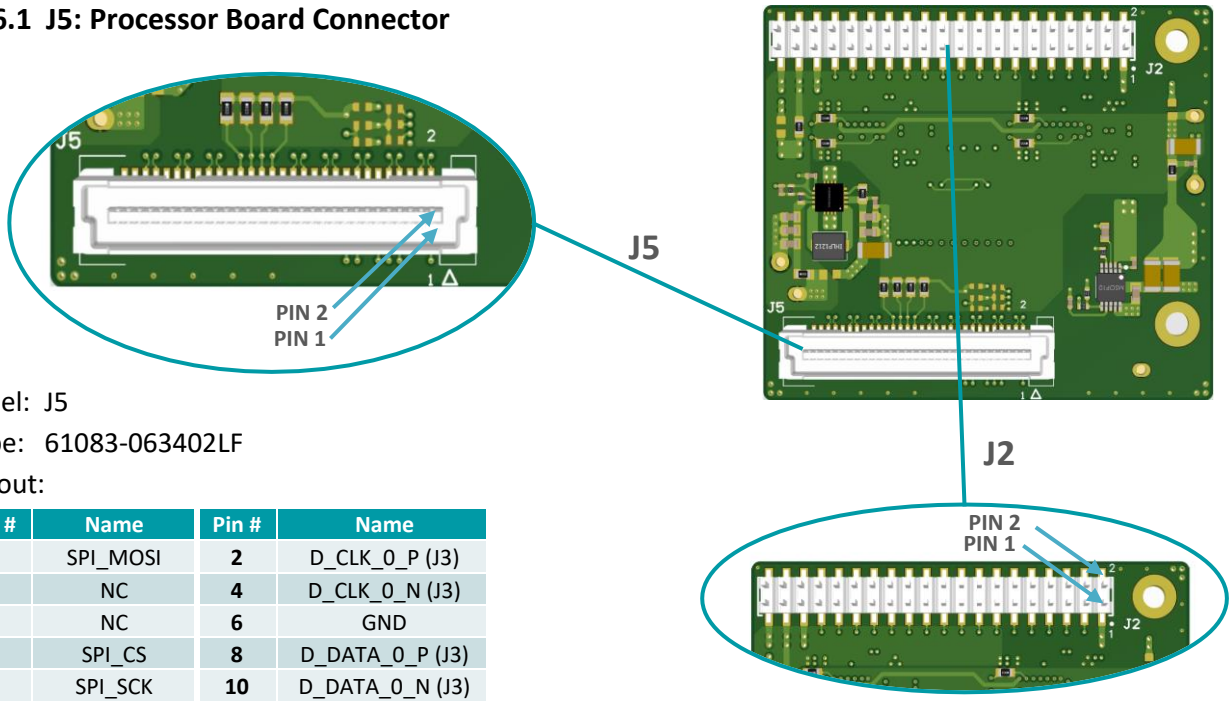
Image Sensor Support per Port

The table below shows the possible MIPI CSI-2 lane configurations per FSM / Processor Board combination, that are supported in HW using the FPA-2.A/96B-V1.

	96Boards CE	
FSM with FSA-FTx/A (all)	**J5**	**J6**
FSM-AR0144	2	2
FSM-AR0521	2 / 4	2
FSM-AR1335	2 / 4	2
FSM-HDP230	4	2
FSM-IMX264	4	-
FSM-IMX283	4	-
FSM-IMX290, 327	2 / 4	2
FSM-IMX296, 297	1	1
FSM-IMX304	4	-
FSM-IMX334	4	-
FSM-IMX335	2 / 4	2
FSM-IMX412, 477, 577	2 / 4	2
FSM-IMX415, 715	2 / 4	2
FSM-IMX462, 662	2 / 4	2
FSM-IMX464	2 / 4	2
FSM-IMX485, 585	2 / 4	2
FSM-IMX530	4	-
FSM-IMX565, 568	2 / 4	2
FSM-IMX678	2 / 4	2

Table 36: Image Sensor Support per Port with FPA-2.A/96B-V1

10.6.1 J5: Processor Board Connector



Label: J5
Type: 61083-063402LF
Pinout:

Pin #	Name	Pin #	Name
1	SPI_MOSI	2	D_CLK_0_P (J3)
3	NC	4	D_CLK_0_N (J3)
5	NC	6	GND
7	SPI_CS	8	D_DATA_0_P (J3)
9	SPI_SCK	10	D_DATA_0_N (J3)
11	SPI_MISO	12	GND
13	GND	14	D_DATA_1_P (J3)
15	MCLK_0	16	D_DATA_1_N (J3)
17	MCLK_1	18	GND
19	GND	20	D_DATA_2_P (J3)
21	NC	22	D_DATA_2_N (J3)
23	NC	24	GND
25	GND	26	D_DATA_3_P (J3)
27	NC	28	D_DATA_3_N (J3)
29	NC	30	GND
31	GND	32	I2C_0_SCL
33	NC	34	I2C_0_SDA
35	NC	36	I2C_2_SCL
37	GND	38	I2C_2_SDA
39	NC	40	GND
41	NC	42	D_DATA_4_P (J4)
43	GND	44	D_DATA_4_N (J4)
45	NC	46	GND
47	NC	48	D_DATA_5_P (J4)
49	GND	50	D_DATA_5_N (J4)
51	NC	52	GND
53	NC	54	D_CLK_0_P (J4)
55	GND	56	D_CLK_0_N (J4)
57	NC	58	GND
59	NC	60	NC

Label: J1/J2
Type: 61083-063402LF
Pinout:

Pin #	Name	Pin #	Name
1	GND	2	GND
3	96B_UART0_CTS	4	96B_PWR_BTNn
5	96B_UART0_TXD	6	96B_PWR_BTNn
7	96B_UART0_RXD	8	96B_SPI0_CLK
9	96B_UART0_RTS	10	96B_SPI0_MISO
11	96B_UART1_TXD	12	96B_SPI0_CS
13	96B_UART1_RXD	14	96B_SPI0_MOSI
15	96B_SCL_0	16	96B_PCM_FS
17	96B_SDA_0	18	96B_PCM_CLK
19	96B_SCL_1	20	96B_PCM_DO
21	96B_SDA_1	22	96B_PCM_DI
23	96B_GPIO_A	24	96B_GPIO_B
25	96B_GPIO_C	26	96B_GPIO_D
27	96B_GPIO_E	28	96B_GPIO_F
29	96B_GPIO_G	30	96B_GPIO_H
31	CAM0_RST_0	32	CAM0_PW_EN_0
33	CAM1_RST_0	34	CAM1_PW_EN_0
35	96B_1V8	36	96B_SYS_DCIN
37	96B_5V0	38	
39	GND	40	GND

Table 37: Pinout of FPA-2.A/96B-V1 connector to 96Boards.org Consumer Edition Standard

10.6.2 SW1: Configuration Switch

The DIP switch SW1 is for interconnecting FSA's triggering signals (XVS, XHS and XTRIG). It is designated to interconnect XVS, XHS and XTRIG pins from FPA in parallel to both FSA connectors.

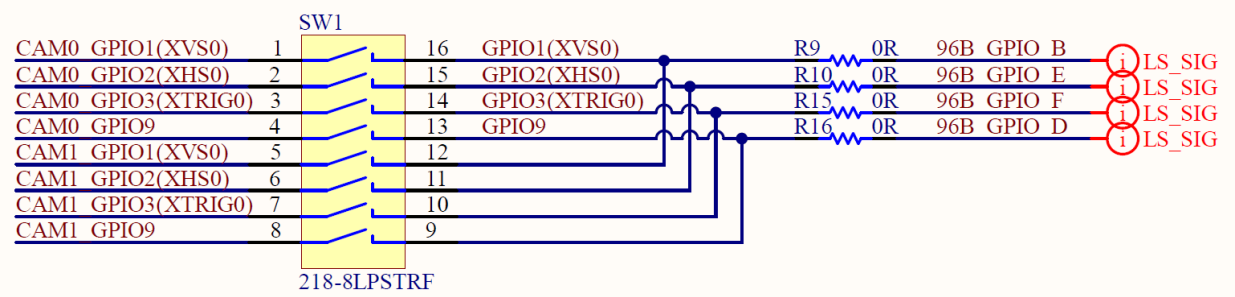


Table 35: Configuration of SW1 on FPA-2.A/96B-V1

Default state of DIP switch

- SW1 – all positions OFF (XVS/XHS pins are NOT interconnected)

10.6.3 TGx, TPx: Test Groups and Test Points

10.6.4 Ungrouped (according to silk print)

Label	Signal	Label	Signal
TP2	GPIO4(MCLK2)	**TP51**	5V0_VDD
TP4	GPIO5(MCLK3)	**TP52**	GND
TP49	1V8_VDD	**TP53**	GND
TP50	3V8_VDD		

TG1: Clocks and SPI

Label	Signal	Label	Signal
TP1	MCLK_0	**TP55**	SPI_CS
TP3	MCLK_1	**TP56**	SPI_SCK
TP54	SPI_MOSI	**TP57**	SPI_MISO

TG2: Synchronisation Signals

Label	Signal	Label	Signal
TP9	CAM0_I2C_0_SCL(SPI_SCK)	**TP18**	CAM1_GPIO3(XTRIG0)
TP10	CAM1_I2C_0_SCL(SPI_SCK)	**TP35**	CAM0_GPIO9
TP11	CAM0_I2C_0_SDA(SPI_MOSI)	**TP36**	CAM1_GPIO9
TP12	CAM1_I2C_0_SDA(SPI_MOSI)		
TP13	CAM0_GPIO1(XVS0)		
TP14	CAM1_GPIO1(XVS0)		
TP15	CAM0_GPIO2(XHS0)		
TP16	CAM1_GPIO2(XHS0)		
TP17	CAM0_GPIO3(XTRIG0)		

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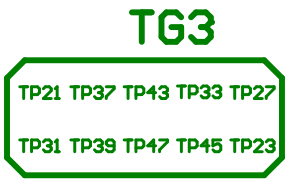
TG3: Control Signals and GPIOs J3 (CAM0)

Label	Signal	Label	Signal
TP21	CAM0_PW_EN_1	TP37	CAM0_GPIO10
TP23	CAM0_GPIO15(SPI_MISO)	TP39	CAM0_GPIO11
TP27	CAM0_RST_1	TP43	CAM0_GPIO16(SYS_PW_EN)
TP31	CAM0_GPIO7	TP45	CAM0_I2C_1_SCL
TP33	CAM0_GPIO8	TP47	CAM0_I2C_1_SDA



TG4: Control Signals and GPIOs J4 (CAM1)

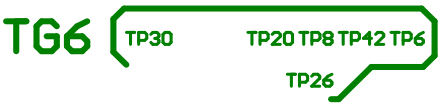
Label	Signal	Label	Signal
TP22	CAM1_PW_EN_1	TP38	CAM1_GPIO10
TP24	CAM1_GPIO15(SPI_MISO)	TP40	CAM1_GPIO11
TP28	CAM1_RST_1	TP44	CAM1_GPIO16(SYS_PW_EN)
TP32	CAM1_GPIO7	TP46	CAM1_I2C_1_SCL
TP34	CAM1_GPIO8	TP48	CAM1_I2C_1_SDA

TG6: Control Signals and GPIOs J3 (CAM0)

Label	Signal	Label	Signal
TP5	CAM0_RST_0	TP25	CAM0_GPIO17(SPI_CS)
TP7	CAM0_GPIO0(XMASTER0)	TP29	CAM0_GPIO6
TP19	CAM0_PW_EN_0	TP41	CAM0_GPIO14

TG6: Control Signals and GPIOs J4 (CAM1)

Label	Signal	Label	Signal
TP6	CAM1_RST_0	TP26	CAM1_GPIO17(SPI_CS)
TP8	CAM1_GPIO0(XMASTER0)	TP30	CAM1_GPIO6
TP20	CAM1_PW_EN_0	TP42	CAM1_GPIO14



10.6.5 Technical Drawing

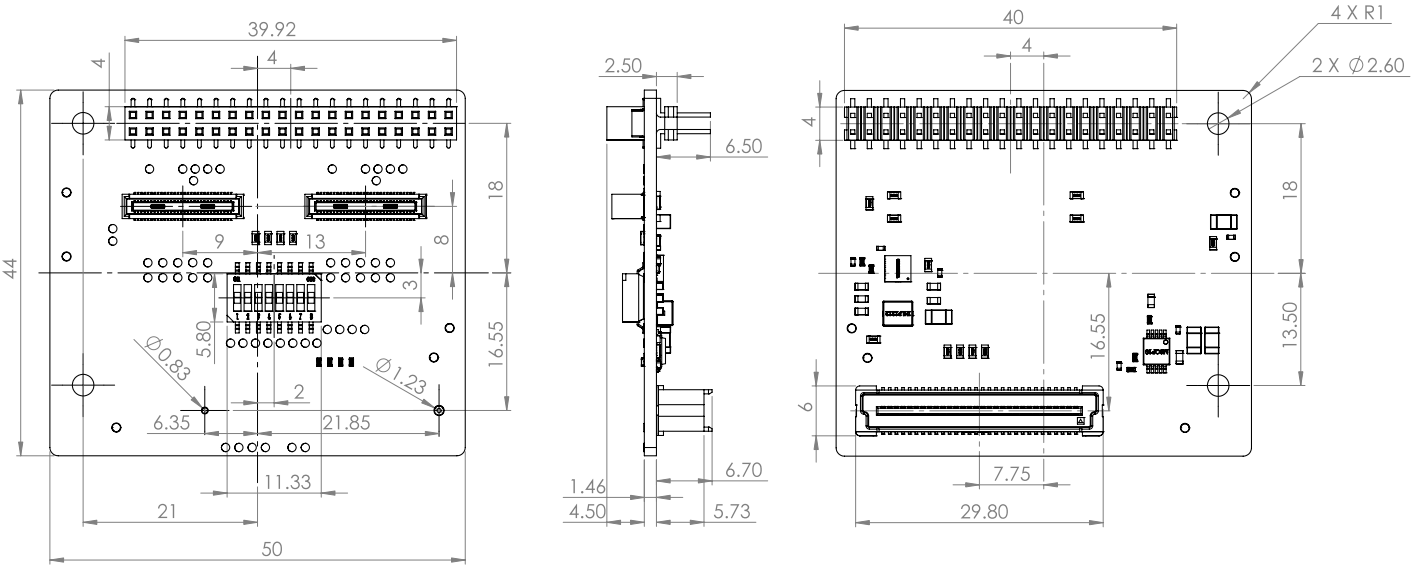


Figure 21: Technical Drawing of FPA-2.A/96B-V1

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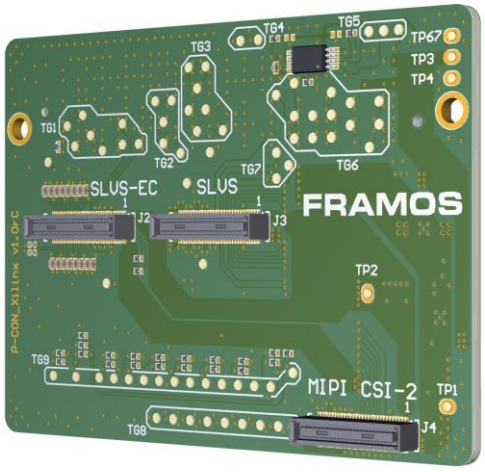
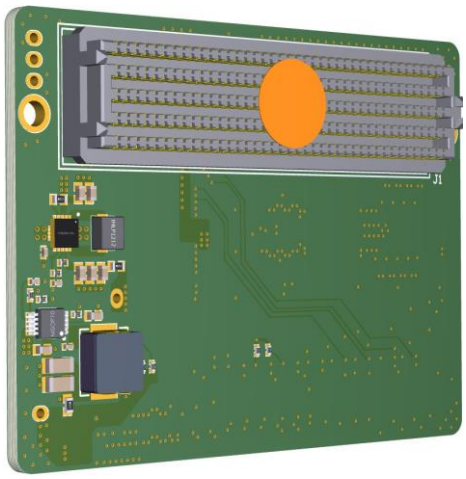
10.7 FPA-ABC/XX1-V1: Multi-Format FPA to Xilinx Development Boards

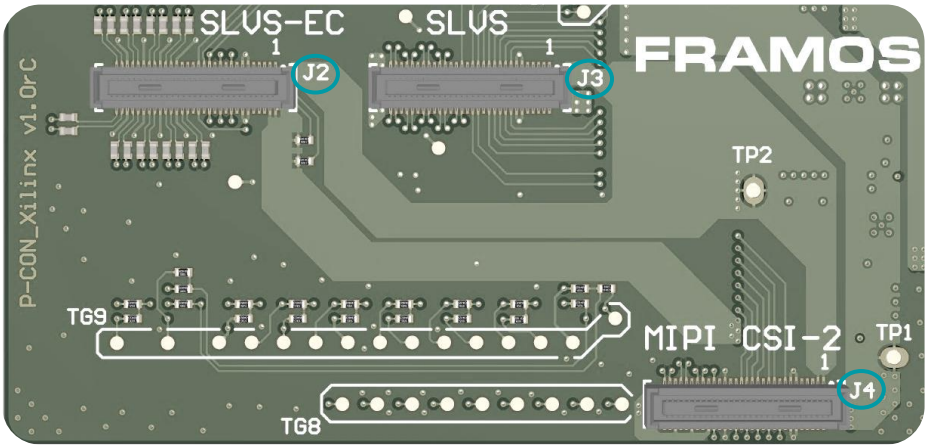
This FPA type connects the FSM Ecosystem via the standardized PixelMate™ interfaces to AMD/Xilinx Development Board deployed with the FPGA Mezzanine Card (FMC) connector.

- Three inputs, one for each interface:
  - SLVS-EC
  - Sub-LVDS / SLVS
  - MIPI CSI-2 (D-PHY)
- EEPROM for dynamic device tree management
- Testpoints to important sensor signals
- Configurable trigger routing
- Compatible to various AMD/Xilinx Development Boards; verified types can be found in the compatibility matrix in this chapter.





10.7.1 Image Sensor Connectors



Label	Name	Description	Connector Type	FPGA Routing
J2	SLVS-EC	Port 2, 8-Lanes SLVS-EC, to FSA	Hirose DF40HC(4.0)-60DS-0.4V	8-Lanes to Transceivers
J3	SLVS	Port 1, 8-Lanes SLVS / Sub-LVDS, to FSA		8-Lanes to differential IOs
J4	MIPI CSI-2	Port 3, 4-Lanes MIPI CSI-2, to FSA		4-Lanes to CSI-2 D-PHY

Table 38: Image Sensor Connectors on FPA-ABC/XX1-V1

All ports provide the same pinout. The pin assignment is according to the corresponding FSA.

Caution: Direct connection of FSM to FPA (without FSA) or wrong cable orientation will lead to permanent damage of FSM, Adapters or the Processor Board. Using flex cable (FMA-FC-150/60-v1) between FSA and FPA is mandatory.

Processor Board Compatibility Matrix

The FPA has been designed to comply to the following Xilinx Development Boards.

Xilinx Development Board	SLVS-EC	SLVS	MIPI CSI-2
AC701-G (Artix-7)	Yes	TBD	TBD
KC705-G (Kintex-7)	Yes	TBD	TBD
ZC706-G (Zynq-7000)	Yes	TBD	TBD
KCU105-G (Kintex UltraScale)	Yes	Yes	TBD
KCU116-G (Kintex UltraScale+)	Yes	TBD	TBD
ZCU102-G (Zynq UltraScale+)	Yes	Yes	Yes

Important Notes:

- **SLVS-EC:** The different AMD/Xilinx Development Boards provide access to a different count of Gigabit Transceivers (GTx). This might limit the utilization of the 8-Lanes available from the FPA. Please refer to the datasheet of the AMD/Xilinx Development Board for more information.
- **MIPI CSI-2 (D-PHY):** The AMD/Xilinx ZCU102-G provides hard D-PHY lanes on the appropriate pins of the FPA connector. The usage of the MIPI CSI-2 port is routed but has not been verified. Operation is in the responsibility of the user. Further AMD/Xilinx Development Kits might be compatible but have not been validated for correct electrical connectivity.
- **Kria KR260:** Boards like the Kria KR260 Robotics Starter Kit integrate the PixelMateS SLVS-EC connector (2-Lane) directly into the carrier board. FSM+FSA are directly connected, an FPA is not needed.

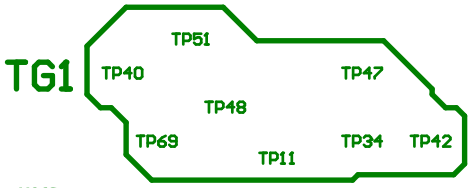
10.7.2 TGx, TPx: Test Groups and Test Points

Ungrouped (according to silk print)

Label	Signal	Label	Signal
TP1	1V8_VDD	**TP67**	UTIL_3V3_10A
TP2	3V8_VDD	**TP75**	GND
TP3	UTIL_3V3	**TP76**	GND
TP4	GND	**TP77**	GND
TP12	CAM1_GPIO0(XMASTER0)	**TP78**	GND

TG1: Clocks and various GPIOs

Label	Signal	Label	Signal
TP11	CAM1_GPIO8(TOUT1)	**TP47**	CAM1_GPIO14
TP34	CAM1_GPIO10	**TP48**	CAM1_MCLK0
TP40	CAM2_GPIO3(XTRIG0)	**TP51**	CAM3_MCLK0
TP42	CAM1_GPIO16	**TP69**	CAM2_MCLK0

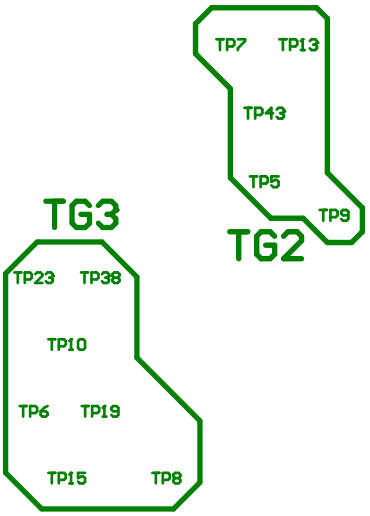


TG2: Various

Label	Signal	Label	Signal
TP5	CAM1_I2C_0_SDA(SPI_MOSI)	**TP13**	CAM1_GPIO9(TOUT2)
TP7	CAM1_GPIO15(SPI_MISO)	**TP43**	CAM1_RST0
TP9	CAM1_GPIO11(TOUT0)		

TG3:

Label	Signal	Label	Signal
TP6	CAM1_I2C_0_SCL(SPI_SCK)	**TP19**	CAM1_GPIO3(XTRIG0)
TP8	CAM1_GPIO17(SPI_CS)	**TP23**	CAM1_GPIO2(XHS0)
TP10	CAM1_GPIO6(SLAMODE)	**TP38**	CAM1_GPIO1(XVS0)
TP15	CAM1_GPIO7(XTRIG2)		



TG4: I2C Clock and Data

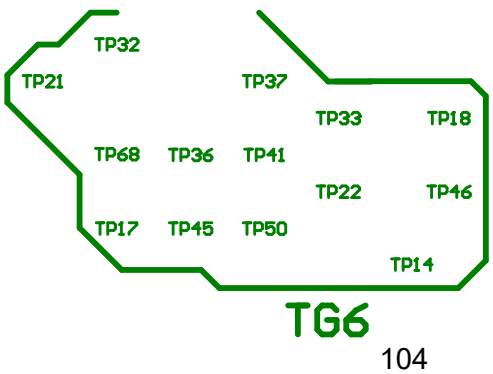
Label	Signal
TP25	SCL
TP26	SDA

TG5: EEPROM Address

Label	Signal
TP27	GA1
TP28	GA0
TP30	GND

TG6:

Label	Signal	Label	Signal
TP14	CAM3_RST0	**TP36**	CAM2_GPIO7(XTRIG2)
TP17	CAM2_GPIO6(SLAMODE)	**TP37**	CAM3_I2C_0_SDA(SPI_MOSI)
TP18	CAM3_GPIO0(XMASTER0)	**TP41**	CAM3_GPIO2(XHS0)
TP21	CAM2_GPIO8(TOUT1)	**TP45**	CAM2_GPIO2(XHS0)
TP22	CAM3_I2C_0_SCL(SPI_SCK)	**TP46**	CAM3_GPIO3(XTRIG0)
TP32	CAM2_GPIO0(XMASTER0)	**TP50**	CAM2_GPIO1(XVS0)
TP33	CAM3_GPIO1(XVS0)	**TP68**	CAM2_RST0



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TG7:

Label	Signal
TP44	CAM2_GPIO9(TOUT2)
TP49	CAM2_GPIO10
TP64	CAM3_GPIO5(MCLK3)

TG8:

Label	Signal
TP52	CAM3_GPIO16(SYS_PW_EN)
TP53	CAM3_GPIO8
TP54	CAM3_GPIO14
TP55	CAM3_RST1
TP60	CAM3_GPIO6
TP61	CAM3_GPIO7

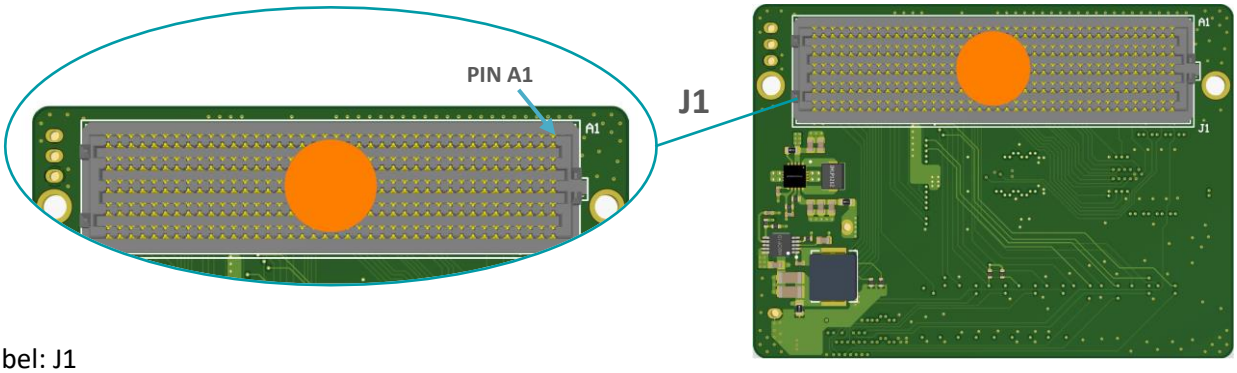
Label	Signal
TP62	CAM3_GPIO4(MCLK2)
TP63	CAM3_MCLK1
TP64	CAM3_GPIO5(MCLK3)

TG9:

Label	Signal
TP16	CAM2_I2C_0_SDA(SPI_MOSI)
TP20	CAM2_I2C_0_SCL(SPI_SCK)
TP24	CAM2_GPIO15(SPI_MISO)
TP35	CAM2_GPIO17(SPI_CS)
TP39	CAM2_GPIO11(TOUT0)
TP56	CAM3_GPIO15(SPI_MISO)
TP57	CAM3_I2C_1_SCL
TP58	CAM3_GPIO17(SPI_CS)

Label	Signal
TP59	CAM3_GPIO9
TP66	CAM2_GPIO14
TP70	CAM3_I2C_1_SDA
TP71	CAM3_GPIO10
TP72	CAM3_GPIO11
TP73	CAM3_PW_EN0
TP74	CAM3_PW_EN1

10.7.3 Processor Board Connector



Label: J1
Type: ASP-134488-01
Pinout (A – J): Table / Table
Notes: **CAM1**: J2 (SLVS-EC), **CAM2**: J3 (SLVS), **CAM3**: J4 (MIPI CSI-2)

Table 39: Pinout J1 - Part1 (A-E) of FPA-ABC/XX1-V1 connector to Xilinx Development Board

PIN #	A	B	C	D	E
1	GND	NC	GND	NC	GND
2	FMC_CAM1_DO1_P	GND	NC	GND	NC
3	FMC_CAM1_DO1_N	GND	NC	GND	NC
4	GND	NC	GND	FMC_CAM1_D_CLK_0_P	GND
5	GND	NC	GND	FMC_CAM1_D_CLK_0_N	GND
6	FMC_CAM1_DO2_P	GND	FMC_CAM1_DO0_P	GND	NC
7	FMC_CAM1_DO2_N	GND	FMC_CAM1_DO0_N	GND	NC
8	GND	NC	GND	CAM2_D_DATA_1_P	GND
9	GND	NC	GND	CAM2_D_DATA_1_N	NC
10	FMC_CAM1_DO3_P	GND	CAM2_D_DATA_5_P	GND	NC
11	FMC_CAM1_DO3_N	GND	CAM2_D_DATA_5_N	CAM2_D_DATA_6_P	GND
12	GND	FMC_CAM1_DO7_P	GND	CAM2_D_DATA_6_N	NC
13	GND	FMC_CAM1_DO7_N	GND	GND	NC
14	FMC_CAM1_DO4_P	GND	CAM2_D_DATA_7_P	CAM1_GPIO15(SPI_MISO)	GND
15	FMC_CAM1_DO4_N	GND	CAM2_D_DATA_7_N	CAM1_GPIO9(TOUT2)	NC
16	GND	FMC_CAM1_DO6_P	GND	GND	NC
17	GND	FMC_CAM1_DO6_N	GND	CAM1_GPIO2(XHS0)	GND
18	FMC_CAM1_DO5_P	GND	CAM1_GPIO1(XVS0)	CAM1_GPIO6(SLAMODE)	NC
19	FMC_CAM1_DO5_N	GND	CAM_GPIO14	GND	NC
20	GND	NC	GND	CAM_GPIO10	GND
21	GND	NC	GND	CAM_GPIO9	NC
22	NC	GND	CAM_GPIO11	GND	NC
23	NC	GND	CAM_GPIO15	CAM3_D_CLK_0_P	GND
24	GND	NC	GND	CAM3_D_CLK_0_N	NC
25	GND	NC	GND	GND	NC
26	NC	GND	CAM_I2C_SDA	CAM3_D_DATA_3_P	GND
27	NC	GND	CAM_GPIO17	CAM3_D_DATA_3_N	NC
28	GND	NC	GND	GND	NC
29	GND	NC	GND	NC	GND
30	NC	GND	SCL	TDI	NC
31	NC	GND	SDA	TDO	NC
32	GND	NC	GND	UTIL_3V3_10A	GND
33	GND	NC	GND	NC	NC
34	NC	GND	GA0	NC	NC
35	NC	GND	NC	GA1	GND
36	GND	NC	NC	UTIL_3V3	NC
37	GND	NC	NC	GND	NC
38	NC	GND	NC	UTIL_3V3	GND
39	NC	GND	UTIL_3V3	GND	VADJ
40	GND	NC	NC	UTIL_3V3	GND

Table 40: Pinout J1 – Part2 (F-J) of FPA-ABC/XX1-V1 connector to Xilinx Development Board

PIN #	F	G	H	I	J
1	NC	GND	NC	GND	NC
2	GND	CAM2_GPIO3(XTRIG)	PRSNT_M2C_L	NC	GND
3	GND	CAM3_MCLK0	GND	NC	GND
4	NC	GND	CAM2_MCLK_0	GND	NC
5	NC	GND	CAM1_MCLK_0	GND	NC
6	GND	CAM2_D_CLK_0_P	GND	NC	GND
7	NC	CAM2_D_CLK_0_N	CAM1_GPIO8(TOUT1)	NC	NC
8	NC	GND	CAM1_GPIO10	GND	NC
9	GND	CAM2_D_DATA_3_P	GND	NC	GND
10	NC	CAM2_D_DATA_3_N	CAM2_D_DATA_0_P	NC	NC
11	NC	GND	CAM2_D_DATA_0_N	GND	NC
12	GND	CAM2_D_DATA_4_P	GND	NC	GND
13	NC	CAM2_D_DATA_4_N	CAM2_D_DATA_2_P	NC	NC
14	NC	GND	CAM2_D_DATA_2_N	GND	NC
15	GND	CAM1_RST0	GND	NC	GND
16	NC	CAM1_I2C_0_SDA(SPI_MOSI)	CAM1_GPIO11(TOUT0)	NC	NC
17	NC	GND	CAM1_GPIO7(XTRIG2)	GND	NC
18	GND	CAM1_I2C_0_SCL(SPI_SCK)	GND	NC	GND
19	NC	CAM1_GPIO3(XTRIG0)	CAM1_GPIO0(XMASTER0)	NC	NC
20	NC	GND	CAM1_GPIO17(SPI_CS)	GND	NC
21	GND	CAM3_D_CLK_1_P	GND	NC	GND
22	NC	CAM3_D_CLK_1_N	CAM3_D_DATA_2_P	NC	NC
23	NC	GND	CAM3_D_DATA_2_N	GND	NC
24	GND	CAM3_D_DATA_0_P	GND	NC	GND
25	NC	CAM3_D_DATA_0_N	CAM3_D_DATA_1_P	NC	NC
26	NC	GND	CAM3_D_DATA_1_N	GND	NC
27	GND	CAM_I2C_SCL	GND	NC	GND
28	NC	CAM2_GPIO8(TOUT1)	CAM2_RST0	NC	NC
29	NC	GND	CAM2_GPIO6(SLAMODE)	GND	NC
30	GND	CAM2_GPIO0(XMASTER0)	GND	NC	GND
31	NC	CAM2_GPIO7(XTRIG2)	CAM2_GPIO2(XHS0)	NC	NC
32	NC	GND	CAM2_GPIO1(XVS0)	GND	NC
33	GND	CAM3_I2C_0_SDA(SPI_MOSI)	GND	NC	GND
34	NC	CAM3_GPIO2(XHS0)	CAM_GPIO16	NC	NC
35	NC	GND	CAM3_I2C_0_SCL(SPI_SCK)	GND	NC
36	GND	CAM3_GPIO1(XVS0)	GND	NC	GND
37	NC	CAM3_GPIO0(XMASTER0)	CAM3_RST0	NC	NC
38	NC	GND	CAM3_GPIO3(XTRIG0)	GND	NC
39	GND	NC	GND	NC	GND
40	NC	GND	NC	GND	NC

10.7.4 Technical Drawing

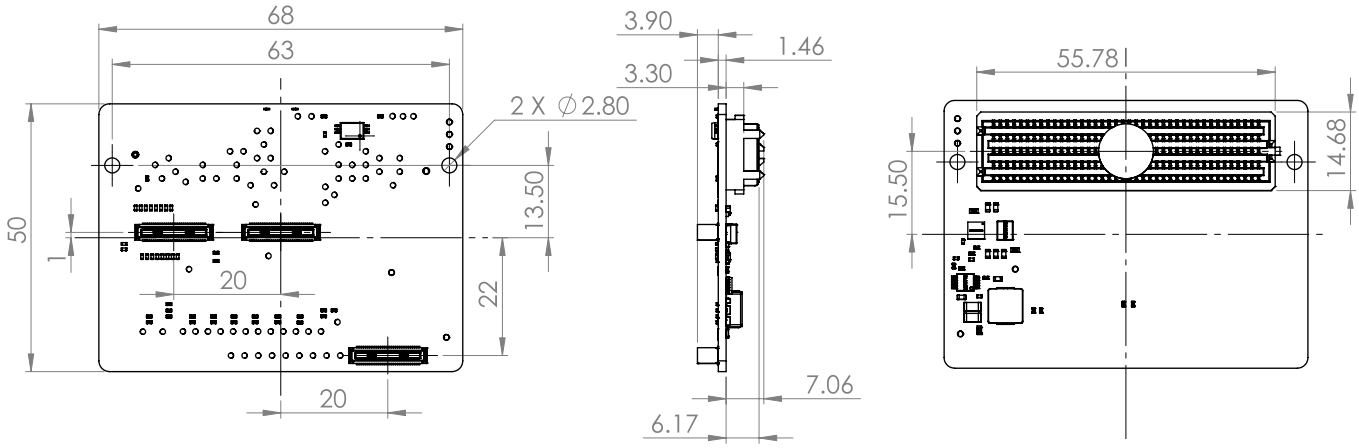


Figure 22: Technical Drawing of FPA-ABC/XX1-V1

11 FRAMOS Module Accessories (FMA)

11.1 FMA-MNT-CCS/265-V1: C/CS-Mount for 26.5mm Footprint

CS-mount body delivered with 5mm CS- to C-Mount extension ring.

- Lens Thread: 1-32 UN 2A
- Extension Ring: CS- to C-Type, BFD + 5 mm
- Material: AlMgSi0.5
- Finish: Black Anodizing
- Optical Filter: Not applicable

Technical Drawing

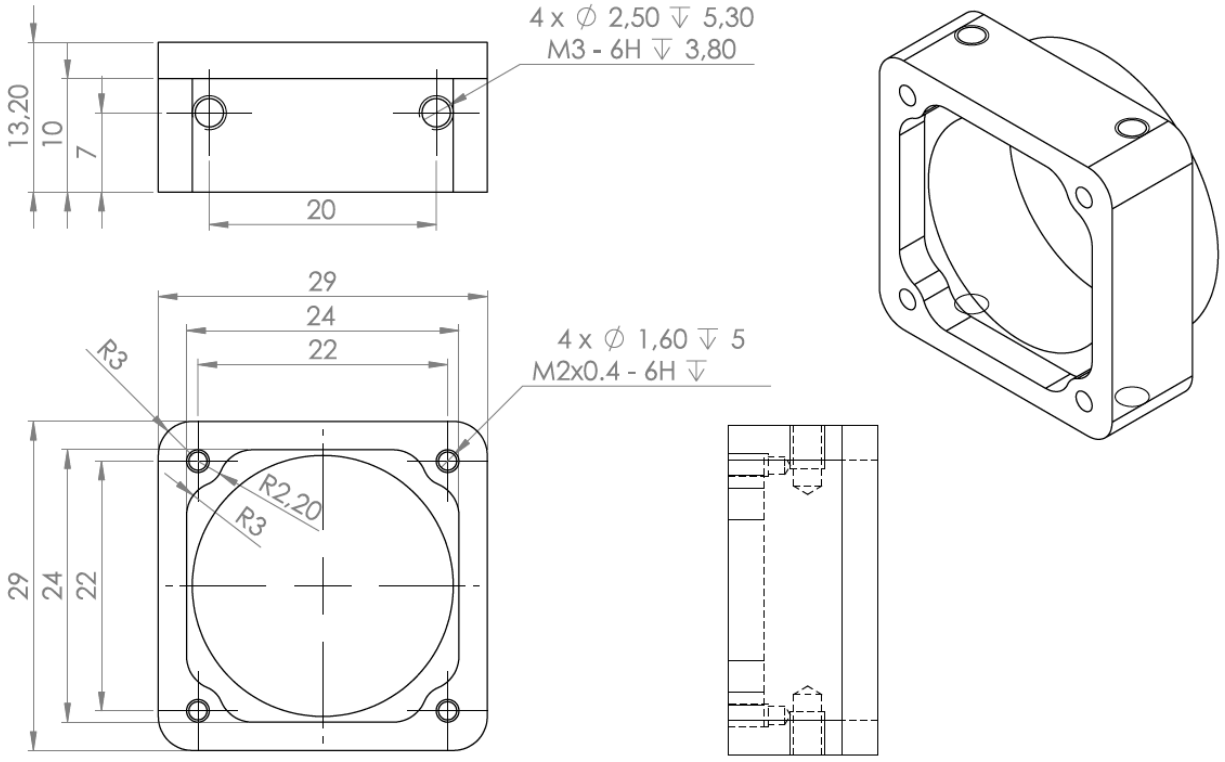


Figure 23: CS-Mount Body for 26.5 mm FSM

Note: The sensor specific distance of the active pixel layer to PCB and different types of sensor cover glasses might require adding a number of 0.1 mm distance rings to raise the flange height. Appropriate spacers or extension rings are not provided with the lens mount. All FSMs delivered with this mount applied are adjusted accordingly to meet the correct back focal distance by C- and CS-Mount standard using thin foils between mount and PCB.

11.2 **FMA-MNT-CCS/280-V1:** C/CS-Mount for 28mm FSM Footprint

CS-mount body delivered with 5mm CS- to C-Mount extension ring.

- Lens Thread: 1-32 UN 2A
- Extension Ring: CS- to C-Type, BFD + 5 mm
- Material: AlMgSi0.5
- Finish: Black Anodizing
- Optical Filter: Not applicable

Technical Drawing

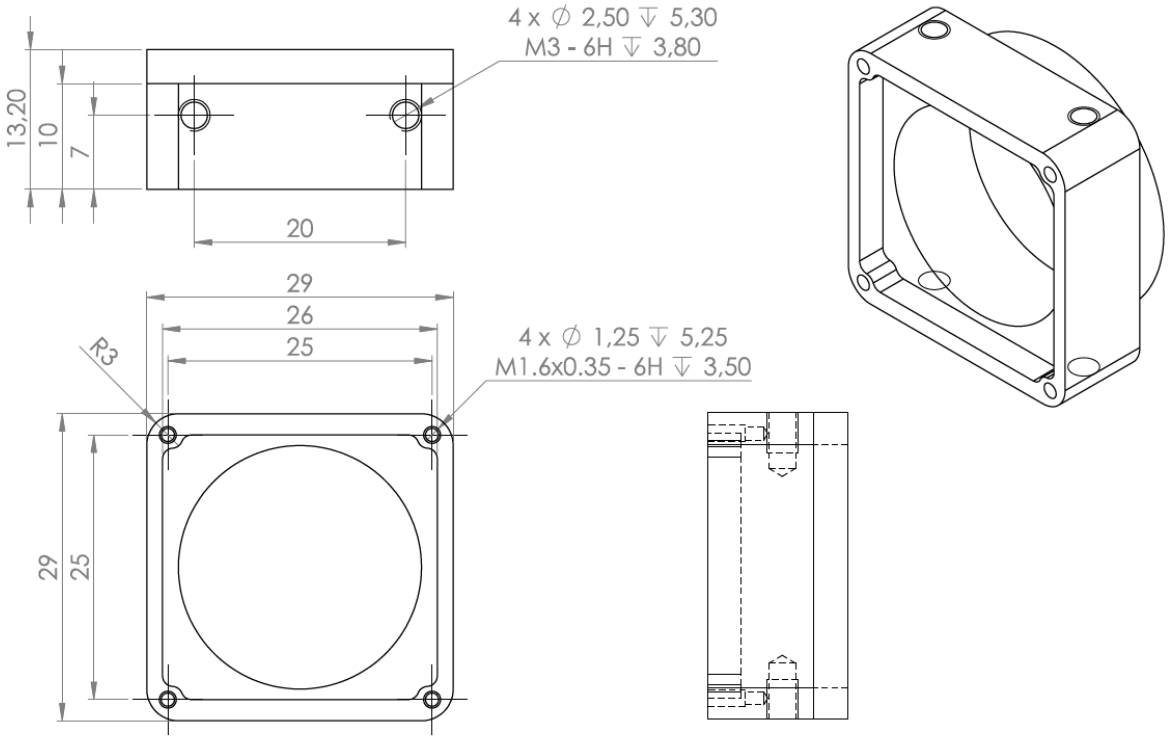


Figure 24: CS-Mount Body for 28 mm FSM

Note: The sensor specific distance of the active pixel layer to PCB and different types of sensor cover glasses might require adding a number of 0.1 mm distance rings to raise the flange height. Appropriate spacers or extension rings are not provided with the lens mount. All FSMs delivered with this mount applied are adjusted accordingly to meet the correct back focal distance by C- and CS-Mount standard using thin foils between mount and PCB.

11.3 FMA-FC-150/60-V1: Flex Cable for MIPI CSI-2 Connections

- FSA to FPA for MIPI CSI-2 connections (mandatory)
- Extension through “daisy-chaining” possible (maximum length is sensor and setup depending)
- Rigid-flex design (connectors on rigid PCBs)

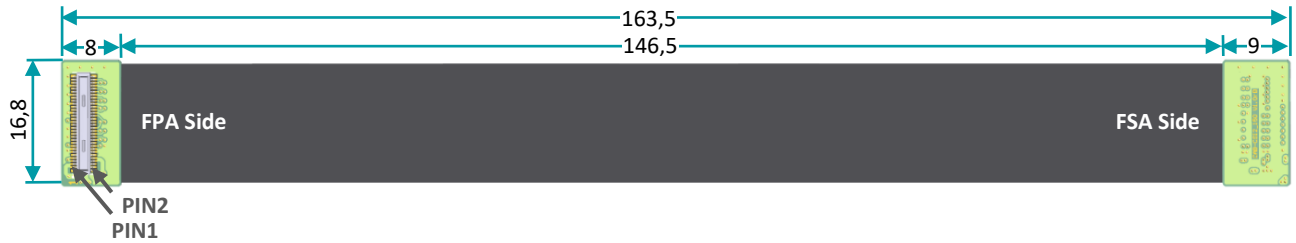
Note: Don’t use for any other connections than for MIPI CSI-2. Might lead to signal degradation and even damage!

Flex Cable Connectors

- FSA Side: Hirose DF40C-60DS-0.4V
- FPA Side: Hirose DF40C-60DP-0.4V
- Pin Assignment: Pin 1 to Pin 1

Mechanical Drawing

Top Side



Bottom Side

11.4 FMA-FC-150/60-LVDS-V1: Flex Cable for Sub-LVDS, SLVS and SLVS-EC Connections

- FSA to FPA for Sub-LVDS, SLVS and SLVS-EC connections (mandatory)
- Extension through “daisy-chaining” possible (maximum length is sensor and setup depending)
- Rigid-flex design (connectors on rigid PCBs)

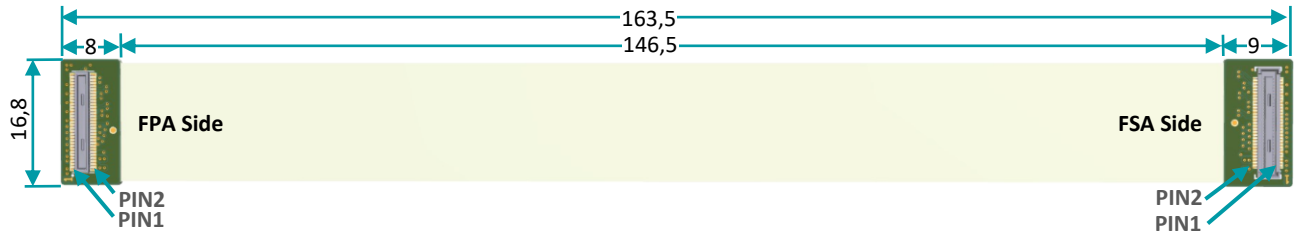
Note: Don’t use for MIPI CSI-2 connections. Might lead to signal degradation and even damage!

11.4.1 Flex Cable Connectors

- FSA Side: Hirose DF40C-60DS-0.4V
- FPA Side: Hirose DF40C-60DP-0.4V
- Pin Assignment: Pin 1 to Pin 1

11.4.2 Mechanical Drawing and Pinout

Top Side



Bottom Side

12 Software Package and Drivers

At FRAMOS, we know the challenge of getting started with new technology. The idea behind the Software Package is to allow embedded software engineers quick access to a streaming system and to provide the required tools to extend and adapt it according to their application needs and use.

What the software package and driver are:

- A reference for a custom sensor implementation
- Demonstrating how to use the required interfaces
- Demonstrating how to communicate with the image sensor
- Demonstrating how to generally initialize and configure the image sensor
- Provide initial image streaming output to the user space
- Demonstrating how to run basic image processing on pixel data

Supported Processor Platforms

The table below shows which platforms are supported by the standard driver package, and how many FSMs can at maximum be operated in parallel.

Sensor Module	NVIDIA Jetson TX2	NVIDIA AGX Xavier / AGX Orin	NVIDIA Jetson Nano, TX2 NX, Xavier NX	DragonBoard 410c	96Boards Consumer Edition	Xilinx Development Boards
FSM-AR0144	4		2		HW only, driver development on project basis.	
FSM-AR0521	4		2	2		
FSM-AR1335	4		2			
FSM-HDP230	4	4	2			
FSM-IMX264	2	4	-			
FSM-IMX283	2	4	-			
FSM-IMX290	4		2	2		
FSM-IMX296	4		2	2		
FSM-IMX297	4		2			
FSM-IMX304	2	4	-			
FSM-IMX327	4		2	2		
FSM-IMX334	2	4	-			
FSM-IMX335	4		2			
FSM-IMX412	4		2	2		
FSM-IMX415	4		2			
FSM-IMX462, 662	4		2			
FSM-IMX464	4		2			
FSM-IMX477	4		2			
FSM-IMX485, 585	4		2			
FSM-IMX565, 568	4		2			
FSM-IMX577	4		2			
FSM-IMX675	4		2			
FSM-IMX678	4		2			
FSM-IMX715	4		2			
FSM-IMX530	2	4	-			1[10]

Table 41: Ecosystem Software Package - Supported number of FSMs per processing board

[10] SLVS-EC based FPGA reference implementation as part of the SLVS-EC RX IP Core offering.

12.1 Reference Software: NVIDIA Jetson Family

The software package provided with the Development Kits of the FRAMOS Sensor Module Ecosystem provided for NVIDIA Jetson platforms provides a reference implementation of sensor and device drivers for MIPI CSI-2. It contains a minimum feature set demonstrating how to utilize the platform specific data interface and communication implementation, as well as the initialization of the image sensor and implementation of basic features.

Package Content:

- Platform and device drivers with Linux for Tegra Support
- V4L2 based subdevice drivers (low-level C API)
- Streamlined V4L2 library (LibSV) providing generic C/C++ API
- Display Examples:
  - OpenCV (Software)
  - LibArgus (Hardware)

Supported Devices:

- NVIDIA Jetson Nano Developer Kit (B01)
- NVIDIA Jetson TX2 Developer Kit
- NVIDIA Jetson TX2 NX Developer Kit
- NVIDIA Jetson Xavier NX Developer Kit
- NVIDIA Jetson Orin NX SoM with carrier Jetson Nano Developer Kit
- NVIDIA Jetson AGX Xavier and AGX Orin Developer Kit

12.1.1 Platform and Sensor Device Drivers

The driver divides into two main parts that are configured in separate ways – the image modes and the general features of the image sensor.

Image Modes

These are major attributes that have impact to the image data stream formatting. They require a static pre-configuration within the device tree (DT):

- Image / streaming resolution
- Pixel format / bit depth
- Data rate / lane configuration

Each driver provides access to 3 – 5 pre-built configurations, reflecting the main operation modes of the imager. Beside the full resolution, that is always available, they allow to receive image streams in common video resolutions like VGA, Full HD and UHD as they are supported or make sense by the imagers, and utilize sensor features like ROI and binning.

They act as an example for implementation and are available as source. Due to the size limitation of the device tree, it is not possible to integrate an extensive set of options.

General Features

These are attributes of the image sensor that do not manipulate the data stream formatting. The drivers provided with the Software Pack integrate the sensor features as shown in the table below.

Pre-Implemented Features per Model	Gain (Analog / Digital)	Frame Rate	Exposure Time	Flip / Mirror	IS Mode (Master / Slave)	Sensor Mode ID	Test Pattern Output	Black Level	HDR Output	Broadcast	Data Rate	Synchronizing Master
FSM-AR0144												
FSM-AR0521												
FSM-AR1335												
FSM-HDP230												
FSM-IMX264												
FSM-IMX283												
FSM-IMX290												
FSM-IMX296												
FSM-IMX297												
FSM-IMX304												
FSM-IMX327												
FSM-IMX334												
FSM-IMX335												
FSM-IMX412												
FSM-IMX415												
FSM-IMX462												
FSM-IMX464												
FSM-IMX477												
FSM-IMX485												
FSM-IMX530												
FSM-IMX565, 568												
FSM-IMX577												
FSM-IMX585												
FSM-IMX662												
FSM-IMX675												
FSM-IMX678												
FSM-IMX715												

V4L (libsv) and libargus
V4L (libsv)
Not Supported/Implemented

Table 42: Supported sensor features on NVIDIA Jetson Family

Further features, as they are supported by the image sensor, can be integrated into the driver sources using the image sensor datasheet.

12.1.2 Image Pre-Processing Examples

The provided image processing examples show the general mechanisms of data handling for an image processing using 3rd-party libraries. The OpenCV example provides data that is raw (mono) or demosaiced (color) and not further optimized for visual experience, while the LibArgus examples leverages the discrete ISP (Image Signal Processor) inside the Jetson SoC to optimize image reproduction.

Argus Camera Example:

- Using hard ISP in NVIDIA Jetson SoCs, most performant option for image preprocessing
- Only applicable for color sensors (color processing can not be disabled)
- Most performant option
- Utilizing libArgus closed source library, support and tuning on individual basis through FRAMOS
- Example Implementation: Shows Demo Tuning per FSM Devkit

	Xavier (AGX, NX)	**Tegra X2** (TX2, TX2 NX)	**Tegra X1** (TX1, Nano)
Performance			
Max. # of streams through ISP	16	12	6
Pixel Bandwidth (max.)	2 Gpix/s	1.4 Gpix/s	1.4 Gpix/s
Image Resolution (max.)	64 MP	24 MP	24 MP
Image Width (max.)	6144 px	6144 px	6144 px

Table 43: ISP capabilities / limitations of NVIDIA Jetson Family

The software package provided with our FSM Devkits contains a functionally and performance limited example configuration for the Jetson ISP. The configuration is sensor and lens related and demonstrates the combination of our standard kit in environments that are illuminated with fluorescent light, like in office or laboratory.

Supported Features in Default Configuration	
Lens Considered (Type)	Yes (Devkit Lens)
IR Cut Filter (Type)	Yes (650nm/50%)
Sensor Configuration	Driver Default
Demosaic	Yes[11]
Black Level Compensation	Yes (Calibrated)
Bad Pixel Correction	Yes (Calibrated)
Color Correction	Yes (Calibrated)
Auto White Balance (A, TL84, D65)	Limited (Calibrated for TL84 only)
Manual White Balancing	Limited (Not Calibrated)
Lens Shading / Falloff Correction	Limited (Calibrated for Devkit lens)
Noise Reduction	Limited (Not Calibrated)
Sharpening	Limited (Not Calibrated)
Auto Exposure, Gain, Gamma, Color/Tone, Contrast Tuning	Requires Application Specific Tuning

[11] Demosaicing is always active and can't be disabled. For monochrome sensors refer to libSV to bypass the ISP.

Table 20: Default tuning of NVIDIA Jetson, supplied with FSM Devkits

A fully featured calibration will be required to achieve the best performance and stable results, even in variable lighting conditions. As an NVIDIA camera partner, FRAMOS provides full ISP configurations for standard setups on request. Full custom calibration services considering lens and application specific requirements for sophisticated applications are provided on per project basis.

OpenCV Example:

- Open software library
- Easy to use and large feature set
- Very resource hungry (CPU)
- Not recommended for pre-processing
- Example Implementation: Demosaicing, Displaying

Due to limited performance and extreme resource utilization, the image pre-processing support utilizing the CPU will not be further enhanced. This does not affect users of OpenCV for their purposes.

13 Ecosystem Compatibility Matrix

13.1 Hardware Support

The following matrix shows the compatibility of FSMs, FSAs and FPAs to each other. The FSAs differentiate to each other by supplied voltages, power up sequence, generated clock (oscillator) and physical attributes.

Sensor Modules with MIPI CSI-2 (D-PHY) Output

Item	FSM-IMX412 FSM-IMX477 FSM-IMX577	FSM-IMX290 FSM-IMX327 FSM-IMX334 FSM-IMX335 FSM-IMX462 FSM-IMX464 FSM-IMX485	FSM-IMX296 FSM-IMX297	FSM-AR0521 FSM-AR1335	FSM-IMX415 FSM-IMX715	FSM-IMX283	FSM-AR0144	FSM-HDP230	FSM-IMX565 FSM-IMX568 FSM-IMX585 FSM-IMX662 FSM-IMX675 FSM-IMX678
FSA-FT1/A	FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]								
FSA-FT3/A		FPA-4.A/TXA FPA-A/NVN[13] FPA-2.A/96B FPA-ABC/XX1[12]							
FSA-FT6/A			FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]						
FSA-FT7/A				FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]					
FSA-FT11/A					FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]				
FSA-FT12/A						FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[12]			
FSA-FT13/A							FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]		
FSA-FT19/A								FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]	
FSA-FT26/A									FPA-4.A/TXA FPA-A/NVN FPA-2.A/96B FPA-ABC/XX1[12]

Table 45: Ecosystem Compatibility Matrix – Native CSI-2 (D-PHY) FSMs

[12] Not verified, Xilinx Development Board with hard MIPI CSI-2 / D-PHY interface.
[13] FSM-IMX334 is not supported due to the sensor requiring 4-lanes MIPI.

Sensor Modules with (Sub-) LVDS and SLVS Output

Item	Data Output (FSA)	FSM-IMX264	FSM-IMX304	FSM-IMX421	FSM-IMX530
FSA-FT14/A-00G	MIPI CSI-2	FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[12]			
FSA-FT15/A-00G	MIPI CSI-2		FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[12]		
FSA-FT18/A-00G	MIPI CSI-2				FPA-4.A/TXA FPA-2.A/96B FPA-ABC/XX1[12]
FSA-FT18/BC	SLVS, SLVS-EC				FPA-ABC/XX1 FPA-C/AGX
FSA-FT20/BC	SLVS-EC			FPA-ABC/XX1	

Table 46: Ecosystem Compatibility Matrix – Sub-LVDS, SLVS and SLVS-EC FSMs

14 Contact Information

FRAMOS GmbH

Technical Support: support@framos.com
Website: https://www.framos.com

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