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Colibri iMX8X

Datasheet

Revision History

Date	Doc. Rev.	Colibri iMX8X Version	Changes
24-Sep-2018	Rev. 0.9	V1.0	Initial Release
05-Oct-2018	Rev. 0.91	V1.0	Update product variants Minor changes
16-Oct-2018	Rev. 0.92	V1.0	Section 5.16.1: Correct I2S Slave pins
07-Dec-2018	Rev. 0.93	V1.0	Section 1.2: Add Colibri iMX8DX 1GB and Colibri iMX8DX 1GB WB Section 3.3: Add more information to compatible FFC connectors Section 3.4: Add more information to compatible FFC connectors
14-Dec-2018	Rev. 0.94	V1.0	Section 2.1: Add not regarding additional signals Section 5.3: Clarify restrictions due to shared MDIO signals Minor changes
12-Jun-20	Rev. 0.95	V1.0	Section 1.2.1: CPU information updated Minor changes
07-Jul-20	Rev. 0.96	V1.0	Sections 1.1 and 1.2.1: HiFi 4 DSP functionality has been removed from the document as it will not be supported anymore by this product
20-Oct-20	Rev. 0.97	V1.0	Adding section 1.2.4 and 1.2.5 Section 3.2: Correction of pin 139, 141, 143, and 145 note Section 3.4: Remove link to OV5640 camera Section 5.3: Add limitations of second RGMII Ethernet port Section 5.21: Change ADC input resistor from 10kΩ to 1kΩ Section 5.22: Update camera section and adding MIPI CSI-2 Minor changes
18-May-2021	Rev. 0.98	V1.0	Section 1.2.1: Correcting SoC part numbers Section 4.3: Clarify reset state Section 4.4.1: Update reset state of pin 127 and 131 Section 5.24: Add support for CAN-FD Section 8.2: Rename Section Section 8.3 Add section with power consumption clarification Minor changes

Contents

1. Introduction

1.1 Hardware

The Colibri iMX8X is a computer module based on the NXP® i.MX 8X Family of embedded System on Chip (SoC). The i.MX 8X Family consists of the i.MX 8QuadXPlus, i.MX 8DualXPlus, and i.MX 8DualX. The top-tier i.MX 8QuadXPlus (i.MX 8QXP) features four Cortex-A35 cores as the main processor cluster. The Cortex-A35 is currently Arm's most efficient Armv8 core. They provide full 64-bit Armv8-A support while maintaining seamless backward compatibility with 32-bit Armv7-A software. The main cores run with up to 1.2 GHz.

Additional to the main CPU complex, the i.MX 8QXP features a Cortex-M4F processor, which peaks up to 266 MHz. This processor is independent of the main complex and features its own dedicated interfaces while also accessing the regular interfaces. This heterogeneous multicore system allows for running additional real-time operating systems on the M4 cores for time- and security-critical tasks. The i.MX 8QXP features a System Controller Unit (SCU), which runs on an additional independent Cortex-M4 processor. This controller's primary task is resource management with proper access and permission control to ensure the M4 core and main CPU complex are isolated from each other. This massively increases the safety of the heterogeneous multicore system in comparison with older SoCs.

The i.MX 8QXP features a powerful GC7000Lite Graphic Processing Unit (GPU) from Vivante®. The GPU provides 16 Vega shader cores with tessellation, geometry, and compute shaders. The GPU can peak with up to 64 GFLOPS and supports OpenGL® 3.0, OpenGL® ES3.1, DirectX® 11, and Vulkan. The SoC features a Video Processing Unit (VPU) for accelerating video decoding and encoding.

The Colibri iMX8X incorporates DVFS (Dynamic Voltage and Frequency Switching) and thermal throttling, enabling the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

The Colibri iMX8X is also available as a version with a Dual-Band (2.4/5 GHz) Wi-Fi ac/a/b/g/n and Bluetooth 5/BLE interface. The Wi-Fi module features MHF4 compatible connectors for external antennas. The module is pre-certified for FCC (US), CE (Europa), and IC (Canada).

The module targets a wide range of applications, including medical devices, navigation, industrial automation, HMIs, avionics, POS, data acquisition, robotics, and much more.

It offers a wide range of interfaces from simple GPIOs, industry-standard I2C, SPI, CAN-FD, and UART buses to high-speed USB 2.0 interfaces. The Colibri iMX8X module features a Fast Ethernet PHY with IEEE1588 support on the module. Additionally, the module allows connecting an additional (Gigabit) Ethernet PHY on the customer carrier board using the RGMII or RMII interface.

The Colibri iMX8X module encapsulates the modern-day electronic design's complexity, such as high-speed impedance controlled layouts with high component density utilizing blind via technology. This allows the customer to create a simple carrier board, which provides his application-specific electronics. The module is compatible with a wide range of other computer modules within the Colibri family. This allows the customer to scale their product without building different carrier boards for each project.

1.2 Main Features

1.2.1 CPU

	Colibri iMX8DX 1GB	Colibri iMX8DX 1GB WB	Colibri iMX8QXP 2GB IT	Colibri iMX8QXP 2GB WB IT
i.MX 8X Family SoC	MIMX8UX5CVLFZAx	MIMX8UX5CVLFZAx	MIMX8QX5CVLFZAx	MIMX8QX5CVLFZAx
Arm Cortex-A35 CPU Cores	2	2	4	4
Arm Cortex-M4F CPU Cores	1	1	1	1
L1 Instruction Cache (each core)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)
L1 Data Cache (each core)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)	32 KByte (A35) 16 KByte (M4)
L2 Cache (shared by all A35 cores)	512 KByte (A35)	512 KByte (A35)	512 KByte (A35)	512 KByte (A35)
Tightly-Coupled Memory	256 KByte (M4)	256 KByte (M4)	256 KByte (M4)	256 KByte (M4)
Maximum CPU frequency	1.2 GHz (A35) 266 MHz (M4)	1.2 GHz (A35) 266 MHz (M4)	1.2 GHz (A35) 266 MHz (M4)	1.2 GHz (A35) 266 MHz (M4)
Maximum VPU frequency	600MHz	600MHz	600MHz	600MHz
NEON MPE	✓	✓	✓	✓
Arm TrustZone	✓	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓	✓
Secure JTAG Controller	✓	✓	✓	✓
Secure Non-Volatile Storage	✓	✓	✓	✓

1.2.2 Memory

	Colibri iMX8DX 1GB	Colibri iMX8DX 1GB WB	Colibri iMX8QXP 2GB IT	Colibri iMX8QXP 2GB WB IT
LPDDR4 RAM Size	1 GByte	1 GByte	2 GByte	2 GByte
LPDDR4 RAM Speed	2400 MT/s	2400 MT/s	2400 MT/s	2400 MT/s
LPDDR4 RAM Memory Width	1x16 bit	1x16-bit	1x32 bit	1x32-bit
eMMC NAND Flash (8bit)* V5.0	4 GByte	4 GByte	8 GByte	8 GByte

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear-leveling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.2.3 Interfaces

	Colibri iMX8DX 1GB	Colibri iMX8DX 1GB WB	Colibri iMX8QXP 2GB IT	Colibri iMX8QXP 2GB WB IT
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	1	-	1
Bluetooth 5/BLE	-	1	-	1
LCD RGB (720p60)	1 (up to 24bit)	1 (up to 24bit)	1 (up to 24bit)	1 (up to 24bit)
MIPI/DSI LVDS	2x 4 data lanes* 1x dual-channel*	2x 4 data lanes* 1x dual-channel*	2x 4 data lanes* 1x dual-channel*	2x 4 data lanes* 1x dual-channel*
Resistive Touch Screen	4 Wire	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)	1 (Mono)	1 (Mono)
SAI (AC97/I^{2}S)	3* (2x only input)	3* (2x only input)	3* (2x only input)	3* (2x only input)
ESAI (AC97/I^{2}S)	1*	1*	1*	1*
S/PDIF	1 in / 1 out	1 in / 1 out	1 in / 1 out	1 in / 1 out
Medium Quality Sound (MQS)	1* (Stereo)	1* (Stereo)	1* (Stereo)	1* (Stereo)
Parallel Camera Interface	1	1	1	1
MIPI/CSI-2	1x 4 data lanes*	1x 4 data lanes*	1x 4 data lanes*	1x 4 data lanes*
I2C	1+7*	1+7*	1+7*	1+7*
SPI	1+2*	1+2*	1+2*	1+2*
UART	3+2*	3+2*	3+2*	3+2*
SD/SDIO/MMC	1	1	1	1
GPIO	94*	97*	94*	97*
USB 2.0 OTG (host/device)	1	1	1	1
USB 2.0 host	1	1	1	1
10/100 MBit/s Ethernet	1	1	1	1
RGMII/RMII interface for 2nd Ethernet PHY on Baseboard	1*	1*	1*	1*
PWM	4+6*	4+6*	4+6*	4+6*
Analogue Inputs	4	4	4	4
CAN/CAN-FD	3*	3*	3*	3*
External Memory Bus	-	-	-	-
QSPI	2*	2*	2*	2*
MLB	1*	1*	1*	1*

*These additional interfaces are available on pins that are not defined as standard interfaces in the Colibri architecture. They are alternate functions for pins that provide primary interfaces. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. For more information, please also check the list in section 4.4.1 and the description of the associated interface in section 5.

1.2.4 Graphic Processing Unit (GPU)

	Colibri iMX8DX 1GB	Colibri iMX8DX 1GB WB	Colibri iMX8QXP 2GB IT	Colibri iMX8QXP 2GB WB IT
Vivante GC7000Lite GPU Units	1	1	1	1
Vega Shaders (per unit)	16	16	16	16
OpenGL® ES 3.2	-	-	-	-
OpenGL® ES 3.1, 3.0	✓	✓	✓	✓
OpenGL 3.0, 2.1	✓	✓	✓	✓
DirectX 11	✓	✓	✓	✓
OpenVG 1.1	✓	✓	✓	✓
DirectFB 1.4+	✓	✓	✓	✓
GDI (Direct Draw)	✓	✓	✓	✓
Vulkan 1.0 support	✓	✓	✓	✓

1.2.5 Video Processing Unit (VPU)

	Colibri iMX8DX 1GB	Colibri iMX8DX 1GB WB	Colibri iMX8QXP 2GB IT	Colibri iMX8QXP 2GB WB IT
H.265 decode (4Kp30)	-	-	✓	✓
H.264 decode (4Kp30)	✓	✓	✓	✓
WMV9/VC-1 simple decode	✓	✓	✓	✓
MPEG 1 and 2 decode	✓	✓	✓	✓
AVS decode	✓	✓	✓	✓
MPEG4.2 ASP, H.263 Sorenson Spark decode	✓	✓	✓	✓
Divx 3.11 including GMC decode	✓	✓	✓	✓
ON2/Google VP6/VP8 decode	✓	✓	✓	✓
RealVideo 8/9/10 decode	✓	✓	✓	✓
JPEG and MJPEG decode	✓	✓	✓	✓
H.264 encode (1080p30)	✓	✓	✓	✓

1.2.6 Supported Operating Systems

- ✓ Embedded Linux
- ✓ For other operating systems, please contact Toradex

1.3 Interface Overview

The table in Figure 1 shows the interfaces supported on the Colibri iMX8X module and whether an interface is provided as a standard (primary) function or as an alternate function of a SODIMM pin. The UART interface is an example of an interface that uses standard and alternate functions – three UART interfaces are provided as standard functions compatible with other Colibri modules. In comparison, two additional interfaces are available as alternate functions. Using alternate function UART interfaces limits the compatibility of the Colibri iMX8X module with other Colibri modules. The alternate function of a pin can only be used if the standard function is not used. Check section 4.4 for a list of all alternate functions of the SODIMM pins.

Some interfaces are located on additional Flexible Flat Cable (FFC) connectors. These connectors are dedicated to the specific interface. The connectors are not compatible with other Colibri modules.

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Colibri iMX8X Module. The tool allows comparing the interfaces of different Colibri modules. More information on this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer.

Feature	Total	Standard	Alternate Function	Dedicated FFC
4 Wire Resistive Touch	1	1		
Analogue Inputs	4	4		
Analogue Audio (Line in/out, Mic in)	1	1		
CAN/CAN-FD	3		3	
ESAI (AC97/I2S)	1		1	
Fast Ethernet	1	1		
GPIO	97*		97*	
I2C	8	1	7	
Medium Quality Sound (MQS)	1		1	
MIPI/CSI-2	1			1
MIPI/DSI; LVDS	2			2
MLB	1		1	
QSPI	2		2	
Parallel Camera	1	1		
Parallel LCD (18bit)	1	1		
PWM	10	4	6	
RMII/MII interface	1		1	
SAI (AC97/I^2S)	3		3	
SD/SDIO/MMC	1	1		
SPDIF (input/output)	1		1	
SPI	3	1	2	
UART	5	3	2	
USB 2.0 OTG (host/device)	1	1		
USB 2.0 host	1	1		

Figure 1: Colibri iMX8X Module Interfaces

*These interfaces are not available on all versions of the Colibri iMX8X module. Please see section 1.2 for more information.

1.4 Reference Documents

1.4.1 NXP i.MX 8X

You will find the details about i.MX 8X SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8x-family-arm-cortex-a35-3d-graphics-4k-video-dsp-error-correcting-code-on-ddr:i.MX8X

1.4.2 Ethernet Transceiver

Colibri iMX8X uses the Micrel KSZ8041NL Ethernet PHY:
http://www.microchip.com/wwwproducts/en/KSZ8041

1.4.3 Audio Codec

Colibri iMX8X uses the NXP SGTL5000 Audio Codec.
http://www.nxp.com/products/interface-and-connectivity/interface-and-system-management/switch-monitoring-ics/ultra-low-power-audio-codec:SGTL5000

1.4.4 Touch Screen Controller

Colibri iMX8X uses the Analog Device AD7879-1 Touchscreen Controller.
http://www.analog.com/en/products/analog-to-digital-converters/integrated-special-purpose-converters/capacitive-to-digital-and-touch-screen-controllers/ad7879.html

1.4.5 Wi-Fi and Bluetooth Module

Some of the Colibri iMX8X use the Azurewave AW-CM276NF wireless module. The AW-CM276NF datasheet is available under NDA from Toradex. Please contact your local sales team for more information.
https://developer.toradex.com/knowledge-base/azurewave-aw-cm276nf-wi-fi-bluetooth-module

1.4.6 Toradex Developer Center

You can find a lot of additional information on the Toradex Developer Center, which is regularly updated with the latest product support information.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the Colibri iMX8X.
http://developer.toradex.com

1.4.7 Colibri Evaluation Board Schematics

We provide the complete schematics and the Altium project file (including library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards) free of charge. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.4.8 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparison of the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

2. Architecture Overview

2.1 Block Diagram

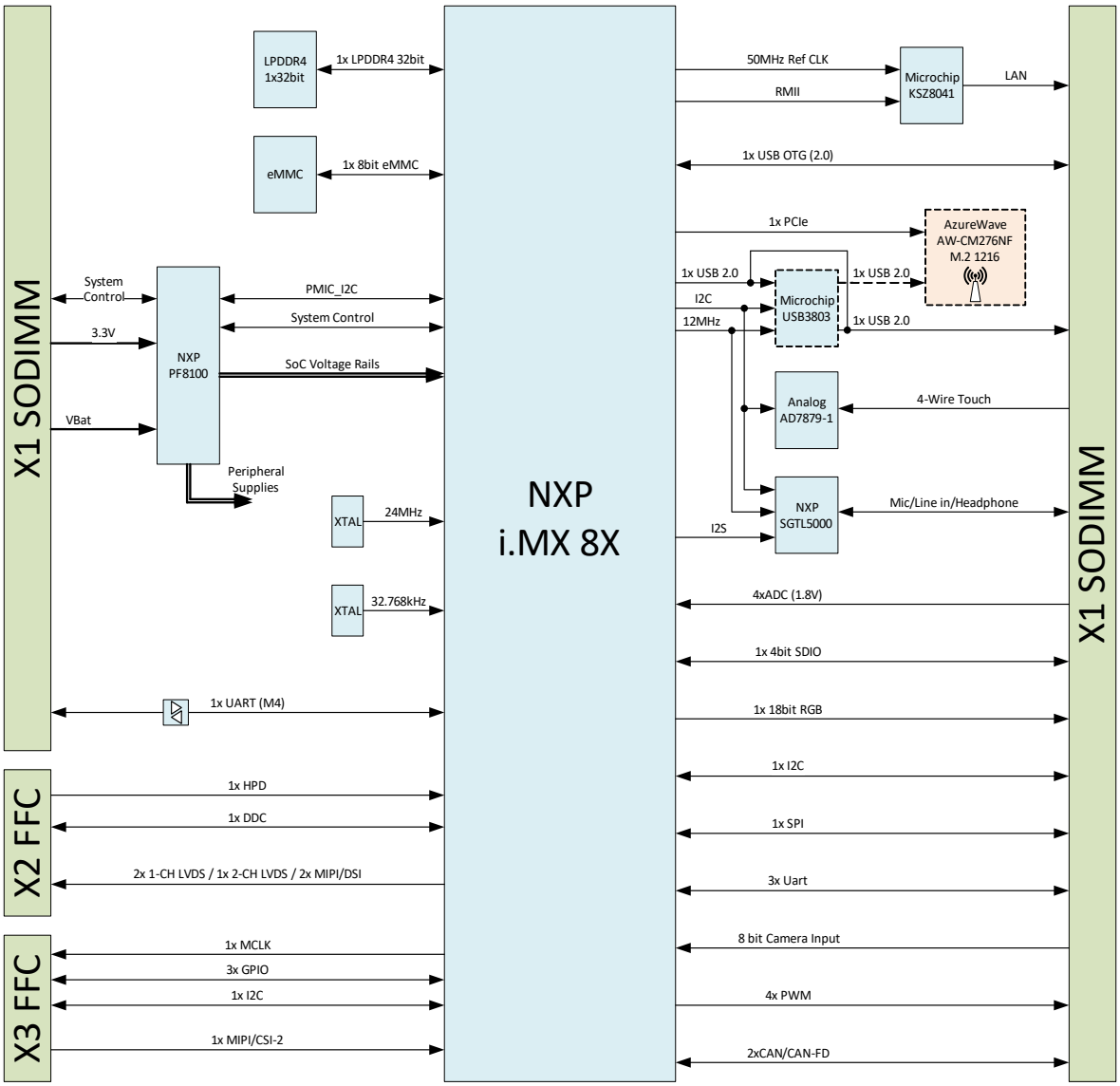

Figure 2 Colibri iMX8X Block Diagram

Additional interfaces such as the second RGMII/RMII Ethernet port, ESAI, SAI, SPDIF, MQS, MLB, QSPI, and additional instances of CAN, I2C, PWM, SPI, and UART are missing in this block diagram. These interfaces are available as alternate functions. Some interfaces cannot be used in combination with others since they are sharing the same pins. More information can be found in section 4.1.

3. Colibri iMX8X Connector

3.1 Physical Locations

The Colibri iMX8X is equipped with a 200-pin SODIMM edge connector (X1) and two FFC connectors. The FFC connectors are located at the bottom of the module. There is a 30-pin (X2) that is dedicated to the MIPI/DSI and LVDS signals. The smaller 24-ball (X3) connector features MIPI/CSI-2 camera signals.

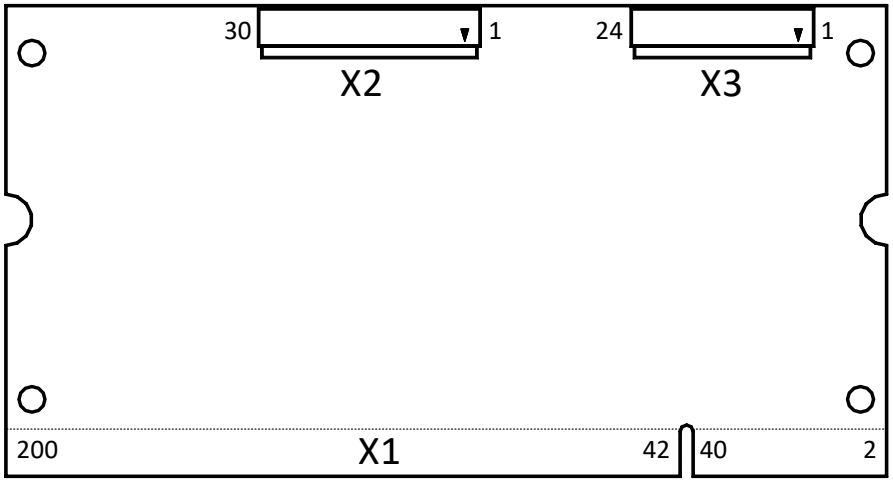

Figure 3: Location of the Colibri iMX8X connectors (bottom view)

3.2 SODIMM 200 Pin Assignment

The table below details the SODIMM 200-way connector pin functionality.

It should be noted that some of the pins are not available on modules with Wi-Fi and Bluetooth. The signals are required for interfacing the wireless module. Please check the availability of pins and functions with the help of the Pinout Designer tool.

Some of the pins are multiplexed. There is more than one i.MX 8X SoC pin connected to one SODIMM module edge connector pin. For example, UART1_RTS_B and CSI_D04 are both connected to SODIMM pin 67. Care should be taken to ensure that multiplexed pins are tri-stated (configured as input) when they are not being used (e.g., if i.MX 8X pin A and B are tied to one SODIMM pin, then if i.MX 8X pin A is driven, pin B needs to be tri-stated). Additional information can be found in section 4.1.

Some of the SoC pins are connected to the SODIMM and one of the FFC connectors. Care should be taken when using them.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Default Colibri function: The default function, which is compatible with all Colibri modules. IMPORTANT: There are a few limitations. You can find more information about pin compatibility in the "**Colibri Compatibility Guide**".
- i.MX 8X Ball: The name of the ball (a.k.a. pin) of the i.MX 8X SoC.
- Non i.MX 8X Ball: Peripheral functions which are not directly provided by the i.MX 8X SoC.
- Note: Additional information. Some pins are noted as "no standard function". These pins can provide only the GPIO functionality and the listed alternate function, but not the Colibri compatible function. Some of the

Colibri compatible functions might be emulated by programmatically manipulating the GPIO.

Table 3-1 X1 Connector

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
1	Audio Analogue Microphone Input		MIC_IN	SGTL5000 Pin 10
3	Audio Analogue Microphone GND		MIC_GND	GND switched, controlled with GPIO3.IO06
5	Audio Analogue Line-In Left		LINEIN_L	SGTL5000 Pin 9
7	Audio Analogue Line-In Right		LINEIN_R	SGTL5000 Pin 8
9	Audio_Analogue GND		VSS_AUDIO	GND
11	Audio_Analogue GND		VSS_AUDIO	GND
13	Audio Analogue Headphone GND		HEADPHONE_GND	Virtual GND, do not connect to normal GND
15	Audio Analogue Headphone Left		HEADPHONE_L	SGTL5000 Pin 4
17	Audio Analogue Headphone Right		HEADPHONE_R	SGTL5000 Pin 1
19	UART_C RXD	UART2_RX		
21	UART_C TXD	UART2_TX		
23	UART_A DTR	MIPI_DSI1_GPIO0_01		no standard function
25	UART_A CTS, Keypad_In<0>	SAI1_RXD		no standard function
27	UART_A RTS	SAI1_RXC		no standard function
29	UART_A DSR	CSI_RESET		no standard function
31	UART_A DCD	USDHC1_CD_B		no standard function
33	UART_A RXD	FLEXCAN2_RX		
35	UART_A TXD	FLEXCAN2_TX		
37	UART_A RI, Keypad_In<4>	CSI_EN		no standard function
39	GND		GND	
41	GND		GND	
43	WAKEUP Source<0>, SDCard CardDetect	QSPI0A_DATA0		no standard function
45	WAKEUP Source<1>	QSPI0A_DATA1		no standard function
47	SDCard CLK	USDHC1_CLK [1)]		
49	SDCard DAT<1>	USDHC1_DATA1 [1)]		
51	SDCard DAT<2>	USDHC1_DATA2 [1)]		
53	SDCard DAT<3>	USDHC1_DATA3 [1)]		
55	PS2 SDA1	FLEXCAN1_TX		no standard function
57	LCD RGB Data<16>	SPI3_CS1/ ENET0_RGMII_TXD2		Multiplexed (Two i.MX 8X Pins)
59	PWM<A>, Camera Input Data<7>	CSI_D05/ SPI0_CS1		Multiplexed (Two i.MX 8X Pins)
61	LCD RGB Data<17>	UART1_CTS_B		
63	PS2 SCL1	FLEXCAN1_RX		no standard function

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	CSI_D07/ ENET0_RGMII_TXD3		Multiplexed (Two i.MX 8X Pins)
67	PWM<D>,Camera Input Data<6>	CSI_D04/ UART1_RTS_B		Multiplexed (Two i.MX 8X Pins)
69	PS2 SCL2	QSPI0A_DATA2		no standard function
71	Camera Input Data<0>, LCD Back-Light GPIO	QSPI0A_DATA3		no standard function
73		QSPI0A_DQS		no standard function
75	Camera Input MCLK	CSI_MCLK		SoC pin is also connected to FFC
77		QSPI0A_SS0_B		SoC pin is also on FFC, no standard function
79	Camera Input Data<4>	CSI_D02/ SAI0_TXC		Multiplexed (Two i.MX 8X Pins)
81	Camera Input VSYNC	CSI_VSYNC/ PCIE_CTRL0_PERST_B [2)]		Multiplexed (two pins), **2nd pin not connected on modules with Wi-Fi**
83	GND		GND	
85	Camera Input Data<8>, Keypad_Out<4>	CSI_D06/ ENET0_RGMII_RXC		Multiplexed (Two i.MX 8X Pins)
87	nReset Out		PMIC Reset Output	
89	nWE	QSPI0A_SS1_B		SoC pin is also on FFC, no standard function
91	nOE		Recovery Circuit	Inverted BOOT_MODE0 signal for recovery
93	RDnWR	QSPI0A_SCLK		SoC pin is also on FFC, no standard function
95	RDY	QSPI0B_SCLK		no standard function
97	Camera Input Data<5>	CSI_D03/ SAI0_RXD		Multiplexed (Two i.MX 8X Pins)
99	nPWE	QSPI0B_DATA0		no standard function
101	Camera Input Data<2>	CSI_D00/ SAI0_TXFS		Multiplexed (Two i.MX 8X Pins)
103	Camera Input Data<3>	CSI_D01/ SAI0_TXD		Multiplexed (Two i.MX 8X Pins)
105	nCS0	QSPI0B_DATA1		no standard function
107	nCS1	QSPI0B_DATA2		no standard function
109	GND		GND	
111	ADDRESS0		GPIO[8]/ UART_SOUT	AW-CM276NF Pin 55, Only on modules with Wi-Fi
113	ADDRESS1		GPIO[9]/ UART_SIN	AW-CM276NF Pin 56, Only on modules with Wi-Fi
115	ADDRESS2		GPIO[10]/ UART_CTSn	AW-CM276NF Pin 54, Only on modules with Wi-Fi
117	ADDRESS3		GPIO[11]/ UART_RTSn	AW-CM276NF Pin 57, Only on modules with Wi-Fi
119	ADDRESS4			no connection
121	ADDRESS5		GPIO[14]/ TCK/ WLAN Wake Host	AW-CM276NF Pin 46, Only on modules with Wi-Fi
123	ADDRESS6		GPIO[13]/ BT IRQ(O)	AW-CM276NF Pin 28, Only on modules with Wi-Fi

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
125	ADDRESS7		GPIO[2]/ WLAN_LED	AW-CM276NF Pin 64, Only on modules with Wi-Fi
127		USB_SS3_TC2		no standard function
129	USB Host Power Enable	USB_SS3_TC0		
131	USB Host Over-Current Detect	USB_SS3_TC3		
133		USB_SS3_TC1		no standard function
135	SPDIF_IN	USB_OTG1_ID/ ENET0_RGMII_RXD3		Multiplexed (Two i.MX 8X Pins)
137	USB Client Cable Detect,SPDIF_OUT	USB_OTG1_VBUS/ ENET0_REFCLK_125M_25M		Multiplexed (Two i.MX 8X Pins)
139	USB Host DP	USB_OTG2_DP	USBDN3_DP	Over USB3803 USB Hub for modules with Wi-Fi
141	USB Host DM	USB_OTG2_DN	USBDN3_DM	Over USB3803 USB Hub for modules with Wi-Fi
143	USB Client DP	USB_OTG1_DP		
145	USB Client DM	USB_OTG1_DN		
147	GND		GND	
149	DATA0			no connection
151	DATA1			no connection
153	DATA2			no connection
155	DATA3			no connection
157	DATA4			no connection
159	DATA5			no connection
161	DATA6			no connection
163	DATA7			no connection
165	DATA8			no connection
167	DATA9			no connection
169	DATA10			no connection
171	DATA11			no connection
173	DATA12			no connection
175	DATA13			no connection
177	DATA14			no connection
179	DATA15			no connection
181	GND		GND	
183	Ethernet Link/Activity Status		LINK_AKT	KSZ8041 LED0
185	Ethernet Speed Status		SPEED100	KSZ8041 LED1
187	Ethernet TXO-		TXO-	KSZ8041 Pin 6
189	Ethernet TXO+		TXO+	KSZ8041 Pin 7
191	Ethernet GND		AGND_LAN	
193	Ethernet RXI-		RXI-	KSZ8041 Pin 4
195	Ethernet RXI+		RXI+	KSZ8041 Pin 5
197	GND		GND	
199	GND		GND	

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
2	Analogue Input <3>	ADC_IN5		**Maximum input voltage 1.8V**
4	Analogue Input <2>	ADC_IN4		**Maximum input voltage 1.8V**
6	Analogue Input <1>	ADC_IN1		**Maximum input voltage 1.8V**
8	Analogue Input <0>	ADC_IN0		**Maximum input voltage 1.8V**
10	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply for ADC
12	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply for ADC
14	Resistive Touch PX		TSPX	AD7819 Ball A3 **(1.8V Level)**
16	Resistive Touch MX		TSMX	AD7819 Ball C3 **(1.8V Level)**
18	Resistive Touch PY		TSPY	AD7819 Ball B3 **(1.8V Level)**
20	Resistive Touch MY		TSMY	AD7819 Ball D3 **(1.8V Level)**
22	VDD Fault Detect		AUX/VBAT/GPIO	AD7819 Ball A1 **(max. 5V input)**
24	Battery Fault Detect			no connection
26	nReset In		Reset input	
28	PWM<B>	UART1_TX		
30	PWM<C>	UART1_RX		
32	UART_B CTS	FLEXCAN0_TX		
34	UART_B RTS	FLEXCAN0_RX		
36	UART_B RXD	UART0_RX		
38	UART_B TXD	UART0_TX		
40	VCC_BATT		VCC_BATT	RTC supply
42	3V3		3V3	
44	LCD RGB DE	MCLK_IN1/ USDHC1_RESET_B		Multiplexed (Two i.MX 8X Pins)
46	LCD RGB Data<7>	ESAI0_TX3_RX2		
48	LCD RGB Data<9>	ESAI0_TX5_RX0		
50	LCD RGB Data<11>	SPDIF0_TX		
52	LCD RGB Data<12>	SPDIF0_EXT_CLK		
54	LCD RGB Data<13>	SPI3_SCK		
56	LCD RGB PCLK	MCLK_OUT0		
58	LCD RGB Data<3>	ESAI0_SCKT		
60	LCD RGB Data<2>	ESAI0_SCKR		
62	LCD RGB Data<8>	ESAI0_TX4_RX1		
64	LCD RGB Data<15>	SPI3_SDI		
66	LCD RGB Data<14>	SPI3_SDO		
68	LCD RGB HSYNC	SPI3_CS0		
70	LCD RGB Data<1>	ESAI0_FST		
72	LCD RGB Data<5>	ESAI0_TX1		
74	LCD RGB Data<10>	SPDIF0_RX		

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
76	LCD RGB Data<0>	ESAI0_FSR/ USDHC1_WP		Multiplexed (Two i.MX 8X Pins)
78	LCD RGB Data<4>	ESAI0_TX0		
80	LCD RGB Data<6>	ESAI0_TX2_RX3		
82	LCD RGB VSYNC	MCLK_IN0		
84	3V3		3V3	
86	SPI CS	SPI2_CS0		
88	SPI CLK	SPI2_SCK		
90	SPI RXD	SPI2_SDI		
92	SPI TXD	SPI2_SDO		
94	Camera Input HSYNC	CSI_HSYNC/ PCIE_CTRL0_WAKE_B [2)]		Multiplexed (two pins), **2nd pin not connected on modules with Wi-Fi**
96	Camera Input PCLK	CSI_PCLK		
98	Camera Input Data<1>	QSPI0B_DATA3		no standard function
100	Keypad_Out<1>	SAI1_RXFS		no standard function
102		QSPI0B_DQS		no standard function
104		QSPI0B_SS0_B		no standard function
106	nCS2	QSPI0B_SS1_B		no standard function
108	3V3		3V3	
110	ADDRESS8			no connection
112	ADDRESS9		GPIO[6]/ PCM_CLK	AW-CM276NF Pin 61 Only on modules with Wi-Fi
114	ADDRESS10		GPIO[7]/ PCM_SYNC	AW-CM276NF Pin 58, Only on modules with Wi-Fi
116	ADDRESS11		GPIO[4]/ PCM_IN	AW-CM276NF Pin 59, Only on modules with Wi-Fi
118	ADDRESS12		GPIO[5]/ PCM_OUT	AW-CM276NF Pin 60, Only on modules with Wi-Fi
120	ADDRESS13		GPIO[15]/ TMS/ Host Wake WLAN	AW-CM276NF Pin 66, Only on modules with Wi-Fi
122	ADDRESS14		GPIO[12]/ UART Host Wake BT	AW-CM276NF Pin 53, Only on modules with Wi-Fi
124	ADDRESS15		GPIO[22]/ PCIE_W_DISABLEn	AW-CM276NF Pin 63, Only on modules with Wi-Fi
126	DQM0		GPIO[3]/ BT_LED	AW-CM276NF Pin 65, Only on modules with Wi-Fi
128	DQM1		GPIO[16]/ LTE_COEX_IN	AW-CM276NF Pin 12, Only on modules with Wi-Fi
130	DQM2		GPIO[17]/ LTE_COEX_OUT	AW-CM276NF Pin 11, Only on modules with Wi-Fi
132	DQM3			no connection
134	ADDRESS25			no connection
136	ADDRESS24			no connection
138	ADDRESS23	MIPI_DSI1_GPIO0_00		SoC pin is also on FFC, no standard function
140	ADDRESS22	MIPI_DSI0_I2C0_SCL		SoC pin is also on FFC, no standard function

X1 Pin	Default Colibri Function	i.MX 8X Ball	Non i.MX 8X Ball	Note
142	ADDRESS21	MIPI_DSI0_I2C0_SDA		SoC pin is also on FFC, no standard function
144	ADDRESS20	SCU_GPIO0_00		Bidirectional level shifter, no standard function
146	ADDRESS19	SCU_GPIO0_01		Bidirectional level shifter, no standard function
148	3V3		3V3	
150	DATA16			no connection
152	DATA17			no connection
154	DATA18			no connection
156	DATA19			no connection
158	DATA20			no connection
160	DATA21			no connection
162	DATA22			no connection
164	DATA23			no connection
166	DATA24			no connection
168	DATA25			no connection
170	DATA26		CONFIG_HOST[0]	AW-CM276NF Pin 8, Only on modules with Wi-Fi, **Maximum voltage 1.8V,** leave unconnected
172	DATA27		CONFIG_HOST[1]	AW-CM276NF Pin 8, Only on modules with Wi-Fi, **Maximum voltage 1.8V,** leave unconnected
174	DATA28		CONFIG_HOST[2]	AW-CM276NF Pin 8, Only on modules with Wi-Fi, **Maximum voltage 1.8V,** leave unconnected
176	DATA29			no connection
178	DATA30	PCIE_CTRL0_CLKREQ_B [2]		**Pin not connected on modules with Wi-Fi**
180	DATA31	ENET0_MDIO		Shared with on-module Ethernet PHY, no standard function
182	3V3		3V3	
184	ADDRESS18	ENET0_MDC		Shared with on-module Ethernet PHY, no standard function
186	ADDRESS17	MIPI_DSI1_I2C0_SCL		SoC pin is also on FFC, no standard function
188	ADDRESS16	MIPI_DSI1_I2C0_SDA		SoC pin is also on FFC, no standard function
190	SDCard CMD	USDHC1_CMD [1]		
192	SDCard DAT<0>	USDHC1_DATA0 [1]		
194	I2C SDA	MIPI_DSI0_GPIO0_01		
196	I2C SCL	MIPI_DSI0_GPIO0_00		
198	3V3		3V3	
200	3V3		3V3	

[1] It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V to support SD UHS-I speeds. Please note that the voltage can only be changed for all the pins simultaneously and not individually. Therefore, use these pins with care. More information can be found in section 5.14.
[2] This SoC pin is not available on modules with Wi-Fi and Bluetooth.

3.3 MIPI/DSI and LVDS FFC Pin Assignment

The table below details the 30-pin MIPI/DSI and LVDS FFC connector (X2) pin functionality. The FCC connector has a pitch of 0.5mm. Suitable connectors are the 687130182122 from Würth or FH34SRJ-30S-0.5SH(50) from Hirose. Some of the SoC pins are connected to the FFC as well as to the SODIMM connector. Care should be taken when using them.

- X2 Pin: Pin number on the FFC connector (X2).
- i.MX 8X Ball: The name of the ball (a.k.a. pin) of the i.MX 8X SoC.
- Non i.MX 8X Ball: Peripheral functions which are not directly provided by the i.MX 8X SoC.
- Note: Additional information.

Table 3-2 X2 Connector

X2 Pin	i.MX 8X Ball	Non i.MX 8X Ball	Note
1	MIPI_DSI0_CLK_N		
2	MIPI_DSI0_CLK_P		
3		GND	
4	MIPI_DSI0_DATA0_N		
5	MIPI_DSI0_DATA0_P		
6		GND	
7	MIPI_DSI0_DATA1_N		
8	MIPI_DSI0_DATA1_P		
9		GND	
10	MIPI_DSI0_DATA2_N		
11	MIPI_DSI0_DATA2_P		
12		GND	
13	MIPI_DSI0_DATA3_N		
14	MIPI_DSI0_DATA3_P		
15	MIPI_DSI0_I2C0_SCL		SoC pin is also on SODIMM, Intended to be used as DDC
16	MIPI_DSI0_I2C0_SDA		SoC pin is also on SODIMM, Intended to be used as DDC
17	MIPI_DSI1_CLK_N		
18	MIPI_DSI1_CLK_P		
19		3.3V Output	Switched 3.3V output for the display adapter
20	MIPI_DSI1_DATA0_N		
21	MIPI_DSI1_DATA0_P		
22		3.3V Output	Switched 3.3V output for the display adapter
23	MIPI_DSI1_DATA1_N		
24	MIPI_DSI1_DATA1_P		

X2 Pin	i.MX 8X Ball	Non i.MX 8X Ball	Note
25	MIPI_DSI1_GPIO0_00		SoC pin is also on SODIMM, Intended to be used as HPD
26	MIPI_DSI1_DATA2_N		
27	MIPI_DSI1_DATA2_P		
28		1.8V Output	Switched 1.8V output for the display adapter
29	MIPI_DSI1_DATA3_N		
30	MIPI_DSI1_DATA3_P		

3.4 MIPI/CSI-2 FFC Pin Assignment

The table below details the 24-pin MIPI/CSI-2 connector's (X2) pin functionality. The FCC connector has a pitch of 0.5mm. Suitable connectors are the 687124182122 from Würth or FH34SRJ-24S-0.5SH(50) from Hirose. Some of the SoC pins are connected to the FFC as well as to the SODIMM connector. Care should be taken when using them. The pinout of this connector compatible with the MIPI/CSI-2 connector found on the Apalis evaluation board and Ixora carrier board for the Apalis module.

- X3 Pin: Pin number on the FFC connector (X3).
- i.MX 8X Ball: The name of the ball (a.k.a. pin) of the i.MX 8X SoC.
- Non i.MX 8X Ball: Peripheral functions that are not directly provided by the i.MX 8X SoC.
- Note: Additional information.

Table 3-3 X3 Connector

X3 Pin	i.MX 8X Ball	Non i.MX 8X Ball	Note
1		GND	
2	MIPI_CSI0_DATA0_N		
3	MIPI_CSI0_DATA0_P		
4		GND	
5	MIPI_CSI0_DATA1_N		
6	MIPI_CSI0_DATA1_P		
7		GND	
8	MIPI_CSI0_CLK_N		
9	MIPI_CSI0_CLK_P		
10		GND	
11	QSPI0A_SS1_B		SoC pin is also on SODIMM, Intended to be used as a camera reset
12	CSI_MCLK		SoC pin is also on SODIMM, Intended to be used as a master clock
13	MIPI_DSI1_I2C0_SCL		SoC pin is also on SODIMM, Intended to be used as I^2C
14	MIPI_DSI1_I2C0_SDA		SoC pin is also on SODIMM, Intended to be used as I^2C
15		3.3V Output	Switched 3.3V output for camera
16	MIPI_CSI0_DATA2_N		
17	MIPI_CSI0_DATA2_P		
18		GND	

X3 Pin	i.MX 8X Ball	Non i.MX 8X Ball	Note
19	MIPI_CSI0_DATA3_N		
20	MIPI_CSI0_DATA3_P		
21		GND	
22	QSPI0A_SS0_B		SoC pin is also on SODIMM, Intended to be used as camera GPIO
23	QSPI0A_SCLK		SoC pin is also on SODIMM, Intended to be used as camera GPIO
24			no connection

4. I/O Pins

4.1 Function Multiplexing

The NXP i.MX 8X SoC (low-speed) I/O pins can be configured for any of the (and up to) five alternate functions. One of the available options for most pins is the GPIO function (General Purpose I/O, sometimes referred to as Digital I/O). For example, the i.MX 8X signal pin on the SODIMM pin 33 has the primary function ADMA.UART3.RX (Colibri standard function UART_A_RXD), but can also provide the following alternate functions: ADMA.FLEXCAN2.RX (CAN), ADMA.SAI3.RXD (Digital Audio), ADMA.SAI1.RXFS (Digital Audio), LSIO.GPIO1.IO19 (GPIO),

The default usage for this pin is the Colibri primary function ADMA.UART3.RX. It is strongly recommended that whenever it is possible, use the primary interfaces before using any alternate interfaces. This ensures the best compatibility between the Toradex standard software, operating systems/BSPs, and other modules in the Colibri family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table in section 4.4, you will find a list of all pins, which have alternate functions. There you can see which alternate functions are available for each individual pin.

Some of the i.MX 8X balls are paired and share the same SODIMM pin. When using one of these pins, make sure that the unused pin of each multiplexed pair is tri-stated or configured as an input to avoid undesired behavior and hardware damage. The following table lists all SODIMM pins that have more than one i.MX 8X pin connected:

Table 4-1 Multiplexed pins

X1 Pin #	i.MX 8X Ball 1	i.MX 8X Ball 2	Remarks
44	MCLK_IN1	USDHC1_RESET_B	
57	SPI3_CS12	ENET0_RGMII_TXD2	
59	CSI_D05	SPI0_CS1	
65	CSI_D07	ENET0_RGMII_TXD3	
67	CSI_D04	UART1_RTS_B	
76	ESAI0_FSR	USDHC1_WP	
79	CSI_D02	SAI0_TXC	
81	CSI_VSYNC	PCIE_CTRL0_PERST_B	i.MX 8X Ball 2 only available on modules without Wi-Fi
85	CSI_D06	ENET0_RGMII_RXC	
94	CSI_HSYNC	PCIE_CTRL0_WAKE_B	i.MX 8X Ball 2 only available on modules without Wi-Fi
97	CSI_D03	SAI0_RXD	
101	CSI_D00	SAI0_TXFS	
103	CSI_D01	SAI0_TXD	
135	USB_OTG1_ID	ENET0_RGMII_RXD3	There is a voltage divider on USB_OTG1_ID to meet the maximum input voltage of 1.8V of this ball.
137	USB_OTG1_VBUS	ENET0_REFCLK_125M_25M	

Some of the i.MX 8X balls are connected to the SODIMM pin as well as to one of the FFC connectors. Make sure that you use the following SoC signals only on one of their connector locations:

Table 4-2 Double used SoC balls

i.MX 8X Ball	SODIMM X1 pin	DSI/LVDS FFC X2 pin	CSI FFC X3 pin	Remarks
CSI_MCLK	75		12	Reference clock for parallel and MIPI/DSI camera
QSPI0A_SS0_B	77		22	
QSPI0A_SS1_B	89		11	Camera reset
QSPI0A_SCLK	93		23	
MIPI_DSI1_GPIO0_00	138	25		
MIPI_DSI0_I2C0_SCL	140	15		I^2C for DDC
MIPI_DSI0_I2C0_SDA	142	16		I^2C for DDC
MIPI_DSI1_I2C0_SCL	186		13	I^2C for MIPI/CSI-2 Camera
MIPI_DSI1_I2C0_SDA	188		14	I^2C for MIPI/CSI-2 Camera

4.2 Pin Control

The alternate function of each pin can be changed independently. On previous i.MX-based SoCs (e.g., i.MX 6 or i.MX 7), the multiplexing and pad control has been changed by directly writing to the IOMUX registers. On the i.MX 8X based SoC, this is no longer possible. The IOMUX registers can only be controlled by the System Controller Unit (SCU). This allows the SCU to do proper resource management of the peripherals. The SCU makes sure only the cores with permission to the according domain are allowed to make changes in the pin configuration.

To change the multiplexing and configuration of the SoC pins, a System Controller API is provided. Please see the System Controller API Reference Guide from NXP for more information. With the help of this API, the following settings can be set individually for every pin:

- Selecting the alternate function for this pin
- Configuring as input, open drain, open-drain input, or regular push-pull output
- Low power behavior such as latching
- Wakeup masking
- Wakeup control which includes falling and rising edge as well as high and low level
- Pull up and down resistor enabling
- Drive strength control
- Locking mechanism for muxing and pad control

4.3 Pin Reset Status

The interface pins of the i.MX 8X are configured by the system controller unit (SCU). After a reset, the SCU firmware (SCFW) configures the pins to a default state. Most of them are configured as input with a pull-down enabled. A few are tri-stated or pulled-up. Please check the table in chapter 4.4.1, 4.4.2, and 4.4.3 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

Please be aware that during the power-up sequence, the pins enter into the reset states indicated when the related IO bank voltages are enabled on the module and the SCFW has configured the pins (while the nRESET_OUT signal is active). The states of the pins are undefined before those conditions are met. After the reset has been released (the nRESET_OUT signal is inactive), the states of the pins may be reconfigured by software components being involved in the boot process (e.g., U-Boot, Kernel).

Reset Status Description

PD:	Pull-Down (Input)
PU:	Pull-Up (Input)
Z:	Tristate (Input)

4.4 Functions List

Below is a list of all the i.MX 8X pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT4 function. The alternate functions used to provide the primary interfaces to ensure the best compatibility with other Colibri modules are highlighted.

Please note: not all pins are available on the module with Wi-Fi. Check the available pins in Table 3-1 or use the Toradex Pinout Designer.

Function Short Forms

ACM:	Audio Clock Mux
ADC:	Analog-Digital Convert input
ADMA:	Audio DMA Subsystem
CI_PI:	Parallel Capture Interface
CONN:	Connectivity Subsystem
CSI:	Camera Serial Interface
DMA:	Direct Memory Access
DSI:	Display Serial Interface
ENET:	Ethernet MAC interface
ESAI:	Enhanced Serial Audio Interface
FLEXCAN:	Flexible Controller Area Network (Flexible CAN)
FTM:	FlexTimer Module
GPIO:	General Purpose Input Output
GPT:	General Purpose Timer
I2C:	Inter Integrated Circuit
KPP:	Keypad Port
LSIO:	Low-Speed I/O
LCD:	Liquid Crystal Display Interface
LVDS:	Low Voltage Differential Signalling (also known as FPD-Link or FlatLink)
M40:	Cortex M4 Processor complex (dedicated interface for the M4 processor)
MIPI_CSI:	MIPI CSI Subsystem
MIPI_DSI:	MIPI DSI/LVDS Subsystem
MLB:	Media Local Bus (MediaLB)
MQS:	Medium Quality Sound
NAND:	Interface for NAND Flash
PCIE:	PCI Express
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
SAI:	Serial Interface for Audio (I2S and AC97)
SCU:	System Controller Unit
SNVS:	Secure Non-Volatile Storage
SPI:	Serial Peripheral Interface Bus
TAMPER:	Tamper detection
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
WDOG:	Watchdog

4.4.1 SODIMM 200

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
19	UART2_RX	AD34	ADMA.UART2.RX	ADMA.FTM.CH0	ADMA.FLEXCAN1.RX		LSIO.GPIO1.IO24	GPIO	ALT0	PD	VDD_CAN_UART_3P3
21	UART2_TX	AC35	ADMA.UART2.TX	ADMA.FTM.CH1	ADMA.FLEXCAN1.TX		LSIO.GPIO1.IO23	GPIO	ALT4	PD	VDD_CAN_UART_3P3
23	MIPI_DSI1_GPIO0_01	AF34	MIPI_DSI1.GPIO0.IO01	ADMA.I2C2.SDA			LSIO.GPIO2.IO00	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
25	SAI1_RXD	M32	ADMA.SAI1.RXD	ADMA.SAI0.RXFS	ADMA.SPI1.CS1	ADMA.LCD_D21	LSIO.GPIO0.IO29	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
27	SAI1_RXC	L35	ADMA.SAI1.RXC	ADMA.SAI1.TXC		ADMA.LCD_D22	LSIO.GPIO0.IO30	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
29	CSI_RESET	AR27	CI_PI.CSI_RESET	CI_PI.CSI_I2C.SDA	ADMA.I2C3.SDA	ADMA.SPI1.CS0	LSIO.GPIO3.IO03	GPIO	ALT0	PD	VDD_CSI_3P3
31	USDHC1_CD_B	E23	CONN.USDHC1.CD_B	CONN.NAND.DQS_P	ADMA.SPI2.CS0	CONN.NAND.DQS	LSIO.GPIO4.IO22	FASTD	ALT0	PU	VDD_USDHC1_VSELECT_3P3
33	FLEXCAN2_RX	AB34	ADMA.FLEXCAN2.RX	ADMA.SAI3.RXD	ADMA.UART3.RX	ADMA.SAI1.RXFS	LSIO.GPIO1.IO19	GPIO	ALT0	PD	VDD_CAN_UART_3P3
35	FLEXCAN2_TX	AA31	ADMA.FLEXCAN2.TX	ADMA.SAI3.RXFS	ADMA.UART3.TX	ADMA.SAI1.RXC	LSIO.GPIO1.IO20	GPIO	ALT4	PD	VDD_CAN_UART_3P3
37	CSI_EN	AP28	CI_PI.CSI_EN	CI_PI.CSI_I2C.SCL	ADMA.I2C3.SCL	ADMA.SPI1.SDI	LSIO.GPIO3.IO02	GPIO	ALT0	PD	VDD_CSI_3P3
43	QSPI0A_DATA0	AK14	LSIO.QSPI0A.DATA0				LSIO.GPIO3.IO09	FASTD	ALT0	PD	VDD_QSPI0A_3P3
45	QSPI0A_DATA1	AR13	LSIO.QSPI0A.DATA1				LSIO.GPIO3.IO10	FASTD	ALT0	PD	VDD_QSPI0A_3P3
47	USDHC1_CLK	G23	CONN.USDHC1.CLK		ADMA.UART3.RX		LSIO.GPIO4.IO23	FASTD	ALT4	PD	VDD_USDHC1_1P8_3P3
49	USDHC1_DATA1	B26	CONN.USDHC1.DATA1	CONN.NAND.RE_B	ADMA.UART3.TX		LSIO.GPIO4.IO26	FASTD	ALT0	PU	VDD_USDHC1_1P8_3P3
51	USDHC1_DATA2	D26	CONN.USDHC1.DATA2	CONN.NAND.WE_B	ADMA.UART3.CTS_B		LSIO.GPIO4.IO27	FASTD	ALT0	PU	VDD_USDHC1_1P8_3P3
53	USDHC1_DATA3	E25	CONN.USDHC1.DATA3	CONN.NAND.ALE	ADMA.UART3.RTS_B		LSIO.GPIO4.IO28	FASTD	ALT0	PU	VDD_USDHC1_1P8_3P3
55	FLEXCAN1_TX	AA35	ADMA.FLEXCAN1.TX	ADMA.SAI3.RXC	ADMA.DMA0.REQ_IN0	ADMA.SAI1.RXD	LSIO.GPIO1.IO18	GPIO	ALT4	PD	VDD_CAN_UART_3P3
57	SPI3_CS1	K30	ADMA.SPI3.CS1	ADMA.I2C3.SCL	ADMA.LCD_RESET	ADMA.SPI2.CS0	ADMA.LCD_D16	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
	ENET0_RGMII_TXD2	E27	CONN.ENET0.RGMII_TXD2	CONN.MLB.CLK	CONN.NAND.CE0_B	CONN.USDHC1.CD_B	LSIO.GPIO5.IO01	FASTD	ALT4	PD	VDD_ENET0_VSELECT_3P3
59	CSI_D05	AM30	CI_PI.CSI_D07		ADMA.SAI2.RXFS	SNVS.TAMPER_IN0		GPIO	ALT0	PD	VDD_CSI_3P3
	SPI0_CS1	R35	ADMA.SPI0.CS1	ADMA.SAI0.RXC	ADMA.SAI1.TXD	ADMA.LCD_PWM0	LSIO.GPIO1.IO07	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
61	UART1_CTS_B	K32	ADMA.UART1.CTS_B	LSIO.PWM3.OUT	ADMA.LCD_D17	LSIO.GPT1.COMPARE	LSIO.GPIO0.IO24	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
63	FLEXCAN1_RX	AA33	ADMA.FLEXCAN1.RX	ADMA.SAI2.RXFS	ADMA.FTM.CH2	ADMA.SAI1.TXD	LSIO.GPIO1.IO17	GPIO	ALT0	PD	VDD_CAN_UART_3P3
65	CSI_D07	AM28	CI_PI.CSI_D09		ADMA.SAI3.RXD	SNVS.TAMPER_IN2		GPIO	ALT0	PD	VDD_CSI_3P3
	ENET0_RGMII_TXD3	F26	CONN.ENET0.RGMII_TXD3	CONN.MLB.SIG	CONN.NAND.RE_B		LSIO.GPIO5.IO02	FASTD	ALT4	PD	VDD_ENET0_VSELECT_3P3
67	CSI_D04	AN29	CI_PI.CSI_D06		ADMA.SAI2.RXD	SNVS.TAMPER_OUT4		GPIO	ALT0	PD	VDD_CSI_3P3
	UART1_RTS_B	N29	ADMA.UART1.RTS_B	LSIO.PWM2.OUT	ADMA.LCD_D16	LSIO.GPT1.CAPTURE	LSIO.GPT0.CLK	GPIO	ALT4	PD	VDD_SPI_MCLK_UART_3P3
69	QSPI0A_DATA2	AJ13	LSIO.QSPI0A.DATA2				LSIO.GPIO3.IO11	FASTD	ALT0	PD	VDD_QSPI0A_3P3
71	QSPI0A_DATA3	AH12	LSIO.QSPI0A.DATA3				LSIO.GPIO3.IO12	FASTD	ALT0	PD	VDD_QSPI0A_3P3
73	QSPI0A_DQS	AL11	LSIO.QSPI0A.DQS				LSIO.GPIO3.IO13	FASTD	ALT0	PD	VDD_QSPI0A_3P3
75	CSI_MCLK [2]	AM26	CI_PI.CSI_MCLK	MIPI_CSI0.I2C0.SDA		ADMA.SPI1.SDO	LSIO.GPIO3.IO01	GPIO	ALT4	PD	VDD_CSI_3P3
77	QSPI0A_SS0_B [2]	AM12	LSIO.QSPI0A.SS0_B				LSIO.GPIO3.IO14	FASTD	ALT4	PU	VDD_QSPI0A_3P3
79	CSI_D02	AP30	CI_PI.CSI_D04		ADMA.SAI0.RXFS	SNVS.TAMPER_OUT2		GPIO	ALT0	PD	VDD_CSI_3P3
	SAI0_TXC	J35	ADMA.SAI0.TXC	ADMA.SAI1.TXD	ADMA.SPI1.SDI	ADMA.LCD_D19	LSIO.GPIO0.IO26	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
81	CSI_VSYNC	AL27	CI_PI.CSI_VSYNC	CI_PI.CSI_D01		SNVS.TAMPER_IN4		GPIO	ALT0	PD	VDD_CSI_3P3
	PCIE_CTRL0_PERST_B [1]	H10	HSIO.PCIE0.PERST_B				LSIO.GPIO4.IO00	GPIO	ALT0	PD	VDD_PCIE_DIG_3P3
85	CSI_D06	AJ25	CI_PI.CSI_D08		ADMA.SAI3.RXC	SNVS.TAMPER_IN1		GPIO	ALT0	PD	VDD_CSI_3P3
	ENET0_RGMII_RXC	D28	CONN.ENET0.RGMII_RXC	CONN.MLB.DATA	CONN.NAND.WE_B	CONN.USDHC1.CLK	LSIO.GPIO5.IO03	FASTD	ALT0	PD	VDD_ENET0_3P3
89	QSPI0A_SS1_B [2]	AK12	LSIO.QSPI0A.SS1_B				LSIO.GPIO3.IO15	FASTD	ALT4	PU	VDD_QSPI0A_3P3
93	QSPI0A_SCLK [2]	AP12	LSIO.QSPI0A.SCLK				LSIO.GPIO3.IO16	FASTD	ALT4	PD	VDD_QSPI0A_3P3
95	QSPI0B_SCLK	AR11	LSIO.QSPI0B.SCLK	LSIO.QSPI1A.SCLK	LSIO.KPP0.COL0		LSIO.GPIO3.IO17	FASTD	ALT4	PD	VDD_QSPI0B_3P3
97	CSI_D03	AJ27	CI_PI.CSI_D05		ADMA.SAI2.RXC	SNVS.TAMPER_OUT3		GPIO	ALT0	PD	VDD_CSI_3P3
	SAI0_RXD	M34	ADMA.SAI0.RXD	ADMA.SAI1.RXFS	ADMA.SPI1.CS0	ADMA.LCD_D20	LSIO.GPIO0.IO27	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
99	QSPI0B_DATA0	AM10	LSIO.QSPI0B.DATA0	LSIO.QSPI1A.DATA0	LSIO.KPP0.COL1		LSIO.GPIO3.IO18	FASTD	ALT0	PD	VDD_QSPI0B_3P3
101	CSI_D00	AK28	CI_PI.CSI_D02		ADMA.SAI0.RXC	SNVS.TAMPER_OUT0		GPIO	ALT0	PD	VDD_CSI_3P3
	SAI0_TXFS	L33	ADMA.SAI0.TXFS	ADMA.SPI2.CS1	ADMA.SPI1.SCK		LSIO.GPIO0.IO28	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
103	CSI_D01	AL29	CI_PI.CSI_D03		ADMA.SAI0.RXD	SNVS.TAMPER_OUT1		GPIO	ALT0	PD	VDD_CSI_3P3
	SAI0_TXD	K34	ADMA.SAI0.TXD	ADMA.SAI1.RXC	ADMA.SPI1.SDO	ADMA.LCD_D18	LSIO.GPIO0.IO25	GPIO	ALT0	PD	VDD_SPI_SAI_3P3

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
105	QSPI0B_DATA1	AL9	LSIO.QSPI0B.DATA1	LSIO.QSPI1A.DATA1	LSIO.KPP0.COL2		LSIO.GPIO3.IO19	FASTD	ALT0	PD	VDD_QSPI0B_3P3
107	QSPI0B_DATA2	AJ11	LSIO.QSPI0B.DATA2	LSIO.QSPI1A.DATA2	LSIO.KPP0.COL3		LSIO.GPIO3.IO20	FASTD	ALT0	PD	VDD_QSPI0B_3P3
127	USB_SS3_TC2	G15	ADMA.I2C1.SDA	CONN.USB_OTG1.OC	CONN.USB_OTG2.OC		LSIO.GPIO4.IO05	GPIO	ALT0	PD	VDD_USB_3P3
129	USB_SS3_TC0	F14	ADMA.I2C1.SCL	CONN.USB_OTG1.PWR	CONN.USB_OTG2.PWR		LSIO.GPIO4.IO03	GPIO	ALT0	PD	VDD_USB_3P3
131	USB_SS3_TC3	C15	ADMA.I2C1.SDA	CONN.USB_OTG2.OC			LSIO.GPIO4.IO06	GPIO	ALT0	PD	VDD_USB_3P3
133	USB_SS3_TC1	H14	ADMA.I2C1.SCL	CONN.USB_OTG2.PWR			LSIO.GPIO4.IO04	GPIO	ALT0	PD	VDD_USB_3P3
135	ENET0_RGMII_RXD3	H26	CONN.ENET0.RGMII_RXD3		CONN.NAND.ALE	CONN.USDHC1.DATA3	LSIO.GPIO5.IO08	FASTD	ALT0	PD	VDD_ENET0_3P3
	USB_OTG1_ID	G17	CONN.USB_OTG1.ID					OTG			VDD_USB_3P3
137	ENET0_REFCLK_125M_25M	F28	CONN.ENET0.REFCLK_125M_25M	CONN.ENET0.PPS	CONN.ENET1.PPS		LSIO.GPIO5.IO09	GPIO	ALT4	PD	VDD_ENET_MDIO_3P3
	USB_OTG1_VBUS	H18	CONN.USB_OTG1.VBUS					OTG			
139	USB_OTG2_DP	E17	CONN.USB_OTG2.DP					OTG			VDD_USB_3P3
141	USB_OTG2_DN	D16	CONN.USB_OTG2.DM					OTG			VDD_USB_3P3
143	USB_OTG1_DP	D18	CONN.USB_OTG1.DP					OTG			VDD_USB_3P3
145	USB_OTG1_DN	E19	CONN.USB_OTG1.DN					OTG			VDD_USB_3P3
2	ADC_IN5	V34	ADMA.ADC.IN5	M40.TPM0.CH1	M40.GPIO0.IO05		LSIO.GPIO1.IO13	GPIO	ALT0	PD	VDD_ADC_DIG_1P8
4	ADC_IN4	W29	ADMA.ADC.IN4	M40.TPM0.CH0	M40.GPIO0.IO04		LSIO.GPIO1.IO14	GPIO	ALT0	PD	VDD_ADC_DIG_1P8
6	ADC_IN1	U33	ADMA.ADC.IN1	M40.I2C0.SDA	M40.GPIO0.IO01		LSIO.GPIO1.IO09	GPIO	ALT0	PD	VDD_ADC_DIG_1P8
8	ADC_IN0	U35	ADMA.ADC.IN0	M40.I2C0.SCL	M40.GPIO0.IO00		LSIO.GPIO1.IO10	GPIO	ALT0	PD	VDD_ADC_DIG_1P8
28	UART1_TX	H34	ADMA.UART1.TX	LSIO.PWM0.OUT	LSIO.GPT0.CAPTURE		LSIO.GPIO0.IO21	GPIO	ALT4	PD	VDD_SPI_MCLK_UART_3P3
30	UART1_RX	L31	ADMA.UART1.RX	LSIO.PWM1.OUT	LSIO.GPT0.COMPARE	LSIO.GPT1.CLK	LSIO.GPIO0.IO22	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
32	FLEXCAN0_TX	Y32	ADMA.FLEXCAN0.TX	ADMA.SAI2.RXD	ADMA.UART0.CTS_B	ADMA.SAI1.TXFS	LSIO.GPIO1.IO16	GPIO	ALT4	PD	VDD_CAN_UART_3P3
34	FLEXCAN0_RX	Y34	ADMA.FLEXCAN0.RX	ADMA.SAI2.RXC	ADMA.UART0.RTS_B	ADMA.SAI1.TXC	LSIO.GPIO1.IO15	GPIO	ALT0	PD	VDD_CAN_UART_3P3
36	UART0_RX	AB32	ADMA.UART0.RX	ADMA.MQS.R	ADMA.FLEXCAN0.RX	SCU.UART0.RX	LSIO.GPIO1.IO21	GPIO	ALT0	PD	VDD_CAN_UART_3P3
38	UART0_TX	AA29	ADMA.UART0.TX	ADMA.MQS.L	ADMA.FLEXCAN0.TX	SCU.UART0.TX	LSIO.GPIO1.IO22	GPIO	ALT4	PD	VDD_CAN_UART_3P3
44	MCLK_IN1	M28	ADMA.ACM.MCLK_IN1	ADMA.I2C3.SDA	ADMA.LCD_EN	ADMA.SPI2.SCK	ADMA.LCD_D17	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
	USDHC1_RESET_B	B24	CONN.USDHC1.RESET_B	CONN.NAND.RE_N	ADMA.SPI2.SCK		LSIO.GPIO4.IO19	FASTD	ALT4	PU	VDD_USDHC1_VSELECT_3P3
46	ESAI0_TX3_RX2	C33	ADMA.ESAI0.TX3_RX2		ADMA.LCD_D07	CONN.ENET1.RGMII_RXD1	LSIO.GPIO0.IO07	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
48	ESAI0_TX5_RX0	J29	ADMA.ESAI0.TX5_RX0		ADMA.LCD_D09	CONN.ENET1.RGMII_TXD1	LSIO.GPIO0.IO09	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
50	SPDIF0_TX	D34	ADMA.SPDIF0.TX	ADMA.MQS.L	ADMA.LCD_D11	CONN.ENET1.RGMII_RX_CTL	LSIO.GPIO0.IO11	GPIO	ALT4	PD	VDD_ESAI_SPDIF_3P3
52	SPDIF0_EXT_CLK	E35	ADMA.SPDIF0.EXT_CLK		ADMA.LCD_D12	CONN.ENET1.REFCLK_125M_25M	LSIO.GPIO0.IO12	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
54	SPI3_SCK	H32	ADMA.SPI3.SCK		ADMA.LCD_D13		LSIO.GPIO0.IO13	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
56	MCLK_OUT0	L29	ADMA.ACM.MCLK_OUT0	ADMA.ESAI0.TX_HF_CLK	ADMA.LCD_CLK	ADMA.SPI2.SDO	LSIO.GPIO0.IO20	GPIO	ALT4	PD	VDD_SPI_MCLK_UART_3P3
58	ESAI0_SCKT	E31	ADMA.ESAI0.SCKT	CONN.MLB.SIG	ADMA.LCD_D03	CONN.ENET1.RGMII_TXD3	LSIO.GPIO0.IO03	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
60	ESAI0_SCKR	H28	ADMA.ESAI0.SCKR		ADMA.LCD_D02	CONN.ENET1.RGMII_TX_CTL	LSIO.GPIO0.IO02	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
62	ESAI0_TX4_RX1	F32	ADMA.ESAI0.TX4_RX1		ADMA.LCD_D08	CONN.ENET1.RGMII_TXD0	LSIO.GPIO0.IO08	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
64	SPI3_SDI	G33	ADMA.SPI3.SDI		ADMA.LCD_D15		LSIO.GPIO0.IO15	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
66	SPI3_SDO	F34	ADMA.SPI3.SDO		ADMA.LCD_D14		LSIO.GPIO0.IO14	GPIO	ALT4	PD	VDD_SPI_MCLK_UART_3P3
68	SPI3_CS0	J31	ADMA.SPI3.CS0	ADMA.ACM.MCLK_OUT1	ADMA.LCD_HSYNC		LSIO.GPIO0.IO16	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
70	ESAI0_FST	G29	ADMA.ESAI0.FST	CONN.MLB.CLK	ADMA.LCD_D01	CONN.ENET1.RGMII_TXD2	LSIO.GPIO0.IO01	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
72	ESAI0_TX1	B34	ADMA.ESAI0.TX1		ADMA.LCD_D05	CONN.ENET1.RGMII_RXD3	LSIO.GPIO0.IO05	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
74	SPDIF0_RX	G31	ADMA.SPDIF0.RX	ADMA.MQS.R	ADMA.LCD_D10	CONN.ENET1.RGMII_RXD0	LSIO.GPIO0.IO10	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
76	ESAI0_FSR	F30	ADMA.ESAI0.FSR	CONN.ENET1.RCLK50M_OUT	ADMA.LCD_D00	CONN.ENET1.RGMII_TXC	CONN.ENET1.RCLK50M_IN	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
	USDHC1_WP	D24	CONN.USDHC1.WP	CONN.NAND.DQS_N	ADMA.SPI2.SDI		LSIO.GPIO4.IO21	FASTD	ALT0	PD	VDD_USDHC1_VSELECT_3P3
78	ESAI0_TX0	D32	ADMA.ESAI0.TX0	CONN.MLB.DATA	ADMA.LCD_D04	CONN.ENET1.RGMII_RXC	LSIO.GPIO0.IO04	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
80	ESAI0_TX2_RX3	K28	ADMA.ESAI0.TX2_RX3	CONN.ENET1.RMII_RX_ER	ADMA.LCD_D06	CONN.ENET1.RGMII_RXD2	LSIO.GPIO0.IO06	GPIO	ALT0	PD	VDD_ESAI_SPDIF_3P3
82	MCLK_IN0	G35	ADMA.ACM.MCLK_IN0	ADMA.ESAI0.RX_HF_CLK	ADMA.LCD_VSYNC	ADMA.SPI2.SDI	LSIO.GPIO0.IO19	GPIO	ALT0	PD	VDD_SPI_MCLK_UART_3P3
86	SPI2_CS0	P28	ADMA.SPI2.CS0				LSIO.GPIO1.IO00	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
88	SPI2_SCK	R29	ADMA.SPI2.SCK				LSIO.GPIO1.IO03	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
90	SPI2_SDI	N31	ADMA.SPI2.SDI				LSIO.GPIO1.IO02	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
92	SPI2_SDO	P32	ADMA.SPI2.SDO				LSIO.GPIO1.IO01	GPIO	ALT4	PD	VDD_SPI_SAI_3P3

X1 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
	CSI_HSYNC	AR29	CI_PI.CSI_HSYNC	CI_PI.CSI_D00	ADMA.SAI3.RXFS	SNVS.TAMPER_IN3		GPIO	ALT0	PD	VDD_CSI_3P3
94	PCIE_CTRL0_WAKE_B [1]	A11	HSIO.PCIE0.WAKE_B				LSIO.GPIO4.IO02	GPIO	ALT0	PU	VDD_PCIE_DIG_3P3
96	CSI_PCLK	AK26	CI_PI.CSI_PCLK	MIPI_CSI0.I2C0.SCL		ADMA.SPI1.SCK	LSIO.GPIO3.IO00	GPIO	ALT0	PD	VDD_CSI_3P3
98	QSPI0B_DATA3	AM8	LSIO.QSPI0B.DATA3	LSIO.QSPI1A.DATA3	LSIO.KPP0.ROW0		LSIO.GPIO3.IO21	FASTD	ALT0	PD	VDD_QSPI0B_3P3
100	SAI1_RXFS	N35	ADMA.SAI1.RXFS	ADMA.SAI1.TXFS		ADMA.LCD_D23	LSIO.GPIO0.IO31	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
102	QSPI0B_DQS	AK10	LSIO.QSPI0B.DQS	LSIO.QSPI1A.DQS	LSIO.KPP0.ROW1		LSIO.GPIO3.IO22	FASTD	ALT0	PD	VDD_QSPI0B_3P3
104	QSPI0B_SS0_B	AH10	LSIO.QSPI0B.SS0_B	LSIO.QSPI1A.SS0_B	LSIO.KPP0.ROW2		LSIO.GPIO3.IO23	FASTD	ALT4	PU	VDD_QSPI0B_3P3
106	QSPI0B_SS1_B	AJ9	LSIO.QSPI0B.SS1_B	LSIO.QSPI1A.SS1_B	LSIO.KPP0.ROW3		LSIO.GPIO3.IO24	FASTD	ALT4	PU	VDD_QSPI0B_3P3
138	MIPI_DSI1_GPIO0_00 [2]	AD30	MIPI_DSI1.GPIO0.IO00	ADMA.I2C2.SCL	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO31	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
140	MIPI_DSI0_I2C0_SCL [2]	AC31	MIPI_DSI0.I2C0.SCL	MIPI_DSI1.GPIO0.IO02			LSIO.GPIO1.IO25	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
142	MIPI_DSI0_I2C0_SDA [2]	AB28	MIPI_DSI0.I2C0.SDA	MIPI_DSI1.GPIO0.IO03			LSIO.GPIO1.IO26	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
144	SCU_GPIO0_00 [4]	AF28	SCU.GPIO0.IO00	SCU.UART0.RX	M40.UART0.RX	ADMA.UART3.RX	LSIO.GPIO2.IO03	GPIO	ALT0	PD	VDD_ANA1_1P8
146	SCU_GPIO0_01 [4]	AH30	SCU.GPIO0.IO01	SCU.UART0.TX	M40.UART0.TX	ADMA.UART3.TX	SCU.WDOG0.WDOG_OUT	GPIO	ALT0	PU	VDD_ANA1_1P8
178	PCIE_CTRL0_CLKREQ_B [1]	D10	HSIO.PCIE0.CLKREQ_B				LSIO.GPIO4.IO01	GPIO	ALT0	PD	VDD_PCIE_DIG_3P3
180	ENET0_MDIO	B32	CONN.ENET0.MDIO	ADMA.I2C3.SDA [3]	CONN.ENET1.MDIO [3]		LSIO.GPIO5.IO10 [3]	GPIO	ALT0	PU	VDD_ENET_MDIO_3P3
184	ENET0_MDC	D30	CONN.ENET0.MDC	ADMA.I2C3.SCL [3]	CONN.ENET1.MDC [3]		LSIO.GPIO5.IO11 [3]	GPIO	ALT4	PD	VDD_ENET_MDIO_3P3
186	MIPI_DSI1_I2C0_SCL [2]	AE33	MIPI_DSI1.I2C0.SCL	MIPI_DSI0.GPIO0.IO02			LSIO.GPIO1.IO29	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
188	MIPI_DSI1_I2C0_SDA [2]	AC29	MIPI_DSI1.I2C0.SDA	MIPI_DSI0.GPIO0.IO03			LSIO.GPIO1.IO30	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
190	USDHC1_CMD	C25	CONN.USDHC1.CMD	CONN.NAND.CE0_B	ADMA.MQS.R		LSIO.GPIO4.IO24	FASTD	ALT0	PU	VDD_USDHC1_1P8_3P3
192	USDHC1_DATA0	A27	CONN.USDHC1.DATA0	CONN.NAND.CE1_B	ADMA.MQS.L		LSIO.GPIO4.IO25	FASTD	ALT0	PU	VDD_USDHC1_1P8_3P3
194	MIPI_DSI0_GPIO0_01	AE35	MIPI_DSI0.GPIO0.IO01	ADMA.I2C1.SDA			LSIO.GPIO1.IO28	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
196	MIPI_DSI0_GPIO0_00	AD32	MIPI_DSI0.GPIO0.IO00	ADMA.I2C1.SCL	MIPI_DSI0.PWM0.OUT		LSIO.GPIO1.IO27	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3

[1] This signal is not available on modules with Wi-Fi.
[2] This signal is shared with one of the FFC connectors
[3] Since the on-module Ethernet PHY shares these pins, only MDIO/MDC function is possible
[4] Bi-directional level shifter on this pin. Interface speed is limited

4.4.2 MIPI/DSI and LVDS FFC

X2 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
1	MIPI_DSI0_CLK_N	AJ19	MIPI_DSI0.CKN					DSI			VDD_MIPI_DSI0_1P8
2	MIPI_DSI0_CLK_P	AK20	MIPI_DSI0.CKP					DSI			VDD_MIPI_DSI0_1P8
4	MIPI_DSI0_DATA0_N	AJ21	MIPI_DSI0.DN0					DSI			VDD_MIPI_DSI0_1P8
5	MIPI_DSI0_DATA0_P	AK22	MIPI_DSI0.DP0					DSI			VDD_MIPI_DSI0_1P8
7	MIPI_DSI0_DATA1_N	AJ17	MIPI_DSI0.DN1					DSI			VDD_MIPI_DSI0_1P8
8	MIPI_DSI0_DATA1_P	AK18	MIPI_DSI0.DP1					DSI			VDD_MIPI_DSI0_1P8
10	MIPI_DSI0_DATA2_N	AJ23	MIPI_DSI0.DN2					DSI			VDD_MIPI_DSI0_1P8
11	MIPI_DSI0_DATA2_P	AK24	MIPI_DSI0.DP2					DSI			VDD_MIPI_DSI0_1P8
13	MIPI_DSI0_DATA3_N	AJ15	MIPI_DSI0.DN3					DSI			VDD_MIPI_DSI0_1P8
14	MIPI_DSI0_DATA3_P	AK16	MIPI_DSI0.DP3					DSI			VDD_MIPI_DSI0_1P8
15	MIPI_DSI0_I2C0_SCL [1]	AC31	MIPI_DSI0.I2C0.SCL	MIPI_DSI1.GPIO0.IO02			LSIO.GPIO1.IO25	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
16	MIPI_DSI0_I2C0_SDA [1]	AB28	MIPI_DSI0.I2C0.SDA	MIPI_DSI1.GPIO0.IO03			LSIO.GPIO1.IO26	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
17	MIPI_DSI1_CLK_N	AM16	MIPI_DSI1.CKN					DSI			VDD_MIPI_DSI1_1P8

X2 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
18	MIPI_DSI1_CLK_P	AP16	MIPI_DSI1.CKP					DSI			VDD_MIPI_DSI1_1P8
20	MIPI_DSI1_DATA0_N	AN15	MIPI_DSI1.DN0					DSI			VDD_MIPI_DSI1_1P8
21	MIPI_DSI1_DATA0_P	AR15	MIPI_DSI1.DP0					DSI			VDD_MIPI_DSI1_1P8
23	MIPI_DSI1_DATA1_N	AN17	MIPI_DSI1.DN1					DSI			VDD_MIPI_DSI1_1P8
24	MIPI_DSI1_DATA1_P	AR17	MIPI_DSI1.DP1					DSI			VDD_MIPI_DSI1_1P8
25	MIPI_DSI1_GPIO0_00 [1]	AD30	MIPI_DSI1.GPIO0.IO00	ADMA.I2C2.SCL	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO31	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
26	MIPI_DSI1_DATA2_N	AM14	MIPI_DSI1.DN2					DSI			VDD_MIPI_DSI1_1P8
27	MIPI_DSI1_DATA2_P	AP14	MIPI_DSI1.DP2					DSI			VDD_MIPI_DSI1_1P8
29	MIPI_DSI1_DATA3_N	AM18	MIPI_DSI1.DN3					DSI			VDD_MIPI_DSI1_1P8
30	MIPI_DSI1_DATA3_P	AP18	MIPI_DSI1.DP3					DSI			VDD_MIPI_DSI1_1P8

[1] This signal is shared with the SODIMM module edge connector

4.4.3 MIPI/CSI-2 FFC

X3 Pin	i.MX 8X Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	Type	Default Mode	Reset State	Power Block
2	MIPI_CSI0_DATA0_N	AM22	MIPI_CSI0.DN0					CSI			VDD_MIPI_CSI0_1P8
3	MIPI_CSI0_DATA0_P	AP22	MIPI_CSI0.DP0					CSI			VDD_MIPI_CSI0_1P8
5	MIPI_CSI0_DATA1_N	AM20	MIPI_CSI0.DN1					CSI			VDD_MIPI_CSI0_1P8
6	MIPI_CSI0_DATA1_P	AP20	MIPI_CSI0.DP1					CSI			VDD_MIPI_CSI0_1P8
8	MIPI_CSI0_CLK_N	AN21	MIPI_CSI0.CKN					CSI			VDD_MIPI_CSI0_1P8
9	MIPI_CSI0_CLK_P	AR21	MIPI_CSI0.CKP					CSI			VDD_MIPI_CSI0_1P8
11	QSPI0A_SS1_B [1]	AK12	LSIO.QSPI0A.SS1_B				LSIO.GPIO3.IO15	FASTD	ALT4	PU	VDD_QSPI0A_3P3
12	CSI_MCLK [1]	AM26	CI_PI.CSI_MCLK	MIPI_CSI0.I2C0.SDA		ADMA.SPI1.SDO	LSIO.GPIO3.IO01	GPIO	ALT0	PD	VDD_CSI_3P3
13	MIPI_DSI1_I2C0_SCL [1]	AE33	MIPI_DSI1.I2C0.SCL	MIPI_DSI0.GPIO0.IO02			LSIO.GPIO1.IO29	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
14	MIPI_DSI1_I2C0_SDA [1]	AC29	MIPI_DSI1.I2C0.SDA	MIPI_DSI0.GPIO0.IO03			LSIO.GPIO1.IO30	GPIO	ALT0	PU	VDD_MIPI_DSI_DIG_3P3
16	MIPI_CSI0_DATA2_N	AN23	MIPI_CSI0.DN2					CSI			VDD_MIPI_CSI0_1P8
17	MIPI_CSI0_DATA2_P	AR23	MIPI_CSI0.DP2					CSI			VDD_MIPI_CSI0_1P8
19	MIPI_CSI0_DATA3_N	AN19	MIPI_CSI0.DN3					CSI			VDD_MIPI_CSI0_1P8
20	MIPI_CSI0_DATA3_P	AR19	MIPI_CSI0.DP3					CSI			VDD_MIPI_CSI0_1P8
22	QSPI0A_SS0_B [1]	AM12	LSIO.QSPI0A.SS0_B				LSIO.GPIO3.IO14	FASTD	ALT4	PU	VDD_QSPI0A_3P3
23	QSPI0A_SCLK [1]	AP12	LSIO.QSPI0A.SCLK				LSIO.GPIO3.IO16	FASTD	ALT4	PD	VDD_QSPI0A_3P3

[1] This signal is shared with the SODIMM module edge connector

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decoupling capacitors on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V Analogue supply for ADC	Connect this pin **to a 3.3V supply**. For better Audio accuracy, we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the 3V3 input supply.
9, 11	VSS_AUDIO	I	Analogue Ground	Connect this pin to GND. This pin is connected with Digital GND on the Colibri iMX8X. For better Audio accuracy, use the module connector as a start point and route the grounds individual for the audio.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is active low and resets the Colibri module. There is a 100k Ohm pull-up on this pin.
87	nRESET_OUT	O	Reset Output	This pin is active low. This pin is driven low at boot up. This signal is an open-drain output which a 10k Ohm pull-up on the module.

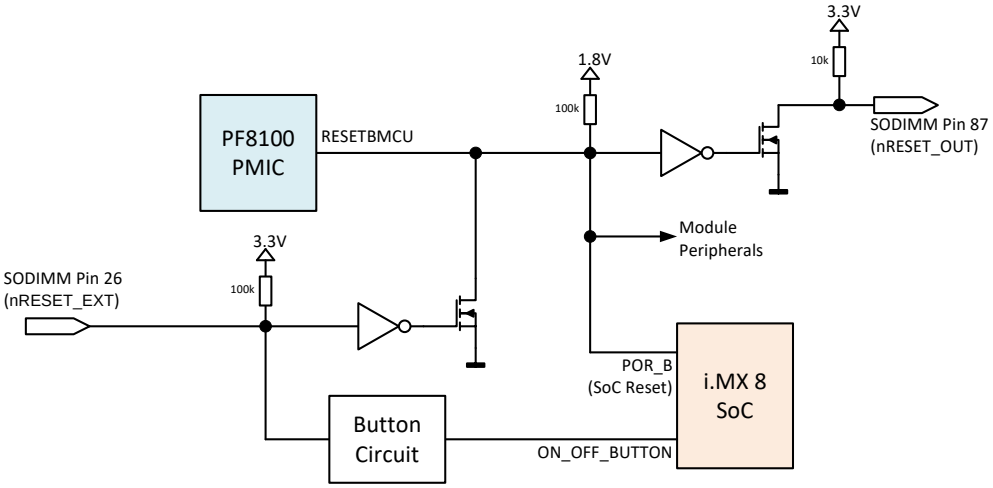

Figure 4: Reset Circuit

The Colibri iMX8X features the NXP PF8100 power management IC (PMIC). Besides managing the power up and down sequence, this IC also controls the voltage level of certain power rails. When applying the main power to the Colibri module, the PMIC will ramp up all rails and releases at the end the RSETBMCU signal. This reset is used for the SoC, some of the on-module peripherals, and is available as a buffered output on pin 87 of the SODIMM module edge connector.

The Colibri iMX8X allows the external reset input on pin 26 of the SODIMM connector to initiate a warm reset cycle. This input signal drives the RESETBMCU signal directly down, which resets the SoC, the on-module peripherals, and generates a reset cycle on pin 87. For proper power-up sequencing, the external reset input on pin 26 is not required to be driven by the carrier board. The pin 26 reset input can be left unconnected if there is no need for initiating the module reset externally.

The external reset signal on pin 26 is also routed to a power button circuit on the module. This circuit generates a button signal on the falling edge of the external reset signal. This button signal is routed to the ON_OFF_BUTTON input of the SoC. It allows to wake up the system after power down. The power button circuit generates this button signal also when the main input voltage is reapplied. More information about the module's power sequencing can be found in the Colibri Carrier Board Design Guide.

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. The GPIO functionality is configured by selecting the correct alternate function. For most of the GPIOs, this is ALT4. All GPIO pins can be used as an interrupt source.

Besides the regular GPIOs that can be accessed by the main Cortex A35 cores and the Cortex M4F core, a few GPIOs are tightly coupled to the real-time capable M4F core. These GPIOs are all located as an alternate function of the ADC pins. Therefore, the pins are only rated at 1.8V.

Table 5-4 Tightly Coupled M4 GPIO signals

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
2	Analogue Input <3>	ADC_IN5	M40.GPIO0.IO05	I/O	**Maximum voltage 1.8V**
4	Analogue Input <2>	ADC_IN4	M40.GPIO0.IO04	I/O	**Maximum voltage 1.8V**
6	Analogue Input <1>	ADC_IN1	M40.GPIO0.IO01	I/O	**Maximum voltage 1.8V**
8	Analogue Input <0>	ADC_IN0	M40.GPIO0.IO00	I/O	**Maximum voltage 1.8V**

5.2.1 Wakeup Source

The Colibri iMX8X uses different sleep modes. In principle, all GPIOs can be used to wake up the Colibri module from the low power states.

Even though there are many pins available with the wake functionally, it is recommended that, whenever possible, use pin 43 (WAKEUP Source<0>) and 45 (WAKEUP Source<1>). This ensures that the design is compatible with other Colibri modules.

Table 5-5 Colibri Standard Wake Signals

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
43	WAKEUP Source<0>, SDCard CardDetect	QSPI0A_DATA0	LSIO.GPIO3.IO09	I	Preferred wake-up source
45	WAKEUP Source<1>	QSPI0A_DATA1	LSIO.GPIO3.IO10	I	Preferred wake-up source

5.3 Ethernet

The Colibri iMX8X features a 10/100 Mbit/s Ethernet interface with Medium Dependent Interface (MDI). The PHY of this interface is located on the module. Therefore, only the magnetics and the connector are needed on the carrier board. The module features the Micrel KSZ8041 Fast Ethernet Transceiver as PHY, connected over RMII with the MAC in the NXP i.MX 8X SoC. The MAC in the SoC features an accurate IEEE 1588 compliant timer for clock synchronization, commonly used in industrial automation applications. The Ethernet interface supports Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN).

Table 5-6 Ethernet Pins

X1 Pin#	Colibri STD Function	PHY Signal Name	I/O	Description
189	TXO+	TX+	O	100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	TXO-	TX-	O	100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	RXI+	RX+	I	100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	RXI-	RX-	I	100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN	GND		Ethernet ground, on the module connected to common GND
183	LINK_AKT	LED0	O	Link activity indication LED
185	SPEED100	LED1	O	100 Mbit/s indication LED

The Colibri iMX8X features a second Ethernet port. If this port is required, an additional PHY needs to be implemented on the carrier board. Since the MDIO configuration port signals are shared

between the on-module and external Ethernet PHY, it is crucial to ensure that the two PHYs are not strapped to the same address. The MDIO interface of the Ethernet PHY on the module is using the address 00010. We recommend using the address 00001 for the external PHY. Since the MDIO signals are shared, the power rail of the internal Ethernet PHY cannot be turned off if an external Ethernet PHY is in use. The second MAC in the SoC provides two different interface standards for the connection with the PHY:

- RMII: Reduced Media Independent Interface. This is the preferred mode for interfacing a 10/100 Mbit/s Ethernet PHY, such as the KSZ8041.
- RGMII: Reduced Gigabit Media Independent Interface. This interface allows connecting a Gigabit Ethernet PHY. I/O voltage is not within the NXP specifications.

When using the second Ethernet interface as RGMII, NXP limits in their datasheet the I/O voltage to 1.8V and 2.5V. The interface pins of the Colibri iMX8X are fixed to 3.3V. Therefore, using the interface in RGMII mode is violating the NXP specifications. Using the same pins for any other alternate function (e.g., RMII, RGB LCD, or GPIO) is not affected by this limitation. Due to this limitation, it is not recommended to use the secondary Ethernet port as RGMII. It is recommended to use the port only as RMII, limiting the speed to 10/100 Mbit/s (Fast Ethernet).

Table 5-7 RMII signals (incompatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
74	LCD RGB Data<10>	SPDIF0_RX	CONN.ENET1.RGMII_RXD0	I	RMII_RXD0
46	LCD RGB Data<7>	ESAI0_TX3_RX2	CONN.ENET1.RGMII_RXD1	I	RMII_RXD1
80	LCD RGB Data<6>	ESAI0_TX2_RX3	CONN.ENET1.RMII_RX_ER	I	RMII_RXER
62	LCD RGB Data<8>	ESAI0_TX4_RX1	CONN.ENET1.RGMII_TXD0	O	RMII_TXD0
48	LCD RGB Data<9>	ESAI0_TX5_RX0	CONN.ENET1.RGMII_TXD1	O	RMII_TXD1
60	LCD RGB Data<2>	ESAI0_SCKR	CONN.ENET1.RGMII_TX_CTL	O	RMII_TXEN
50	LCD RGB Data<11>	SPDIF0_TX	CONN.ENET1.RGMII_RX_CTL	O	RMII_TXEN
184	ADDRESS18	ENET0_MDC	CONN.ENET1.MDC	O	RMII_MDC **shared with PHY on the module**
180	DATA31	ENET0_MDIO	CONN.ENET1.MDIO	I/O	RMII_MDIO **shared with PHY on the module**
76	LCD RGB Data<0>	ESAI0_FSR	CONN.ENET1.RCLK50M_OUT	I/O	50MHz Reference clock that is provided from the MAC to the PHY or from the PHY to the MAC
137	USB Client Cable Detect,SPDIF_OUT	ENET0_REFCLK_125M_25M	CONN.ENET1.PPS	O	IEEE1588 pulse per second output

Table 5-8 RGMII signals (incompatible with other modules, I/O voltage not withing NXP specification)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
50	LCD RGB Data<11>	SPDIF0_TX	CONN.ENET1.RGMII_RX_CTL	I	RGMII_RX_CTL
78	LCD RGB Data<4>	ESAI0_TX0	CONN.ENET1.RGMII_RXC	I	RGMII_RXC
74	LCD RGB Data<10>	SPDIF0_RX	CONN.ENET1.RGMII_RXD0	I	RGMII_RXD0
46	LCD RGB Data<7>	ESAI0_TX3_RX2	CONN.ENET1.RGMII_RXD1	I	RGMII_RXD1
80	LCD RGB Data<6>	ESAI0_TX2_RX3	CONN.ENET1.RGMII_RXD2	I	RGMII_RXD2
72	LCD RGB Data<5>	ESAI0_TX1	CONN.ENET1.RGMII_RXD3	I	RGMII_RXD3
60	LCD RGB Data<2>	ESAI0_SCKR	CONN.ENET1.RGMII_TX_CTL	O	RGMII_TX_CTL
76	LCD RGB Data<0>	ESAI0_FSR	CONN.ENET1.RGMII_TXC	O	RGMII_TXC
62	LCD RGB Data<8>	ESAI0_TX4_RX1	CONN.ENET1.RGMII_TXD0	O	RGMII_TXD0
48	LCD RGB Data<9>	ESAI0_TX5_RX0	CONN.ENET1.RGMII_TXD1	O	RGMII_TXD1
70	LCD RGB Data<1>	ESAI0_FST	CONN.ENET1.RGMII_TXD2	O	RGMII_TXD2
58	LCD RGB Data<3>	ESAI0_SCKT	CONN.ENET1.RGMII_TXD3	O	RGMII_TXD3
184	ADDRESS18	ENET0_MDC	CONN.ENET1.MDC	O	RGMII_MDC **shared with PHY on the module**
180	DATA31	ENET0_MDIO	CONN.ENET1.MDIO	I/O	RGMII_MDIO **shared with PHY on the module**
52	LCD RGB Data<12>	SPDIF0_EXT_CLK	CONN.ENET1.REFCLK_125M_25M	I	Optional 125MHz reference clock input
137	USB Client Cable Detect,SPDIF_OUT	ENET0_REFCLK_125M_25M	CONN.ENET1.PPS	O	IEEE1588 pulse per second output

5.4 Wi-Fi and Bluetooth

The Colibri iMX8X is available as a version with on-module Wi-Fi and Bluetooth interface. The additional "WB" in the product name indicates that this version features Wi-Fi and Bluetooth. These Colibri module versions are making use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from Azurewave.

Features:

- Wi-Fi 802.11ac/a/b/g/n
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for a dual external antenna in 2x2 configuration compatible with the IPX/IPEX connector MHF4 series.
- Pre-certified for CE (Europe), FCC (United States), and IC (Canada)

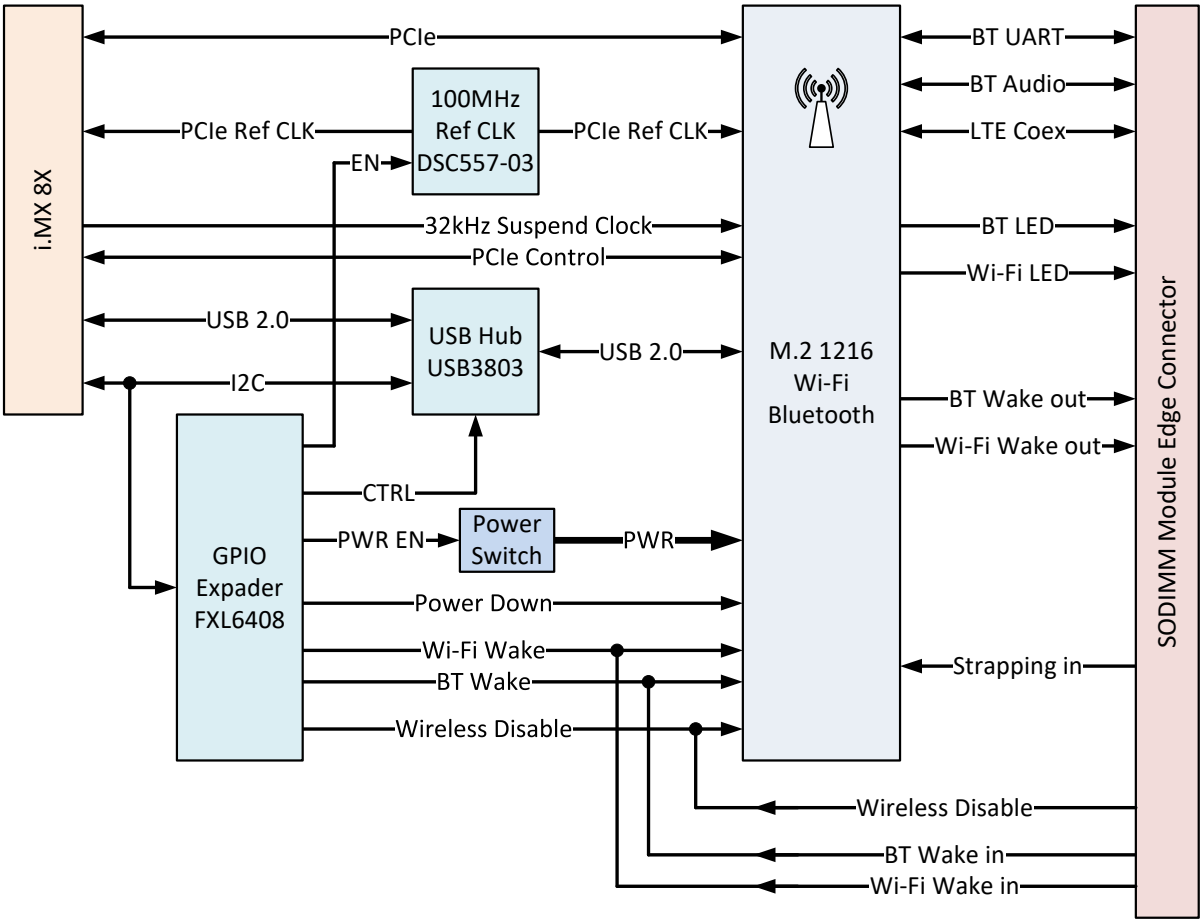

Figure 5: Wi-Fi and Bluetooth block diagram

The Wi-Fi module is connected over a PCI Express interface with the i.MX 8X SoC. The Bluetooth part requires a USB connection. Since the SoC does not have enough USB ports, there is a USB hub on the Colibri module. To reduce the number of GPIO pins that have to be removed from the SODIMM module edge connector for controlling certain functions, an additional 8-port GPIO expander assembled on Colibri iMX8X modules with wireless features. The GPIO expander outputs are used to control the Wi-Fi and Bluetooth module itself, the USB hub, and enable the PCIe reference clock.

Table 5-9 Signal Pins between AW-CM276NF and i.MX 8X

AW-CM276NF Pin Name	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
PCIE_RX_P	PCIE0_TX0_P	HSIO.PCIE0.TX0_P	I	PCI Express interface
PCIE_RX_N	PCIE0_TX0_N	HSIO.PCIE0.TX0_N		
PCIE_TX_P	PCIE0_RX0_P	HSIO.PCIE0.RX0_P	O	
PCIE_TX_N	PCIE0_RX0_N	HSIO.PCIE0.RX0_N		
PCIE_WAKEn	PCIE_CTRL0_WAKE_B	HSIO.PCIE0.WAKE_B	I/O	PCIe wake
PCIE_CLKREQn	PCIE_CTRL0_CLKREQ_B	HSIO.PCIE0.CLKREQ_B	I/O	PCIe reference clock request
GPIO[21]	PCIE_CTRL0_PERST_B	HSIO.PCIE0.PERST_B	I	PCIe reset
SLP_CLK	SCU_BOOT_MODE3	SCU.DSC.RTC_ CLOCK_OUTPUT_32K	I	32.768kHz sleep clock input for low power operation

The AW-CM276NF features four wake signals. Two are input signals (one for the Wi-Fi and one for Bluetooth), allowing for waking up the radio. These wake signals are connected to the SoC but are also available on the module edge connector. The Wi-Fi and Bluetooth receiver can use the additional two output signals to wake up the system. These signals are only available at the module edge connector. If the SoC needs to be woken up, route these pins back to the regular wake input signals of the Colibri module.

Besides the USB interface for Bluetooth communication, the AW-CM276NF also features a dedicated UART and digital audio (I2S) interface. The interface pins are available on the module edge connector.

Table 5-10 SODIMM Signal Pins of the AW-CM276NF

X1 Pin#	Colibri STD Function	AW-CM276NF Pin Name	I/O	Description
111	ADDRESS0	GPIO[8]/UART_SOUT	O	BT UART mode: TX data
113	ADDRESS1	GPIO[9]/UART_SIN	I	BT UART mode: RX data
115	ADDRESS2	GPIO[10]/UART_CTSn	I	BT UART mode: Clear to send
117	ADDRESS3	GPIO[11]/UART_RTSn	O	BT UART mode: Request to send
121	ADDRESS5	GPIO[14]/TCK/ WLAN Wake Host	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output
123	ADDRESS6	GPIO[13]/BT IRQ(O)	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output
125	ADDRESS7	GPIO[2]/WLAN_LED	O	Wi-Fi activity LED
112	ADDRESS9	GPIO[6]/PCM_CLK	I/O	PCM clock signal for audio interface
114	ADDRESS10	GPIO[7]/PCM_SYNC	I/O	PCM sync signal for audio interface
116	ADDRESS11	GPIO[4]/PCM_DIN	I	PCM data input for audio interface
118	ADDRESS12	GPIO[5]/PCM_DOUT	O	PCM data output for audio interface
120	ADDRESS13	GPIO[15]/ TMS/ Host Wake WLAN	I	HOST_WKUP_WLAN: SoC to AW-CM276NF Wi-Fi Wakeup, the signal is also connected to SoC
122	ADDRESS14	GPIO[12]/ UART Host Wake BT	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup, the signal is also connected to SoC
124	ADDRESS15	GPIO[22]/ PCIE_W_DISABLEn	I	PCIe Wireless Disable Input (active low), the signal is also connected to SoC
126	DQM0	GPIO3/BT_LED	O	Bluetooth activity LED
128	DQM1	GPIO[16]/ LTE_COEX_IN	I	Optional LTE coexistence protocol input
130	DQM2	GPIO[17]/ LTE_COEX_OUT	O	Optional LTE coexistence protocol output

Table 5-11 GPIO Expander Signals

FXL6408 Port	Signal	AW-CM276NF Pin Name	I/O	Description
GPIO0	Wi-Fi_W_DISABLE	GPIO[22]/ PCIE_W_DISABLEn		PCIe Wireless Disable Input (active low), the signal is also available on SODIMM
GPIO1	Wi-Fi_WKUP_WLAN	GPIO[15]/ TMS/ Host Wake WLAN		HOST_WKUP_WLAN: SoC to AW-CM276NF Wi-Fi Wakeup, the signal is also available on SODIMM
GPIO2	PWR_EN_+V3.3_WiFi_N			Enables power rails for Wi-Fi/BT module (active low)
GPIO3	PCIe_REF_CLK_EN			Enables PCIe reference clock (active high)
GPIO4	USB_RESET_N			USB Hub reset (active low)
GPIO5	USB_BYPASS_N			Enables bypass mode of USB hub (active low)

FXL6408 Port	Signal	AW-CM276NF Pin Name	I/O	Description
GPIO6	Wi-Fi_PDn	PDn		Power Down of complete Wi-Fi/BT module (active low). Firmware needs to be re-downloaded.
GPIO7	Wi-Fi_WKUP_BT	GPIO[12]/ UART Host Wake BT		HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup, the signal is also available on SODIMM

By default, the AW-CM276NF is strapped for using the PCIe for Wi-Fi and the USB interface for Bluetooth. The strapping pins are available on the SODIMM connector. This allows one to strap the Wi-Fi/BT module for different operation modes. The strapping pins can be left unconnected for the PCIe/USB option since there are strapping resistors on the module. If you need to use the wireless module in a different mode, place 1k pull resistors on the carrier board. Be aware, the signals are only 1.8V capable. Please contact the local Toradex support team and visit our developer website to check whether the mode is supported in software.

Table 5-12 AW-CM276NF Strapping Pins

X1 Pin#	Colibri STD Function	AW-CM276NF Pin Name	I/O	Description
170	DATA26	CONFIG_HOST[0]	I	**Maximum voltage 1.8V**. Pulled down on the module
172	DATA27	CONFIG_HOST[1]	I	**Maximum voltage 1.8V**. Pulled up on the module
174	DATA28	CONFIG_HOST[2]	I	**Maximum voltage 1.8V**. Pulled down on the module

Table 5-13 AW-CM276NF Strapping Options

CONFIG_HOST[2:0]	Wi-Fi	Bluetooth	Remarks
000	SDIO	UART	Not possible on Colibri iMX8X
001	SDIO	SDIO	Not possible on Colibri iMX8X
010	PCIe	USB	Default configuration
011	PCIe	UART	
100	USB3.0	UART	Not possible on Colibri iMX8X
101	USB2.0	USB2.0	
110	USB3/2.0	USB3/2.0	Not possible on Colibri iMX8X
111	USB3.0	USB3.0	Not possible on Colibri iMX8X

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. Please contact Toradex about certifying the Colibri iMX8X WB: Contact your local sales office or support@toradex.com.

5.5 USB

The i.MX 8X SoC features two USB 2.0 High-Speed (480 Mbit/s) ports. The SoC would even have SuperSpeed signals for upgrading one of the USB ports to USB3.0. However, the Colibri Standard does not feature pins for the extra SuperSpeed signals. Therefore, the interface speed is limited to USB 2.0 High-Speed.

Both SoC USB ports are OTG capable. This means they can change their role from host to client and vice versa. The first Colibri iMX8X USB port (USBC) is intended to be used either in the host or client mode. However, the Colibri standard does not support full OTG functionality. The USBC port is also used for the serial loader mode (recovery mode). For more information, see section 6. The second Colibri USB Port (USBH) is only intended to be used as a USB host port.

Since the Wi-Fi/Bluetooth module requires an additional 2.0 USB interface for its Bluetooth features, there is a USB 2.0 Hub on the modules with assembled wireless features. The hub features a bypass function that is enabled by default. This feature shuts down the hub functionality and bypasses the upstream signal to the downstream port 3. This dramatically reduces the power consumption of the USB hub. Therefore, it is recommended to put the hub in bypass mode if the USB connection to the Bluetooth of the wireless module is not required.

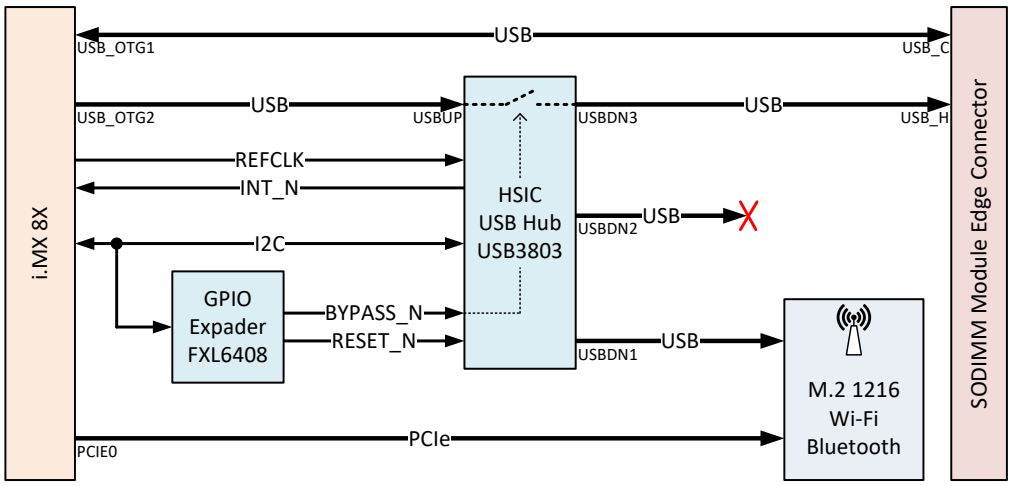

Figure 6: USB Block Diagram (Modules with Wi-Fi/Bluetooth)

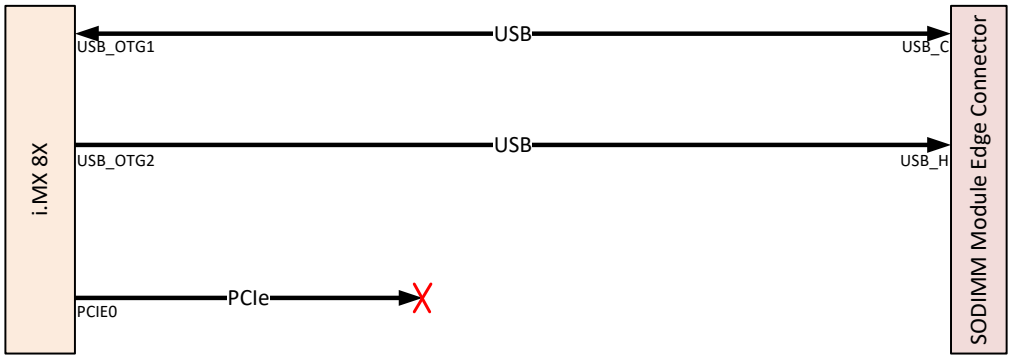

Figure 7: USB Block Diagram (Modules without Wi-Fi/Bluetooth feature)

5.5.1 USB Data Signal

Table 5-14 USB Data Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	I/O	Description
143	USBC_P	USB_OTG1_DP	I/O	Differential Signal for the shared USB Host / Client port
145	USBC_N	USB_OTG1_DN	I/O	
139	USBH_P	USB_OTG2_DP	I/O	Differential Signal for USB Host port
141	USBH_N	USB_OTG2_DN	I/O	

5.5.2 USB Control Signals

Table 5-15 USB OTG Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
135	SPDIF_IN	USB_OTG1_ID	CONN.USB_OTG1.ID	I	USB OTG ID, not used on standard Colibri carrier boards.
137	USB Client Cable Detect,SPDIF_OUT	USB_OTG1_VBUS	CONN.USB_OTG1.VBUS	I	Use this pin to detect if VBUS is present (5V USB supply). There is a second SoC pin connected. Therefore, this pin is **only 3.3V tolerant!**

The Colibri iMX8X module does not support true OTG, but the interface can be configured as host or client. Due to compatibility with other Colibri modules, the current evaluation board and the other Toradex carrier board do not use the USB OTG ID pin to detect whether a Type A or Type B cable is plugged in. Instead, the VBUS is used for detecting the Host or Client mode. We recommend implementing the same circuit as on the evaluation board to ensure the design is compatible with the provided Toradex OS images (BSP).

If you use the USB Host function, you need to generate the 5V USB supply voltage on your carrier board. The Colibri iMX8X provides two optional signals for USB power supply control. We recommend using the following pins to ensure the best possible compatibility. However, the use of these signals is not mandatory.

Table 5-16 USB Power Control Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
129	USB Host Power Enable	USB_SS3_TC0	CONN.USB_OTG2.PWR	O	This pin enables the external USB voltage supply
131	USB Host Over-Current Detect	USB_SS3_TC3	CONN.USB_OTG2.OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply

Table 5-17 Additional USB Power Control Pins (not compatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
133		USB_SS3_TC1	CONN.USB_OTG2.PWR	O	Alternate power enable pin for USBH
127		USB_SS3_TC2	CONN.USB_OTG2.OC	I	Alternate overcurrent pin for USBH
129	USB Host Power Enable	USB_SS3_TC0	CONN.USB_OTG1.PWR	O	Power enable pin for USBC, not required in standard Colibri carrier board designs
127		USB_SS3_TC2	CONN.USB_OTG1.OC	I	Power current pin for USBC, not required in standard Colibri carrier board designs

5.6 Display

The i.MX 8X features one display controller. This display controller has two outputs, which allow driving two independent displays. Each output of the display controller is connected to a MIPI-DSI/LVDS PHY. One of the outputs of the display controller is additionally routed to the parallel display interface.

5.6.1 Parallel RGB LCD interface

The Colibri iMX8X provides one parallel LCD interface on the SODIMM connector. It supports up to 24-bit colors per pixel. Only the 18-bit mode is ensured to be compatible with other Colibri

modules. The additional signals required for the 24-bit interface are located as alternate functions, which are not located at the same place as on other Colibri modules with 24-bit color support. We recommend using the LCD interface of the Colibri iMX8X only in the 18-bit mode.

Features:

- Up to 720p60 (720 x 1280 @ 60 Hz)
- Up to 24-bit color (18-bit recommended)
- Supports parallel TTL displays and smart displays
- Digital video interface output supported with ITU-R BT.656 format
- Max pixel clock 85MHz

Table 5-18 Standard Parallel RGB LCD Interface Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	24-bit RGB Interface	18-bit RGB Interface	16-bit RGB Interface
76	LCD RGB Data<0>	ESAI0_FSR	ADMA.LCD_D00	O	B0	B0	B0
70	LCD RGB Data<1>	ESAI0_FST	ADMA.LCD_D01	O	B1	B1	B1
60	LCD RGB Data<2>	ESAI0_SCKR	ADMA.LCD_D02	O	B2	B2	B2
58	LCD RGB Data<3>	ESAI0_SCKT	ADMA.LCD_D03	O	B3	B3	B3
78	LCD RGB Data<4>	ESAI0_TX0	ADMA.LCD_D04	O	B4	B4	B4
72	LCD RGB Data<5>	ESAI0_TX1	ADMA.LCD_D05	O	B5	B5	G0
80	LCD RGB Data<6>	ESAI0_TX2_RX3	ADMA.LCD_D06	O	B6	G0	G1
46	LCD RGB Data<7>	ESAI0_TX3_RX2	ADMA.LCD_D07	O	B7	G1	G2
62	LCD RGB Data<8>	ESAI0_TX4_RX1	ADMA.LCD_D08	O	G0	G2	G3
48	LCD RGB Data<9>	ESAI0_TX5_RX0	ADMA.LCD_D09	O	G1	G3	G4
74	LCD RGB Data<10>	SPDIF0_RX	ADMA.LCD_D10	O	G2	G4	G5
50	LCD RGB Data<11>	SPDIF0_TX	ADMA.LCD_D11	O	G3	G5	R0
52	LCD RGB Data<12>	SPDIF0_EXT_CLK	ADMA.LCD_D12	O	G4	R0	R1
54	LCD RGB Data<13>	SPI3_SCK	ADMA.LCD_D13	O	G5	R1	R2
66	LCD RGB Data<14>	SPI3_SDO	ADMA.LCD_D14	O	G6	R2	R3
64	LCD RGB Data<15>	SPI3_SDI	ADMA.LCD_D15	O	G7	R3	R4
57	LCD RGB Data<16>	SPI3_CS1	ADMA.LCD_D16	O	R0	R4	
61	LCD RGB Data<17>	UART1_CTS_B	ADMA.LCD_D17	O	R1	R5	
103	Camera Input Data<3>	SAI0_TXD	ADMA.LCD_D18	O	R2		
79	Camera Input Data<4>	SAI0_TXC	ADMA.LCD_D19	O	R3		
97	Camera Input Data<5>	SAI0_RXD	ADMA.LCD_D20	O	R4		
25	UART_A CTS, Keypad_In<0>	SAI1_RXD	ADMA.LCD_D21	O	R5		
27	UART_A RTS	SAI1_RXC	ADMA.LCD_D22	O	R6		
100	Keypad_Out<1>	SAI1_RXFS	ADMA.LCD_D23	O	R7		
44	LCD RGB DE	MCLK_IN1	ADMA.LCD_EN	O	Data Enable (other names: Output Enable, L_BIAS)		
68	LCD RGB HSYNC	SPI3_CS0	ADMA.LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
82	LCD RGB VSYNC	MCLK_IN0	ADMA.LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
56	LCD RGB PCLK	MCLK_OUT0	ADMA.LCD_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

Many applications will also require some signals to control the backlight or display enabling. You can use any of the free GPIOs for these functions. Still, we recommend using the same signals as used on our standard carrier boards to ensure minimal software configuration overhead. PWM capable signals can be used to control the backlight brightness on many display panels - see section 5.12.

5.6.2 LVDS

The Colibri form factor does not feature a native LVDS interface on the SODIMM connector. However, the Colibri iMX8X is equipped with an additional FFC connector that hosts a dual-channel LVDS interface that can be configured to two independent single-channels. This LVDS FFC connector is not compatible with other Colibri modules. If compatibility with other modules is required, it is recommended to add an LVDS transmitter instead from the parallel RGB LCD interface on the carrier board. Such a transmitter can be found on the Colibri Evaluation Board and is described in the Colibri Carrier Board Design Guide.

The official name for the LVDS interface is actually FPD-Link or FlatLink, which uses the low voltage differential signaling (LVDS) technology. However, very often, this interface is simply called LVDS.

The LVDS interface serializes the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to Seven parallel signals. For an 18-bit RGB interface, including the control signals (Display Enable, Vertical, and Horizontal Synch), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional color bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two color-mapping standards for the 24-bit interface. The less common “24-bit / 18-bit compatible” (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each color into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit color mapping standard (VESA format, Intel 24.1 LVDS data format) serializes each color's two most significant bits into the fourth LVDS pair. This mode is not backward compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this color mapping. The LVDS interfaces of Colibri iMX8X are configurable to support different color mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of color mappings.

Figure 8 shows the LVDS output signals for the “24-bit /18-bit Compatible Colour Mapping” (JEIDA format, Intel 24.0 LVDS data format)

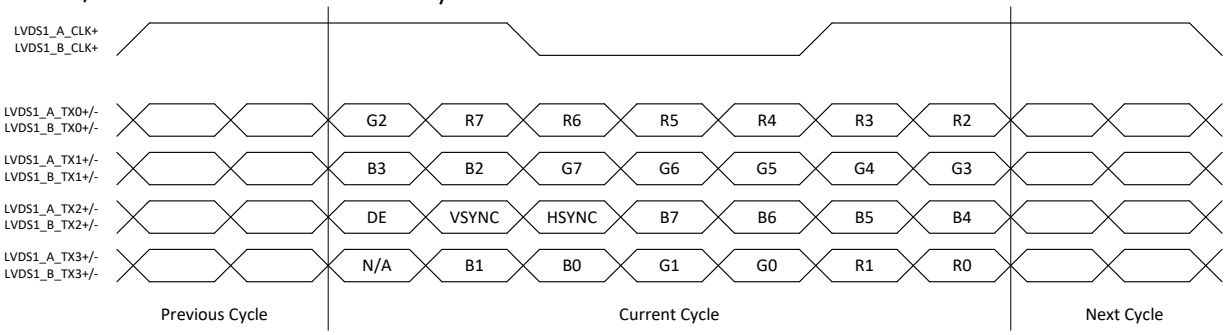

Figure 8: 24-bit / 18-bit Compatible Colour Mapping (Intel 24.0 LVDS Data Format)

Figure 9 shows the LVDS output signals for the common 24-bit color mapping (VESA format, Intel 24.1 LVDS data format).

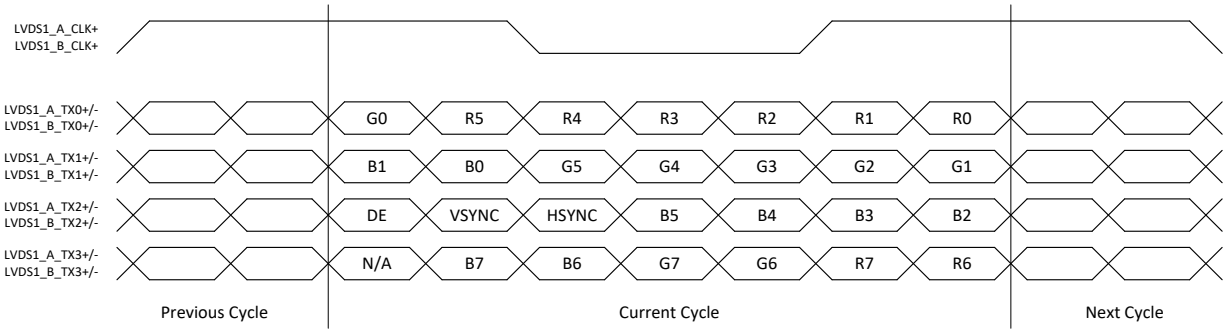

Figure 9: Common 24-bit VESA Colour Mapping (Intel 24.1 LVDS Data Format)

Figure 10 shows the LVDS output signals for the 18-bit interface.

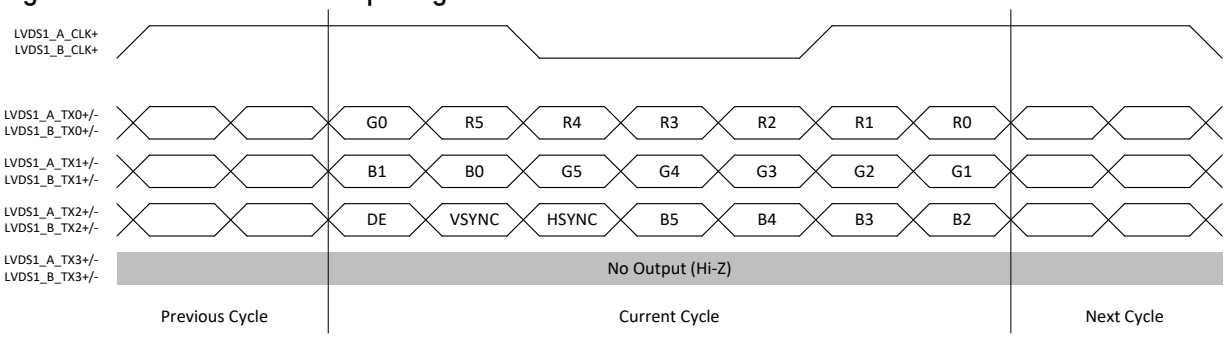

Figure 10: 18-bit Mode

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (85MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel. The dual-channel LVDS interface can support resolutions up to 1920x1200 @60fps (170MHz pixel clock maximum).

The i.MX 8X features two single-channel LVDS ports. It is possible to combine these two LVDS ports to a dual-channel interface for higher resolution displays. Figure 11 shows the possible LVDS display configurations.

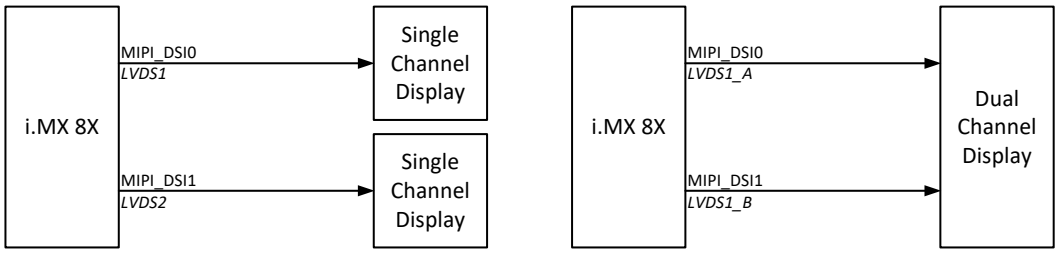

Figure 11: Possible LVDS Display configurations

Table 5-19 LVDS Interface Pins (not compatible with other modules)

X2 Pin#	i.MX 8X Ball Name	i.MX 8X Function	LVDS Function	I/O	Description
2	MIPI_DSI0_CLK_P	MIPI_DSI0.CKP	LVDS1_CLK+	O	LVDS Clock out (odd pixels for dual channel)
1	MIPI_DSI0_CLK_N	MIPI_DSI0.CKN	LVDS1_CLK-		
5	MIPI_DSI0_DATA0_P	MIPI_DSI0.DP0	LVDS1_TX0+	O	LVDS data lane 0 (odd pixels for dual channel)
4	MIPI_DSI0_DATA0_N	MIPI_DSI0.DN0	LVDS1_TX0-		
8	MIPI_DSI0_DATA1_P	MIPI_DSI0.DP1	LVDS1_TX1+	O	LVDS data lane 1 (odd pixels for dual channel)
7	MIPI_DSI0_DATA1_N	MIPI_DSI0.DN1	LVDS1_TX1-		
11	MIPI_DSI0_DATA2_P	MIPI_DSI0.DP2	LVDS1_TX2+	O	LVDS data lane 2 (odd pixels for dual channel)
10	MIPI_DSI0_DATA2_N	MIPI_DSI0.DN2	LVDS1_TX2-		
14	MIPI_DSI0_DATA3_P	MIPI_DSI0.DP3	LVDS1_TX3+	O	LVDS data lane 3 (odd pixels for dual-channel; unused for 18bit)
13	MIPI_DSI0_DATA3_N	MIPI_DSI0.DN3	LVDS1_TX3-		
18	MIPI_DSI1_CLK_P	MIPI_DSI1.CKP	LVDS2_CLK+	O	LVDS Clock out (even pixels for dual channel)
17	MIPI_DSI1_CLK_N	MIPI_DSI1.CKN	LVDS2_CLK-		
21	MIPI_DSI1_DATA0_P	MIPI_DSI1.DP0	LVDS2_TX0+	O	LVDS data lane 0 (even pixels for dual channel)
20	MIPI_DSI1_DATA0_N	MIPI_DSI1.DN0	LVDS2_TX0-		
24	MIPI_DSI1_DATA1_P	MIPI_DSI1.DP1	LVDS2_TX1+	O	LVDS data lane 1 (even pixels for dual channel)
23	MIPI_DSI1_DATA1_N	MIPI_DSI1.DN1	LVDS2_TX1-		
27	MIPI_DSI1_DATA2_P	MIPI_DSI1.DP2	LVDS2_TX2+	O	LVDS data lane 2 (even pixels for dual channel)
26	MIPI_DSI1_DATA2_N	MIPI_DSI1.DN2	LVDS2_TX2-		
30	MIPI_DSI1_DATA3_P	MIPI_DSI1.DP3	LVDS2_TX3+	O	LVDS data lane 3 (even pixels for dual-channel; unused for 18bit)
29	MIPI_DSI1_DATA3_N	MIPI_DSI1.DN3	LVDS2_TX3-		

As the LVDS is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Colibri Carrier Board Design Guide as it is not a standard interface.

Table 5-20 LVDS Signal Routing Requirements

Parameter	Requirement
Max Frequency	Depending on the maximum resolution of the module. The maximum frequency is 7 times higher than the pixel clock in single-channel mode.
Configuration / Device Organization	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	100Ω ±15% differential; 55Ω ±15% single-ended
Max intra-pair skew	<1ps ≈150µm
Max trace length skew between clock and data pairs	<3.5ps ≈500µm, depends on LVDS frequency since the clock is not embedded, can be relaxed for lower resolutions
Max trace length on carrier board and display cable	<500mm
Minimum pair to pair spacing	>2x intra-pair spacing
Maximum allowed via	Minimize the number of via in LVDS traces

5.6.3 Display Serial Interface (DSI)

The Colibri form factor does not feature a native MIPI/DSI interface on the SODIMM connector. However, the Colibri iMX8X is equipped with an additional FFC connector that hosts two MIPI/DSI interfaces. It is a combined subsystem with LVDS and DS capability. The two LVDS channels can be configured as two MIPI/DSI interfaces with up to 4 data lanes. The lanes are capable of up to 1.05GHz data. The interface is bidirectional (high-speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer. Each of the interfaces allows programming the display resolution from 160x120 (QQVGA) to 1920x1200 (WUXGA) with 60Hz and 24bit.

Table 5-21 MIPI/DSI Interface Pins (not compatible with other modules)

X2 Pin#	i.MX 8X Ball Name	i.MX 8X Function	MIPI/DSI Function	I/O	Description
2	MIPI_DSI0_CLK_P	MIPI_DSI0.CKP	DSI1_CLK+	O	DSI Interface 1 clock
1	MIPI_DSI0_CLK_N	MIPI_DSI0.CKN	DSI1_CLK-		
5	MIPI_DSI0_DATA0_P	MIPI_DSI0.DP0	DSI1_D1+	I/O	DSI Interface 1 data lane 1
4	MIPI_DSI0_DATA0_N	MIPI_DSI0.DN0	DSI1_D1-		
8	MIPI_DSI0_DATA1_P	MIPI_DSI0.DP1	DSI1_D2+	O	DSI Interface 1 data lane 2
7	MIPI_DSI0_DATA1_N	MIPI_DSI0.DN1	DSI1_D2-		
11	MIPI_DSI0_DATA2_P	MIPI_DSI0.DP2	DSI1_D3+	O	DSI Interface 1 data lane 3
10	MIPI_DSI0_DATA2_N	MIPI_DSI0.DN2	DSI1_D3-		
14	MIPI_DSI0_DATA3_P	MIPI_DSI0.DP3	DSI1_D4+	O	DSI Interface 1 data lane 4
13	MIPI_DSI0_DATA3_N	MIPI_DSI0.DN3	DSI1_D4-		
18	MIPI_DSI1_CLK_P	MIPI_DSI1.CKP	DSI2_CLK+	O	DSI Interface 2 clock
17	MIPI_DSI1_CLK_N	MIPI_DSI1.CKN	DSI2_CLK-		
21	MIPI_DSI1_DATA0_P	MIPI_DSI1.DP0	DSI2_D1+	I/O	DSI Interface 2 data lane 1
20	MIPI_DSI1_DATA0_N	MIPI_DSI1.DN0	DSI2_D1-		
24	MIPI_DSI1_DATA1_P	MIPI_DSI1.DP1	DSI2_D2+	O	DSI Interface 2 data lane 2
23	MIPI_DSI1_DATA1_N	MIPI_DSI1.DN1	DSI2_D2-		
27	MIPI_DSI1_DATA2_P	MIPI_DSI1.DP2	DSI2_D3+	O	DSI Interface 2 data lane 3
26	MIPI_DSI1_DATA2_N	MIPI_DSI1.DN2	DSI2_D3-		
30	MIPI_DSI1_DATA3_P	MIPI_DSI1.DP3	DSI2_D4+	O	DSI Interface 2 data lane 4
29	MIPI_DSI1_DATA3_N	MIPI_DSI1.DN3	DSI2_D4-		

As the DSI is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Colibri Carrier Board Design Guide as it is not a standard interface.

Table 5-22 DSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	502.5MHz (1.05GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm
Minimum pair to pair spacing	>2x intra-pair spacing
Maximum allowed via	Minimize the number of via in DSI traces

5.6.4 HDMI

The Colibri iMX8X does not have a native HDMI interface. However, there are multiple ways to implement an HDMI interface on the carrier board.

- MIPI/DSI to HDMI converter. Since only a single DSI interface is used for 1080p60 resolution, it is possible to add up to two MIPI/DSI converters to the Colibri iMX8X module.
- LVDS to HDMI converter. For 1080p60, a dual-lane LVDS interface is required. This means, only a single HDMI port is possible. In general, a greater number of differential pair LVDS signals are needed than for a DSI solution.
- Parallel RGB to HDMI converter. If the 18bit parallel RGB is used, the solution would be compatible with other Colibri modules. The resolution is limited to 720p60 due to limitations of the parallel interface on the i.MX 8X.

5.6.5 Analog VGA

The Colibri iMX8X does not have a native Analog VGA interface. However, it is possible to implement a VGA interface on the carrier board using a VGA DAC. The Colibri Evaluation board features a reference design for such a VGA DAC.

5.7 PCI Express

The i.MX 8X SoC features one single lane PCI Express interface. This interface is used for the Wi-Fi module. Even on Colibri iMX8X modules without the wireless module, the PCIe interface is not available on module edge connector pins.

5.8 External Memory Bus

The i.MX 8X SoC does not feature a parallel memory interface. The memory bus signals on the module edge connector are either left unconnected or used for other purposes. See section 3.2 for more information.

5.9 I²C

The i.MX 8X SoC features a total number of ten I²C controllers. Not all of these interfaces are available externally. Some of them are dedicated interfaces with limited function.

- General-purpose I²C with DMA support
  - 4x general-purpose I²C. Three of them are available on the module edge connector, one as standard Colibri I²C. The fourth is used on the module for the audio codec, the GPIO expander, and USB hub (if assembled).
  - 1x I²C interface which is tightly coupled with the Cortex-M4 core)
- Low-speed I²C without DMA support for a dedicated purpose. It could also be used as general-purpose but require the associated PHY (for example, MIPI) to be powered on
  - 2x master I²C for LVDS and MIPI/DSI, all available externally
  - 1x master I²C for MIPI/CSI-2, available externally
  - 1x master I²C for parallel camera input, available externally
- I²C tightly coupled with SCU
  - 1x Dedicated for PMIC, cannot be used externally

The Colibri module standard features only one I²C interface. The rest of the available interfaces are alternate functions of other interface pins. These additional interfaces are not compatible with other Colibri modules. Therefore, it is highly recommended to use the standard I²C interface primarily. For example, the parallel camera interface features dedicated I²C ports. However, to be compatible with the Toradex BSP and other Colibri modules, we recommend using the standard instead.

General-purpose I²C ports features:

- Supports standard and fast mode of operation (0-400KHz), Fm+ (1Mbit/s), and high-speed mode (3.2 MHz).
- System Management Bus (SMBus) compliant specifications
- Master and slave mode (slave mode may not be supported in regular BSP)
- Multi-master support
- Clock stretching support
- 7-bit or 10-bit addressing
- DMA support

There are many low-speed devices, which use I²C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB (System Management Bus) devices.

Table 5-23 I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
194	I2C SDA	MIPI_DSI0_GPIO0_01	ADMA.I2C1.SDA	I/O	Open drain data signal
196	I2C SCL	MIPI_DSI0_GPIO0_00	ADMA.I2C1.SCL	I/O	Open drain data signal

Table 5-24 Alternate DMA I²C Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
127		USB_SS3_TC2	ADMA.I2C1.SDA	I/O	Alternate open-drain data signal for standard port
131	USB Host Over-Current Detect	USB_SS3_TC3			
129	USB Host Power Enable	USB_SS3_TC0	ADMA.I2C1.SCL	I/O	Alternate open-drain clock signal for standard port
133		USB_SS3_TC1			

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
23	UART_A DTR	MIPI_DSI1_GPIO0_01	ADMA.I2C2.SDA	I/O	Open-drain data signal for additional port
138	ADDRESS23	MIPI_DSI1_GPIO0_00	ADMA.I2C2.SCL	I/O	Open-drain clock signal for additional port
25 (X2)					
29	UART_A DSR	CSI_RESET	ADMA.I2C3.SDA	I/O	Open-drain data signal for additional port
44	LCD RGB DE	MCLK_IN1			
37	UART_A RI, Keypad_In<4>	CSI_EN	ADMA.I2C3.SCL	I/O	Open-drain clock signal for additional port
57	LCD RGB Data<16>	SPI3_CS1			

Table 5-25 Tightly coupled M4 I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
6	Analogue Input <1>	ADC_IN1	M40.I2C0.SDA	I/O	Open-drain data signal, **maximum voltage 1.8V**
8	Analogue Input <0>	ADC_IN0	M40.I2C0.SCL	I/O	Open-drain data signal , **maximum voltage 1.8V**

Table 5-26 Dedicated low-speed I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
29	UART_A DSR	CSI_RESET	CI_PI.CSI_I2C.SDA	I/O	Dedicated I²C port for the parallel camera input port
37	UART_A RI, Keypad_In<4>	CSI_EN	CI_PI.CSI_I2C.SCL	I/O	
75	Camera Input MCLK	CSI_MCLK	MIPI_CSI0.I2C0.SDA	I/O	Dedicated I²C port for the MIPI/CSI-2 port
96	Camera Input PCLK	CSI_PCLK	MIPI_CSI0.I2C0.SCL	I/O	
142	ADDRESS21	MIPI_DSI0_I2C0_SDA	MIPI_DSI0.I2C0.SDA	I/O	Dedicated I²C port for the first LVDS and MIPI/DSI port. The pins are available on the SODIMM (X1) and the FFC (X2) connector.
16 (X2)					
140	ADDRESS22	MIPI_DSI0_I2C0_SCL	MIPI_DSI0.I2C0.SCL	I/O	
15 (X2)					
188	ADDRESS16	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	I/O	Dedicated I²C port for the second LVDS and MIPI/DSI port. The pins are available on the SODIMM (X1) and the FFC (X3) connector.
14 (X3)					
186	ADDRESS17	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	I/O	
13 (X3)					

5.9.1 Real-Time Clock (RTC) recommendation

The Colibri iMX8X module features an RTC circuit, which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time-keeping. The RTC is sourced from the VCC_BATT (pin 40) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section **Error! Reference source not found.**). Therefore, a standard l ithium coin cell battery can be drained faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the standard interface (pin

194/196) of the module and source the VCC_BACKUP pin from the 3.3V rail that also sources the main module rail. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board.

5.10 UART

The i.MX 8X SoC features a total number of six UARTs. There are four regular UARTs, of which three are available on the standard Colibri module edge connector pins and therefore are compatible with other Colibri modules. The fourth UART is available as an alternate function and, therefore, not compatible with other modules. Additional to the regular UARTs, the SoC features one UART tightly coupled with the Cortex-M4 core. The last UART is tightly coupled to the System Controller Unit. It is used for the debugging messages of the SCU.

The Colibri UART_A is, according to the Colibri specification, a full-featured UART. The i.MX 8X does not feature the DTR, DSR, DCD, and RI signals. The CTS and RTS signals of this port are only available as an alternate function of the SD card interface signals. Therefore, the UART_A on the Colibri iMX8X only features RX and TX, no other hardware control signals on their standard location. The UART_A is used as a standard debug interface for the Toradex Linux operating systems. Therefore, it is desirable to keep this port accessible for system debugging.

General-purpose UART Features

- Full-duplex, standard non-return-to-zero (NRZ format)
- Programmable baud rates
- Interrupt, DMA, or polled operation.
- Hardware parity generation and checking
- Character length 7 to 10bit
- Programmable 1-bit or 2-bit stop bits
- Idle line, address mark, and receive data match wakeup method
- Automatic address matching to reduce ISR overhead
- IrDA 1.4 support

Table 5-27 UART_A Signal Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
33	UART_A RXD	FLEXCAN2_RX	ADMA.UART3.RX	I	Received Data
35	UART_A TXD	FLEXCAN2_TX	ADMA.UART3.TX	O	Transmitted Data

Table 5-28 UART_B Signal Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
36	UART_B RXD	UART0_RX	ADMA.UART0.RX	I	Received Data
38	UART_B TXD	UART0_TX	ADMA.UART0.TX	O	Transmitted Data
34	UART_B RTS	FLEXCAN0_RX	ADMA.UART0.RTS_B	O	Request to Send
32	UART_B CTS	FLEXCAN0_TX	ADMA.UART0.CTS_B	I	Clear to Send

Table 5-29 UART_C Signal Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
19	UART_C RXD	UART2_TX	ADMA.UART2.TX	I	Received Data
21	UART_C TXD	UART2_RX	ADMA.UART2.RX	O	Transmitted Data

Table 5-30 Signal Pins of additional UART Ports

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
30	PWM<C>	UART1_RX	ADMA.UART1.RX	I	Received Data
28	PWM<B>	UART1_TX	ADMA.UART1.TX	O	Transmitted Data
67	PWM<D>,Camera Input Data<6>	UART1_RTS_B	ADMA.UART1.RTS_B	O	Request to Send
61	LCD RGB Data<17>	UART1_CTS_B	ADMA.UART1.CTS_B	I	Clear to Send
144	ADDRESS20	SCU_GPIO0_00	M40.UART0.RX	I	Received Data, tightly coupled with M4 core, bidirectional level shifter on the module
146	ADDRESS19	SCU_GPIO0_01	M40.UART0.TX	O	Transmitted Data, tightly coupled with M4 core, bidirectional level shifter on the module
36	UART_B RXD	UART0_RX	SCU.UART0.RX	I	Received Data, debug interface of system controller unit, bidirectional level shifter on pin 144
144	ADDRESS20	SCU_GPIO0_00			
38	UART_B TXD	UART0_TX	SCU.UART0.TX	O	Transmitted Data, debug interface of system controller unit, bidirectional level shifter on pin 146
146	ADDRESS19	SCU_GPIO0_01			

These UART ports are only available as alternate functions. Compatibility with other Colibri modules cannot be guaranteed, as they are not standard Colibri module interfaces.

Table 5-31 Alternate UART Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
47	SDCard CLK	USDHC1_CLK	ADMA.UART3.RX	I	Alternate Received Data for UART_A, bidirectional level shifter on pin 144
144	ADDRESS20	SCU_GPIO0_00			
49	SDCard DAT<1>	USDHC1_DATA1	ADMA.UART3.TX	O	Alternate Transmitted Data for UART_A, bidirectional level shifter on pin 146
146	ADDRESS19	SCU_GPIO0_01			
53	SDCard DAT<3>	USDHC1_DATA3	ADMA.UART3.RTS_B	O	Request to Send for UART_A
51	SDCard DAT<2>	USDHC1_DATA2	ADMA.UART3.CTS_B	I	Clear to Send for UART_A

5.11 SPI

The i.MX 8X SoC provides four SPI controllers (which are called Low Power Serial Peripheral Interface, LPSPI in the reference manual). Only three are available on the module edge connector.

One SPI interface is available as the standard Colibri module interface. This interface is compatible with other Colibri modules. The other SPI interfaces are available as alternate functions. These interfaces are incompatible with other Colibri modules. Please use the standard Colibri SPI interface first before using others.

The SPI ports operate at up to 60MHz in master mode and up to 40MHz in slave mode. However, there are exceptions. Some of the additional SPI interface pins are limited to 40MHz in master mode and 20MHz in slave mode. Check the NXP datasheet for more information.

Features:

- Up to 60 Mbps in master mode
- Up to 40 Mbps in slave mode
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable

- Simultaneous receive and transmit (1-bit mode)
- Wakeup function on receiving data match

Each SPI channel supports four different modes of the SPI protocol:

Table 5-32 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock is positive polarity, and the data is latched on the positive edge of the SCK
1	0	1	The clock is positive polarity, and the data is latched on the negative edge of the SCK
2	1	0	The clock is negative polarity, and the data is latched on the positive edge of the SCK
4	1	1	The clock is negative polarity, and the data is latched on the negative edge of the SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some displays require configuration over SPI before being driven via the RGB or LVDS interface.

Table 5-33 SPI Signals (Colibri family compatible interface)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
92	SPI TXD	SPI2_SDO	ADMA.SPI2.SDO	O	Master Output, Slave Input
90	SPI RXD	SPI2_SDI	ADMA.SPI2.SDI	I	Master Input, Slave Output
86	SPI CS	SPI2_CS0	ADMA.SPI2.CS0	O	Slave Select
88	SPI CLK	SPI2_SCK	ADMA.SPI2.SCK	O	Serial Clock

Table 5-34 SPI Signals (additional and incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
66	LCD RGB Data<14>	SPI3_SDO	ADMA.SPI3.SDO	O	Master Output, Slave Input
64	LCD RGB Data<15>	SPI3_SDI	ADMA.SPI3.SDI	I	Master Input, Slave Output
68	LCD RGB HSYNC	SPI3_CS0	ADMA.SPI3.CS0	O	Slave Select 0
57	LCD RGB Data<16>	SPI3_CS1	ADMA.SPI3.CS1	O	Slave Select 1
54	LCD RGB Data<13>	SPI3_SCK	ADMA.SPI3.SCK	O	Serial Clock
75	Camera Input MCLK	CSI_MCLK	ADMA.SPI1.SDO	O	Master Output, Slave Input
12 (X3)		CSI_MCLK			
103	Camera Input Data<3>	SAI0_TXD			
37	UART_A RI, Keypad_In<4>	CSI_EN	ADMA.SPI1.SDI	I	Master Input, Slave Output
79	Camera Input Data<4>	SAI0_TXC			
29	UART_A DSR	CSI_RESET	ADMA.SPI1.CS0	O	Slave Select 0
97	Camera Input Data<5>	SAI0_RXD			
25	UART_A CTS, Keypad_In<0>	SAI1_RXD	ADMA.SPI1.CS1	O	Slave Select 1
96	Camera Input PCLK	CSI_PCLK	ADMA.SPI1.SCK	O	Serial Clock
101	Camera Input Data<2>	SAI0_TXFS			

Table 5-35 Alternate Signals of main SPI (incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
56	LCD RGB PCLK	MCLK_OUT0	ADMA.SPI2.SDO	O	Alternate Master Output, Slave Input
76	LCD RGB Data<0>	USDHC1_WP	ADMA.SPI2.SDI	I	Alternate Master Input, Slave Output
82	LCD RGB VSYNC	MCLK_IN0			
31	UART_A DCD	USDHC1_CD_B	ADMA.SPI2.CS0	O	Alternate Slave Select 0
57	LCD RGB Data<16>	SPI3_CS1			
101	Camera Input Data<2>	SAI0_TXFS	ADMA.SPI2.CS1	O	Additional Slave Select 1
44	LCD RGB DE	MCLK_IN1 USDHC1_RESET_B	ADMA.SPI2.SCK	O	Alternate Serial Clock

5.12 PWM (Pulse Width Modulation)

The i.MX 8X features a four-channel general-purpose Pulse Width Modulator (PWM). It has a 16-bit counter and is optimized to generate simple sound samples and generate tones. It has a 16-bit resolution and a 4-level deep FIFO available to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock. Due to the SoC's multiplexing limitations, only three of the four PWM output signals are available on the module edge connector as Colibri standard PWM signals. The fourth general-purpose PWM is available as an alternate function of the parallel LCD interface.

Additional to the general-purpose PWM, the i.MX 8X features dedicated PWM generators for the Parallel LCD as well as the LVDS and MIPI/DSI interfaces. These PWM outputs are intended to be used for driving the backlight intensity of a liquid crystal display. One of these dedicated PWMs is available on one of the standard Colibri PWM pins. The other dedicated PWM signals are available as an alternate function.

Table 5-36 PWM Interface Signals

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Remarks
59	PWM<A>,Camera Input Data<7>	SPI0_CS1	ADMA.LCD_PWM0	O	PWM Output 1 (dedicated LCD PWM)
28	PWM<B>	UART1_TX	LSIO.PWM0.OUT	O	PWM Output 2 (general purpose PWM)
30	PWM<C>	UART1_RX	LSIO.PWM1.OUT	O	PWM Output 3 (general purpose PWM)
67	PWM<D>,Camera Input Data<6>	UART1_RTS_B	LSIO.PWM2.OUT	O	PWM Output 4 (general purpose PWM)

Table 5-37 Locations of additional PWM Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Remarks
61	LCD RGB Data<17>	UART1_CTS_B	LSIO.PWM3.OUT	O	General-purpose PWM
196	I2C SCL	MIPI_DSI0_GPIO0_00	MIPI_DSI0.PWM0.OUT	O	Dedicated LVDS and DSI PWM
138	ADDRESS23	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Dedicated LVDS and DSI PWM
25 (X2)					

Besides the standard PWM interfaces, the i.MX 8X features a Timer PWM Modules (TPM), tightly coupled to f the Cortex M4 core. The TMB is based on a simple timer known for many years from the HCS08 8-bit microcontrollers. Besides generating PWM signals, it can also be used for input-capture and output-compare functions. The TPM is dedicated to the M4 core. However, there is a FlexTimer (FTM) module for the main cores. The FTM builds upon the TPM, but enhances it by additional dead time insertion hardware, fault control input, signed up counter function, enhancing the triggering functionality, and allowing the polarity and initialization to be controlled. The FTM and the TPM for the M4 core are available on the module edge connector as alternate functions.

Table 5-38 TPM and FTM Interface Signals (incompatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Remarks
4	Analogue Input <2>	ADC_IN4	M40.TPM0.CH0	I/O	Timer PWM Module output tightly coupled with the Cortex M4 core; **maximum voltage 1.8V**
2	Analogue Input <3>	ADC_IN5	M40.TPM0.CH1	I/O	
19	UART_C RXD	UART2_RX	ADMA.FTM.CH0	I/O	Flex Timer Module channel signals. It can be used with all the CPU cores
21	UART_C TXD	UART2_TX	ADMA.FTM.CH1	I/O	
63	PS2 SCL1	FLEXCAN1_RX	ADMA.FTM.CH2	I/O	

5.13 OWR (One-Wire)

The Colibri iMX8X does not feature a One-Wire interface.

5.14 SD/MMC

The i.MX 8X SoC provides two SDIO interfaces; one is used internally for the eMMC Flash, and the other is available on the module edge connector Pins as a standard interface. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, and eMMC devices.

The Colibri iMX8X supports UHS-I, which allows up to 104 Mbyte/s transfer speed on its standard SD card interface. However, UHS-I requires a 1.8V IO level, which is not in the Colibri module specification. Since the 1.8V capability is not mandatory in the Colibri module specification, other modules may support only the 3.3V logic level. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interface is used in the 1.8V mode, it is recommended to remove the pull-up resistors on the carrier board. The i.MX 8X features internal pull-up resistors, which can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MByte/s	3.3V	Colibri Standard
High Speed	50 MHz	25 MByte/s	3.3V	
SDR12	25 MHz	12.5 MByte/s	1.8V	UHS-I May not compatible with other modules
SDR25	50 MHz	25 MByte/s	1.8V	
DDR50	50 MHz	50 MByte/s	1.8V	
SDR50	100 MHz	50 MByte/s	1.8V	
SDR104	208 MHz	104 MByte/s	1.8V	

Features:

- Supports SD Memory Card Specification 2.0 and 3.0
- Supports SDIO Card Specification Version 2.0 and 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, 5.0, and 5.1
- Supports addressing larger capacity SD 3.0 or SDXC cards up to 2 TByte
- Supports SPI mode
- Supports SD UHS-I mode (up to 208MHz) with a 1.8V IO voltage level.

Table 5-39 Colibri SD/MMC Signal Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
190	SDCard CMD	USDHC1_CMD	CONN.USDHC1.CMD	I/O	Command
192	SDCard DAT<0>	USDHC1_DATA0	CONN.USDHC1.DATA0	I/O	Serial Data 0
49	SDCard DAT<1>	USDHC1_DATA1	CONN.USDHC1.DATA1	I/O	Serial Data 1
51	SDCard DAT<2>	USDHC1_DATA2	CONN.USDHC1.DATA2	I/O	Serial Data 2
53	SDCard DAT<3>	USDHC1_DATA3	CONN.USDHC1.DATA3	I/O	Serial Data 3
47	SDCard CLK	USDHC1_CLK	CONN.USDHC1.CLK	O	Serial Clock
43	WAKEUP Source<0>, SDCard CardDetect	QSPI0A_DATA0	LSIO.GPIO3.IO09	I	Card Detect (regular GPIO)

Due to limitations of the multiplexing options of the i.MX 8X, there is only a regular GPIO pin placed on pin 43, which is reserved as a card-detect signal. Even though the dedicated card-detect signal of the SD card interface is available as an alternate function on the RGB interface and the UART_A, it is recommended to use the GPIO on pin 43 as card detect. This makes sure the carrier board design is compatible with other Colibri modules, and the SD card interface works out of the box with our standard board support package.

Table 5-40 Additional SD/MMC Signal Pins (usually not required, not compatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
135	SPDIF_IN	ENET0_RGMII_RXD3	CONN.USDHC1.DATA3	I/O	Alternate pin for serial data 3
85	Camera Input Data<8>, Keypad_Out<4>	ENET0_RGMII_RXC	CONN.USDHC1.CLK	O	Alternate pin for the serial clock
31	UART_A DCD	USDHC1_CD_B	CONN.USDHC1.CD_B	I	Dedicated card detect signal.
57	LCD RGB Data<16>	ENET0_RGMII_TXD2			
44	LCD RGB DE	USDHC1_RESET_B	CONN.USDHC1.RESET_B	O	Card reset signal
76	LCD RGB Data<0>	USDHC1_WP	CONN.USDHC1.WP	I	Write-protect

5.15 Analogue Audio

The Colibri iMX8X offers analog audio input and output channels. The module features an NXP SGTL5000 chip to provide the analog audio interface. The SGTL5000 is connected over I2S (SAI0) with the i.MX 7 SoC. Please consult the NXP SGTL5000 datasheet for more information.

Table 5-41 Analogue Audio Interface Pins

X1 Pin #	Colibri STD Function	I/O	Description	Pin on the SGTL5000 (20pin QFN)
1	MIC_IN	I	Microphone input	10
3	MIC_GND		Microphone pseudo-ground. Possible to connect to GND. Controlled by GPIO3.IO06 (ball MIPI_CSI0_I2C0_SDA)	
5	LINEIN_L	I	Left Line Input	9
7	LINEIN_R	I	Right Line Input	8
15	HEADPHONE_L	O	Headphone Left Output	4
17	HEADPHONE_R	O	Headphone Right Output	1
13	HEADPHONE_GND		Headphone pseudo-ground (do not connect to ground!)	2

5.16 Audio Codec Interface

The i.MX 8X SoC features four Synchronous Audio Interfaces (SAI). Two of them can transmit and receive audio streams, while the other two interfaces can only receive. The Colibri module does not feature an audio codec interface as standard. Nevertheless, all four digital audio interfaces are available on the module edge connector as an alternate function. However, one of the full-featured interfaces is used for the on-module SGTL5000 audio codec. The interface is still available on the external module edge pin connector but can only be used if the internal codec is not in use.

The interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS). The interfaces can be used to connect an external audio codec.

Table 5-42 Synchronous Audio Interface (incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
27	UART_A RTS	SAI1_RXC	ADMA.SAI1.TXC	I/O	Transmit Clock
34	UART_B RTS	FLEXCAN0_RX			
32	UART_B CTS	FLEXCAN0_TX	ADMA.SAI1.TXFS	I/O	Transmit Frame Sync
100	Keypad_Out<1>	SAI1_RXFS			
59	PWM<A>,Camera Input Data<7>	SPI0_CS1	ADMA.SAI1.TXD	O	Data Transmit
63	PS2 SCL1	FLEXCAN1_RX			
79	Camera Input Data<4>	SAI0_TXC			
27	UART_A RTS	SAI1_RXC	ADMA.SAI1.RXC	I/O	Receive Clock
35	UART_A TXD	FLEXCAN2_TX			
103	Camera Input Data<3>	SAI0_TXD			
33	UART_A RXD	FLEXCAN2_RX	ADMA.SAI1.RXFS	I/O	Receive Frame Sync
97	Camera Input Data<5>	SAI0_RXD			
100	Keypad_Out<1>	SAI1_RXFS			
25	UART_A CTS, Keypad_In<0>	SAI1_RXD	ADMA.SAI1.RXD	I	Data Receive
55	PS2 SDA1	FLEXCAN1_TX			

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
34	UART_B RTS	FLEXCAN0_RX	ADMA.SAI2.RXC	I/O	Receive Clock
97	Camera Input Data<5>	CSI_D03			
59	PWM<A>,Camera Input Data<7>	CSI_D05	ADMA.SAI2.RXFS	I/O	Receive Frame Sync
63	PS2 SCL1	FLEXCAN1_RX			
32	UART_B CTS	FLEXCAN0_TX	ADMA.SAI2.RXD	I	Data Receive
67	PWM<D>,Camera Input Data<6>	CSI_D04			
55	PS2 SDA1	FLEXCAN1_TX	ADMA.SAI3.RXC	I/O	Receive Clock
85	Camera Input Data<8>, Keypad_Out<4>	CSI_D06			
35	UART_A TXD	FLEXCAN2_TX	ADMA.SAI3.RXFS	I/O	Receive Frame Sync
94	Camera Input HSYNC	CSI_HSYNC			
33	UART_A RXD	FLEXCAN2_RX	ADMA.SAI3.RXD	I	Data Receive
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_D07			
79	Camera Input Data<4>	SAI0_TXC	ADMA.SAI0.TXC	I/O	Transmit Clock, only available if the internal codec is not in use
101	Camera Input Data<2>	SAI0_TXFS	ADMA.SAI0.TXFS	I/O	Transmit Frame Sync, only available if the internal codec is not in use
103	Camera Input Data<3>	SAI0_TXD	ADMA.SAI0.TXD	O	Data Transmit, only available if the internal codec is not in use
59	PWM<A>,Camera Input Data<7>	SPI0_CS1	ADMA.SAI0.RXC	I/O	Receive Clock, only available if the internal codec is not in use
101	Camera Input Data<2>	CSI_D00			
25	UART_A CTS, Keypad_In<0>	SAI1_RXD	ADMA.SAI0.RXFS	I/O	Receive Frame Sync, only available if the internal codec is not in use
79	Camera Input Data<4>	CSI_D02			
97	Camera Input Data<5>	SAI0_RXD	ADMA.SAI0.RXD	I	Data Receive, only available if the internal codec is not in use
103	Camera Input Data<3>	CSI_D01			
82	LCD RGB VSYNC	MCLK_IN0	ADMA.ACM.MCLK_IN0	I	Audio Master Clock Input
44	LCD RGB DE	MCLK_IN1	ADMA.ACM.MCLK_IN1	I	Audio Master Clock Input
56	LCD RGB PCLK	MCLK_OUT0	ADMA.ACM.MCLK_OUT0	O	Audio Master Clock Output
68	LCD RGB HSYNC	SPI3_CS0	ADMA.ACM.MCLK_OUT1	O	Audio Master Clock Output

5.16.1 Digital Audio Port used as I²S

The following signals are used for the I²S interface:

Table 5-43 Digital Audio port used as Master I²S

i.MX 8X Function	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.TXD	SDIN	O	Serial Data Output from i.MX 8X SoC
SAIx.RXD	SDOUT	I	Serial Data Input to i.MX 8X SoC
SAIx.TXFS	WS	O	Word Select, also known as Field Select or LRCLK
SAIx.TXC	SCK	O	Serial Continuous Clock

Table 5-44 Digital Audio port used as Slave I²S

i.MX 8X Function	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.TXD	SDOUT	I	Serial Data Input to i.MX 8X SoC
SAIx.RXD	SDIN	O	Serial Data Output from i.MX 8X SoC
SAIx.TXFS	WS	I	Word Select, also known as Field Select or LRCLK
SAIx.TXC	SCK	I	Serial Continuous Clock

The audio codecs require a master clock input and often an I²C interface for control. Any of the available I²C interfaces can be used (see section 0). There is a dedicated audio master clock input and output that can be used according to the codec's need.

5.16.2 Digital Audio Port used as AC'97

The SAI interface can be configured as an AC'97 compatible interface. The AC'97 Audio interface does not require an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec requires a master reference clock. There are dedicated audio master clock outputs, which can be used for this purpose. However, it is also possible to use a separate crystal/oscillator. Please take care of the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host (e.g., i.MX 8X SoC) and not to the signal direction.

Table 5-45 Digital Audio port used as AC'97

i.MX 8X Function	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.TXD	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 8X
SAIx.RXD	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 8X
SAIx.TXFS	SYNC	O	AC'97 Audio Sync
SAIx.TXC	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.17 Medium Quality Sound (MQS)

The medium quality sound interface can be used to generate medium quality audio via a standard GPIO. The PWM output signal does not require an external DAC or codec chip. The advantage over using the high-quality analog audio output of the on-module SGTL5000 is the option to use a simple switching power amplifier circuit (Class-D amplifier).

SAI1 sources the MQS with two-channel 16-bit 44.1 kHz or 48 kHz audio signals, which is basically an I²S signal. Since this is a different SAI channel used by the on-module audio codec, it is possible to use MQS simultaneous with the module's analog audio outputs. The signal-to-noise ratio (SNR) is expected to be no more than 20 dB for signals below 10 kHz. For signals with higher frequencies, the SNR is even worse.

Table 5-46 MQS Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
38	UART_B TXD	UART0_TX	mqs.LEFT	O	Left MQS Channel
50	LCD RGB Data<11>	SPDIF0_TX			
192	SDCard DAT<0>	USDHC1_DATA0			
36	UART_B RXD	UART0_RX	mqs.RIGHT	O	Right MQS Channel
74	LCD RGB Data<10>	SPDIF0_RX			
190	SDCard CMD	USDHC1_CMD			

5.18 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with various serial audio devices, including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Colibri module standard.

Features:
- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 6 transmitters and up to 4 receivers at the module edge connector available
- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20, or 24-bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-47 ESAI Signal Pins (incompatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
58	LCD RGB Data<3>	ESAI0_SCKT	ADMA.ESAI0.SCKT	I/O	TX serial bit clock
70	LCD RGB Data<1>	ESAI0_FST	ADMA.ESAI0.FST	I/O	Frame sync for transmitters and receivers in the synchronous mode and the transmitters only in asynchronous mode
56	LCD RGB PCLK	MCLK_OUT0	ADMA.ESAI0.TX_HF_CLK	I/O	TX high-frequency clock
78	LCD RGB Data<4>	ESAI0_TX0	ADMA.ESAI0.TX0	I/O	TX data 0
72	LCD RGB Data<5>	ESAI0_TX1	ADMA.ESAI0.TX1	I/O	TX data 1
80	LCD RGB Data<6>	ESAI0_TX2_RX3	ADMA.ESAI0.TX2_RX3	I/O	TX data 2 or RX data 3
46	LCD RGB Data<7>	ESAI0_TX3_RX2	ADMA.ESAI0.TX3_RX2	I/O	TX data 3 or RX data 2
62	LCD RGB Data<8>	ESAI0_TX4_RX1	ADMA.ESAI0.TX4_RX1	I/O	TX data 4 or RX data 1
48	LCD RGB Data<9>	ESAI0_TX5_RX0	ADMA.ESAI0.TX5_RX0	I/O	TX data 5 or RX data 0
60	LCD RGB Data<2>	ESAI0_SCKR	ADMA.ESAI0.SCKR	I/O	RX serial bit clock
76	LCD RGB Data<0>	ESAI0_FSR	ADMA.ESAI0.FSR	I/O	RX frame sync signal in asynchronous mode

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
82	LCD RGB VSYNC	MCLK_IN0	ADMA.ESAI0.RX_HF_CLK	I/O	RX high-frequency clock

5.19 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format data. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. The S/PDIF signals are only available as an alternate function. Therefore the interface is not compatible with other modules.

Features:

- Input sampling rate measurement
- CD-Text
- S/PDIF receiver to S/PDIF transmitter bypass mode
- IEC 60958 consumer format
- Sampling rates from 32kHz to 192kHz

Table 5-48 S/PDIF Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
50	LCD RGB Data<11>	SPDIF0_TX	ADMA.SPDIF0.TX	O	Serial data output
74	LCD RGB Data<10>	SPDIF0_RX	ADMA.SPDIF0.RX	I	Serial data input
52	LCD RGB Data<12>	SPDIF0_EXT_CLK	ADMA.SPDIF0.EXT_CLK	I	External clock input

5.20 Touch Panel Interface

The Colibri iMX8X provides a 4-wire resistive touch interface using the Analog Device AD7879-1 Touchscreen Controller. It is connected with the i.MX 8X SoC via the first I²C interface (ADMA.I2C0). This I²C interface is also connected to the on-module audio codec and on modules with wireless features to the USB hub and the GPIO expander. The AD7879-1 does not support a 5-wire operation mode. Please consult the Analog Device AD7879-1 documentation for more information.

Table 5-49 Touch Interface Pins

X1 Pin#	Colibri STD Function	AD7879 Pin#	AD7879 Pin Name	I/O	Description
14	TSPX	A3	X+	I/O	X+ (4-wire)
16	TSMX	C3	X-	I/O	X- (4-wire)
18	TSPY	B3	Y+	I/O	Y+ (4-wire)
20	TSMY	D3	Y-	I/O	Y- (4-wire)

5.21 Analogue Inputs

The analog inputs are provided by the NXP i.MX 8X SoC itself. The SoC features one ADCs with six-channel inputs. Only four of these six channels are available on the module edge connector. Pay attention, the input voltage range is only 1.8V and not 3.3V as on other Colibri modules. There are 1kΩ series resistors placed in the ADC lines on the module to protect the SoC input.

Features

- 12-bit ADC
- Linear successive approximation algorithm
- 0 to 1.8V (full scale)
- DMA support
- Trigger detection
- Automatic compare for less-than, greater-than, within-range, or out-of-range with “store on true” and “repeat until true” option
- Interrupt support

Table 5-50 Analogue Inputs Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
8	Analogue Input <0>	ADC_IN0	ADMA.ADC.IN0	I	Standard analog input 1 **maximum voltage 1.8V**
6	Analogue Input <1>	ADC_IN1	ADMA.ADC.IN1	I	Standard analog input 2 **maximum voltage 1.8V**
4	Analogue Input <2>	ADC_IN4	ADMA.ADC.IN4	I	Standard analog input 3 **maximum voltage 1.8V**
2	Analogue Input <3>	ADC_IN5	ADMA.ADC.IN5	I	Standard analog input 4 **maximum voltage 1.8V**

5.22 Camera Interface

The i.MX 8X SoC features a single Imagining Subsystem with three input sources and stores streams into the memory. The subsystem consists of the Imaging Sensor Interface (ISI), MJPEG Encoder, and Decoder. The three input sources are the MIPI CSI-2, the parallel camera input port, and an internal link from the Display Controller.

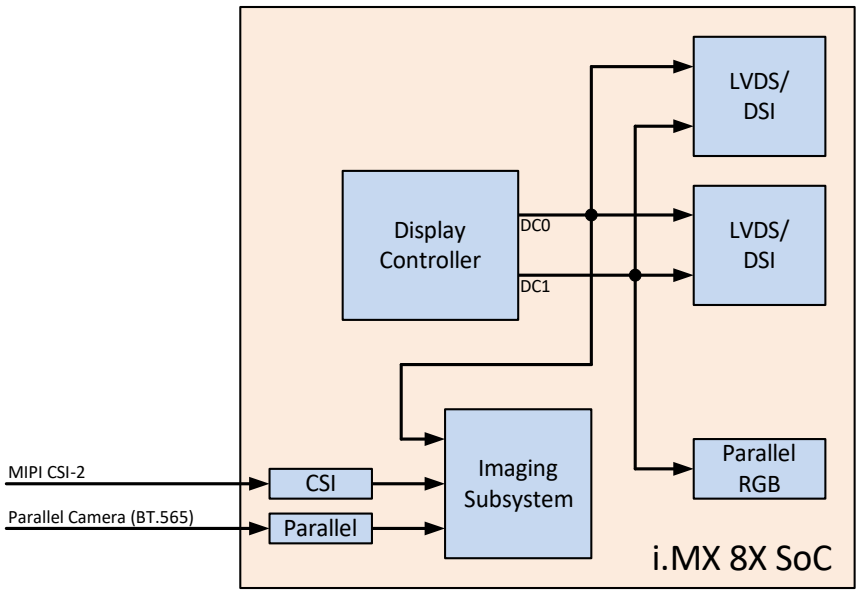

Figure 12: Display and Imaging Block Diagram

5.22.1 Parallel Camera Interface

The i.MX 8X SoC itself features one parallel camera interface called Parallel Capture Interface (PI_CI). In some parts of the NXP documentation, the term CMOS sensor interface (CSI) is used. It is important not to confuse this name with the interface standard MIPI/CSI-2, a serial camera interface.

The camera interface on the i.MX 8X SoC features up to 10 data bits. However, only 8bit BT.656 is compatible with other Colibri modules. The remaining two bits are located as an alternate function of the camera sync signals.

Features:

- Raw (Bayer), RGB, YUV, YCbCr input
- Support for CCIR656 (BT.656)
- Maximum pixel clock frequency 150 MHz
- 8/10-bit parallel video interface
- Dedicated synchronization signals (VSYNC, HSYNC) or embedded in the data stream (BT.656)

Table 5-51 Parallel Camera Interface Pins

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8 Function	I/O	Description
101	Camera Input Data<2>	CSI_D00	CI_PI.CSI_D02	I	Camera pixel data
103	Camera Input Data<3>	CSI_D01	CI_PI.CSI_D03	I	Camera pixel data
79	Camera Input Data<4>	CSI_D02	CI_PI.CSI_D04	I	Camera pixel data
97	Camera Input Data<5>	CSI_D03	CI_PI.CSI_D05	I	Camera pixel data
67	PWM<D>, Camera Input Data<6>	CSI_D04	CI_PI.CSI_D06	I	Camera pixel data
59	PWM<A>, Camera Input Data<7>	CSI_D05	CI_PI.CSI_D07	I	Camera pixel data
85	Camera Input Data<8>, Keypad_Out<4>	CSI_D06	CI_PI.CSI_D08	I	Camera pixel data
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	CSI_D07	CI_PI.CSI_D09	I	Camera pixel data
96	Camera Input PCLK	CSI_PCLK	CI_PI.CSI_PCLK	I	Camera pixel clock
94	Camera Input HSYNC	CSI_HSYNC	CI_PI.CSI_HSYNC	I	Camera horizontal sync
81	Camera Input VSYNC	CSI_VSYNC	CI_PI.CSI_VSYNC	I	Camera vertical sync
75	Camera Input MCLK	CSI_MCLK	CI_PI.CSI_MCLK	O	Camera reference clock output

The camera modules often require an additional I²C interface for control purposes. Any available I²C interface can be used (see section 0). The following table shows the additional signals for the CSI camera interface for up to 10-bit connections. Please be aware that these signals are alternate functions and are incompatible with other modules.

Table 5-52 Additional Parallel Camera Interface Pins (not compatible with other modules)

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
94	Camera Input HSYNC	CSI_HSYNC	CI_PI.CSI_D00	I	Additional camera pixel data for 10bit
81	Camera Input VSYNC	CSI_VSYNC	CI_PI.CSI_D01	I	Additional camera pixel data for 10bit
37	UART_A RI, Keypad_In<4>	CSI_EN	CI_PI.CSI_EN	O	Camera enables

X1 Pin#	Colibri Standard Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
29	UART_A DSR	CSI_RESET	CI_PI.CSI_RESET	O	Camera reset
37	UART_A RI, Keypad_In<4>	CSI_EN	CI_PI.CSI_I2C.SCL	I/O	Dedicated I^2C interface for the parallel camera
29	UART_A DSR	CSI_RESET	CI_PI.CSI_I2C.SDA	I/O	

Table 5-53 Camera Interface Color Pin Mapping

iMX /X Port Name	Bayer 10bit Generic	BT656/ YUV 8bit/ CCIR656	RGB888 8bit 3 cycle	YCbCr 8bit 2 cycle
CSI_D00	D0			
CSI_D01	D1			
CSI_D02	D2	Y/C0	R/G/B0	Y/C0
CSI_D03	D3	Y/C1	R/G/B1	Y/C1
CSI_D04	D4	Y/C2	R/G/B2	Y/C2
CSI_D05	D5	Y/C3	R/G/B3	Y/C3
CSI_D06	D6	Y/C4	R/G/B4	Y/C4
CSI_D07	D7	Y/C5	R/G/B5	Y/C5
CSI_D08	D8	Y/C6	R/G/B6	Y/C6
CSI_D09	D9	Y/C7	R/G/B7	Y/C7

5.22.2 Camera Serial Interface (MIPI CSI-2)

The NXP i.MX 8X supports one quad lane MIPI CSI-2 interface for connecting compatible cameras. The interface is compatible with single and dual lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV, and RAW color space definitions. 24-bit down to 6-bit per pixel are supported.

The MIPI CSI-2 signals are located on a dedicated FFC connector. This connector's pinout is compatible with the MIPI/CSI-2 connector found on the Apalis evaluation board and Ixora carrier board for the Apalis module.

Features:

- Scalable data lane support, 1 to 4 data lanes
- Up to 1.5Gbps per lane, providing 4K30 capability for the four lanes
- Supports 10Mbps data rate in low power modes
- Implements all three CSI-2 MIPI layers (pixel to byte backing, low-level protocol, and lane management)
- Unidirectional master operation supported

As the CSI is a high-speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Colibri Carrier Board Design Guide as this interface is not in the Colibri standard. Please find the related information in the table below.

Table 5-54 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single-ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-55 MIPI CSI-2 Interface Pins (on additional FFC)

X3 Pin#	i.MX 8X Ball Name	i.MX 8X Function	MIPI/CSI Function	I/O	Description
9	MIPI_CSI0_CLK_P	MIPI_CSI0.CKP	CSI1_CLK+	I	CSI interface 1 clock
8	MIPI_CSI0_CLK_N	MIPI_CSI0.CKN	CSI1_CLK-		
3	MIPI_CSI0_DATA0_P	MIPI_CSI0.DP0	CSI1_D1+	I/O	CSI interface 1 data lane 1
2	MIPI_CSI0_DATA0_N	MIPI_CSI0.DN0	CSI1_D1-		
6	MIPI_CSI0_DATA1_P	MIPI_CSI0.DP1	CSI1_D2+	I	CSI interface 1 data lane 2
5	MIPI_CSI0_DATA1_N	MIPI_CSI0.DN1	CSI1_D2-		
17	MIPI_CSI0_DATA2_P	MIPI_CSI0.DP2	CSI1_D3+	I	CSI interface 1 data lane 3
16	MIPI_CSI0_DATA2_N	MIPI_CSI0.DN2	CSI1_D3-		
20	MIPI_CSI0_DATA3_P	MIPI_CSI0.DP3	CSI1_D4+	I	CSI interface 1 data lane 4
19	MIPI_CSI0_DATA3_N	MIPI_CSI0.DN3	CSI1_D4-		
12	CSI_MCLK	CI_PI.CSI_MCLK		O	Master clock output. **This pin is shared with the SODIMM connector pin 75!**
13	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL		O	I^2C control interface for the camera **This pin is shared with the SODIMM connector pin 186 and 188!**
14	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA		I/O	
11	QSPI0A_SS1_B	LSIO.GPIO3.IO15		I/O	GPIO, intended to be used as a camera reset. **This pin is shared with the SODIMM connector pin 89!**
22	QSPI0A_SS0_B	LSIO.GPIO3.IO14		I/O	GPIO for the camera. **This pin is shared with the SODIMM connector pin 77!**
23	QSPI0A_SCLK	LSIO.GPIO3.IO16		I/O	GPIO for the camera. **This pin is shared with the SODIMM connector pin 93!**

5.23 Keypad

You can use any free GPIOs to realize a matrix keypad interface. Such a software solution does not come with any additional hardware support. This is the preferred solution if a carrier board needs to be compatible with different Colibri modules.

Additionally, the i.MX 8X SoC features a keyboard controller with hardware support. As the keyboard controller is only available as an alternate function, this interface is incompatible with

other Colibri modules. It can only be used if the required pins are not being used for their primary function.

The keyboard controller eliminates the requirement for de-bounce capacitors and pull-up resistors. It can handle up to two buttons being pressed without the need for de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 4 by 4.

Features:

- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- 2-point and 3-point key-matrix supported

Table 5-56 Keyboard Matrix Interface Signals

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
95	RDY	QSPI0B_SCLK	LSIO.KPP0.COL0	O	Keyboard column 0
99	nPWE	QSPI0B_DATA0	LSIO.KPP0.COL1	O	Keyboard column 1
105	nCS0	QSPI0B_DATA1	LSIO.KPP0.COL2	O	Keyboard column 2
107	nCS1	QSPI0B_DATA2	LSIO.KPP0.COL3	O	Keyboard column 3
98	Camera Input Data<1>	QSPI0B_DATA3	LSIO.KPP0.ROW0	I	Keyboard row 0
102		QSPI0B_DQS	LSIO.KPP0.ROW1	I	Keyboard row 1
104		QSPI0B_SS0_B	LSIO.KPP0.ROW2	I	Keyboard row 2
106	nCS2	QSPI0B_SS1_B	LSIO.KPP0.ROW3	I	Keyboard row 3

5.24 Controller Area Network (CAN)

The NXP i.MX 8X SoC Flexible Controller Area Network (FlexCAN) peripheral implements the CAN protocol according to the CAN 2.0B specifications and ISO11898-1 standard. The interface fully supports CAN-FD (CAN with Flexible Data rate). It features a buffer for up to 64 messages and supports standard and extended message frames.

The CAN interface is not part of the standard Colibri interfaces, and therefore, it is incompatible with the complete Colibri module family. However, the CAN interface located at pin 63/55 is compatible with the Colibri iMX6, the Colibri iMX6ULL, the Colibri iMX7, and the Colibri VFxx modules. Therefore, whenever only one CAN interface is required, it is recommended to use the one available at pin 63/55. Additionally, the CAN interface on pin 34/32 is compatible with the Colibri iMX6ULL, but not with the rest of the Colibri modules. For more information, check the Toradex Pinout Designer Tool.

Features:

- Full implementation of CAN-FD protocol specification
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight-byte data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free-running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-57 CAN Signal Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
63	PS2 SCL1	FLEXCAN1_RX	ADMA.FLEXCAN1.RX	I	CAN receive pin, compatible with Colibri iMX6, iMX6ULL, iMX7, and VFxx
19	UART_C RXD	UART2_RX			Alternate CAN receive pin
55	PS2 SDA1	FLEXCAN1_TX	ADMA.FLEXCAN1.TX	O	CAN transmit pin, compatible with Colibri iMX6, iMX6ULL, iMX7, and VFxx
21	UART_C TXD	UART2_TX			Alternate CAN transmit pin
34	UART_B RTS	FLEXCAN0_RX	ADMA.FLEXCAN0.RX	I	CAN receive pin, compatible with Colibri iMX6ULL
36	UART_B RXD	UART0_RX			Alternate CAN receive pin
32	UART_B CTS	FLEXCAN0_TX	ADMA.FLEXCAN0.TX	O	CAN transmit pin, compatible with Colibri iMX6ULL
38	UART_B TXD	UART0_TX			Alternate CAN transmit pin
33	UART_A RXD	FLEXCAN2_RX	ADMA.FLEXCAN2.RX	I	CAN receive pin
35	UART_A TXD	FLEXCAN2_TX	ADMA.FLEXCAN2.TX	O	CAN transmit pin

5.25 Flexible SPI Controller (FlexSPI)

Additional to the regular SPI controller (which is called LPSPI in the NXP documentation), the i.MX 8X features a Flexible SPI Controller (FlexSPI). The controller supports single, dual, quad, and octal mode data transfer. It can be used for interfacing NAND and NOR flashes with QuadSPI interfaces. Besides that, it can also be used for interfacing HyperBus and FPGA devices.

Features

- Various flash vendor devices supported
- Double Data Rate (DDR) and Single Data Rate (SDR) supported
- Single, dual, quad, and octal mode
- DMA support
- Execute in place (XiP) possible

Table 5-58 QuadSPI Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
77		QSPI0A_SS0_B	LSIO.QSPI0A.SS0_B	O	Chip Select 0
22 (X3)					
89	nWE	QSPI0A_SS1_B	LSIO.QSPI0A.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
11 (X3)					
93	RDnWR	QSPI0A_SCLK	LSIO.QSPI0A.SCLK	O	Serial Clock
23 (X3)					
43	WAKEUP Source<0>, SDCard CardDetect	QSPI0A_DATA0	LSIO.QSPI0A.DATA0	I/O	Serial I/O for command, address, and data
45	WAKEUP Source<1>	QSPI0A_DATA1	LSIO.QSPI0A.DATA1	I/O	Serial I/O for command, address, and data
69	PS2 SCL2	QSPI0A_DATA2	LSIO.QSPI0A.DATA2	I/O	Serial I/O for command, address, and data
71	Camera Input Data<0>, LCD Back-Light GPIO	QSPI0A_DATA3	LSIO.QSPI0A.DATA3	I/O	Serial I/O for command, address, and data
73		QSPI0A_DQS	LSIO.QSPI0A.DQS	I	Data Strobe signal, required on some high-speed DDR devices
104		QSPI0B_SS0_B	LSIO.QSPI0B.SS0_B	O	Chip Select 0
106	nCS2	QSPI0B_SS1_B	LSIO.QSPI0B.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
95	RDY	QSPI0B_SCLK	LSIO.QSPI0B.SCLK	O	Serial Clock
99	nPWE	QSPI0B_DATA0	LSIO.QSPI0B.DATA0	I/O	Serial I/O for command, address, and data
105	nCS0	QSPI0B_DATA1	LSIO.QSPI0B.DATA1	I/O	Serial I/O for command, address, and data
107	nCS1	QSPI0B_DATA2	LSIO.QSPI0B.DATA2	I/O	Serial I/O for command, address, and data
98	Camera Input Data<1>	QSPI0B_DATA3	LSIO.QSPI0B.DATA3	I/O	Serial I/O for command, address, and data
102		QSPI0B_DQS	LSIO.QSPI0B.DQS	I	Data Strobe signal, required on some high-speed DDR devices
104		QSPI0B_SS0_B	LSIO.QSPI1A.SS0_B	O	Chip Select 0
106	nCS2	QSPI0B_SS1_B	LSIO.QSPI1A.SS1_B	O	Chip Select 1, used to select the second instance of QuadSPI device (dual die flash require CS0 and CS1)
95	RDY	QSPI0B_SCLK	LSIO.QSPI1A.SCLK	O	Serial Clock
99	nPWE	QSPI0B_DATA0	LSIO.QSPI1A.DATA0	I/O	Serial I/O for command, address, and data
105	nCS0	QSPI0B_DATA1	LSIO.QSPI1A.DATA1	I/O	Serial I/O for command, address, and data
107	nCS1	QSPI0B_DATA2	LSIO.QSPI1A.DATA2	I/O	Serial I/O for command, address, and data
98	Camera Input Data<1>	QSPI0B_DATA3	LSIO.QSPI1A.DATA3	I/O	Serial I/O for command, address, and data
102		QSPI0B_DQS	LSIO.QSPI1A.DQS	I	Data Strobe signal, required on some high-speed DDR devices

5.26 Media Local Bus (MLB50)

The Media Local Bus is predominantly used in automotive for high-bandwidth audio, video, and control information transport. MLB is a standardized on-PCB, inter-chip communication bus for MOST (Media Oriented Systems Transport) based devices. As MLB is not part of the Colibri module specifications, the interface is not compatible with other Colibri modules. The i.MX 8X SoC features a 3-pin (single-ended) interface for the MLB, which is available on the module edge connector. The standard Toradex BSP might not support the MLB interface.

Table 5-59 MLB Signal Pins

X1 Pin#	Colibri STD Function	i.MX 8X Ball Name	i.MX 8X Function	I/O	Description
57	LCD RGB Data<16>	ENET0_RGMII_TXD2	CONN.MLB.CLK	I	Single-ended clock
70	LCD RGB Data<1>	ESAI0_FST			
78	LCD RGB Data<4>	ESAI0_TX0	CONN.MLB.DATA	I/O	Single-ended data
85	Camera Input Data<8>, Keypad_Out<4>	ENET0_RGMII_RXC			
58	LCD RGB Data<3>	ESAI0_SCKT	CONN.MLB.SIG	I/O	Single-ended signal
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	ENET0_RGMII_TXD3			

5.27 JTAG

The JTAG interface is not generally required for software development with the Colibri iMX8X. There is always the possibility of reprogramming the module using the Recovery Mode over USB. It is strongly recommended that the USBC (USB_OTG1) interface is accessible even if not needed in the production system to flash the module in recovery mode and for debugging reasons. Additionally, UART_A should also be accessible.

The JTAG interface is located on test points on the underside of the module. The location is the same for all modules in the Colibri family. On the Evaluation Board 3.1 and later, the signals are accessible through pogo pins. Please pay attention, the interface voltage is **1.8V**. Hence jumper JP 29 must be in position 1-2. Since the Aster carrier board features only a 3.3V logic level for the JTAG interface, it cannot be used with the Colibri iMX8X.

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Colibri iMX8X even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the USBC (USB_OTG1) interface is used to connect it to a host computer. You will find additional information at our Developer Center: http://developer.toradex.com.

To enter the recovery mode, either connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10 kΩ resistor while power up the module. If the Colibri Evaluation Board V3.x is used, the SW9 button can be pressed during switching on the module's power supply.

Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module tries to boot from the external SD card instead of the USB serial loader.

Figure 13: Location of recovery mode pads

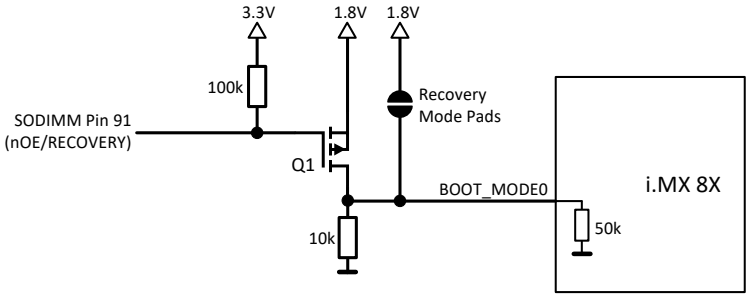

Figure 14: Recovery Mode Glue Logic

7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded on our website at:

https://developer.toradex.com/products/colibri-som-family/modules/colibri-imx8x#errata

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_3V3	Main power supply	-0.3	3.6	V
Vmax_AVDD	Analog power supply	-0.3	3.6	V
Vmax_VCC_BATT	RTC power supply	-0.3	4.3	V
Vmax_IO	IO pins with GPIO function	-0.3	3.6	V
Vmax_ADC	ADC input pins	-0.5	2.1	V
Vmax_TOUCH	Touch interface pins	-0.3	2.1	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
3V3	Main power supply*	3.135	3.3	3.465	V
AVDD	Analogue power supply	3.0	3.3	3.6	V
VCC_BATT	RTC power supply	2.5	3.3	3.6	V

* The limiting device is the KSZ8041 Ethernet PHY. All other devices on the module work from 3.0V to 3.6V.

8.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Colibri product family. Following those recommendations ensures that the carrier board being designed is compatible with all existing and future Colibri modules. For details, please refer to the Colibri Carrier Board Design Guide.

For designing carrier boards for a particular Colibri module only, please consult our Developer Website for module-specific power consumption information. However, please note that scaling the carrier board power supplies for a particular module only may cause compatibility issues with other existing and future modules within the Colibri family.

8.4 Mechanical Characteristics

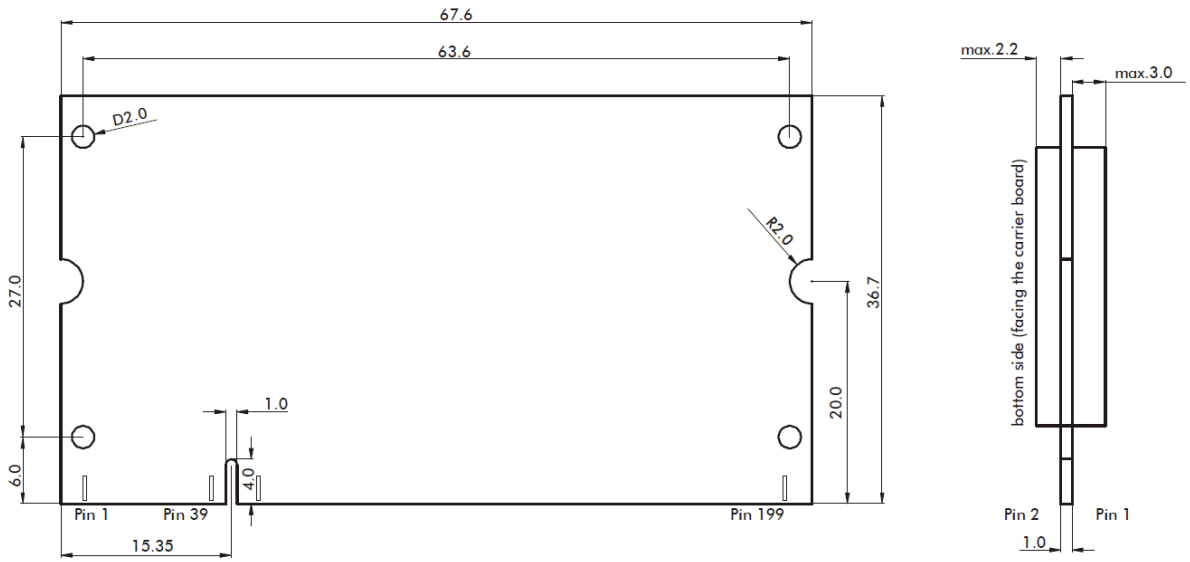

Figure 15 Mechanical dimensions of the Colibri module (top view)
Tolerance for all measures: +/- 0.1mm

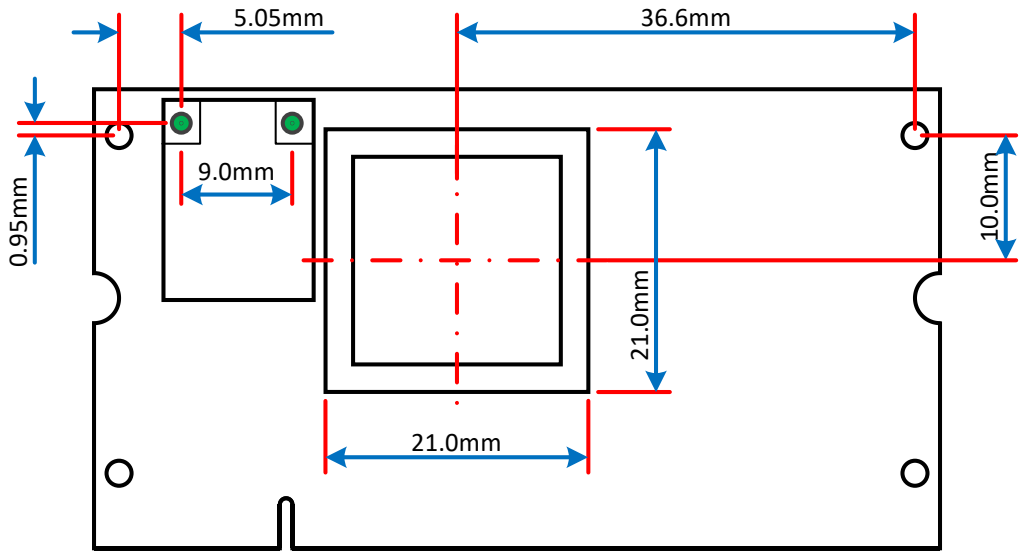

Figure 16 Mechanical position of SoC and Wi-Fi module (top view)
Tolerance for all measures: +/- 0.1mm

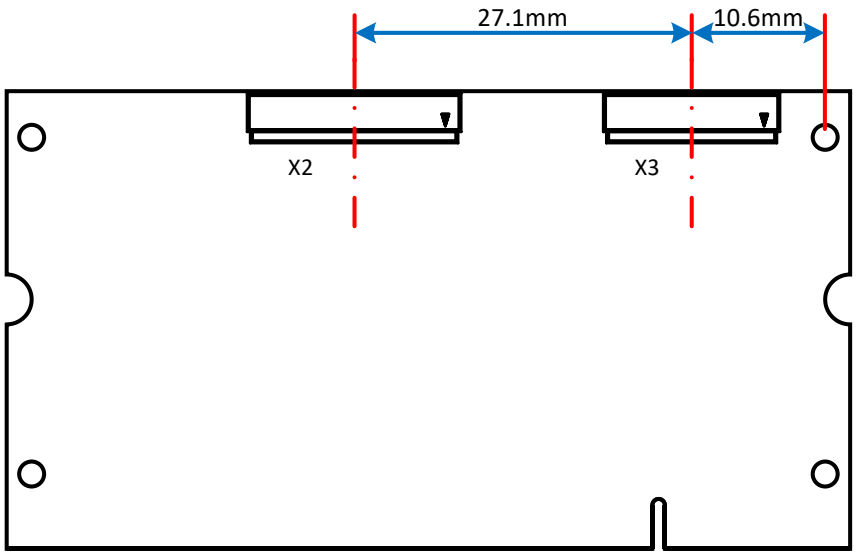

Figure 17 Mechanical position of FFC connectors (bottom view)
Tolerance for all measures: +/- 0.1mm

8.4.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A selection of SODIMM200 socket manufacturers is detailed below:

AUK Connectors:	http://www.aukconnector.com
CONCRAFT:	http://www.concraft.com.tw
Morethanall Co Ltd.:	http://www.morethanall.com
Tyco Electronics (AMP):	http://www.te.com
NEXUS COMPONENTS GmbH	http://www.nexus-de.com

8.5 Thermal Specification

The Colibri iMX8X incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling, enabling the system to continuously adjust the operating frequency and voltage in response to the workload and temperature changes. The i.MX 8X SoC features DVFS on the CPU cluster, as well as on the GPU. This allows the Colibri iMX8X to deliver higher performance at lower average power consumption compared to other solutions.

The Colibri iMX8X modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and are used to determine whether the cores need to be throttled to prevent overheating. If the temperature of the i.MX 8X reaches the maximum permitted temperature limit, the system will automatically shut down.

Here some general considerations:

- Suppose you only use the peak performance for a short time. In that case, heat dissipation is less of a problem because advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents in idle. A die temperature increase from 25°C to 125°C will increase the leakage by a factor of 10
- The Cortex-A35 is currently Arm's most efficient Armv8 core

Table 8-3 Thermal Specification Colibri iMX8DX 1GB

Description	Min	Typ	Max	Unit
Operating temperature range	-25[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The LPDDR4 RAM is limiting the minimum operating temperature. The rest of the components are capable of running until -40°C

Table 8-4 Thermal Specification Colibri iMX8DX 1GB WB

Description	Min	Typ	Max	Unit
Operating temperature range	-25[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The LPDDR4 RAM is limiting the minimum operating temperature. The rest of the components can run until -40°C, except for the Wi-Fi module, limiting to -30°C.

Table 8-5 Thermal Specification Colibri iMX8QXP 2GB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] All components are rated to run until -40°C.

Table 8-6 Thermal Specification Colibri iMX8QXP 2GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8X only. ($R_{\theta JA}$)[2]		15.2		°C/W
Thermal Resistance Junction-to-Top of i.MX 8X chip case. ($R_{\theta JCtop}$)[2]		0.7		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

8.6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance

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