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Apalis iMX8

Datasheet

Revision History

Date	Doc. Rev.	Apalis iMX8 Version	Changes
28-Aug-2018	Rev. 0.9	V1.0	Initial Release
05-Oct-2018	Rev. 0.91	V1.0	Apalis iMX8QP 2GB added Minor changes
16-Oct-2018	Rev. 0.92	V1.0	Section 5.16.1: Correct I2S Slave pins Section 5.16.2: Correct AC'97 pins
07-Dec-2018	Rev. 0.93	V1.0	Section 1.2: Update SoC part number Section 1.2: Remove DSP feature from QP module versions
30-Jan-2019	Rev. 0.94	V1.0	Section 5.5.1: Correct pin numbers in Table 5-12
16-May-2019	Rev. 0.95	V1.0	Section 1.4.5: Added link to Azurewave website
28-Oct-2019	Rev. 0.96	V1.0	Section 5.3: Add information regarding RGMII limitation
28-Oct-2019	Rev. 0.97	V1.1	Section 3.2, 5.3: Secondary RGMII/RMII Ethernet interface additional notes added Section 5.4: Remove Wi-Fi power gating Section 3.2, 4.4, 5.6, 5.9: HDMI DDC Pins 205/207 changed Minor changes
23-Apr-2020	Rev. 0.98	V1.1	Disclaimer update Minor cosmetic improvements
07-Jul-2020	Rev. 0.99	V1.1	Sections 1.1 and 1.2.1: HiFi 4 DSP functionality has been removed from the document as it will not be supported anymore by this product
30-Sep-2020	Rev. 1.0	V1.1	Section 8.5.1: Update the MXM3 connector
19-Jan-2021	Rev. 1.1	V1.1	Section 5.21: Change ADC input resistor from 10kΩ to 1kΩ

Contents

1. Introduction

1.1 Hardware

The Apalis iMX8 is a computer module based on the i.MX 8 Family of embedded System on Chips (SoC) from NXP®. The i.MX 8 Family consists of the i.MX 8QuadMax, i.MX 8QuadPlus, and i.MX 8DualMax. The top-tier i.MX 8QuadMax (i.MX 8QM) features eight CPU cores. The two core complexes are configured as big/LITTLE. There are two Arm Cortex-A72 CPU (big) which peak up to 1.6GHz and are optimized for high computing performance. The quad-core Arm Cortex-A53 (LITTLE) cluster can run with up to 1.2GHz and are running most of the use cases at a low-power consumption.

Additional to the main CPU complex, all i.MX 8 family members features two Arm Cortex-M4 processors which peak up to 266MHz. These two processors are independent of each other and feature their own dedicated interfaces while they can also access the regular interfaces. This heterogeneous multi-core system allows for running additional real-time operating systems on the M4 cores for time- and security-critical tasks. The i.MX 8 features a System Controller Unit (SCU), which runs on an independent Cortex-M processor. A major task of this controller is resource management with proper access and permission control in order to make sure the different M4 cores and main CPU complex are isolated from each other. This massively increases the safety of the heterogeneous multicore system in comparison with older SoC.

The i.MX 8QM features two powerful GC7000 XSVX Graphic Processing Units (GPU) from Vivante®. Each independent GPU provides 32 Vega shader cores with tessellation, geometry, and compute shaders. The GPUs are able to peak with up to 128 GFLOPS each and support OpenGL® 3.0, OpenGL® ES3.2, and DirectX® 11.

The Apalis iMX8 incorporates DVFS (Dynamic Voltage and Frequency Switching) and Thermal Throttling, which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption.

The module targets a wide range of applications, including advanced graphics, imaging, machine vision, audio, voice, video and safety-critical; automotive: infotainment, instrument cluster, head unit, heads-up display (HUD), rear seat entertainment and full digital electronic cockpit (eCockpit); home/building automation; Digital Signage; Industrial Automation, Data Acquisition, Thin Clients, Robotics, and much more.

It offers a wide range of interfaces from simple GPIOs, industry standard I2C, and SPI buses through to high-speed USB 3.0 interfaces, high-speed PCI Express, and SATA. The HDMI and LVDS interfaces make it very easy to connect large, up to 4K resolution displays.

The Apalis iMX8 module is available with on board Dual-Band (2.4/5 GHz) Wi-Fi 802.11a/b/g/n/ac and Bluetooth v5.0 (BR/EDR/BLE) interface. The Wi-Fi module features a MHF4-compatible connector for an external antenna. The module is pre-certified for FCC (US), CE (Europe), and IC (Canada).

The Apalis iMX8 module encapsulates the complexity associated with modern day electronic design, such as high-speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a carrier board that implements the application-specific electronics, which is generally much less complicated. The Apalis iMX8 module takes this one step further and implements an interface pinout which allows direct connection of real world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed, serial technologies that use impedance controlled differential pairs, as it allows them to easily route such interfaces to common connectors in a simple, robust fashion.

1.2 Main Features

1.2.1 CPU

	Apalis iMX8QP 2GB	Apalis iMX8QP 2GB WB	Apalis iMX8QM 4GB IT	Apalis iMX8QM 4GB WB IT
i.MX 8 Family SoC	PIMX8QP5AVUFFAx	PIMX8QP5AVUFFAx	PIMX8QM6AVUFFAx	PIMX8QM6AVUFFAx
Arm Cortex-A72 CPU Cores	1	1	2	2
Arm Cortex-A53 CPU Cores	4	4	4	4
Arm Cortex-M4F CPU Cores	2	2	2	2
L1 Instruction Cache (each core)	48 KByte (A72) 32 KByte (A53) 16 KByte (M4)	48 KByte (A72) 32 KByte (A53) 16 KByte (M4)	48 KByte (A72) 32 KByte (A53) 16 KByte (M4)	48 KByte (A72) 32 KByte (A53) 16 KByte (M4)
L1 Data Cache (each core)	32 KByte (A72) 32 KByte (A53) 16 KByte (M4)	32 KByte (A72) 32 KByte (A53) 16 KByte (M4)	32 KByte (A72) 32 KByte (A53) 16 KByte (M4)	32 KByte (A72) 32 KByte (A53) 16 KByte (M4)
L2 Cache (shared by cores)	1 MByte (A72) 1 MByte (A53)	1 MByte (A72) 1 MByte (A53)	1 MByte (A72) 1 MByte (A53)	1 MByte (A72) 1 MByte (A53)
Tightly-Coupled Memory	256 KByte (M4)	256 KByte (M4)	256 KByte (M4)	256 KByte (M4)
NEON MPE	✓	✓	✓	✓
Maximum CPU frequency	1.6 GHz (A72) 1.26 GHz (A53) 266 MHz (M4)	1.6 GHz (A72) 1.26 GHz (A53) 266 MHz (M4)	1.6 GHz (A72) 1.26 GHz (A53) 266 MHz (M4)	1.6 GHz (A72) 1.26 GHz (A53) 266 MHz (M4)
Arm TrustZone	✓	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓	✓
Secure JTAG Controller	✓	✓	✓	✓
Secure Non-Volatile Storage	✓	✓	✓	✓

1.2.2 Memory

	Apalis iMX8QP 2GB	Apalis iMX8QP 2GB WB	Apalis iMX8QM 4GB IT	Apalis iMX8QM 4GB WB IT
LPDDR4 RAM Size	2 GByte	2 GByte	4G Byte	4G Byte
LPDDR4 RAM Speed	3200 MT/s	3200 MT/s	3200 MT/s	3200 MT/s
LPDDR4 RAM Memory Width	2x32 bit	2x32 bit	2x32 bit	2x32 bit
eMMC NAND Flash (8bit)* V5.0	16 GByte	16 GByte	16G Byte	16G Byte

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear levelling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.2.3 Interfaces

	Apalis iMX8QP 2GB	Apalis iMX8QP 2GB WB	Apalis iMX8QM 4GB IT	Apalis iMX8QM 4GB WB IT
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	1	-	1
Bluetooth 5/BLE	-	1	-	1
LCD RGB	-	-	-	-
LVDS (2x single channel 85 Mpxiel/s or 1x dual channel 165 Mpixel/s)	1	1	1	1
LVDS (1x single channel 85 Mpxiel/s)	1*	1*	1*	1*
HDMI 2.0a (max 4096x2160) eDP 1.4 / DP1.3	1	1	1	1
VGA Analogue Video	-	-	-	-
MIPI DSI	1x 1 Data Lanes*	1x 1 Data Lanes*	1x 1 Data Lanes*	1x 1 Data Lanes*
Resistive Touch Screen	4 Wire	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)	1 (Mono)	1 (Mono)
Medium Quality Sound (MQS)	1* (Stereo)	1* (Stereo)	1* (Stereo)	1* (Stereo)
SAI (AC97/I^2S)	1+2*	1+2*	1+2*	1+2*
ESAI (AC97/I^2S)	1*	1*	1*	1*
S/PDIF	1 in / 1 out	1 in / 1 out	1 in / 1 out	1 in / 1 out
Parallel Camera Interface	-	-	-	-
MIPI CSI-2	2x 4 Data Lanes*	2x 4 Data Lanes*	2x 4 Data Lanes*	2x 4 Data Lanes*
I^2C	3+4*	3+4*	3+4*	3+4*
SPI	2+2*	2+2*	2+2*	2+2*
UART	4+3*	4+3*	4+3*	4+3*
SD/SDIO/MMC	2	2	2	2
GPIO	8+125*	8+125*	8+125*	8+125*
USB 2.0 OTG (host/device)	1	1	1	1
USB 3.0 host	1	1	1	1
USB 2.0 host	2	2	2	2
PCIe (Gen 3.0)	1+1*	1+1*	1+1*	1+1*
Serial ATA III (6Gbit/s)	1	1	1	1
10/100/1000 MBit/s Ethernet	1	1	1	1
RGMII/RMII/MII interface for 2nd Ethernet PHY on Baseboard	1*	1*	1*	1*
PWM	4+4*	4+4*	4+4*	4+4*
Analogue Inputs	4+4*	4+4*	4+4*	4+4*
CAN	2+1*	2+1*	2+1*	2+1*

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the type-specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints.

1.2.4 Graphics Processing Unit

	Apalis iMX8QP 2GB	Apalis iMX8QP 2GB WB	Apalis iMX8QM 4GB IT	Apalis iMX8QM 4GB WB IT
Vivante GC7000 XSVX GPU Units			2	2
Vivante GC7000Lite XSVX GPU Units	2	2		
Vega Shaders (per unit)	16	16	32	32
OpenGL® ES 3.2			✓	✓
OpenGL® ES 3.1, 3.0	✓	✓	✓	✓
OpenGL 3.0, 2.1	✓	✓	✓	✓
DirectX 11	✓	✓	✓	✓
OpenVG 1.1	✓	✓	✓	✓
DirectFB 1.4+	✓	✓	✓	✓
GDI (Direct Draw)	✓	✓	✓	✓
Vulkan 1.0 support	✓	✓	✓	✓

1.2.5 HD Video Decode

- ✓ H.265 HEVC Main Profile 2160p60 Level 5.1
- ✓ H.254 AVC Constrained Baseline, Main and High profile 1080p60
- ✓ H.254 MVC
- ✓ WMV9/VC-1 Simple, Main and Advanced Profile
- ✓ MPEG 1 and 2 Main Profile at High Level 1080p60
- ✓ AVS Jizhun Profile (JP)
- ✓ MJPEG4.2 ASP, H263, Sorenson Spark
- ✓ Divx 3.11, with Global Motion Compensation (GMC)
- ✓ ON2/Google VP6/VP8 1080p60
- ✓ RealVideo 8/9/10
- ✓ JPEG and MJPEG A/B Baseline

1.2.6 HD Video Encode

- ✓ Two encoders for H.264 (Baseline, Main, High Profile) 1080p30

1.2.7 Supported Operating Systems

- ✓ Embedded Linux
- ✓ Android available through Toradex partners

1.3 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Apalis® iMX8 module, and whether an interface is provided on standard or type-specific pins. The LVDS interface is an example of an interface that makes use of standard and type-specific pins; two single channel LVDS' (can be used as one dual channel) are provided as part of the standard interface pinout while an additional single channel LVDS is available as type-specific.

Some interfaces are available as an alternate function of a pin. This function can only be used if the primary function of the pin is not used. Check section 4.4 for a list of all alternate functions of the MXM3 pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis iMX8 Module. The tool allows comparing the interfaces of different Apalis modules.

More information to this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	Standard	Type Specific	Alternate Function
4 Wire Resistive Touch	4	4		
Analogue Inputs	8	4		4
Analogue Audio (Line in/out, Mic in)	1	1		
Medium Quality Sound (MQS)	1			1
CAN	3	2		1
CSI Ports	2		2	
DSI Ports	1		1	
Single Channel LVDS Display	3	2	1	
Dual Channel LVDS Display (shared with single channel)	1	1		
Gigabit Ethernet	1	1		
RGMII/RMII (2nd Ethernet	1			1
GPIO	133	8	6	119
SAI (I^2S)	3	1		2
ESAI	1			1
HDMI (TDMS)	1	1		
eDP/DP	1			1
I^2C	7	3		4
Parallel Camera				
Parallel LCD				
PCI-Express (lane count)	2	1		1
PWM	8	4		4
SATA	1	1		
SD/SDIO/MMC	2	2		
S/PDIF In	1	1		
S/PDIF Out	1	1		
SPI	4	2		2
UART	7	4		3
USB 2.0 host/device	1	1		
USB 3.0 host	1	1		
USB 2.0 host	2	2		
VGA				

Figure 1: Apalis® iMX8 Module Interfaces

1.4 Reference Documents

1.4.1 NXP i.MX 8

You will find the details about i.MX 8 SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors/i.mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8

1.4.2 Ethernet Transceiver

Apalis iMX8 uses the Micrel KSZ9031RNX Gigabit Ethernet Transceiver (PHY).
https://www.microchip.com/wwwproducts/en/KSZ9031

1.4.3 Audio Codec

Apalis iMX8 uses the NXP SGTL5000 Audio Codec.
http://www.nxp.com/products/interface-and-connectivity/interface-and-system-management/switch-monitoring-ics/ultra-low-power-audio-codec:SGTL5000

1.4.4 USB Hub

The Apalis iMX8 features an HSIC USB Hub.
https://www.microchip.com/wwwproducts/en/USB3503

1.4.5 Wi-Fi and Bluetooth Module

Some of the Apalis iMX8 use the Azurewave AW-CM276NF wireless module. The AW-CM276NF datasheet is available under NDA from Toradex. Please contact your local sales team for more information.
http://wen.azurewave.com/wireless-modules

1.4.6 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide in order to make the board compatible within the Apalis module family. Please study this document in detail prior to starting your carrier board design.
http://docs.toradex.com/101123-apalis-arm-carrier-board-design-guide.pdf

1.4.7 Layout Design Guide

This document contains information about high-speed layout design and additional information that helps to get the carrier board layout the first time right.
http://docs.toradex.com/102492-layout-design-guide.pdf

1.4.8 Toradex Developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information on a regular basis.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Apalis iMX8.
http://www.developer.toradex.com

1.4.9 Apalis Carrier Board Schematics

We provide the completed schematics plus the Altium project file, which includes library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board as well as other carrier boards free of charge. This is of great help when designing your own carrier board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.4.10 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

2. Architecture Overview

2.1 Block Diagram

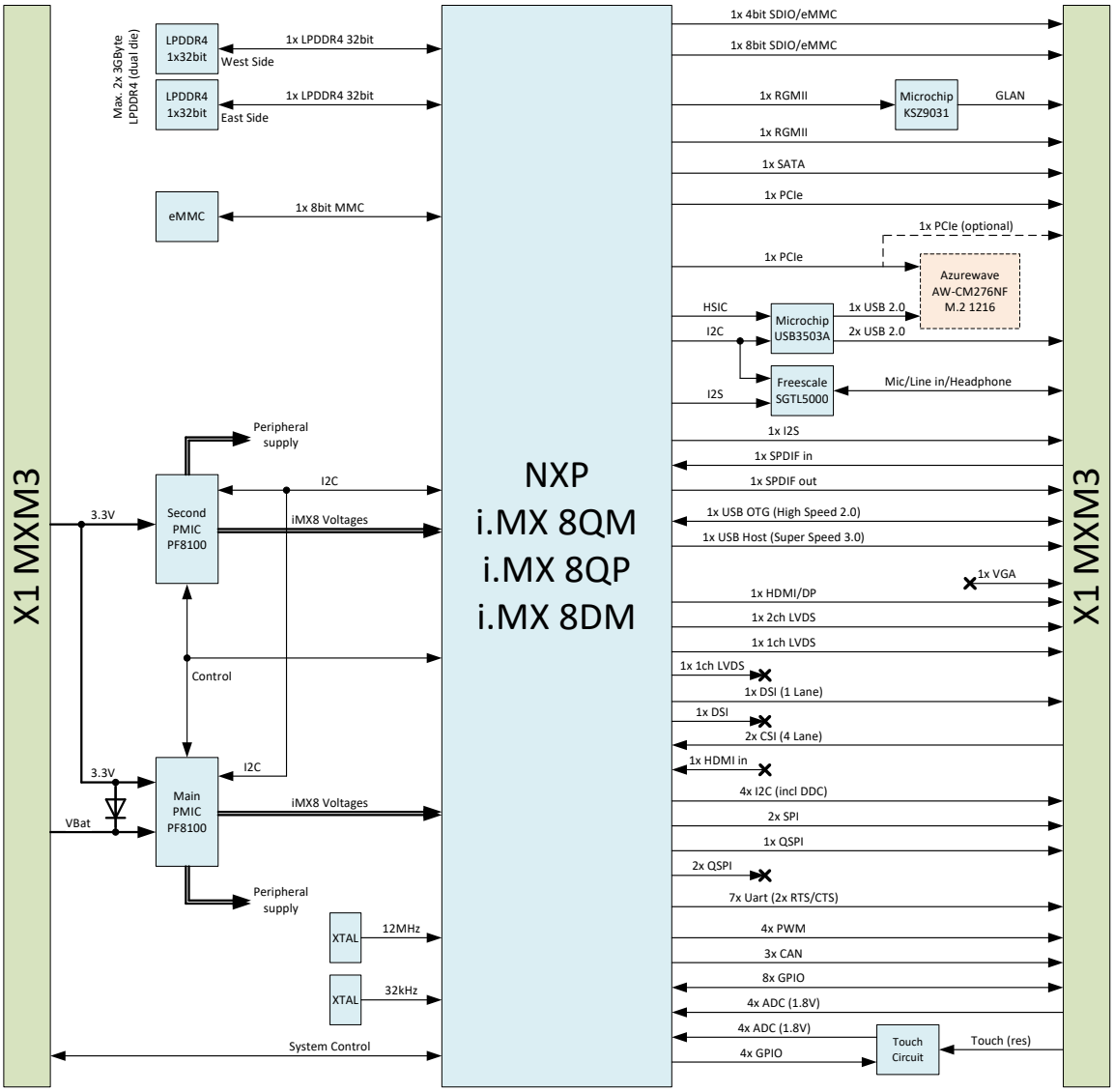

Figure 2 Apalis iMX8 Block Diagram

3. Apalis iMX8 Connectors

3.1 Pin Numbering

The diagrams in Figure 3 and Figure 4 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema. Pins on the top side of the module have even numbers and pins on the bottom side have odd numbers.

The pin number increases linearly as a multiple of the pitch – that is, pins which are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins which do not exist due to the connector notch are also accounted for (pins 166 through 172).

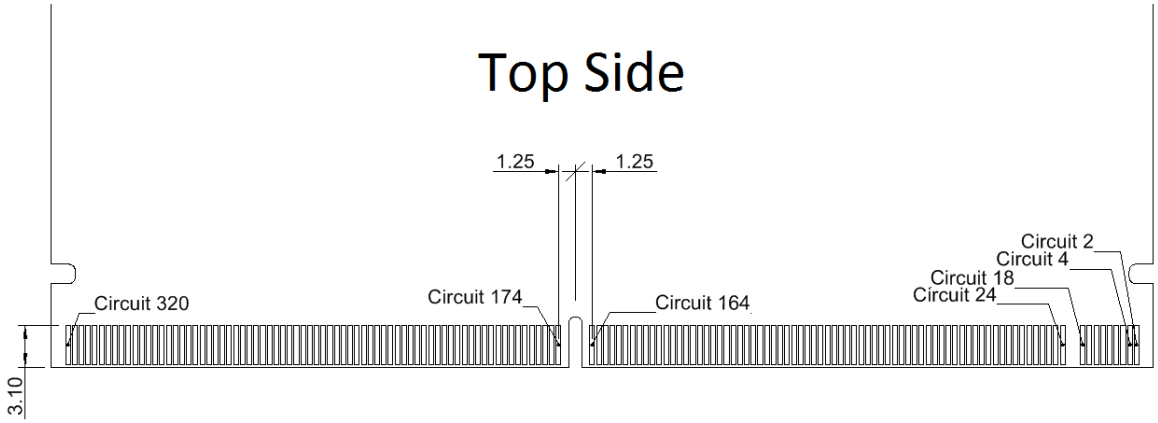

Figure 3: Pin numbering schema on the top side of the module

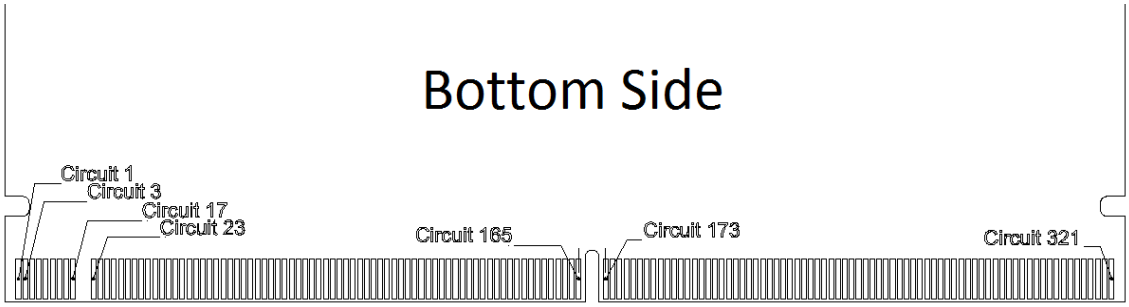

Figure 4: Pin numbering schema on the bottom side of the module

3.2 Assignment

The following table describes the MXM3 connector pin out. Some pins are shaded dark grey as type-specific interfaces. These pins might not be compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that type-specific interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both module A and module B have three additional PCI-Express lanes which are available in the same configurations as a type-specific interface, then they shall be assigned to the same pins in the type-

specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

- X1: Pin number on the MXM3 module edge connector (X1).
- Apalis Signal Name: The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have alternate function, but in order to be compatible with other Apalis modules, only the default function should be used and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- iMX8 Ball Name: The name of the pin of the i.MX 8 SoC.

Table 3-1 X1 Connector

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes	X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
1	GPIO1	M40_GPIO0_00		2	PWM1	GPT1_COMPARE	
3	GPIO2	M40_GPIO0_01		4	PWM2	GPT0_COMPARE	
5	GPIO3	M41_GPIO0_00		6	PWM3	UART0_RTS_B	
7	GPIO4	M41_GPIO0_01		8	PWM4	UART0_CTS_B	
9	GND			10	VCC		
11	GPIO5	FLEXCAN2_RX		12	CAN1_RX	FLEXCAN0_RX	
13	GPIO6	FLEXCAN2_TX		14	CAN1_TX	FLEXCAN0_TX	
15	GPIO7	MLB_SIG		16	CAN2_RX	FLEXCAN1_RX	
17	GPIO8	MLB_DATA		18	CAN2_TX	FLEXCAN1_TX	
23	GND			24	POWER_ENABLE_MOCI		PWR Management
25	SATA1_RX+	PCIE_SATA0_RX0_P		26	RESET_MOCI#		PWR Management
27	SATA1_RX-	PCIE_SATA0_RX0_N		28	RESET_MICO#		PWR Management
29	GND			30	VCC		
31	SATA1_TX-	PCIE_SATA0_TX0_N		32	ETH1_MDI2+		KSZ9031 Pin 7
33	SATA1_TX+	PCIE_SATA0_TX0_P		34	ETH1_MDI2-		KSZ9031 Pin 8
35	SATA1_ACT#	ESAI1_TX0		36	VCC		
37	WAKE1_MICO	SPI3_CS0		38	ETH1_MDI3+		KSZ9031 Pin 10
39	GND			40	ETH1_MDI3-		KSZ9031 Pin 11
41	PCIE1_RX-	PCIE0_RX0_N		42	ETH1_ACT		KSZ9031 Pin17 (buffered)
43	PCIE1_RX+	PCIE0_RX0_P		44	ETH1_LINK		KSZ9031 Pin15 (buffered)
45	GND			46	ETH1_CTREF		NC
47	PCIE1_TX-	PCIE0_TX0_N		48	ETH1_MDI0-		KSZ9031 Pin 3
49	PCIE1_TX+	PCIE0_TX0_P		50	ETH1_MDI0+		KSZ9031 Pin 2
51	GND			52	VCC		
53	PCIE1_CLK-		PCIe reference clock source	54	ETH1_MDI1-		KSZ9031 Pin6

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
55	PCIE1_CLK+		PCIe reference clock source
57	GND		
59	TS_DIFF1-	LVDS0_CH0_CLK_N	
61	TS_DIFF1+	LVDS0_CH0_CLK_P	
63	TS_1	MLB_CLK	Shared with recovery circuit
65	TS_DIFF2-	LVDS0_CH0_TX0_N	
67	TS_DIFF2+	LVDS0_CH0_TX0_P	
69	GND		
71	TS_DIFF3-	HDMI_TX0_AUX_N	
73	TS_DIFF3+	HDMI_TX0_AUX_P	
75	GND		
77	TS_DIFF4-	LVDS0_CH0_TX1_N	
79	TS_DIFF4+	LVDS0_CH0_TX1_P	
81	GND		
83	TS_DIFF5-	LVDS0_CH0_TX2_N	
85	TS_DIFF5+	LVDS0_CH0_TX2_P	
87	TS_2	LVDS0_I2C0_SCL	
89	TS_DIFF6-	LVDS0_CH0_TX3_N	
91	TS_DIFF6+	LVDS0_CH0_TX3_P	
93	GND		
95	TS_DIFF7-	MIPI_DSI1_DATA0_N	
97	TS_DIFF7+	MIPI_DSI1_DATA0_P	
99	TS_3	LVDS0_I2C0_SDA	
101	TS_DIFF8-	MIPI_CSI0_DATA3_N	
103	TS_DIFF8+	MIPI_CSI0_DATA3_P	
105	GND		
107	TS_DIFF9-	MIPI_CSI0_DATA2_N	
109	TS_DIFF9+	MIPI_CSI0_DATA2_P	
111	GND		
113	TS_DIFF10-	MIPI_CSI0_DATA1_N	
115	TS_DIFF10+	MIPI_CSI0_DATA1_P	
117	GND		
119	TS_DIFF11-	MIPI_CSI0_DATA0_N	
121	TS_DIFF11+	MIPI_CSI0_DATA0_P	
123	TS_4	MIPI_DSI1_GPIO0_00	
125	TS_DIFF12-	MIPI_CSI0_CLK_N	

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
56	ETH1_MDI1+		KSZ9031 Pin5
58	VCC		
60	USBO1_VBUS	USB_OTG1_VBUS	
62	USBO1_SSRX+	PCIE1_RX0_P	**Pins not connected on modules with Wi-Fi**
64	USBO1_SSRX-	PCIE1_RX0_N	
66	VCC		
68	USBO1_SSTX+	PCIE1_TX0_P	**Pins not connected on modules with Wi-Fi**
70	USBO1_SSTX-	PCIE1_TX0_N	
72	USBO1_ID	USB_OTG1_ID	
74	USBO1_D+	USB_OTG1_DP	
76	USBO1_D-	USB_OTG1_DN	
78	VCC		
80	USBH2_D+		USB3503A (C2) USBDN2_DP
82	USBH2_D-		USB3503A (D2) USBDN2_DM
84	USBH_EN	USB_SS3_TC1	
86	USBH3_D+		USB3503A (C1) USBDN3_DP
88	USBH3_D-		USB3503A (D1) USBDN3_DM
90	VCC		
92	USBH4_SSRX-	USB_SS3_RX_N	
94	USBH4_SSRX+	USB_SS3_RX_P	
96	USBH_OC#	USB_SS3_TC3	
98	USBH4_D+	USB_OTG2_DP	
100	USBH4_D-	USB_OTG2_DN	
102	VCC		
104	USBH4_SSTX-	USB_SS3_TX_N	
106	USBH4_SSTX+	USB_SS3_TX_P	
108	VCC		
110	UART1_DTR	M40_I2C0_SCL	
112	UART1_TXD	UART1_TX	
114	UART1_RTS	UART1_RTS_B	
116	UART1_CTS	UART1_CTS_B	
118	UART1_RXD	UART1_RX	
120	UART1_DSR	M40_I2C0_SDA	
122	UART1_RI	M41_I2C0_SDA	
124	UART1_DCD	M41_I2C0_SCL	
126	UART2_TXD	LVDS1_I2C1_SCL	

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
127	TS_DIFF12+	MIPI_CSI0_CLK_P	
129	GND		
131	TS_DIFF13-	MIPI_DSI1_CLK_N	
133	TS_DIFF13+	MIPI_DSI1_CLK_P	
135	TS_5	SIM0_IO	
137	TS_DIFF14-	MIPI_CSI1_DATA3_N	
139	TS_DIFF14+	MIPI_CSI1_DATA3_P	
141	GND		
143	TS_DIFF15-	MIPI_CSI1_DATA2_N	
145	TS_DIFF15+	MIPI_CSI1_DATA2_P	
147	GND		
149	TS_DIFF16-	MIPI_CSI1_DATA1_N	
151	TS_DIFF16+	MIPI_CSI1_DATA1_P	
153	GND		
155	TS_DIFF17-	MIPI_CSI1_DATA0_N	
157	TS_DIFF17+	MIPI_CSI1_DATA0_P	
159	TS_6	USDHC1_STROBE	Shares voltage rail with MMC1
161	TS_DIFF18-	MIPI_CSI1_CLK_N	
163	TS_DIFF18+	MIPI_CSI1_CLK_P	
165	GND		

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
128	UART2_RTS	ENET1_RGMII_TXD3	Configurable voltage
130	UART2_CTS	ENET1_RGMII_RXC	Configurable voltage
132	UART2_RXD	LVDS1_I2C1_SDA	
134	UART3_TXD	UART0_TX	
136	UART3_RXD	UART0_RX	
138	UART4_TXD	LVDS0_I2C1_SCL	
140	UART4_RXD	LVDS0_I2C1_SDA	
142	GND		
144	MMC1_D2	USDHC1_DATA2	
146	MMC1_D3	USDHC1_DATA3	
148	MMC1_D4	USDHC1_DATA4	
150	MMC1_CMD	USDHC1_CMD	
152	MMC1_D5	USDHC1_DATA5	
154	MMC1_CLK	USDHC1_CLK	
156	MMC1_D6	USDHC1_DATA6	
158	MMC1_D7	USDHC1_DATA7	
160	MMC1_D0	USDHC1_DATA0	
162	MMC1_D1	USDHC1_DATA1	
164	MMC1_CD#	ESAI1_TX1	

173	CAM1_D7	MIPI_DSI1_I2C0_SCL	
175	CAM1_D6	MIPI_DSI1_I2C0_SDA	
177	CAM1_D5	ESAI0_TX0	
179	CAM1_D4	ESAI0_TX1	
181	CAM1_D3	ESAI0_TX2_RX3	
183	CAM1_D2	ESAI0_TX3_RX2	
185	CAM1_D1	ESAI0_TX4_RX1	
187	CAM1_D0	ESAI0_TX5_RX0	
189	GND		
191	CAM1_PCLK	MCLK_IN0	
193	CAM1_MCLK	SPI3_SDO	
195	CAM1_VSYNC	ESAI0_SCKR	
197	CAM1_HSYNC	ESAI0_SCKT	

174	VCC_BACKUP		
176	SD1_D2	USDHC2_DATA2	
178	SD1_D3	USDHC2_DATA3	
180	SD1_CMD	USDHC2_CMD	
182	GND		
184	SD1_CLK	USDHC2_CLK	
186	SD1_D0	USDHC2_DATA0	
188	SD1_D1	USDHC2_DATA1	
190	SD1_CD#	USDHC2_CD_B	
192	GND		
194	DAP1_MCLK	SPI3_SDI	
196	DAP1_D_OUT	SAI1_RXC	
198	DAP1_RESET#	ESAI1_SCKT	

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
199	GND		
201	I2C3_SDA (CAM)	SIM0_POWER_EN	
203	I2C3_SCL (CAM)	SIM0_PD	
205	I2C2_SDA (DDC)	HDMI_TX0_DDC_SDA	
207	I2C2_SCL (DDC)	HDMI_TX0_DDC_SCL	
209	I2C1_SDA	GPT1_CAPTURE	
211	I2C1_SCL	GPT1_CLK	
213	GND		
215	SPDIF1_OUT	SPDIF0_TX	
217	SPDIF1_IN	SPDIF0_RX	
219	GND		
221	SPI1_CLK	SPI0_SCK	
223	SPI1_MISO	SPI0_SDI	
225	SPI1_MOSI	SPI0_SDO	
227	SPI1_CS	SPI0_CS0	
229	SPI2_MISO	SPI2_SDI	
231	SPI2_MOSI	SPI2_SDO	
233	SPI2_CS	SPI2_CS0	
235	SPI2_CLK	SPI2_SCK	
237	GND		
239	BKL1_PWM	LVDS1_GPIO00	
241	GND		
243	LCD1_PCLK	ENET1_RGMII_RXD3	Configurable block voltage
245	LCD1_VSYNC	ENET1_RGMII_RXD2	Configurable block voltage
247	LCD1_HSYNC	ENET1_RGMII_RXD1	Configurable block voltage
249	LCD1_DE	ENET1_RGMII_RXD0	Configurable block voltage
251	LCD1_R0	ENET1_MDIO	3.3V
253	LCD1_R1	ENET1_MDC	3.3V
255	LCD1_R2	ENET1_RGMII_TXD2	Configurable block voltage
257	LCD1_R3	ENET1_RGMII_TXD1	Configurable block voltage
259	LCD1_R4	ENET1_RGMII_TXD0	Configurable block voltage
261	LCD1_R5	ENET1_RGMII_TXC	Configurable block voltage
263	LCD1_R6	ENET1_RGMII_TX_CTL	Configurable block voltage
265	LCD1_R7	ENET1_RGMII_RX_CTL	Configurable block voltage
267	GND		
269	LCD1_G0	ENET1_REFCLK_125M_25M	3.3V

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
200	DAP1_BIT_CLK	SPI0_CS1	
202	DAP1_D_IN	SAI1_RXFS	
204	DAP1_SYNC	SPI2_CS1	
206	GND		
208	VGA1_R		NC
210	VGA1_G		NC
212	VGA1_B		NC
214	VGA1_HSYNC		NC
216	VGA1_VSYNC		NC
218	GND		
220	HDMI1_CEC	HDMI_TX0_CEC	
222	HDMI1_TXD2+	HDMI_TX0_DATA2_EDP0_P	
224	HDMI1_TXD2-	HDMI_TX0_DATA2_EDP0_N	
226	GND		
228	HDMI1_TXD1+	HDMI_TX0_DATA1_EDP1_P	
230	HDMI1_TXD1-	HDMI_TX0_DATA1_EDP1_N	
232	HDMI1_HPD	HDMI_TX0_HPD	
234	HDMI1_TXD0+	HDMI_TX0_DATA0_EDP2_P	
236	HDMI1_TXD0-	HDMI_TX0_DATA0_EDP2_N	
238	GND		
240	HDMI1_TXC+	HDMI_TX0_CLK_EDP3_P	
242	HDMI1_TXC-	HDMI_TX0_CLK_EDP3_N	
244	GND		
246	LVDS1_A_CLK-	LVDS1_CH0_CLK_N	
248	LVDS1_A_CLK+	LVDS1_CH0_CLK_P	
250	GND		
252	LVDS1_A_TX0-	LVDS1_CH0_TX0_N	
254	LVDS1_A_TX0+	LVDS1_CH0_TX0_P	
256	GND		
258	LVDS1_A_TX1-	LVDS1_CH0_TX1_N	
260	LVDS1_A_TX1+	LVDS1_CH0_TX1_P	
262	USBO1_OC#	USB_SS3_TC2	
264	LVDS1_A_TX2-	LVDS1_CH0_TX2_N	
266	LVDS1_A_TX2+	LVDS1_CH0_TX2_P	
268	GND		
270	LVDS1_A_TX3-	LVDS1_CH0_TX3_N	

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
271	LCD1_G1	ESAI0_FSR	
273	LCD1_G2	ESAI0_FST	
275	LCD1_G3	SIM0_GPIO0_00	
277	LCD1_G4	SIM0_RST	
279	LCD1_G5	SIM0_CLK	
281	LCD1_G6	LVDS1_I2C0_SCL	
283	LCD1_G7	LVDS1_I2C0_SDA	
285	GND		
287	LCD1_B0	QSPI1A_DATA0	
289	LCD1_B1	QSPI1A_DATA1	
291	LCD1_B2	QSPI1A_DATA2	
293	LCD1_B3	QSPI1A_DATA3	
295	LCD1_B4	QSPI1A_SS0_B	
297	LCD1_B5	QSPI1A_DQS	
299	LCD1_B6	QSPI1A_SS1_B	
301	LCD1_B7	QSPI1A_SCLK	
303	AGND		
305	AN1_ADC0	ADC_IN0	**1.8V max**
307	AN1_ADC1	ADC_IN1	**1.8V max**
309	AN1_ADC2	ADC_IN2	**1.8V max**
311	AN1_TSWIP_ADC3	ADC_IN3	**1.8V max**
313	AGND		
315	AN1_TSPX	ADC_IN4	**1.8V max**, Touch Circuit
317	AN1_TSMX	ADC_IN5	**1.8V max**, Touch Circuit
319	AN1_TSPY	ADC_IN6	**1.8V max**, Touch Circuit
321	AN1_TSMY	ADC_IN7	**1.8V max**, Touch Circuit

X1	Apalis Signal Name	i.MX 8 Ball Name	Notes
272	LVDS1_A_TX3+	LVDS1_CH0_TX3_P	
274	USBO1_EN	USB_SS3_TC0	
276	LVDS1_B_CLK-	LVDS1_CH1_CLK_N	
278	LVDS1_B_CLK+	LVDS1_CH1_CLK_P	
280	GND		
282	LVDS1_B_TX0-	LVDS1_CH1_TX0_N	
284	LVDS1_B_TX0+	LVDS1_CH1_TX0_P	
286	BKL1_ON	LVDS0_GPIO00	
288	LVDS1_B_TX1-	LVDS1_CH1_TX1_N	
290	LVDS1_B_TX1+	LVDS1_CH1_TX1_P	
292	GND		
294	LVDS1_B_TX2-	LVDS1_CH1_TX2_N	
296	LVDS1_B_TX2+	LVDS1_CH1_TX2_P	
298	GND		
300	LVDS1_B_TX3-	LVDS1_CH1_TX3_N	
302	LVDS1_B_TX3+	LVDS1_CH1_TX3_P	
304	AGND		
306	AAP1_MICIN		SGTL5000 Pin 10
308	AGND		
310	AAP1_LIN_L		SGTL5000 Pin 9
312	AAP1_LIN_R		SGTL5000 Pin 8
314	AVCC		
316	AAP1_HP_L		SGTL5000 Pin 4
318	AAP1_HP_R		SGTL5000 Pin 1
320	AVCC		

4. I/O Pins

4.1 Function Multiplexing

The NXP i.MX 8 SoC (low-speed) I/O pins can be configured for any of the (and up to) four alternate functions. Most of the pins can also be used as GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). As an example: The i.MX 8 signal pin on the MXM3 finger pin 118 has the primary function UART1.RX (Apalis standard function UART1_RXD). Besides this UART function, the pin can also be configured as SPI3.SDO (SPI data output) and GPIO0.IO25 (GPIO)

The default setting for this pin is the primary function UART1.RX. It is strongly recommended to, whenever possible, use a pin for a function which is compatible with all Apalis modules. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In the table listed in chapter 4.4, you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

Special care has to be taken with the MXM3 pin 63 (TS_1). This pin is connected to the MLB_CLK ball of the SoC. Additionally, the pin is also connected to a recovery circuit. In order to boot the module correctly, make sure the MXM3 pin 63 is not driven high during the power up cycle. If the module edge pin 63 is driven high, the recovery glue logic will drive the SCU_BOOT_MODE2 ball of the SoC high in order to enter the serial loader mode. More details to the recovery mode can be found in section 6 of this document.

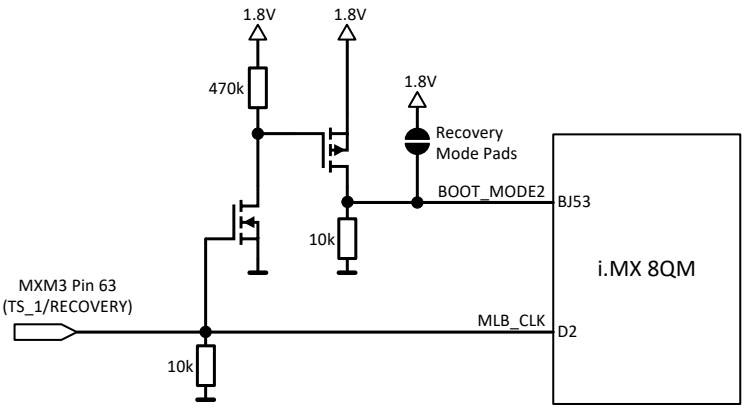

Figure 5: Recovery Mode Glue Logic

4.2 Pin Control

The alternate function of each pin can be changed independently. On previous i.MX based SoCs (e.g. i.MX 6 or i.MX 7), the multiplexing and pad control have been changed by directly writing to the IOMUX registers. On the i.MX 8 based SoC, this is no longer possible. The IOMUX registers can only be controlled by the System Controller Unit (SCU). This allows the SCU to do proper resource management of the peripherals. The SCU makes sure only the cores which have permission to the according domain are allowed to make changes in the pin configuration.

In order to change the multiplexing and configuration of the SoC pins, a System Controller API is provided. Please see the System Controller API Reference Guide from NXP for more information. With help of this API, the following settings can be set individually for every pin:

- Selecting the alternate function for this pin
- Configuring as input, open drain, open drain input, or regular push-pull output
- Low power behaviour such as latching
- Wakeup masking
- Wakeup control which includes falling and rising edge as well as high and low level
- Pull up and down resistor enabling
- Drive strength control
- Locking mechanism for muxing and pad control

4.3 Pin Reset Status

After a reset, the i.MX 8 pins can be in different modes. Most of them are pulled low. A few are driven low or high, tri-stated, or pulled up. Please check the table in chapter 0 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

Please be aware, the pin reset status is only guaranteed during the release of the reset signal. During the power up sequence, the states of the pins might be undefined until the IO bank voltage is enabled on the module.

Reset Status Description

Hi-Z:	Tristate (Input)
PD:	Pull-Down (Input)
PU:	Pull-Up (Input)
Drive-0:	Drive Low (Output)
Drive-1:	Drive High (Output)

4.4 SoC Functions List

Below is a list of all the i.MX 8 pins that are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The GPIO functionality is always defined as the ALT3 function. The alternate functions used to provide the primary interfaces to ensure best compatibility with other Apalis modules are highlighted.

Function Short Forms

ACM:	Audio Clock Mux
ADC:	Analog Digital Convert input
CEC:	Consumer Electronic Control
CSI:	Camera Sensor Interface
ENET:	Ethernet MAC interface
ESAI:	Enhanced Serial Audio Interface
FLEXCAN:	Flexible Controller Area Network (Flexible CAN)
GPIO:	General Purpose Input Output
GPT:	General Purpose Timer
HDMI:	High-Definition Multimedia Interface
HPD:	Hot Plug Detect
HSIO:	High Speed I/O
I2C:	Inter Integrated Circuit
KPP:	Keypad Port
LSIO:	Low Speed I/O
LVDS:	Low Voltage Differential Signalling (also known as FPD-Link or FlatLink)
M40:	Cortex M4 Processor complex 0 (dedicated interface for first M4 processor)
M41:	Cortex M4 Processor complex 1 (dedicated interface for second M4 processor)
MLB:	Media Local Bus (MediaLB)
MQS:	Medium Quality Sound
NAND:	Interface for NAND Flash
PCIE:	PCI Express
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
SAI:	Serial Interface for Audio (I2S and AC97)
SIM:	Subscriber Identification Module
SPI:	Serial Peripheral Interface Bus
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
VPU:	Video Processing Unit

X1 Pin	i.MX 8 Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	Type	Default Mode	Reset State	Power Block
1	M40_GPIO0_00	AR47	M40.GPIO0.IO00	M40.TPM0.CH0	DMA.UART4.RX	LSIO.GPIO0.IO08	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
3	M40_GPIO0_01	AU53	M40.GPIO0.IO01	M40.TPM0.CH1	DMA.UART4.TX	LSIO.GPIO0.IO09	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
5	M41_GPIO0_00	AP44	M41.GPIO0.IO00	M41.TPM0.CH0	DMA.UART3.RX	LSIO.GPIO0.IO12	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
7	M41_GPIO0_01	AU47	M41.GPIO0.IO01	M41.TPM0.CH1	DMA.UART3.TX	LSIO.GPIO0.IO13	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
11	FLEXCAN2_RX	C3	DMA.FLEXCAN2.RX			LSIO.GPIO4.IO01	GPIO	ALT0	PD	VDD_FLEXCAN_3P3
13	FLEXCAN2_TX	E7	DMA.FLEXCAN2.TX			LSIO.GPIO4.IO02	GPIO	ALT0	Drive-1	VDD_FLEXCAN_3P3
15	MLB_SIG	E1	CONN.MLB.SIG	AUD.SAI3.RXC		LSIO.GPIO3.IO26	GPIO	ALT0	PD	VDD_MLB_DIG_3P3
17	MLB_DATA	E3	CONN.MLB.DATA	AUD.SAI3.RXD		LSIO.GPIO3.IO28	GPIO	ALT0	PD	VDD_MLB_DIG_3P3
25	PCIE_SATA0_RX0_P	A19	HSIO.PCIE2.RX0_P							VDD_PCIE_CLEAN_1P8
27	PCIE_SATA0_RX0_N	B20	HSIO.PCIE2.RX0_N							VDD_PCIE_CLEAN_1P8
31	PCIE_SATA0_TX0_N	C17	HSIO.PCIE2.TX0_N							VDD_PCIE_CLEAN_1P8
33	PCIE_SATA0_TX0_P	B16	HSIO.PCIE2.TX0_P							VDD_PCIE_CLEAN_1P8
35	ESAI1_TX0	BF10	AUD.ESAI1.TX0	AUD.SAI2.RXD		LSIO.GPIO2.IO08	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3
37	SPI3_CS0	BG5	DMA.SPI3.CS0	DMA.FTM.CH2		LSIO.GPIO2.IO20	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3
41	PCIE0_RX0_N	B30	HSIO.PCIE0.RX0_N							VDD_PCIE_CLEAN_1P8
43	PCIE0_RX0_P	A29	HSIO.PCIE0.RX0_P							VDD_PCIE_CLEAN_1P8
47	PCIE0_TX0_N	C27	HSIO.PCIE0.TX0_N							VDD_PCIE_CLEAN_1P8
49	PCIE0_TX0_P	B26	HSIO.PCIE0.TX0_P							VDD_PCIE_CLEAN_1P8
59	LVDS0_CH0_CLK_N	BL41	LVDS0.T0CLKN							VDD_LVDS0_1P8
61	LVDS0_CH0_CLK_P	BN41	LVDS0.T0CLKP							VDD_LVDS0_1P8
63	MLB_CLK	D2	CONN.MLB.CLK	AUD.SAI3.RXFS		LSIO.GPIO3.IO27	GPIO	ALT0	PD	VDD_MLB_DIG_3P3
65	LVDS0_CH0_TX0_N	BK42	LVDS0.T0AN							VDD_LVDS0_1P8
67	LVDS0_CH0_TX0_P	BM42	LVDS0.T0AP							VDD_LVDS0_1P8
71	HDMI_TX0_AUX_N	BG3	HDMI_TX0.AUX_M							VDD_HDMI_TX0_1P8
73	HDMI_TX0_AUX_P	BH2	HDMI_TX0.AUX_P							VDD_HDMI_TX0_1P8
77	LVDS0_CH0_TX1_N	BL43	LVDS0.T0BN							VDD_LVDS0_1P8
79	LVDS0_CH0_TX1_P	BN43	LVDS0.T0BP							VDD_LVDS0_1P8
83	LVDS0_CH0_TX2_N	BK44	LVDS0.T0CN							VDD_LVDS0_1P8
85	LVDS0_CH0_TX2_P	BM44	LVDS0.T0CP							VDD_LVDS0_1P8
87	LVDS0_I2C0_SCL	BD38	LVDS0.I2C0.SCL	LVDS0.GPIO0.IO02		LSIO.GPIO1.IO06	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
89	LVDS0_CH0_TX3_N	BL45	LVDS0.T0DN							VDD_LVDS0_1P8
91	LVDS0_CH0_TX3_P	BN45	LVDS0.T0DP							VDD_LVDS0_1P8
95	MIPI_DSI1_DATA0_N	BH32	MIPI_DSI1.DN0							VDD_MIPI_DSI1_1P8
97	MIPI_DSI1_DATA0_P	BG33	MIPI_DSI1.DP0							VDD_MIPI_DSI1_1P8
99	LVDS0_I2C0_SDA	BD36	LVDS0.I2C0.SDA	LVDS0.GPIO0.IO03		LSIO.GPIO1.IO07	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
101	MIPI_CSI0_DATA3_N	BE17	MIPI_CSI0.DN3							VDD_MIPI_CSI0_1P8
103	MIPI_CSI0_DATA3_P	BF16	MIPI_CSI0.DP3							VDD_MIPI_CSI0_1P8
107	MIPI_CSI0_DATA2_N	BE25	MIPI_CSI0.DN2							VDD_MIPI_CSI0_1P8
109	MIPI_CSI0_DATA2_P	BF24	MIPI_CSI0.DP2							VDD_MIPI_CSI0_1P8
113	MIPI_CSI0_DATA1_N	BE19	MIPI_CSI0.DN1							VDD_MIPI_CSI0_1P8
115	MIPI_CSI0_DATA1_P	BF18	MIPI_CSI0.DP1							VDD_MIPI_CSI0_1P8
119	MIPI_CSI0_DATA0_N	BE23	MIPI_CSI0.DN0							VDD_MIPI_CSI0_1P8
121	MIPI_CSI0_DATA0_P	BF22	MIPI_CSI0.DP0							VDD_MIPI_CSI0_1P8
123	MIPI_DSI1_GPIO0_00	BM24	MIPI_DSI1.GPIO0.IO00	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO22	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
125	MIPI_CSI0_CLK_N	BE21	MIPI_CSI0.CKN							VDD_MIPI_CSI0_1P8
127	MIPI_CSI0_CLK_P	BF20	MIPI_CSI0.CKP							VDD_MIPI_CSI0_1P8
131	MIPI_DSI1_CLK_N	BH30	MIPI_DSI1.CKN							VDD_MIPI_DSI1_1P8

X1 Pin	i.MX 8 Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	Type	Default Mode	Reset State	Power Block
133	MIPI_DSI1_CLK_P	BG31	MIPI_DSI1.CKP							VDD_MIPI_DSI1_1P8
135	SIM0_IO	AN45	DMA.SIM0.IO			LSIO.GPIO0.IO02	GPIO	ALT0	Drive-0	VDD_SIM_3P3
137	MIPI_CSI1_DATA3_N	BH12	MIPI_CSI1.DN3							VDD_MIPI_CSI_1P8
139	MIPI_CSI1_DATA3_P	BJ13	MIPI_CSI1.DP3							VDD_MIPI_CSI_1P8
143	MIPI_CSI1_DATA2_N	BH20	MIPI_CSI1.DN2							VDD_MIPI_CSI_1P8
145	MIPI_CSI1_DATA2_P	BJ21	MIPI_CSI1.DP2							VDD_MIPI_CSI_1P8
149	MIPI_CSI1_DATA1_N	BH14	MIPI_CSI1.DN1							VDD_MIPI_CSI_1P8
151	MIPI_CSI1_DATA1_P	BJ15	MIPI_CSI1.DP1							VDD_MIPI_CSI_1P8
155	MIPI_CSI1_DATA0_N	BH18	MIPI_CSI1.DN0							VDD_MIPI_CSI_1P8
157	MIPI_CSI1_DATA0_P	BJ19	MIPI_CSI1.DP0							VDD_MIPI_CSI_1P8
159	USDHC1_STROBE	J43	CONN.USDHC1.STROBE	CONN.NAND.CE1_B		LSIO.GPIO5.IO23	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
161	MIPI_CSI1_CLK_N	BH16	MIPI_CSI1.CKN							VDD_MIPI_CSI_1P8
163	MIPI_CSI1_CLK_P	BJ17	MIPI_CSI1.CKP							VDD_MIPI_CSI_1P8
173	MIPI_DSI1_I2C0_SCL	BE27	MIPI_DSI1.I2C0.SCL			LSIO.GPIO1.IO20	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
175	MIPI_DSI1_I2C0_SDA	BG25	MIPI_DSI1.I2C0.SDA			LSIO.GPIO1.IO21	GPIO	ALT0	PD	VDD_MIPI_DSI_DIG_3P3
177	ESAI0_TX0	BA9	AUD.ESAI0.TX0			LSIO.GPIO2.IO26	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
179	ESAI0_TX1	BA7	AUD.ESAI0.TX1			LSIO.GPIO2.IO27	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
181	ESAI0_TX2_RX3	AU9	AUD.ESAI0.TX2_RX3			LSIO.GPIO2.IO28	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
183	ESAI0_TX3_RX2	BC5	AUD.ESAI0.TX3_RX2			LSIO.GPIO2.IO29	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
185	ESAI0_TX4_RX1	AV8	AUD.ESAI0.TX4_RX1			LSIO.GPIO2.IO30	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
187	ESAI0_TX5_RX0	AU7	AUD.ESAI0.TX5_RX0			LSIO.GPIO2.IO31	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
191	MCLK_IN0	BC3	AUD.ACM.MCLK_IN0	AUD.ESAI0.RX_HF_CLK		LSIO.GPIO3.IO00	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
193	SPI3_SDO	BF2	DMA.SPI3.SDO	DMA.FTM.CH0		LSIO.GPIO2.IO18	GPIO	ALT0	Drive-1	VDD_ESAI1_SPI_SPDIF_3P3
195	ESAI0_SCKR	BB8	AUD.ESAI0.SCKR			LSIO.GPIO2.IO24	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
197	ESAI0_SCKT	AY8	AUD.ESAI0.SCKT			LSIO.GPIO2.IO25	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
201	SIM0_POWER_EN	AT48	DMA.SIM0.POWER_EN	DMA.I2C3.SDA		LSIO.GPIO0.IO04	GPIO	ALT0	Drive-0	VDD_SIM_3P3
203	SIM0_PD	AL43	DMA.SIM0.PD	DMA.I2C3.SCL		LSIO.GPIO0.IO03	GPIO	ALT0	PD	VDD_SIM_3P3
205	HDMI_TX0_DDC_SDA	BN5	HDMI_TX0.DDC_SDA							VDD_HDMI_TX0_1P8
207	HDMI_TX0_DDC_SCL	BG1	HDMI_TX0.DDC_SCL							VDD_HDMI_TX0_1P8
209	GPT1_CAPTURE	AY50	LSIO.GPT1.CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
211	GPT1_CLK	BA53	LSIO.GPT1.CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
215	SPDIF0_TX	BC9	AUD.SPDIF0.TX	AUD.MQS.L	AUD.ACM.MCLK_OUT1	LSIO.GPIO2.IO15	GPIO	ALT0	Drive-0	VDD_ESAI1_SPI_SPDIF_3P3
217	SPDIF0_RX	BC7	AUD.SPDIF0.RX	AUD.MQS.R	AUD.ACM.MCLK_IN1	LSIO.GPIO2.IO14	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3
221	SPI0_SCK	BB4	DMA.SPI0.SCK	AUD.SAI0.RXC		LSIO.GPIO3.IO02	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
223	SPI0_SDI	BA5	DMA.SPI0.SDI	AUD.SAI0.RXD		LSIO.GPIO3.IO04	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
225	SPI0_SDO	AY6	DMA.SPI0.SDO	AUD.SAI0.TXD		LSIO.GPIO3.IO03	GPIO	ALT0	Drive-1	VDD_SPI_SAI_3P3
227	SPI0_CS0	BC1	DMA.SPI0.CS0	AUD.SAI0.RXFS		LSIO.GPIO3.IO05	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
229	SPI2_SDI	AY4	DMA.SPI2.SDI			LSIO.GPIO3.IO09	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
231	SPI2_SDO	BA1	DMA.SPI2.SDO			LSIO.GPIO3.IO08	GPIO	ALT0	Drive-1	VDD_SPI_SAI_3P3
233	SPI2_CS0	AW1	DMA.SPI2.CS0			LSIO.GPIO3.IO10	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
235	SPI2_SCK	AW5	DMA.SPI2.SCK			LSIO.GPIO3.IO07	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
239	LVDS1_GPIO00	BD34	LVDS1.GPIO0.IO00	LVDS1.PWM0.OUT		LSIO.GPIO1.IO10	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
243	ENET1_RGMII_RXD3	E53	CONN.ENET1.RGMII_RXD3	DMA.UART3.RX	VPU.TSI_S1.CLK	LSIO.GPIO6.IO21	GPIO	ALT0	PD	VDD_ENET1_3P3
245	ENET1_RGMII_RXD2	D52	CONN.ENET1.RGMII_RXD2	CONN.ENET1.RMII_RX_ER	VPU.TSI_S0.CLK	LSIO.GPIO6.IO20	GPIO	ALT0	PD	VDD_ENET1_3P3
247	ENET1_RGMII_RXD1	C51	CONN.ENET1.RGMII_RXD1		VPU.TSI_S0.DATA	LSIO.GPIO6.IO19	GPIO	ALT0	PD	VDD_ENET1_3P3

X1 Pin	i.MX 8 Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	Type	Default Mode	Reset State	Power Block
249	ENET1_RGMII_RXD0	E51	CONN.ENET1.RGMII_RXD0		VPU.TSI_S0.SYNC	LSIO.GPIO6.IO18	GPIO	ALT0	PD	VDD_ENET1_3P3
251	ENET1_MDIO	C13	CONN.ENET1.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO17	GPIO	ALT0	PD	VDD_ENET_MDIO_3P3
253	ENET1_MDC	A13	CONN.ENET1.MDC	DMA.I2C4.SCL		LSIO.GPIO4.IO18	GPIO	ALT0	Drive-0	VDD_ENET_MDIO_3P3
255	ENET1_RGMII_TXD2	G47	CONN.ENET1.RGMII_TXD2	DMA.UART3.TX	VPU.TSI_S1.VID	LSIO.GPIO6.IO14	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
257	ENET1_RGMII_TXD1	C47	CONN.ENET1.RGMII_TXD1			LSIO.GPIO6.IO13	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
259	ENET1_RGMII_TXD0	A49	CONN.ENET1.RGMII_TXD0			LSIO.GPIO6.IO12	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
261	ENET1_RGMII_TXC	D46	CONN.ENET1.RGMII_TXC	CONN.ENET1.RCLK50M_OUT	CONN.ENET1.RCLK50M_IN	LSIO.GPIO6.IO10	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
263	ENET1_RGMII_TX_CTL	B48	CONN.ENET1.RGMII_TX_CTL			LSIO.GPIO6.IO11	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
265	ENET1_RGMII_RX_CTL	E49	CONN.ENET1.RGMII_RX_CTL		VPU.TSI_S0.VID	LSIO.GPIO6.IO17	GPIO	ALT0	PD	VDD_ENET1_3P3
269	ENET1_REFCLK_125M_25M	A11	CONN.ENET1.REFCLK_125M_25M	CONN.ENET1.PPS		LSIO.GPIO4.IO16	GPIO	ALT0	Drive-0	VDD_ENET_MDIO_3P3
271	ESAI0_FSR	AW9	AUD.ESAI0.FSR			LSIO.GPIO2.IO22	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
273	ESAI0_FST	BG9	AUD.ESAI0.FST			LSIO.GPIO2.IO23	GPIO	ALT0	PD	VDD_ESAI0_MCLK_3P3
275	SIM0_GPIO0_00	AP46	DMA.SIM0.POWER_EN			LSIO.GPIO0.IO05	GPIO	ALT0	Drive-0	VDD_SIM_3P3
277	SIM0_RST	AP48	DMA.SIM0.RST			LSIO.GPIO0.IO01	GPIO	ALT0	Drive-0	VDD_SIM_3P3
279	SIM0_CLK	AL45	DMA.SIM0.CLK			LSIO.GPIO0.IO00	GPIO	ALT0	Drive-0	VDD_SIM_3P3
281	LVDS1_I2C0_SCL	BL35	LVDS1.I2C0.SCL	LVDS1.GPIO0.IO02		LSIO.GPIO1.IO12	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
283	LVDS1_I2C0_SDA	BE33	LVDS1.I2C0.SDA	LVDS1.GPIO0.IO03		LSIO.GPIO1.IO13	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
287	QSPI1A_DATA0	D12	LSIO.QSPI1A.DATA0			LSIO.GPIO4.IO26	GPIO	ALT0	PD	VDD_QSPI1A_3P3
289	QSPI1A_DATA1	D14	LSIO.QSPI1A.DATA1			LSIO.GPIO4.IO25	GPIO	ALT0	PD	VDD_QSPI1A_3P3
291	QSPI1A_DATA2	E13	LSIO.QSPI1A.DATA2			LSIO.GPIO4.IO24	GPIO	ALT0	PD	VDD_QSPI1A_3P3
293	QSPI1A_DATA3	E11	LSIO.QSPI1A.DATA3			LSIO.GPIO4.IO23	GPIO	ALT0	PD	VDD_QSPI1A_3P3
295	QSPI1A_SS0_B	J11	LSIO.QSPI1A.SS0_B			LSIO.GPIO4.IO19	GPIO	ALT0	PD	VDD_QSPI1A_3P3
297	QSPI1A_DQS	H12	LSIO.QSPI1A.DQS			LSIO.GPIO4.IO22	GPIO	ALT0	PD	VDD_QSPI1A_3P3
299	QSPI1A_SS1_B	G11	LSIO.QSPI1A.SS1_B			LSIO.GPIO4.IO20	GPIO	ALT0	PD	VDD_QSPI1A_3P3
301	QSPI1A_SCLK	F10	LSIO.QSPI1A.SCLK			LSIO.GPIO4.IO21	GPIO	ALT0	PD	VDD_QSPI1A_3P3
305	ADC_IN0	AP10	DMA.ADC.IN0		LSIO.KPP0.COL0	LSIO.GPIO3.IO18	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
307	ADC_IN1	AN11	DMA.ADC.IN1		LSIO.KPP0.COL1	LSIO.GPIO3.IO19	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
309	ADC_IN2	AP8	DMA.ADC.IN2		LSIO.KPP0.COL2	LSIO.GPIO3.IO20	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
311	ADC_IN3	AR9	DMA.ADC.IN3	DMA.SPI1.SCK	LSIO.KPP0.COL3	LSIO.GPIO3.IO21	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
315	ADC_IN4	AN9	DMA.ADC.IN4	DMA.SPI1.SDO	LSIO.KPP0.ROW0	LSIO.GPIO3.IO22	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
317	ADC_IN5	AR7	DMA.ADC.IN5	DMA.SPI1.SDI	LSIO.KPP0.ROW1	LSIO.GPIO3.IO23	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
319	ADC_IN6	AL9	DMA.ADC.IN6	DMA.SPI1.CS0	LSIO.KPP0.ROW2	LSIO.GPIO3.IO24	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
321	ADC_IN7	AP6	DMA.ADC.IN7	DMA.SPI1.CS1	LSIO.KPP0.ROW3	LSIO.GPIO3.IO25	Analog/ GPIO	ALT0	PD	VDD_ADC_1P8 **(only 1.8V)**
2	GPT1_COMPARE	BA51	LSIO.GPT1.COMPARE	LSIO.PWM2.OUT	LSIO.KPP0.ROW5	LSIO.GPIO0.IO19	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
4	GPT0_COMPARE	AW53	LSIO.GPT0.COMPARE	LSIO.PWM3.OUT	LSIO.KPP0.COL6	LSIO.GPIO0.IO16	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
6	UART0_RTS_B	AU45	DMA.UART0.RTS_B	LSIO.PWM0.OUT	DMA.UART2.RX	LSIO.GPIO0.IO22	GPIO	ALT0	Drive-1	VDD_M4_GPT_UART_3P3
8	UART0_CTS_B	AW49	DMA.UART0.CTS_B	LSIO.PWM1.OUT	DMA.UART2.TX	LSIO.GPIO0.IO23	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3

X1 Pin	i.MX 8 Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	Type	Default Mode	Reset State	Power Block
12	FLEXCAN0_RX	C5	DMA.FLEXCAN0.RX			LSIO.GPIO3.IO29	GPIO	ALT0	PD	VDD_FLEXCAN_3P3
14	FLEXCAN0_TX	H6	DMA.FLEXCAN0.TX			LSIO.GPIO3.IO30	GPIO	ALT0	Drive-1	VDD_FLEXCAN_3P3
16	FLEXCAN1_RX	E5	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31	GPIO	ALT0	PD	VDD_FLEXCAN_3P3
18	FLEXCAN1_TX	G7	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00	GPIO	ALT0	Drive-1	VDD_FLEXCAN_3P3
60	USB_OTG1_VBUS	A39	CONN.USB_OTG1.VBUS							VDD_USB_OTG1_3P3
62	PCIE1_RX0_P	A21	HSIO.PCIE1.RX0_P							VDD_PCIE_CLEAN_1P8
64	PCIE1_RX0_N	B22	HSIO.PCIE1.RX0_N							VDD_PCIE_CLEAN_1P8
68	PCIE1_TX0_P	B24	HSIO.PCIE1.TX0_P							VDD_PCIE_CLEAN_1P8
70	PCIE1_TX0_N	C25	HSIO.PCIE1.TX0_N							VDD_PCIE_CLEAN_1P8
72	USB_OTG1_ID	A37	CONN.USB_OTG1.ID							VDD_USB_OTG1_3P3
74	USB_OTG1_DP	B40	CONN.USB_OTG1.DP							VDD_USB_OTG1_3P3
76	USB_OTG1_DN	C39	CONN.USB_OTG1.DN							VDD_USB_OTG1_3P3
84	USB_SS3_TC1	L9	DMA.I2C1.SCL	CONN.USB_OTG2.PWR		LSIO.GPIO4.IO04	GPIO	ALT0	PD	VDD_USB_SS3_3P3
92	USB_SS3_RX_N	B34	CONN.USB_SS3.RX_M_LN_0							VDD_USB_SS3_1P8
94	USB_SS3_RX_P	C35	CONN.USB_SS3.RX_P_LN_0							VDD_USB_SS3_1P8
96	USB_SS3_TC3	H10	DMA.I2C1.SDA	CONN.USB_OTG2.OC		LSIO.GPIO4.IO06	GPIO	ALT0	PD	VDD_USB_SS3_3P3
98	USB_OTG2_DP	B38	CONN.USB_OTG2.DP							VDD_USB_OTG2_3P3
100	USB_OTG2_DN	C37	CONN.USB_OTG2.DM							VDD_USB_OTG2_3P3
104	USB_SS3_TX_N	B32	CONN.USB_SS3.TX_M_LN_0							VDD_USB_SS3_1P8
106	USB_SS3_TX_P	A33	CONN.USB_SS3.TX_P_LN_0							VDD_USB_SS3_1P8
110	M40_I2C0_SCL	AM44	M40.I2C0.SCL	M40.UART0.RX	M40.GPIO0.IO02	LSIO.GPIO0.IO06	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
112	UART1_TX	AY48	DMA.UART1.TX	DMA.SPI3.SCK		LSIO.GPIO0.IO24	GPIO	ALT0	Drive-1	VDD_M4_GPT_UART_3P3
114	UART1_RTS_B	AR43	DMA.UART1.RTS_B	DMA.SPI3.SDI	DMA.UART1.CTS_B	LSIO.GPIO0.IO26	GPIO	ALT0	Drive-1	VDD_M4_GPT_UART_3P3
116	UART1_CTS_B	AV46	DMA.UART1.CTS_B	DMA.SPI3.CS0	DMA.UART1.RTS_B	LSIO.GPIO0.IO27	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
118	UART1_RX	AT44	DMA.UART1.RX	DMA.SPI3.SDO		LSIO.GPIO0.IO25	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
120	M40_I2C0_SDA	AU51	M40.I2C0.SDA	M40.UART0.TX	M40.GPIO0.IO03	LSIO.GPIO0.IO07	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
122	M41_I2C0_SDA	AU49	M41.I2C0.SDA	M41.UART0.TX	M41.GPIO0.IO03	LSIO.GPIO0.IO11	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
124	M41_I2C0_SCL	AR45	M41.I2C0.SCL	M41.UART0.RX	M41.GPIO0.IO02	LSIO.GPIO0.IO10	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
126	LVDS1_I2C1_SCL	BD32	LVDS1.I2C1.SCL	DMA.UART3.TX		LSIO.GPIO1.IO14	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
128	ENET1_RGMII_TXD3	D48	CONN.ENET1.RGMII_TXD3	DMA.UART3.RTS_B	VPU.TSI_S1.SYNC	LSIO.GPIO6.IO15	GPIO	ALT0	Drive-0	VDD_ENET1_3P3
130	ENET1_RGMII_RXC	B50	CONN.ENET1.RGMII_RXC	DMA.UART3.CTS_B	VPU.TSI_S1.DATA	LSIO.GPIO6.IO16	GPIO	ALT0	PD	VDD_ENET1_3P3
132	LVDS1_I2C1_SDA	BN35	LVDS1.I2C1.SDA	DMA.UART3.RX		LSIO.GPIO1.IO15	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
134	UART0_TX	AV48	DMA.UART0.TX			LSIO.GPIO0.IO21	GPIO	ALT0	Drive-1	VDD_M4_GPT_UART_3P3
136	UART0_RX	AV50	DMA.UART0.RX			LSIO.GPIO0.IO20	GPIO	ALT0	PD	VDD_M4_GPT_UART_3P3
138	LVDS0_I2C1_SCL	BE37	LVDS0.I2C1.SCL	DMA.UART2.TX		LSIO.GPIO1.IO08	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
140	LVDS0_I2C1_SDA	BE35	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
144	USDHC1_DATA2	E39	CONN.USDHC1.DATA2	CONN.NAND.DQS_N		LSIO.GPIO5.IO17	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
146	USDHC1_DATA3	F40	CONN.USDHC1.DATA3	CONN.NAND.DQS_P		LSIO.GPIO5.IO18	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
148	USDHC1_DATA4	H40	CONN.USDHC1.DATA4	CONN.NAND.CE0_B		LSIO.GPIO5.IO19	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
150	USDHC1_CMD	G41	CONN.USDHC1.CMD			LSIO.GPIO5.IO14	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
152	USDHC1_DATA5	G43	CONN.USDHC1.DATA5	CONN.NAND.RE_B		LSIO.GPIO5.IO20	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
154	USDHC1_CLK	J39	CONN.USDHC1.CLK				GPIO	ALT0	Drive-0	VDD_USDHC1_1P8_3P3
156	USDHC1_DATA6	F42	CONN.USDHC1.DATA6	CONN.NAND.WE_B	CONN.USDHC1.WP	LSIO.GPIO5.IO21	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
158	USDHC1_DATA7	H42	CONN.USDHC1.DATA7	CONN.NAND.ALE	CONN.USDHC1.CD_B	LSIO.GPIO5.IO22	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
160	USDHC1_DATA0	E37	CONN.USDHC1.DATA0	CONN.NAND.RE_N		LSIO.GPIO5.IO15	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
162	USDHC1_DATA1	F38	CONN.USDHC1.DATA1	CONN.NAND.RE_P		LSIO.GPIO5.IO16	GPIO	ALT0	PD	VDD_USDHC1_1P8_3P3
164	ESAI1_TX1	BA11	AUD.ESAI1.TX1	AUD.SAI2.RXFS		LSIO.GPIO2.IO09	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3

X1 Pin	i.MX 8 Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	Type	Default Mode	Reset State	Power Block
176	USDHC2_DATA2	L45	CONN.USDHC2.DATA2	DMA.UART4.CTS_B		LSIO.GPIO5.IO28	GPIO	ALT0	PD	VDD_USDHC2_1P8_3P3
178	USDHC2_DATA3	J45	CONN.USDHC2.DATA3	DMA.UART4.RTS_B		LSIO.GPIO5.IO29	GPIO	ALT0	PD	VDD_USDHC2_1P8_3P3
180	USDHC2_CMD	H44	CONN.USDHC2.CMD	AUD.MQS.L		LSIO.GPIO5.IO25	GPIO	ALT0	PD	VDD_USDHC2_1P8_3P3
184	USDHC2_CLK	F46	CONN.USDHC2.CLK	AUD.MQS.R		LSIO.GPIO5.IO24	GPIO	ALT0	Drive-0	VDD_USDHC2_1P8_3P3
186	USDHC2_DATA0	H48	CONN.USDHC2.DATA0	DMA.UART4.RX		LSIO.GPIO5.IO26	GPIO	ALT0	PD	VDD_USDHC2_1P8_3P3
188	USDHC2_DATA1	G45	CONN.USDHC2.DATA1	DMA.UART4.TX		LSIO.GPIO5.IO27	GPIO	ALT0	PD	VDD_USDHC2_1P8_3P3
190	USDHC2_CD_B	B8	CONN.USDHC2.CD_B			LSIO.GPIO4.IO12	GPIO	ALT0	PD	USDHC2_CD_B
194	SPI3_SDI	BE5	DMA.SPI3.SDI	DMA.FTM.CH1		LSIO.GPIO2.IO19	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3
196	SAI1_RXC	AV6	AUD.SAI1.RXC	AUD.SAI0.TXD		LSIO.GPIO3.IO12	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
198	ESAI1_SCKT	AY10	AUD.ESAI1.SCKT	AUD.SAI2.RXC		LSIO.GPIO2.IO07	GPIO	ALT0	PD	VDD_ESAI1_SPI_SPDIF_3P3
200	SPI0_CS1	BA3	DMA.SPI0.CS1	AUD.SAI0.TXC		LSIO.GPIO3.IO06	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
202	SAI1_RXFS	AU3	AUD.SAI1.RXFS	AUD.SAI0.RXD		LSIO.GPIO3.IO14	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
204	SPI2_CS1	AY2	DMA.SPI2.CS1	AUD.SAI0.TXFS		LSIO.GPIO3.IO11	GPIO	ALT0	PD	VDD_SPI_SAI_3P3
220	HDMI_TX0_CEC	BJ1	HDMI_TX0.CEC							VDD_HDMI_TX0_1P8
222	HDMI_TX0_DATA2_EDP0_P	BL9	HDMI_TX0.TX_P_LN_0							VDD_HDMI_TX0_1P8
224	HDMI_TX0_DATA2_EDP0_N	BM8	HDMI_TX0.TX_M_LN_0							VDD_HDMI_TX0_1P8
228	HDMI_TX0_DATA1_EDP1_P	BL7	HDMI_TX0.TX_P_LN_1							VDD_HDMI_TX0_1P8
230	HDMI_TX0_DATA1_EDP1_N	BM6	HDMI_TX0.TX_M_LN_1							VDD_HDMI_TX0_1P8
232	HDMI_TX0_HPD	BH8	HDMI_TX0.HPD							VDD_HDMI_TX0_1P8
234	HDMI_TX0_DATA0_EDP2_P	BL5	HDMI_TX0.TX_P_LN_2							VDD_HDMI_TX0_1P8
236	HDMI_TX0_DATA0_EDP2_N	BM4	HDMI_TX0.TX_M_LN_2							VDD_HDMI_TX0_1P8
240	HDMI_TX0_CLK_EDP3_P	BL3	HDMI_TX0.TX_P_LN_3							VDD_HDMI_TX0_1P8
242	HDMI_TX0_CLK_EDP3_N	BK2	HDMI_TX0.TX_M_LN_3							VDD_HDMI_TX0_1P8
246	LVDS1_CH0_CLK_N	BK36	LVDS1.T0CLKN							VDD_LVDS0_1P8
248	LVDS1_CH0_CLK_P	BM36	LVDS1.T0CLKP							VDD_LVDS0_1P8
252	LVDS1_CH0_TX0_N	BL37	LVDS1.T0AN							VDD_LVDS0_1P8
254	LVDS1_CH0_TX0_P	BN37	LVDS1.T0AP							VDD_LVDS0_1P8
258	LVDS1_CH0_TX1_N	BK38	LVDS1.T0BN							VDD_LVDS0_1P8
260	LVDS1_CH0_TX1_P	BM38	LVDS1.T0BP							VDD_LVDS0_1P8
262	USB_SS3_TC2	F8	DMA.I2C1.SDA	CONN.USB_OTG1.OC		LSIO.GPIO4.IO05	GPIO	ALT0	PD	VDD_USB_SS3_3P3
264	LVDS1_CH0_TX2_N	BL39	LVDS1.T0CN							VDD_LVDS0_1P8
266	LVDS1_CH0_TX2_P	BN39	LVDS1.T0CP							VDD_LVDS0_1P8
270	LVDS1_CH0_TX3_N	BK40	LVDS1.T0DN							VDD_LVDS0_1P8
272	LVDS1_CH0_TX3_P	BM40	LVDS1.T0DP							VDD_LVDS0_1P8
274	USB_SS3_TC0	J9	DMA.I2C1.SCL	CONN.USB_OTG1.PWR		LSIO.GPIO4.IO03	GPIO	ALT0	PD	VDD_USB_SS3_3P3
276	LVDS1_CH1_CLK_N	BK34	LVDS1.T1CLKN							VDD_LVDS0_1P8
278	LVDS1_CH1_CLK_P	BM34	LVDS1.T1CLKP							VDD_LVDS0_1P8
282	LVDS1_CH1_TX0_N	BL33	LVDS1.T1AN							VDD_LVDS0_1P8
284	LVDS1_CH1_TX0_P	BN33	LVDS1.T1AP							VDD_LVDS0_1P8
286	LVDS0_GPIO00	BE39	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04	GPIO	ALT0	PD	VDD_LVDS_DIG_3P3
288	LVDS1_CH1_TX1_N	BK32	LVDS1.T1BN							VDD_LVDS0_1P8
290	LVDS1_CH1_TX1_P	BM32	LVDS1.T1BP							VDD_LVDS0_1P8
294	LVDS1_CH1_TX2_N	BL31	LVDS1.T1CN							VDD_LVDS0_1P8
296	LVDS1_CH1_TX2_P	BN31	LVDS1.T1CP							VDD_LVDS0_1P8
300	LVDS1_CH1_TX3_N	BK30	LVDS1.T1DN							VDD_LVDS0_1P8
302	LVDS1_CH1_TX3_P	BM30	LVDS1.T1DP							VDD_LVDS0_1P8

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	3.3V main power supply	Use decoupling capacitors on all pins.
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	Digital Ground	
174	VCC_BACKUP	I/O	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
314, 320	AVCC	I	3.3V Analogue supply	Connect this pin to a 3.3V supply. For better audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the VCC 3.3V input supply.
303, 313, 304, 308	AGND	I	Analogue Ground	Connect this pin to GND. For better audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis iMX8.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
28	RESET_MICO#	I	Reset Input	This pin is low active and resets the Apalis module. This pin is connected to the power manger IC. There is a 100k pull-up resistor on the module.
26	RESET_MOCI#	O	Reset Output	This pin is active low. This pin is driven low at boot up. This is an open drain signal with a 10k pull-up resistor on the module.
24	POWER_ENABLE_MOCI	O	Signal for the carrier board to enable the peripheral voltage rails	More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide

The RESET_MOCI# reset output for the peripherals on the carrier board is generated from the general module reset signal. This reset signal is provided by the power manager IC (RESETBMCU output) and is used for resetting the i.MX 8 SoC as well as other on module peripherals. In order to meet the reset timing requirements of PCI Express, the external reset output RESET_MOCI# needs to be delayed. Figure 6 shows the circuit that is used for delaying the RESET_MOCI# signal. The transistor holds down the external reset signal until the bootloader is releasing the signal by driving the LSIO.GPIO0.IO30 (ball SCU_GPIO0_02) low.

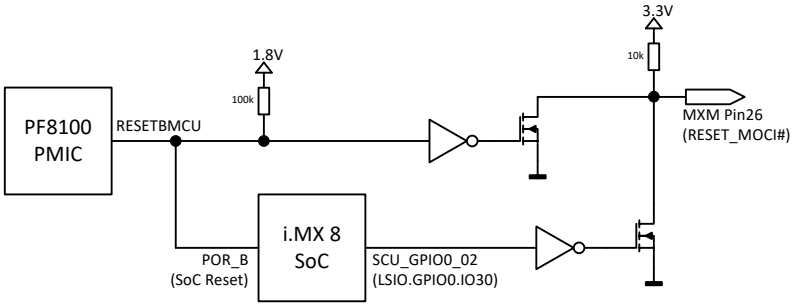

Figure 6 RESET_MOCI# circuit

5.2 GPIOs

The Apalis form factor features 8 dedicated general purpose input output (GPIO) pins. Besides these 8 GPIOs, several pins can be used as GPIO if their primary function is not in use. For compatibility reasons, it is recommended to use the 8 dedicated GPIOs first.

Table 5-4 Dedicated GPIO signals

X1 Pin#	Apalis Standard Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
1	GPIO1	M40_GPIO0_00	LSIO.GPIO0.IO08	I/O	
3	GPIO2	M40_GPIO0_01	LSIO.GPIO0.IO09	I/O	
5	GPIO3	M41_GPIO0_00	LSIO.GPIO0.IO12	I/O	
7	GPIO4	M41_GPIO0_01	LSIO.GPIO0.IO13	I/O	
11	GPIO5	FLEXCAN2_RX	LSIO.GPIO4.IO01	I/O	
13	GPIO6	FLEXCAN2_TX	LSIO.GPIO4.IO02	I/O	
15	GPIO7	MLB_SIG	LSIO.GPIO3.IO26	I/O	
17	GPIO8	MLB_DATA	LSIO.GPIO3.IO28	I/O	

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Apalis module from a suspend state. In the Apalis module standard, pin 37 is the default wakeup source. Only this pin is guaranteed to be wakeup-compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules. The wake signal of the Ethernet PHY is connected to GPIO1.IO05.

Table 5-5 Apalis Wakeup Source

X1 Pin#	Apalis Standard Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
37	WAKE1_MICO	SPI3_CS0	LSIO.GPIO2.IO20	I/O	Standard external wake signal
		LVDS0_GPIO01	LSIO.GPIO1.IO05	I/O	Internal Ethernet PHY wake signal

5.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC is integrated in the i.MX 8 SoC and connected to a separate PHY located on the module, therefore only the magnetics are required on the carrier board. The Micrel KSZ9031 Gigabit Ethernet Transceiver chip is connected via RGMII to the NXP i.MX 8.

The Gigabit Ethernet MAC in the SoC integrates an accurate IEEE 1588 compliant timer for clock synchronization for distributed control nodes used in industrial automation applications. The Ethernet interface supports Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN).

Table 5-6 Ethernet Pins

X1 Pin #	Apalis Signal Name	KSZ9031 Signal Name	I/O	Description	Remarks
50	ETH1_MDI0+	TXRXP_A	I/O	Media Dependent Interface	100BASE-TX: Transmit +
48	ETH1_MDI0-	TXRXM_A	I/O	Media Dependent Interface	100BASE-TX: Transmit -
56	ETH1_MDI1+	TXRXP_B	I/O	Media Dependent Interface	100BASE-TX: Receive +
54	ETH1_MDI1-	TXRXM_B	I/O	Media Dependent Interface	100BASE-TX: Receive -
32	ETH1_MDI2+	TXRXP_C	I/O	Media Dependent Interface	100BASE-TX: Unused
34	ETH1_MDI2-	TXRXM_C	I/O	Media Dependent Interface	100BASE-TX: Unused
38	ETH1_MDI3+	TXRXP_D	I/O	Media Dependent Interface	100BASE-TX: Unused
40	ETH1_MDI3-	TXRXM_D	I/O	Media Dependent Interface	100BASE-TX: Unused
46	ETH+_CTREF	NC	O	Center tap supply	KSZ9031 does not need center tap supply
42	ETH1_ACT	LED1	O	LED indication output	Toggles during RX/TX activity
44	ETH1_LINK	LED2	O	LED indication output	Is low if a link (any speed) is established

The Micrel KSZ9031 does not require a center tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the center tap of the magnetics to pin 46 of the Apalis module. This guarantees the full compatibility with other Apalis modules which require a center tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

The Apalis iMX8 features a second Ethernet port. If this port is required, an additional PHY needs to be implemented on the carrier board. The second MAC in the SoC is able to provide two different interface standards for the connection with the PHY:

- RGMII: Reduced Gigabit Media Independent Interface. This interface allows connecting a Gigabit Ethernet PHY such as a secondary KSZ9031.
- RMII: Reduced Media Independent Interface. This is the preferred mode for interfacing a 10/100 Mbit/s Ethernet PHY such as the KSZ8041.

The secondary RGMII/RMII Ethernet interface is not part of the Apalis standard. Therefore, the signals are not compatible with other Apalis modules. Most of the signals are located on the module edge connector pins which were originally reserved as parallel RGB LCD interface.

The secondary RGMII/RMII Ethernet interface needs special attention regarding the supply voltage level. The RGMII/RMII voltage is switchable through LDO1OUT of the second PMIC PF8100. The voltage level must be defined by software configuration and is turned off during the boot sequence in order to prevent outputting wrong voltage levels to the peripherals during the power up sequence.

If the secondary Ethernet interface is used as RGMII, the output voltages are limited to 1.8V and 2.5V. For RMII and other alternate functions (e.g. GPIO) of these pins, also 3.3V logic level is available. Please note that the ENET1_MDC and ENET1_MDIO are always set to 3.3V, independent of the output voltage settings of the RGMII/RMII signals. This switchable I/O rail was introduced on V1.1 of the Apalis iMX8 module. The V1.0 is only able to output 3.3V. Therefore, the RGMII has to be used with care on these early modules.

Table 5-7 RGMII signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
265	LCD1_R7	ENET1_RGMII_RX_CTL	CONN.ENET1.RGMII_RX_CTL	I	RGMII_RX_CTL
130	UART2_CTS	ENET1_RGMII_RXC	CONN.ENET1.RGMII_RXC	I	RGMII_RXC
249	LCD1_DE	ENET1_RGMII_RXD0	CONN.ENET1.RGMII_RXD0	I	RGMII_RXD0
247	LCD1_HSYNC	ENET1_RGMII_RXD1	CONN.ENET1.RGMII_RXD1	I	RGMII_RXD1
245	LCD1_VSYNC	ENET1_RGMII_RXD2	CONN.ENET1.RGMII_RXD2	I	RGMII_RXD2
243	LCD1_PCLK	ENET1_RGMII_RXD3	CONN.ENET1.RGMII_RXD3	I	RGMII_RXD3
263	LCD1_R6	ENET1_RGMII_TX_CTL	CONN.ENET1.RGMII_TX_CTL	O	RGMII_TX_CTL
261	LCD1_R5	ENET1_RGMII_TXC	CONN.ENET1.RGMII_TXC	O	RGMII_TXC
259	LCD1_R4	ENET1_RGMII_TXD0	CONN.ENET1.RGMII_TXD0	O	RGMII_TXD0
257	LCD1_R3	ENET1_RGMII_TXD1	CONN.ENET1.RGMII_TXD1	O	RGMII_TXD1
255	LCD1_R2	ENET1_RGMII_TXD2	CONN.ENET1.RGMII_TXD2	O	RGMII_TXD2
128	UART2_RTS	ENET1_RGMII_TXD3	CONN.ENET1.RGMII_TXD3	O	RGMII_TXD3
253	LCD1_R1	ENET1_MDC	CONN.ENET1.MDC	O	RMII_MDC
251	LCD1_R0	ENET1_MDIO	CONN.ENET1.MDIO	I/O	RMII_MDIO
269	LCD1_G0	ENET1_REFCLK_125M_25M	CONN.ENET1.REFCLK_125M_25M	I	Optional 125MHz reference clock input
269	LCD1_G0	ENET1_REFCLK_125M_25M	CONN.ENET1.PPS	O	IEEE1588 pulse per second output

Table 5-8 RMII signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
249	LCD1_DE	ENET1_RGMII_RXD0	CONN.ENET1.RGMII_RXD0	I	RMII_RXD0
247	LCD1_HSYNC	ENET1_RGMII_RXD1	CONN.ENET1.RGMII_RXD1	I	RMII_RXD1
245	LCD1_VSYNC	ENET1_RGMII_RXD2	CONN.ENET1.RMII_RX_ER	I	RMII_RXER
259	LCD1_R4	ENET1_RGMII_TXD0	CONN.ENET1.RGMII_TXD0	O	RMII_TXD0
257	LCD1_R3	ENET1_RGMII_TXD1	CONN.ENET1.RGMII_TXD1	O	RMII_TXD1
263	LCD1_R6	ENET1_RGMII_TX_CTL	CONN.ENET1.RGMII_TX_CTL	O	RMII_TXEN
265	LCD1_R7	ENET1_RGMII_RX_CTL	CONN.ENET1.RGMII_RX_CTL	I	RMII_CRS_DV
253	LCD1_R1	ENET1_MDC	CONN.ENET1.MDC	O	RMII_MDC
251	LCD1_R0	ENET1_MDIO	CONN.ENET1.MDIO	I/O	RMII_MDIO
261	LCD1_R5	ENET1_RGMII_TXC	CONN.ENET1.RCLK50M_OUT	O	50MHz Reference clock that is provided from the MAC to the PHY
261	LCD1_R5	ENET1_RGMII_TXC	CONN.ENET1.RCLK50M_IN	I	50MHz Reference clock that is provided from the PHY to the MAC
269	LCD1_G0	ENET1_REFCLK_125M_25M	CONN.ENET1.PPS	O	IEEE1588 pulse per second output

5.4 Wi-Fi and Bluetooth

The Apalis iMX8 is available as a version with on-module Wi-Fi and Bluetooth interfaces. The additional "WB" in the product name indicates that this version features Wi-Fi and Bluetooth. These Apalis module versions are making use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from Azurewave.

Features:

- Wi-Fi 802.11a/b/g/n/ac
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.0 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for dual external antenna in 2x2 configuration, compatible to IPX/IPEX connector MHF4 series
- Pre-certified for CE (Europe), FCC (United States), and IC (Canada)

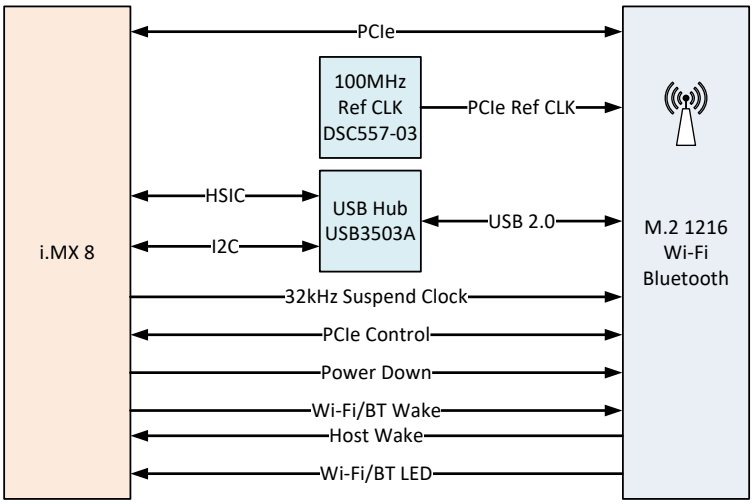

Figure 7: Wi-Fi and Bluetooth block diagram

The Wi-Fi module is connected over a PCI Express interface with the i.MX 8 SoC. The Bluetooth part requires an USB connection. Since the SoC does not have enough USB ports, there is a HSIC USB hub on the Apalis module. The following table contains the interface and control signals between the Azurewave Wi-Fi and Bluetooth module and the i.MX 8 SoC.

Table 5-9 Signal Pins between AW-CM276NF and i.MX 8

AW-CM276NF Pin Name	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
PCIE_RX_P	PCIE1_TX0_P	HSIO.PCIE1.TX0_P	I	PCI Express interface
PCIE_RX_N	PCIE1_TX0_N	HSIO.PCIE1.TX0_N		
PCIE_TX_P	PCIE1_RX0_P	HSIO.PCIE1.RX0_P	O	
PCIE_TX_N	PCIE1_RX0_N	HSIO.PCIE1.RX0_N		
PCIE_WAKEn	PCIE_CTRL1_WAKE_B	HSIO.PCIE1.WAKE_B	I/O	PCIe wake
PCIE_CLKREQn	PCIE_CTRL1_CLKREQ_B	HSIO.PCIE1.CLKREQ_B	I/O	PCIe reference clock request
GPIO[21]	PCIE_CTRL1_PERST_B	HSIO.PCIE1.PERST_B	I	PCIe reset
SLP_CLK	SCU_GPIO0_07	SCU.DSC.RTC_ CLOCK_OUTPUT_32K	I	32.768kHz sleep clock input for low power operation
PDn	MIPI_CSI0_GPIO0_01	LSIO.GPIO1.IO28	I	0 = full power-down, 1 = normal mode
GPIO[22]	MIPI_CSI0_MCLK_OUT	LSIO.GPIO1.IO24	I	Wireless Disable Input (active low)
GPIO[14]	MIPI_CSI0_I2C0_SCL	LSIO.GPIO1.IO25	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output
GPIO[13]	MIPI_CSI0_GPIO0_00	LSIO.GPIO1.IO27	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output
GPIO[15]	MIPI_CSI1_GPIO0_01	LSIO.GPIO1.IO31	I	HOST_WKUP_WLAN : SoC to AW-CM276NF Wi-Fi Wakeup
GPIO[12]	MIPI_CSI0_I2C0_SDA	LSIO.GPIO1.IO26	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup
GPIO[2]	MIPI_CSI1_I2C0_SCL	LSIO.GPIO2.IO00	O	Wi-Fi activity LED
GPIO[3]	MIPI_CSI1_I2C0_SDA	LSIO.GPIO2.IO01	O	Bluetooth activity LED

The AW-CM276NF features four wake signals. Two are input signals (one for the Wi-Fi and one for Bluetooth) which allow for waking up the radio. The other two wake signals are an output of the AW-CM276NF which are used by the Wi-Fi and Bluetooth receiver to wake up the system (SoC).

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. Please contact Toradex about how to certify the Apalis iMX8 WB: Contact your local sales office or support@toradex.com.

The Wi-Fi and Bluetooth module features a power down signal. With this signal, the wireless module can be shut down completely. After re-enabling the module, the firmware for the AW-CM276NF has to be downloaded again.

5.5 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.0 SuperSpeed (backward compatible) and two USB 2.0 High-Speed interfaces. The i.MX 8 SoC on the other hand features only one USB 3.0 port with SuperSpeed signals and a second USB 2.0 High-Speed interface with integrated PHY. Additional to these two USB ports, the i.MX 8 features a third USB port with an HSIC (High-Speed Inter-Chip) interface. This interface is used for the USB3503A HSIC USB Hub. This hub provides an additional three USB ports and is located on the module. Two ports are accessible as USB_H2 and USB_H3, while the third one is used for the Bluetooth interface of the Wi-Fi module.

Since the i.MX 8 features only one USB port with SuperSpeed signals, the USB 3.0 functionality is only available on the USB_H4 port of the Apalis form factor. The USB_O1 port does not feature the SuperSpeed signals, only USB High-Speed is available. However, on modules which do not have the Wi-Fi/Bluetooth module assembled, the SuperSpeed signals of the USB_O1 port are used for

providing the secondary PCIe port (PCIE1). The PCIe signals on these pins cannot be used for USB 3.0 SuperSpeed, they can only be used as secondary PICe port, independently on the actual function of the USB_O1 port.

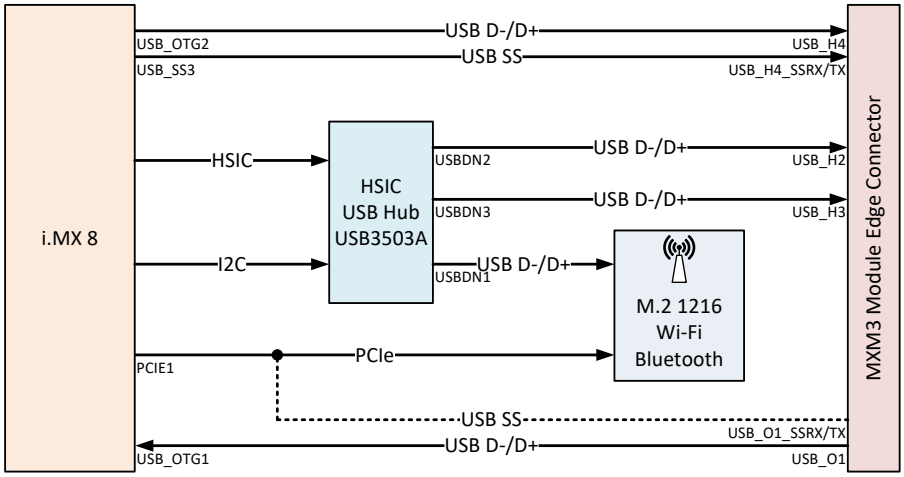

Figure 8: USB block diagram

5.5.1 USB Data Signal

Table 5-10 USBO1 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
74	USBO1_D+	USB_OTG1_DP	CONN.USB_OTG1.DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB_OTG1_DN	CONN.USB_OTG1.DN	I/O	Negative Differential USB Signal, OTG capable
62	USBO1_SSRX+	PCIE1_RX0_P	HSIO.PCIE1.RX0_P	I	**Not connected on modules with Wi-Fi.** No USB SuperSpeed function, only PCIe receive data for secondary PICe interface
64	USBO1_SSRX-	PCIE1_RX0_N	HSIO.PCIE1.RX0_N	I	
68	USBO1_SSTX+	PCIE1_TX0_P	HSIO.PCIE1.TX0_P	O	**Not connected on modules with Wi-Fi.** No USB SuperSpeed function, only PCIe transmit data for secondary PICe interface
70	USBO1_SSTX-	PCIE1_TX0_N	HSIO.PCIE1.TX0_N	O	

Table 5-11 USBH2 Data Pins

X1 Pin#	Apalis Std Function	USB3503A Ball Name	I/O	Description
80	USBH2_D+	USBDN2_DP	I/O	Positive Differential USB Signal
82	USBH2_D-	USBDN2_DM	I/O	Negative Differential USB Signal

Table 5-12 USBH3 Data Pins

X1 Pin#	Apalis Std Function	USB3503A Ball Name	I/O	Description
86	USBH3_D+	USBDN3_DP	I/O	Positive Differential USB Signal
88	USBH3_D-	USBDN3_DM	I/O	Negative Differential USB Signal

Table 5-13 USBH4 Data Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
98	USBH4_D+	USB_OTG2_DP	CONN.USB_OTG2.DP	I/O	Positive Differential USB Signal
100	USBH4_D-	USB_OTG2_DN	CONN.USB_OTG2.DM	I/O	Negative Differential USB Signal

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
94	USBH4_SSRX+	USB_SS3_RX_P	CONN.USB_SS3.RX_P_LN_0	I	Positive differential receiving host signal for USB3.0
92	USBH4_SSRX-	USB_SS3_RX_N	CONN.USB_SS3.RX_M_LN_0	I	Negative differential receiving host signal for USB3.0
106	USBH4_SSTX+	USB_SS3_TX_P	CONN.USB_SS3.TX_P_LN_0	O	Positive differential transmission host signal for USB3.0
104	USBH4_SSTX-	USB_SS3_TX_N	CONN.USB_SS3.TX_M_LN_0	O	Negative differential transmission host signal for USB3.0

5.5.2 USB Control Signals

Table 5-14 USB OTG Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
72	USBO1_ID	USB_OTG1_ID	CONN.USB_OTG1.ID	I	Use this pin to detect the ID pin if you use USB OTG.
60	USBO1_VBUS	USB_OTG1_VBUS	CONN.USB_OTG1.VBUS	I	Use this pin to detect if VBUS is present.

If you use the USB Host function you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis iMX8 provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. The USBH2, USBH3, and USBH4 interfaces share the bus power control signals whereas USBO1 has its own dedicated control signals.

Table 5-15 USB Power Control Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
274	USBO1_EN	USB_SS3_TC0	CONN.USB_OTG1.PWR	O	This pin enables the external USB voltage supply for the USBO1 interface.
262	USBO1_OC#	USB_SS3_TC2	CONN.USB_OTG1.OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBO1 interface.
84	USBH_EN	USB_SS3_TC1	CONN.USB_OTG2.PWR	O	This pin enables the external USB voltage supply for the USBH2, USBH3, and USBH4 interfaces.
96	USBH_OC#	USB_SS3_TC3	CONN.USB_OTG2.OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USBH2, USBH3, and USBH4 interfaces.

5.6 Display

The i.MX 8 features two independent (identical) display controllers. Each display controller has two outputs which are routed to the different display outputs such as HDMI, DisplayPort (DP), LVDS, and MIPI/DSI. This allows to drive up to four independent displays (1x HDMI or DP, 2x LVDS, 1x MIPI/DSI).

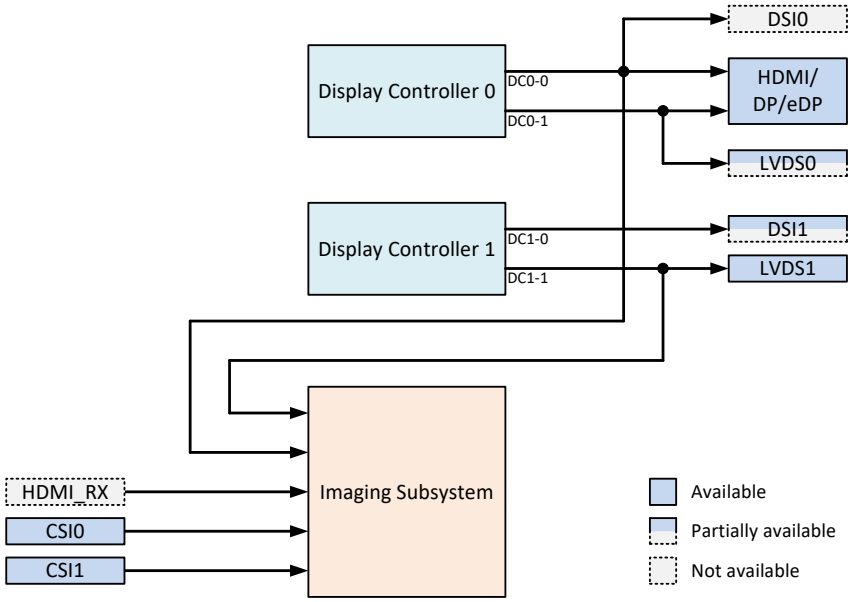

Figure 9: Display and imaging block diagram

The routing of the display outputs comes with some limitation. If the HDMI/DP runs with 4K60 resolution, it requires both output ports of the display controller 0. This means the DSI0 and the LVDS0 cannot be used. Conversely, if either DSI0 or LVDS0 are used, the HDMI/DP are limited to 4K30. The Imaging Subsystem loopback is only available on LVDS1, not on LVDS0. A second loopback is only available on DSI0 or HDMI 4K30, not on DSI1 or HDMI 4K60.

Due to the limited number of interface pins on the module edge connector, not all display interfaces of the i.MX 8 SoC are available externally. The HDMI/DP/eDP interface and the LVDS1 port are fully available. Only one channel of the LVDS0 port is available. DSI0 is not available at all while just one lane of the DSI1 is available on the module edge connector. Besides the two loopback inputs, the Imaging Subsystem has also two MIPI/CSI-2 and an HDMI input. The two MIPI/CSI-2 camera inputs are available on type specific pins. However, the HDMI_RX is not available on the Apalis iMX8 module.

5.6.1 Parallel RGB LCD interface

The Apalis iMX8 does not feature a parallel RGB LCD interface. Nevertheless, it is possible to implement an LVDS or DSI to RGB converter on the carrier board in order to attach such a display.

5.6.2 LVDS

The official name for the LVDS interface is actually FPD-Link or FlatLink which uses the low voltage differential signalling (LVDS) technology. However, very often this interface is simply called LVDS.

The LVDS interface serialises the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to Seven parallel signals. For an 18-bit RGB interface including the control signals (Display Enable, Vertical, and Horizontal Synch), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional colour bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two colour-mapping standards for the 24-bit interface. The less

common “24-bit / 18-bit compatible” (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each colour into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit colour mapping standard (VESA format, Intel 24.1 LVDS data format) serializes the two most significant bits of each colour into the fourth LVDS pair. This mode is not backward compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this colour mapping. The LVDS interfaces of Apalis iMX8 are configurable to support different colour mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of colour mappings.

Figure 10 shows the LVDS output signals for the “24-bit /18-bit Compatible Colour Mapping” (JEIDA format, Intel 24.0 LVDS data format)

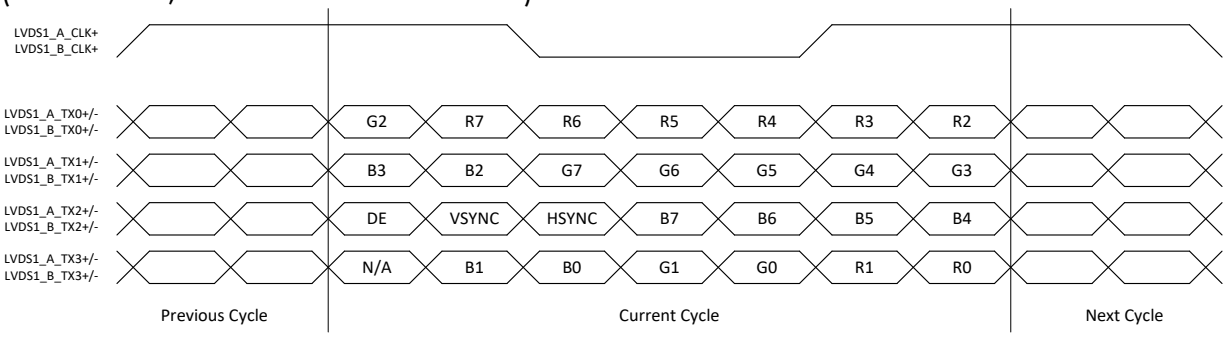

Figure 10: 24-bit / 18-bit Compatible Colour Mapping (Intel 24.0 LVDS Data Format)

Figure 11 shows the LVDS output signals for the common 24-bit colour mapping (VESA format, Intel 24.1 LVDS data format).

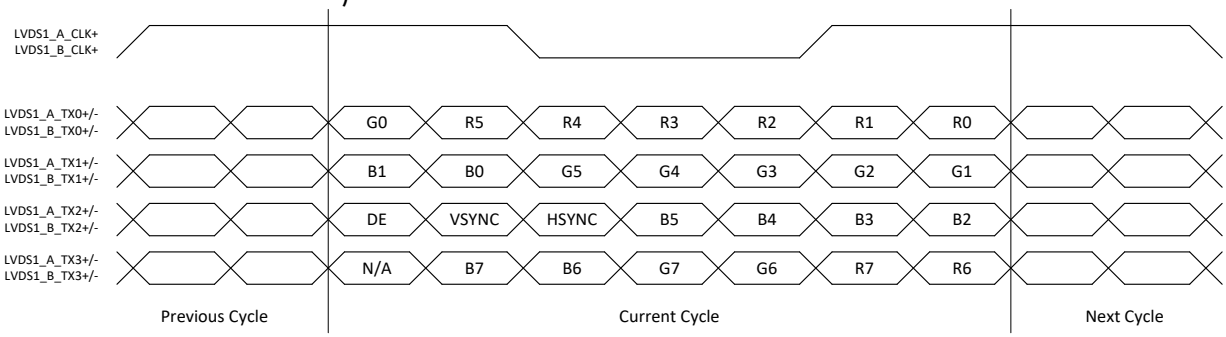

Figure 11: Common 24-bit VESA Colour Mapping (Intel 24.1 LVDS Data Format)

Figure 12 shows the LVDS output signals for the 18-bit interface.

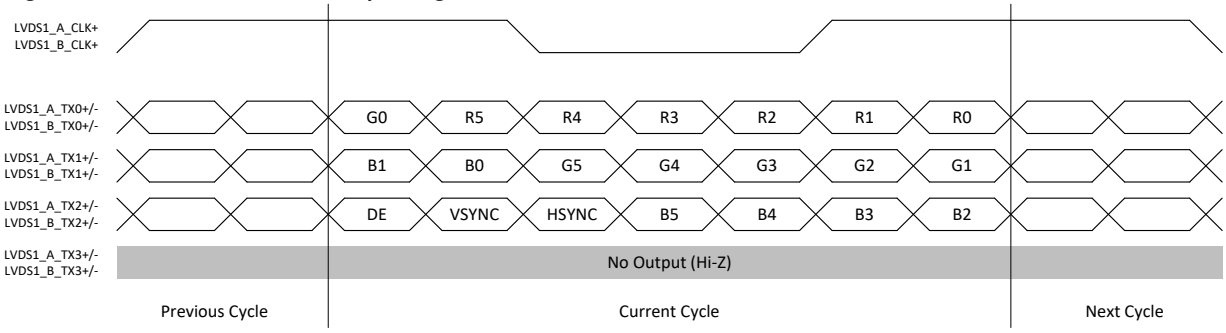

Figure 12: 18-bit Mode

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (85MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual channel configuration, the odd bits are transmitted in the first channel and the even bits

transmitted in the second channel. The dual channel LVDS interface can support resolutions up to 1920x1200 @60fps (170MHz pixel clock maximum).

The i.MX 8 features two dual channel LVDS ports (LVDS0 and LVDS1). Each of the i.MX 8 LVDS ports is capable of outputting up to 1080p60. It is possible to split each LVDS port to two single channel ports. On the Apalis iMX8, the LVDS1 port is available as dual channel LVDS on the Apalis standard pins. Only one single channel LVDS port is available on the Apalis iMX8 module. This means in total, the Apalis iMX8 provides up to three single channel LVDS ports or one dual channel LVDS with one single channel.

Figure 13 shows the possible LVDS display configurations. Even though it is possible to use the LVDS1_CH0 and LVDS0_CH0 interfaces for attaching two single channel displays, it is recommended to use LVDS1_CH0 and LVDS1_CH1 instead. This makes sure the design is compatible with other Apalis modules, since LVDS0_CH0 is on the type-specific area of the module edge connector.

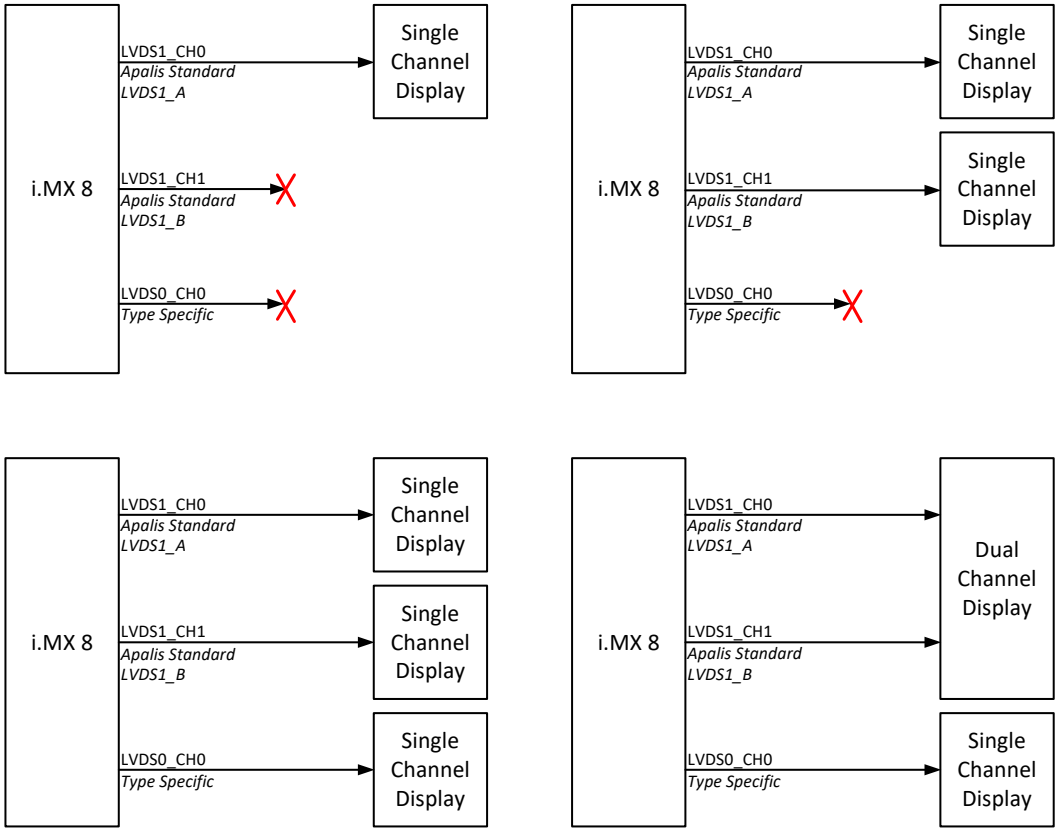

Figure 13: Possible LVDS Display configurations

Table 5-16 LVDS interface signals (Apalis standard)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	I/O	Description
248	LVDS1_A_CLK+	LVDS1_CH0_CLK_P	O	LVDS Clock out for channel A (odd pixels/single channel)
246	LVDS1_A_CLK-	LVDS1_CH0_CLK_N	O	
254	LVDS1_A_TX0+	LVDS1_CH0_TX0_P	O	LVDS data lane 0 for channel A (odd pixels/single channel)
252	LVDS1_A_TX0-	LVDS1_CH0_TX0_N	O	
260	LVDS1_A_TX1+	LVDS1_CH0_TX1_P	O	LVDS data lane 1 for channel A (odd pixels/single channel)
258	LVDS1_A_TX1-	LVDS1_CH0_TX1_N	O	

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	I/O	Description
266	LVDS1_A_TX2+	LVDS1_CH0_TX2_P	O	LVDS data lane 2 for channel A (odd pixels/single channel)
264	LVDS1_A_TX2-	LVDS1_CH0_TX2_N	O	
272	LVDS1_A_TX3+	LVDS1_CH0_TX3_P	O	LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18bit)
270	LVDS1_A_TX3-	LVDS1_CH0_TX3_N	O	
278	LVDS1_B_CLK+	LVDS1_CH1_CLK_P	O	LVDS Clock out for channel B (even pixels/unused for single channel)
276	LVDS1_B_CLK-	LVDS1_CH1_CLK_N	O	
284	LVDS1_B_TX0+	LVDS1_CH1_TX0_P	O	LVDS data lane 0 for channel B (odd pixels/unused for single channel)
282	LVDS1_B_TX0-	LVDS1_CH1_TX0_N	O	
290	LVDS1_B_TX1+	LVDS1_CH1_TX1_P	O	LVDS data lane 1 for channel B (odd pixels/unused for single channel)
288	LVDS1_B_TX1-	LVDS1_CH1_TX1_N	O	
296	LVDS1_B_TX2+	LVDS1_CH1_TX2_P	O	LVDS data lane 2 for channel B (odd pixels/unused for single channel)
294	LVDS1_B_TX2-	LVDS1_CH1_TX2_N	O	
302	LVDS1_B_TX3+	LVDS1_CH1_TX3_P	O	LVDS data lane 3 for channel B (odd pixels/unused for single channel; unused for 18bit)
300	LVDS1_B_TX3-	LVDS1_CH1_TX3_N	O	

Table 5-17 LVDS Interface Signals on Type-specific Pins (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	I/O	Description
61	TS_DIFF1+	LVDS0_CH0_CLK_P		LVDS Clock out
59	TS_DIFF1-	LVDS0_CH0_CLK_N		
67	TS_DIFF2+	LVDS0_CH0_TX0_P	O	LVDS data lane 0
65	TS_DIFF2-	LVDS0_CH0_TX0_N	O	
79	TS_DIFF4+	LVDS0_CH0_TX1_P	O	LVDS data lane 1
77	TS_DIFF4-	LVDS0_CH0_TX1_N	O	
85	TS_DIFF5+	LVDS0_CH0_TX2_P	O	LVDS data lane 2
83	TS_DIFF5-	LVDS0_CH0_TX2_N	O	
91	TS_DIFF6+	LVDS0_CH0_TX3_P	O	LVDS data lane 3 (unused for 18bit)
89	TS_DIFF6-	LVDS0_CH0_TX3_N	O	

Table 5-18 LVDS Display Control Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
239	BKL1_PWM	LVDS1_GPIO00	LVDS1.PWM0.OUT	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	LVDS0_GPIO00	LSIO.GPIO1.IO04	O	Enable signal for the backlight
209	I2C1_SDA	GPT1_CAPTURE	DMA.I2C2.SDA	I/O	I^2C interface might be used for the extended display identification data (EDID)
211	I2C1_SCL	GPT1_CLK	DMA.I2C2.SCL	O	I^2C interface might be used for the extended display identification data (EDID)

Table 5-19 Additional LVDS Display Control Signals (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
239	BKL1_PWM	LVDS1_GPIO00	LVDS1.GPIO0.IO00	I/O	Dedicated GPIO functions for the LVDS1 (Apalis standard LVDS) port. These pins feature also regular GPIO functionality on ALT3
281	LCD1_G6	LVDS1_I2C0_SCL	LVDS1.GPIO0.IO02	I/O	
283	LCD1_G7	LVDS1_I2C0_SDA	LVDS1.GPIO0.IO03	I/O	
281	LCD1_G6	LVDS1_I2C0_SCL	LVDS1.I2C0.SCL	O	Dedicated I²C for channel A of the Apalis standard LVDS port.
283	LCD1_G7	LVDS1_I2C0_SDA	LVDS1.I2C0.SDA	I/O	
126	UART2_TXD	LVDS1_I2C1_SCL	LVDS1.I2C1.SCL	O	Dedicated I²C for channel B of the Apalis standard LVDS port.
132	UART2_RXD	LVDS1_I2C1_SDA	LVDS1.I2C1.SDA	I/O	
286	BKL1_ON	LVDS0_GPIO00	LVDS0.GPIO0.IO00	I/O	Dedicated GPIO functions for the LVDS0 (type-specific LVDS) port. These pins feature also regular GPIO functionality on ALT3
87	TS_2	LVDS0_I2C0_SCL	LVDS0.GPIO0.IO02	I/O	
99	TS_3	LVDS0_I2C0_SDA	LVDS0.GPIO0.IO03	I/O	
87	TS_2	LVDS0_I2C0_SCL	LVDS0.I2C0.SCL	O	Dedicated I²C for channel A of the type specific LVDS port.
99	TS_3	LVDS0_I2C0_SDA	LVDS0.I2C0.SDA	I/O	
138	UART4_TXD	LVDS0_I2C1_SCL	LVDS0.I2C1.SCL	O	Dedicated I²C for channel B (not available on Apalis iMX8).
140	UART4_RXD	LVDS0_I2C1_SDA	LVDS0.I2C1.SDA	I/O	
286	BKL1_ON	LVDS0_GPIO00	LVDS0.PWM0.OUT	O	Backlight PWM for type specific LVDS port

5.6.3 HDMI

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

The HDMI interface of the i.MX 8 is also capable of outputting DisplayPort signals. The DisplayPort Dual Mode (DP++) standard would make it possible to use “passive” DisplayPort to HDMI adapter. Even though the silicon IP in the i.MX 8 supports DisplayPort Dual Mode, the function is currently not supported by NXP or validated. This means “passive” DisplayPort to HDMI adapter are not working. The carrier board either must implement a HDMI or a regular DisplayPort without DP++ feature. More information to the DisplayPort interface of the Apalis iMX8 can be found in section 5.6.5.

HDMI Features

- HDMI 2.0a up to 4K60 (3840x2160@60Hz) if both display controller outputs are used
- HDMI 1.4b up to 4K30 (3840x2160@30Hz) if single display controller output is used
- Pixel Clock from 25MHz up to 600MHz
- Supports digital sound
- High-bandwidth Content Protection Revision 2.2 (HDCP, separate license needed)
- CEC interface

Table 5-20 HDMI Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
240	HDMI1_TXC+	HDMI_TX0_CLK_EDP3_P	HDMI_TX0.TX_P_LN_3	O	HDMI Differential Clock
242	HDMI1_TXC-	HDMI_TX0_CLK_EDP3_N	HDMI_TX0.TX_M_LN_3	O	
234	HDMI1_TXD0+	HDMI_TX0_DATA0_EDP2_P	HDMI_TX0.TX_P_LN_2	O	HDMI Differential Data 0
236	HDMI1_TXD0-	HDMI_TX0_DATA0_EDP2_N	HDMI_TX0.TX_M_LN_2	O	
228	HDMI1_TXD1+	HDMI_TX0_DATA1_EDP1_P	HDMI_TX0.TX_P_LN_1	O	HDMI Differential Data 1
230	HDMI1_TXD1-	HDMI_TX0_DATA1_EDP1_N	HDMI_TX0.TX_M_LN_1	O	
222	HDMI1_TXD2+	HDMI_TX0_DATA2_EDP0_P	HDMI_TX0.TX_P_LN_0	O	HDMI Differential Data 2
224	HDMI1_TXD2-	HDMI_TX0_DATA2_EDP0_N	HDMI_TX0.TX_M_LN_0	O	

Table 5-21 Additional Display Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
220	HDMI1_CEC	HDMI_TX0_CEC	HDMI_TX0.CEC	I/O	HDMI Consumer Electronic Control.
232	HDMI1_HPD	HDMI_TX0_HPD	HDMI_TX0.HPD	I	Hot Plug Detect
205	I2C2_SDA (DDC)	HDMI_TX0_DDC_SDA	HDMI_TX0.DDC_.SDA	I/O	Display Data Channel Data
207	I2C2_SCL (DDC)	HDMI_TX0_DDC_SCL	HDMI_TX0.DDC_SCL	O	Display Data Channel Clock

5.6.4 Analogue VGA

The Apalis iMX8 does not feature an analogue VGA interface. The pins on the module edge connector are left unconnected.

5.6.5 DisplayPort (DP) and Embedded DisplayPort (eDP)

The HDMI interface pins of the i.MX 8 SoC can be configured to be used as DisplayPort (DP) or embedded DisplayPort interface (eDP). The DisplayPort Dual Mode (DP++) standard would make it possible to use “passive” DisplayPort to HDMI adapter. Even though the silicon IP in the i.MX 8 supports DisplayPort Dual Mode, the function is currently not supported by NXP or validated. This means “passive” DisplayPort to HDMI adapter are not working.

DisplayPort Features:

- DisplayPort specification version 1.3
- High-bandwidth Content Protection Revision 2.2 (HDCP, separate license needed)
- 1, 2, and 4 lanes supported
- RBR, HBR, and HBR2 supported
- 1Mbps AUX channel

The Embedded DisplayPort is used for driving local displays. The interface adds additional power saving features.

Embedded DisplayPort Features:

- Embedded DisplayPort specification version 1.4
- Supports backlights and multi-touch commands
- eDP DPCD registers
- Variable link rate R162/R216/R243/R270/R324/R432/R540
- Fast link training

Since the DP and eDP interface are not part of the Apalis module specifications, it is not guaranteed that other Apalis modules also have the possibility to use the HDMI interface pins as DP or eDP. Use this interface only if compatibility with other modules is not mandatory.

The DP/eDP requires additional 100nF series capacitors to be placed in the auxiliary data lines (AUX channel). The series capacitors are not required for the high-speed data line pairs. Be aware of the different numbering of the data lanes between HDMI and DP. When using the HDMI port as DisplayPort, the on-module 604Ω termination resistors on the high-speed data lines need to be disabled. This is done by setting the LSIO.GPIO1.IO30 (SoC pad MIPI_CSI1_GPIO0_00) low.

The DP/eDP signals are located as a secondary function of the HDMI interface. The routing requirements of the DP/eDP signals are different from the HDMI interface.

Table 5-22 DP/eDP Signal Routing Requirements

Parameter	Requirement
Max Frequency	1.62 Gb/s per lane (RBR) 2.7 Gb/s per lane (HBR) 5.4 Gb/s per lane (HBR2)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between different data pairs	<150ps ≈22.5mm
Max Trace Length from Module Connector	215mm (RBR and HBR) 127mm (HBR2)

The Apalis iMX8 supports up to 4 lanes of Display Port signals. The interface is backward compatible with one or two lane displays. Simply use only the lane 0 for a single lane display respectively lane 0 and 1 for a two lane display.

Table 5-23 DP/eDP interface signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	eDP Signal Name	I/O	Description
222	HDMI1_TXD2+	HDMI_TX0_DATA2_EDP0_P	eDP_1_D0+	O	Link Lane 0
224	HDMI1_TXD2-	HDMI_TX0_DATA2_EDP0_N	eDP_1_D0-	O	
228	HDMI1_TXD1+	HDMI_TX0_DATA1_EDP1_P	eDP_1_D1+	O	Link Lane 1
230	HDMI1_TXD1-	HDMI_TX0_DATA1_EDP1_N	eDP_1_D1-	O	
234	HDMI1_TXD0+	HDMI_TX0_DATA0_EDP2_P	eDP_1_D2+	O	Link Lane 2
236	HDMI1_TXD0-	HDMI_TX0_DATA0_EDP2_N	eDP_1_D2-	O	
240	HDMI1_TXC+	HDMI_TX0_CLK_EDP3_P	eDP_1_D3+	O	Link Lane 3
242	HDMI1_TXC-	HDMI_TX0_CLK_EDP3_N	eDP_1_D3-	O	
73	TS_DIFF3+	HDMI_TX0_AUX_P	eDP_1_AUX_CH0_P	I/O	Aux channel, contains control data such as EDID information
71	TS_DIFF3-	HDMI_TX0_AUX_N	eDP_1_AUX_CH0_N	I/O	
232	HDMI1_HPD	HDMI_TX0_HPD	eDP_1_HPD	I	Hot plug detect

5.6.6 Display Serial Interface (DSI)

The i.MX 8 SoC provides up to two MIPI/DSI interfaces to connect compatible displays. However, due to a limitation of the available module edge connector pins, only one MIPI/DSI interface with only one data lane is available on the Apalis iMX8. The data lane is capable of up to 1.5Gbps data rate and is bidirectional (high-speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer.

The DSI signals are located in the type-specific area of the Apalis module. Therefore, it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning on using the DSI interface, please be aware that other Apalis modules might not be compatible with your carrier board.

As the DSI is a high-speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Apalis Carrier Board Design Guide as the interface is type specific.

Table 5-24 DSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max Intra-pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-25 DSI interface signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	DSI Signal Name	I/O	Description
133	TS_DIFF13+	MIPI_DSI1_CLK_P	DSI1_CLK+	O	DSI Interface 1 clock
131	TS_DIFF13-	MIPI_DSI1_CLK_N	DSI1_CLK-	O	
97	TS_DIFF7+	MIPI_DSI1_DATA0_P	DSI1_D1+	I/O	DSI Interface 1 data lane 1
95	TS_DIFF7-	MIPI_DSI1_DATA0_N	DSI1_D1-	I/O	

Table 5-26 Additional Display Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
123	TS_4	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Dedicated PWM functions for the DSI1 port.
123	TS_4	MIPI_DSI1_GPIO0_00	MIPI_DSI1.GPIO0.IO00	O	Dedicated GPIO functions for the DSI1 port. This pin features also regular GPIO functionality on ALT3.
175	CAM1_D6	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	I/O	Dedicated I^2C for the DSI1 port.
173	CAM1_D7	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	O	

5.7 PCI Express

The i.MX 8 SoC features two PCI Express (PCIe) and one SATA controller. PCIe controller 0 features single and dual lane while the controller 1 only features single lane operation. There are two PHY blocks in the SoC. One of this PHY blocks consists of two lanes while the other one is only a single lane PHY. One output of the dual PHY (PCIE0) is available externally on the module edge connector as Apalis standard PICe interface. The second output of this PHY (PCIE1) is either connected to the internal Wi-Fi module or is available on the USBO1 SuperSpeed signals for modules without Wi-Fi. The output of the single PHY (PCIE_SATA0) is available on the module edge connector as Apalis standard SATA interface.

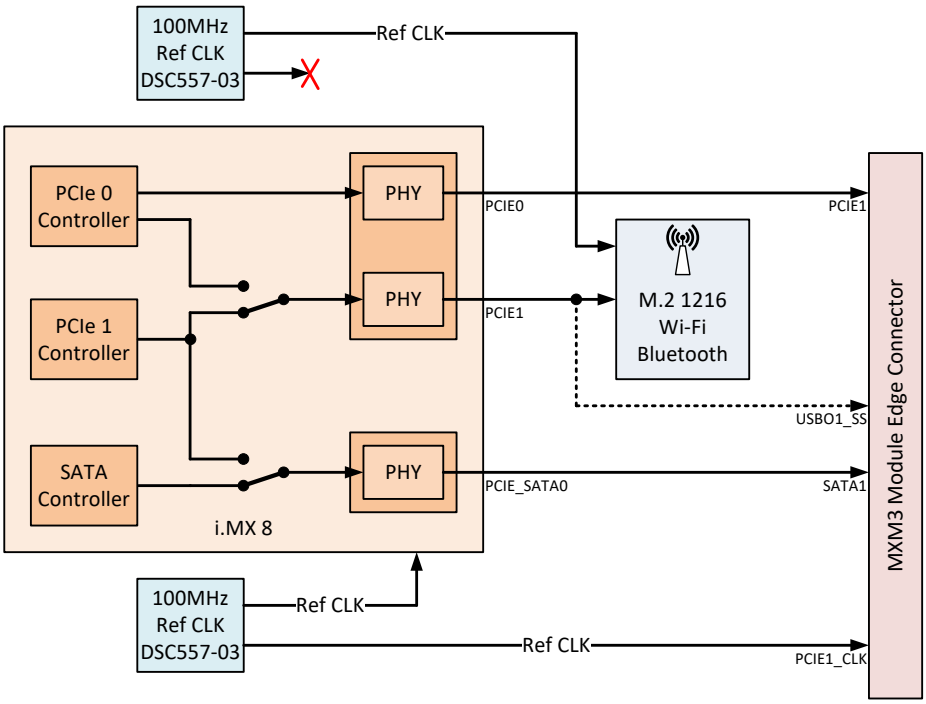

Figure 14: PCI Express block diagram

The following table shows all mapping options for the PICe and SATA that are possible. On modules with an assembled Wi-Fi and Bluetooth module, only the first two options are possible.

Table 5-27 PCIe mapping options

PCIE0 (Apalis PCIE1)	PCIE1 (Wi-Fi Module)	PCIE1 (Apalis USBO1_SS)	PCIE_SATA0 (Apalis SATA1)	Remarks
PCIE_0 Lane 0	PCIE_1 Lane 0	Not available	SATA	Default configuration, fully compatible with other Apalis Modules
PCIE_0 Lane 0	Unused	Not available	PCIE_1 Lane 0	Wi-Fi cannot be used, but Bluetooth is still available over USB
PCIE_0 Lane 0	No Wi-Fi Module	PCIE_0 Lane 1	SATA	Dual Lane PCIe, only possible on modules without Wi-Fi/Bluetooth
PCIE_0 Lane 0	No Wi-Fi Module	PCIE_1 Lane 0	SATA	Two single lane PCIe, only possible on modules without Wi-Fi/Bluetooth
PCIE_0 Lane 0	No Wi-Fi Module	PCIE_0 Lane 1	PCIE_1 Lane 0	Dual Lane plus single lane PCIe, only possible on modules without Wi-Fi/Bluetooth

The PCIe interface is compliant with the PCIe 3.0 specification and supports 8 Gb/s transfer rate. It is backward compatible with the PCIe 2.0 standard (5Gb/s) and the PCIe 1.1 standard which

supports 2.5 Gb/s. PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-28 PCIe Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
55	PCIE1_CLK+			O	100MHz Reference clock differential pair. Sourced by a reference clock oscillator
53	PCIE1_CLK-			O	
49	PCIE1_TX+	PCIE0_TX0_P	HSIO.PCIE0.TX0_P	O	Apalis standard PCIe interface Transmit data lane 0
47	PCIE1_TX-	PCIE0_TX0_N	HSIO.PCIE0.TX0_N	O	
43	PCIE1_RX+	PCIE0_RX0_P	HSIO.PCIE0.RX0_P	I	Apalis standard PCIe interface Receive data lane 0
41	PCIE1_RX-	PCIE0_RX0_N	HSIO.PCIE0.RX0_N	I	
68	USBO1_SSTX+	PCIE1_TX0_P	HSIO.PCIE1.TX0_P	O	Only available on modules without Wi-Fi/Bluetooth module
70	USBO1_SSTX-	PCIE1_TX0_N	HSIO.PCIE1.TX0_N	O	
62	USBO1_SSRX+	PCIE1_RX0_P	HSIO.PCIE1.RX0_P	I	Only available on modules without Wi-Fi/Bluetooth module
64	USBO1_SSRX-	PCIE1_RX0_N	HSIO.PCIE1.RX0_N	I	
33	SATA1_TX+	PCIE_SATA0_TX0_P	HSIO.PCIE2.TX0_P	O	SATA interface on Apalis standard
31	SATA1_TX-	PCIE_SATA0_TX0_N	HSIO.PCIE2.TX0_N	O	
25	SATA1_RX+	PCIE_SATA0_RX0_P	HSIO.PCIE2.RX0_P	I	SATA interface on Apalis standard
27	SATA1_RX-	PCIE_SATA0_RX0_N	HSIO.PCIE2.RX0_N	I	

Table 5-29 Additional PCIe Control Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
37	WAKE1_MICO	SPI3_CS0	LSIO.GPIO2.IO20	I	General purpose wake signal
26	RESET_MOCI#			O	General reset output
209	I2C1_SDA	GPT1_CAPTURE	DMA.I2C2.SDA	I/O	Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if interface is necessary
211	I2C1_SCL	GPT1_CLK	DMA.I2C2.SCL	O	

5.8 SATA

The Serial ATA (SATA) interface can be used to attach, for example, an external hard drive, SSD or a mSATA SSD. The interface is a single Gen 3 SATA link with a maximum transfer rate of 6 Gb/s. The interface is backward compatible with Gen 2 (3 Gb/S) and Gen 1 (1.5 Gb/s). SATA is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-30 Apalis standard SATA Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
33	SATA1_TX+	PCIE_SATA0_TX0_P	HSIO.PCIE2.TX0_P	O	SATA transmit data, Series decoupling capacitor are provided on the module
31	SATA1_TX-	PCIE_SATA0_TX0_N	HSIO.PCIE2.TX0_N	O	
25	SATA1_RX+	PCIE_SATA0_RX0_P	HSIO.PCIE2.RX0_P	I	SATA receive data, Series decoupling capacitor are provided on the module
27	SATA1_RX-	PCIE_SATA0_RX0_N	HSIO.PCIE2.RX0_N	I	
35	SATA1_ACT#	ESAI1_TX0	LSIO.GPIO2.IO08	O	SATA activity indicator (regular GPIO)

5.9 I²C

The i.MX 8 SoC features a total number of nineteen I²C controllers. Not all of these interfaces are available externally. Some of them are dedicated interfaces with limited function.

- General purpose I²C with DMA support
  - 4x general purpose I²C. Three of them are available on the module edge connector. The fourth is only available externally if the on-module audio codec and the USB hub are unused
  - 2x I²C interfaces which are tightly coupled with the Cortex-M4 cores (one per each M4 core)
- Low-speed I²C without DMA support for dedicated purpose. Could also be used as general purpose, but require the associated PHY (for example MIPI) to be powered on
  - 2x master I²C for MIPI/DSI, only 1x available externally
  - 2x master I²C for MIPI/CSI-2, not available externally
  - 4x master I²C for LVDS, all available externally
  - 2x master I²C for HDMI-TX, only 1x available externally, cannot be used as General purpose I²C
  - 1x master I²C for HDMI-RX, not available externally
- I²C tightly coupled with SCU
  - 1x Dedicated for PMIC, cannot be used externally

The Apalis module standard features only three I²C interfaces. The rest of the available interfaces are alternate functions of other interface pins. These additional interfaces are not compatible with other Apalis modules. Therefore, it is highly recommended to use primarily the three standard I²C interfaces.
Please note that I2C2 (Pin 205 and 207) only can be used as a dedicated HDMI DDC interface.

General purpose I²C ports features:

- Supports standard and fast mode of operation (0-400KHz), Fm+ (1Mbit/s) as well as high-speed mode (3.2 MHz).
- System Management Bus (SMBus) compliant specifications
- Master and slave mode (slave mode may not supported in regular BSP)
- Multi-master support
- Clock stretching support
- 7-bit or 10-bit addressing
- DMA support

Table 5-31 Apalis standard I²C Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I2C Port	Description
209	I2C1_SDA	GPT1_CAPTURE	DMA.I2C2.SDA	I2C2	Generic I²C
211	I2C1_SCL	GPT1_CLK	DMA.I2C2.SCL		
205	I2C2_SDA (DDC)	HDMI_TX0_DDC_SDA	HDMI_TX0.DDC_SDA	I2C0	I²C port for the DDC interface. Cannot be used as general purpose I²C
207	I2C2_SCL (DDC)	HDMI_TX0_DDC_SCL	HDMI_TX0.DDC_SCL		
201	I2C3_SDA (CAM)	SIM0_POWER_EN	DMA.I2C3.SDA	I2C3	I²C port for the camera interface, can also be used for other purposes
203	I2C3_SCL (CAM)	SIM0_PD	DMA.I2C3.SCL		

Table 5-32 Additional General Purpose I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I2C Port	Description
251	LCD1_R0	ENET1_MDIO	DMA.I2C4.SDA	I2C4	General purpose I²C
253	LCD1_R1	ENET1_MDC	DMA.I2C4.SCL		
262	USBO1_OC#	USB_SS3_TC2	DMA.I2C1.SDA	I2C1	The USB hub and the audio codec on the module are connected with the same I²C Port I2C1. Therefore, this I²C can only be used if no I²C communication with the USB hub and the audio codec are required.
96	USBH_OC#	USB_SS3_TC3			
274	USBO1_EN	USB_SS3_TC0	DMA.I2C1.SCL		
84	USBH_EN	USB_SS3_TC1			

Table 5-33 Tightly coupled M4 I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	Description
120	UART1_DSR	M40_I2C0_SDA	M40.I2C0.SDA	Dedicated I²C port for the M4 core 0. It is tightly coupled with this core.
110	UART1_DTR	M40_I2C0_SCL	M40.I2C0.SCL	
122	UART1_RI	M41_I2C0_SDA	M41.I2C0.SDA	Dedicated I²C port for the M4 core 1. It is tightly coupled with this core.
124	UART1_DCD	M41_I2C0_SCL	M41.I2C0.SCL	

Table 5-34 Dedicated low-speed I²C Signals (not compatible with other Apalis family modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	Description
283	LCD1_G7	LVDS1_I2C0_SDA	LVDS1.I2C0.SDA	Dedicated I²C port for the Apalis standard LVDS port channel A
281	LCD1_G6	LVDS1_I2C0_SCL	LVDS1.I2C0.SCL	
132	UART2_RXD	LVDS1_I2C1_SDA	LVDS1.I2C1.SDA	Dedicated I²C port for the Apalis standard LVDS port channel B
126	UART2_TXD	LVDS1_I2C1_SCL	LVDS1.I2C1.SCL	
99	TS_3	LVDS0_I2C0_SDA	LVDS0.I2C0.SDA	Dedicated I²C port for the additional LVDS port on the type-specific pins
87	TS_2	LVDS0_I2C0_SCL	LVDS0.I2C0.SCL	
140	UART4_RXD	LVDS0_I2C1_SDA	LVDS0.I2C1.SDA	Dedicated I²C port for the LVDS channel that is not available on the module edge connector pins
138	UART4_TXD	LVDS0_I2C1_SCL	LVDS0.I2C1.SCL	
205	I2C2_SDA (DDC)	HDMI_TX0_DDC_SDA	HDMI_TX0.DDC_SDA	Dedicated I²C port for the HDMI interface. Cannot be used as general purpose I²C
207	I2C2_SCL (DDC)	HDMI_TX0_DDC_SCL	HDMI_TX0.DDC_SCL	
175	CAM1_D6	MIPI_DSI1_I2C0_SDA	MIPI_DSI1.I2C0.SDA	Dedicated I²C port for the MIPI/DSI port
173	CAM1_D7	MIPI_DSI1_I2C0_SCL	MIPI_DSI1.I2C0.SCL	

5.9.1 Real-Team Clock (RTC) recommendation

The Apalis module features an RTC circuit which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time-keeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC needs to be retained even without the module's main voltage, a coin cell needs to be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 8.3). Therefore, a standard lithium coin cell battery can drain faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case,

add the external RTC to the I2C1 (pin 209/211) interface of the module and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.

5.10 UART

The i.MX 8 SoC features a total number of 8 UARTs. There are 5 regular UARTs of which four are available on the standard Apalis module edge connector pins and therefore are compatible with other Apalis module. One of the regular UART is available as alternate functions of the SD card interface. Additional to the regular UARTs, the SoC features two UARTs which are tightly coupled to each one of the Cortex-M4 cores. These UARTs are also available on the module edge connector. The last UART is tightly coupled to the System Controller Unit. It is used for the debugging messages of the SCU. The interface pins of this UART are only available on test pads.

The Apalis UART1 is according to the Apalis specification a full-featured UART. Since the i.MX 8 does not feature the DTR, DSR, DCD, and RI signals, only RX/TX, as well as RTS/CTS is available. The UART1 is used as standard debug interface for the Toradex Linux operating systems. Therefore, it is desirable to keep this port accessible for system debugging.

General purpose UART Features

- Full-duplex, standard non-return-to-zero (NRZ format)
- Programmable baud rates
- Interrupt, DMA, or polled operation.
- Hardware parity generation and checking
- Character length 7 to 10bit
- Programmable 1-bit or 2-bit stop bits
- Idle line, address mark, and receive data match wakeup method
- Automatic address matching to reduce ISR overhead
- IrDA 1.4 support

Table 5-35 UART1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
118	UART1_RXD	UART1_RX	DMA.UART1.RX	I	Received Data
112	UART1_TXD	UART1_TX	DMA.UART1.TX	O	Transmitted Data
114	UART1_RTS	UART1_RTS_B	DMA.UART1.RTS_B	O	Request to Send
116	UART1_CTS	UART1_CTS_B	DMA.UART1.CTS_B	I	Clear to Send
110	UART1_DTR	M40_I2C0_SCL	LSIO.GPIO0.IO06	O	DTR function not available, only GPIO
120	UART1_DSR	M40_I2C0_SDA	LSIO.GPIO0.IO07	I	CTS function not available, only GPIO
122	UART1_RI	M41_I2C0_SDA	LSIO.GPIO0.IO11	I	RI function not available, only GPIO
124	UART1_DCD	M41_I2C0_SCL	LSIO.GPIO0.IO10	I	DCD function not available, only GPIO

Table 5-36 UART2 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
132	UART2_RXD	LVDS1_I2C1_SDA	DMA.UART3.RX	I	Received Data
126	UART2_TXD	LVDS1_I2C1_SCL	DMA.UART3.TX	O	Transmitted Data
128	UART2_RTS	ENET1_RGMII_TXD3	DMA.UART3.RTS_B	O	Request to Send
130	UART2_CTS	ENET1_RGMII_RXC	DMA.UART3.CTS_B	I	Clear to Send

Table 5-37 UART3 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
136	UART3_RXD	UART0_RX	DMA.UART0.RX	I	Received Data
134	UART3_TXD	UART0_TX	DMA.UART0.TX	O	Transmitted Data

Table 5-38 UART4 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
140	UART4_RXD	LVDS0_I2C1_SDA	DMA.UART2.RX	I	Received Data
138	UART4_TXD	LVDS0_I2C1_SCL	DMA.UART2.TX	O	Transmitted Data

For the UART3, there are additional hardware flow signals available. The signals are not compatible with other Apalis modules.

Table 5-39 Additional UART3 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
6	PWM3	UART0_RTS_B	DMA.UART0.RTS_B	O	Additional Request to Send for UART 3
8	PWM4	UART0_CTS_B	DMA.UART0.CTS_B	I	Additional Clear to Send UART 3

For the UART1, UART2, and UART4, there are alternate pins available. However, for compatibility purposes, it is recommended to use the standard Apalis pins instead.

Table 5-40 Alternate UART1, UART2, and UART4 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
116	UART1_CTS	UART1_CTS_B	DMA.UART1.RTS_B	O	Alternate Request to Send for UART 1
114	UART1_RTS	UART1_RTS_B	DMA.UART1.CTS_B	I	Alternate Clear to Send for UART 1
5	GPIO3	M41_GPIO0_00	DMA.UART3.RX	I	Alternate Received Data for UART 2
243	LCD1_PCLK	ENET1_RGMII_RXD3			
7	GPIO4	M41_GPIO0_01	DMA.UART3.TX	O	Alternate Transmitted Data for UART 2
255	LCD1_R2	ENET1_RGMII_TXD2			
6	PWM3	UART0_RTS_B	DMA.UART2.RX	I	Alternate Received Data for UART 4
8	PWM4	UART0_CTS_B	DMA.UART2.TX	O	Alternate Transmitted Data for UART 4

A fifth UART is available as an alternate function of the SD card or GPIO interface. For compatibility reasons, it is only recommended to use this interface if more than four UART ports are required. This port is not compatible with other Apalis modules.

Table 5-41 Additional UART Port Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
1	GPIO1	M40_GPIO0_00	DMA.UART4.RX	I	Received Data
186	SD1_D0	USDHC2_DATA0			
3	GPIO2	M40_GPIO0_01	DMA.UART4.TX	O	Transmitted Data
188	SD1_D1	USDHC2_DATA1			
178	SD1_D3	USDHC2_DATA3	DMA.UART4.RTS_B	O	Request to Send
176	SD1_D2	USDHC2_DATA2	DMA.UART4.CTS_B	I	Clear to Send

For each M4 core, there is a tightly coupled UART available. The pins are located on the DTR, DSR, DCD, and RI signals of the Apalis standard UART1. Since the i.MX 8 anyway does not support these modem control signals, there will be no conflicts with the UART1 interface. However, it is still not guaranteed that the tightly coupled UART interfaces are compatible with any other Apalis module.

Table 5-42 Tightly Coupled M4 UART Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
120	UART1_DSR	M40_I2C0_SDA	M40.I2C0.SDA	I	Received Data tightly coupled with M4 core 0
110	UART1_DTR	M40_I2C0_SCL	M40.I2C0.SCL	O	Transmitted Data tightly coupled with M4 core 0
122	UART1_RI	M41_I2C0_SDA	M41.I2C0.SDA	I	Received Data tightly coupled with M4 core 1
124	UART1_DCD	M41_I2C0_SCL	M41.I2C0.SCL	O	Transmitted Data tightly coupled with M4 core 1

The System Controller Unit (SCU) has its own tightly coupled UART interface. The interface is used as debug port for the SCU. The pins are only available on test pads on the bottom side of the module. For normal software development, there is no need for having access to this interface. Important, the interface features only 1.8V logic level. 3.3V is not supported and could damage the SoC.

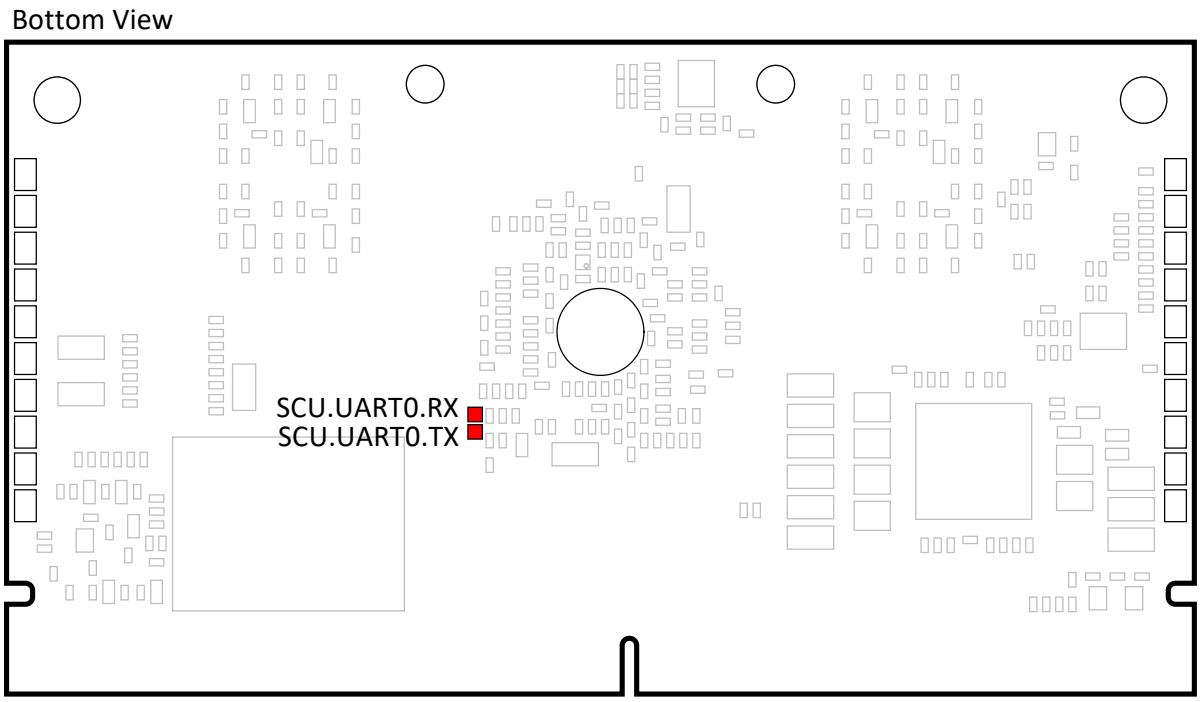

Figure 15: SCU UART test pin location

5.11 SPI

The i.MX 8 SoC features a total of four SPI interfaces. Two of them are available on the Apalis module standard pins. The other two ports are also available. They are located on alternate functions of other interfaces. One of the additional interfaces is located on the touch and ADC pins. Special care has to be taken when using these pins. The signal level is 1.8V, not 3.3V as for the rest of the low-speed module edge connector pins. Applying 3.3V to these signals could damage the module.

The SPI ports operate at up to 60MHz in master mode and up to 40MHz in slave mode. However, there is one exception. One of the additional SPI interfaces is available as alternate functions of the UART1 is limited to 40MHz in master mode and 20MHz in slave mode. Since the UART1 port

should be made available for debugging purpose, it is anyway not recommended to use this SPI interface.

Features:

- Up to 60 Mbps in master mode
- Up to 40 Mbps in slave mode
- 32-bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit (1-bit mode)
- Wakeup function on receiving data match

Each SPI channel supports four different modes of the SPI protocol:

Table 5-43 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
3	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

Pay attention to the data direction of the signals in master respectively slave mode. The following table describes the data direction of the signals at the module side.

Table 5-44 SPI Signal Direction in Master and Slave Mode

iMX 8 Port Name	Master Mode		Slave Mode	
	I/O	Description	I/O	Description
SPIx_SDO	O	Master Output, Slave Input	O	Master Input, Slave Output
SPIx_SDI	I	Master Input, Slave Output	I	Master Output, Slave Input
SPIx_CS0	O	Slave Select	I	Slave Select
SPIx_SCK	O	Serial Clock	I	Serial Clock

In the Apalis module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-45 Apalis SPI Port 1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
225	SPI1_MOSI	SPI0_SDO	DMA.SPI0.SDO	O	Master Output, Slave Input
223	SPI1_MISO	SPI0_SDI	DMA.SPI0.SDI	I	Master Input, Slave Output
227	SPI1_CS	SPI0_CS0	DMA.SPI0.CS0	I/O	Slave Select
221	SPI1_CLK	SPI0_SCK	DMA.SPI0.SCK	I/O	Serial Clock
200	DAP1_BIT_CLK	SPI0_CS1	DMA.SPI0.CS1	O	Additional slave select, not compatible with other modules

Table 5-46 Apalis SPI Port 2 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
231	SPI2_MOSI	SPI2_SDO	DMA.SPI2.SDO	O	Master Output, Slave Input
229	SPI2_MISO	SPI2_SDI	DMA.SPI2.SDI	I	Master Input, Slave Output
233	SPI2_CS	SPI2_CS0	DMA.SPI2.CS0	I/O	Slave Select
235	SPI2_CLK	SPI2_SCK	DMA.SPI2.SCK	I/O	Serial Clock
204	DAP1_SYNC	SPI2_CS1	DMA.SPI2.CS1	O	Additional slave select, not compatible with other modules

Table 5-47 Additional SPI ports, incompatible with other modules

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
315	AN1_TSPX	ADC_IN4	DMA.SPI1.SDO	O	Master Output, Slave Input, **only 1.8V**
317	AN1_TSMX	ADC_IN5	DMA.SPI1.SDI	I	Master Input, Slave Output, **only 1.8V**
319	AN1_TSPY	ADC_IN6	DMA.SPI1.CS0	I/O	Slave Select, **only 1.8V**
321	AN1_TSMY	ADC_IN7	DMA.SPI1.CS1	O	Slave Select, **only 1.8V**
311	AN1_TSWIP_ADC3	ADC_IN3	DMA.SPI1.SCK	I/O	Serial Clock, **only 1.8V**
118	UART1_RXD	UART1_RX	DMA.SPI3.SDO	O	Master Output, Slave Input, reduced interface speed
193	CAM1_MCLK	SPI3_SDO			
114	UART1_RTS	UART1_RTS_B	DMA.SPI3.SDI	I	Master Input, Slave Output, reduced interface speed
194	DAP1_MCLK	SPI3_SDI			
116	UART1_CTS	UART1_CTS_B	DMA.SPI3.CS0	I/O	Slave Select, reduced interface speed
37	WAKE1_MICO	SPI3_CS0			
112	UART1_TXD	UART1_TX	DMA.SPI3.SCK	I/O	Serial Clock, reduced interface speed

5.12 PWM (Pulse Width Modulation)

The i.MX 8 features a four channel general purpose Pulse Width Modulator (PWM). It has a 16-bit counter and is optimized to generate simple sound samples and generate tomes. It has 16-bit resolution and there is a 4-level deep FIFO available in order to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock. These four PWM output signals are available on the module edge connector as Apalis standard PWM signals.

Table 5-48 General Purpose PWM Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
2	PWM1	GPT1_COMPARE	LSIO.PWM2.OUT	O	
4	PWM2	GPT0_COMPARE	LSIO.PWM3.OUT	O	
6	PWM3	UART0_RTS_B	LSIO.PWM0.OUT	O	
8	PWM4	UART0_CTS_B	LSIO.PWM1.OUT	O	

Additional to the general purpose PWM, the i.MX 8 features dedicated PWM generators for the LVDS and MIPI/DSI interface. These PWM outputs are intended to be used for driving the backlight intensity of a liquid crystal display. One of these dedicated PWMs is available as an Apalis standard pin for backlight control. Two additional PWM signals dedicated for backlight controlling are available as an alternate function.

Table 5-49 Dedicated PWM Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
239	BKL1_PWM	LVDS1_GPIO00	LVDS1.PWM0.OUT	O	Apalis standard backlight PWM output. Use this output for the standard LVDS interface, compatible with other Apalis modules
286	BKL1_ON	LVDS0_GPIO00	LVDS0.PWM0.OUT	O	Dedicated PWM output for the LVDS interface on type specific pin. Not compatible with other Apalis modules
123	TS_4	MIPI_DSI1_GPIO0_00	MIPI_DSI1.PWM0.OUT	O	Dedicated PWM output for the MIPI/DSILVDS interface. Not compatible with other Apalis modules

Besides the regular PWM interfaces, the i.MX 8 features Timer PWM Modules (TPM) which are tightly coupled to each of the two Cortex M4 cores. The TMB is based on a simple timer which is known since many years from the HCS08 8-bit microcontrollers. Besides the generation of PWM signals, it can also be used for input capture and output compare function. The TPM are dedicated to the M4 cores. However, there is a FlexTimer (FTM) module for the main cores. The FTM builds upon the TPM, but enhances it by additional dead time insertion hardware, fault control input, signed up counter function, enhancing the triggering functionality, and allowing the polarity and initialization to be controlled. The FTM as well as the TPM for the M4 cores are available on the module edge connector as alternate functions.

Table 5-50 TPM and FTM Interface Signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
1	GPIO1	M40_GPIO0_00	M40.TPM0.CH0	I/O	Timer PWM Module output tightly coupled with the Cortex M4 core 0
3	GPIO2	M40_GPIO0_01	M40.TPM0.CH1	I/O	
5	GPIO3	M41_GPIO0_00	M41.TPM0.CH0	I/O	Timer PWM Module output tightly coupled with the Cortex M4 core 1
7	GPIO4	M41_GPIO0_01	M41.TPM0.CH1	I/O	
193	CAM1_MCLK	SPI3_SDO	DMA.FTM.CH0	I/O	Flex Timer Module channel signals. Can be used with all the CPU cores
194	DAP1_MCLK	SPI3_SDI	DMA.FTM.CH1	I/O	
37	WAKE1_MICO	SPI3_CS0	DMA.FTM.CH2	I/O	

5.13 OWR (One Wire)

The Apalis iMX8 does not feature a One Wire interface. However, it is possible to implement a bit-banging One Wire driver.

5.14 SD/MMC

The i.MX 8 SoC provides three SDIO interfaces; one is used internally for the eMMC Flash and two are available on the module edge connector Pins. Following the Apalis standard, one of the external ports can be used with up to eight data pins (8-bit MMC or eMMC) while the other one only supports up to four data pins.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

Features

- Supports SD Memory Card Specification 3.0 (up to UHS-I, no UHS-II)
- Supports SDIO Card Specification Version 3.0 (up to UHS-I, no UHS-II)

- Supports MMC System Specification Version 5.1 (one interface up to 8-bit)
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- Both interface supports 3.3V and 1.8V IO voltage mode (Apalis standard is only 3.3V)
- Card bus clock frequency up to 208 MHz

i.MX 8 SDIO interface	Max Bus Width	Description
USDHC0 / EMMC0	8-bit	Connected to internal eMMC boot device. Not available at the module edge connector
USDHC1	8-bit	Apalis Standard MMC1 interface
USDHC2	4-bit	Apalis Standard SD1 interface

According to the Apalis module specification, the IO voltage level of the SD/MMC interface supports only 3.3V logic level. Therefore, the SD interfaces are limited to default or high-speed mode; UHS-I modes are not supported. Nevertheless, the MMC1 interface (i.MX 8 USDHC1) as well as the SD1 interface (i.MX 8 USDHC2) are capable to switch independently to the 1.8V IO level. This allows using the interface in UHS-I mode with higher speed. Please note that this IO voltage level is not mandatory in the Apalis module specification and therefore other modules might do not support this mode as well. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interfaces are used in the 1.8V mode, it is recommended to remove the pull up resistors on the carrier board. The i.MX 8 features internal pull-up resistors that can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage
Default Speed	25 MHz	12.5 MByte/s	3.3V
High Speed	50 MHz	25 MByte/s	3.3V
SDR12	25 MHz	12.5 MByte/s	1.8V
SDR25	50 MHz	25 MByte/s	1.8V
DDR50	50 MHz	50 MByte/s	1.8V
SDR50	100 MHz	50 MByte/s	1.8V
SDR104	208 MHz	104 MByte/s	1.8V

The I/O voltage of one power block can be changed independently from the other block, but all signals of the corresponding block change their voltages together. The signals of the Apalis SD1 interface (i.MX 8 USDHC2) are located on one block while the signals of the Apalis MMC1 interface (i.MX 8 USDHC1) are on a different block. This means the SD1 and the MMC1 can change the I/O Voltage level independently. The USDHC2 power block consists only of the pins that are on the Apalis SD1 interface. However, the USDHC1 power block consists of one additional signal that is not in the Apalis MMC1 interface, module edge connector pin 159. If the MMC1 interface is used with 1.8V, the pin 159 also changes the voltage level.

The I/O voltage of the Apalis SD1 interface (i.MX 8 USDHC2) is provided by the LDO2OUT output of the main power management IC (PMIC). The I/O voltage of the Apalis MMC1 interface (i.MX 8 USDHC1) is provided by the LDO2OUT output of the secondary PMIC. The voltages are changed by controlling the according VSELECT of the PMICs.

Table 5-51 Apalis MMC1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
150	MMC1_CMD	USDHC1_CMD	CONN.USDHC1.CMD	I/O	Command
160	MMC1_D0	USDHC1_DATA0	CONN.USDHC1.DATA0	I/O	Serial Data 0
162	MMC1_D1	USDHC1_DATA1	CONN.USDHC1.DATA1	I/O	Serial Data 1

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
144	MMC1_D2	USDHC1_DATA2	CONN.USDHC1.DATA2	I/O	Serial Data 2
146	MMC1_D3	USDHC1_DATA3	CONN.USDHC1.DATA3	I/O	Serial Data 3
148	MMC1_D4	USDHC1_DATA4	CONN.USDHC1.DATA4	I/O	Serial Data 4, not used for SD cards
152	MMC1_D5	USDHC1_DATA5	CONN.USDHC1.DATA5	I/O	Serial Data 5, not used for SD cards
156	MMC1_D6	USDHC1_DATA6	CONN.USDHC1.DATA6	I/O	Serial Data 6, not used for SD cards
158	MMC1_D7	USDHC1_DATA7	CONN.USDHC1.DATA7	I/O	Serial Data 7, not used for SD cards
154	MMC1_CLK	USDHC1_CLK	CONN.USDHC1.CLK	O	Serial Clock
164	MMC1_CD#	ESAI1_TX1	LSIO.GPIO2.IO09	I	Card Detect (regular GPIO)

Table 5-52 Apalis SD1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
180	SD1_CMD	USDHC2_CMD	CONN.USDHC2.CMD	I/O	Command
186	SD1_D0	USDHC2_DATA0	CONN.USDHC2.DATA0	I/O	Serial Data 0
188	SD1_D1	USDHC2_DATA1	CONN.USDHC2.DATA1	I/O	Serial Data 1
176	SD1_D2	USDHC2_DATA2	CONN.USDHC2.DATA2	I/O	Serial Data 2
178	SD1_D3	USDHC2_DATA3	CONN.USDHC2.DATA3	I/O	Serial Data 3
184	SD1_CLK	USDHC2_CLK	CONN.USDHC2.CLK	O	Serial Clock
190	SD1_CD#	USDHC2_CD_B	CONN.USDHC2.CD_B	I	Card Detect (dedicated signal)

There are a few extra interface signals available for the MMC1 interface. These pins are not required for regular usage of the interface. The signals are available as alternate functions and therefore are not compatible with other Apalis modules.

Table 5-53 Additional MMC1 Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
158	MMC1_D7	USDHC1_DATA7	CONN.USDHC1.CD_B	I	Dedicated card detect signal. For compatibility reason, it is recommended to use the GPIO on pin 164 instead.
159	TS_6	USDHC1_STROBE	CONN.USDHC1.STROBE	I	Input clock for eMMC HS400 mode
156	MMC1_D6	USDHC1_DATA6	CONN.USDHC1.WP	I	Card write protec

5.15 Analogue Audio

The Apalis iMX8 offers analogue audio input and output channels. On the module, a NXP SGTL5000 chip handles the analogue audio interface. The SGTL5000 is connected over I²S (SAI1) with the i.MX 8 SoC. Please consult the NXP SGTL5000 datasheet for more information.

Table 5-54 Analogue Audio Interface Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
306	AAP1_MICIN	Analogue Input	Microphone input	10
310	AAP1_LIN_L	Analogue Input	Left Line Input	9
312	AAP1_LIN_R	Analogue Input	Right Line Input	8
316	AAP1_HP_L	Analogue Output	Headphone Left Output	4
318	AAP1_HP_R	Analogue Output	Headphone Right Output	1

5.16 Synchronous Audio Interface (SAI)

The i.MX 8 SoC features multiple Synchronous Audio Interfaces (SAI). Some of them are only used internally of the SoC for connecting other audio interfaces, others are available external.

Table 5-55 SAI Instance Configuration

SAI Instance	Tx/Rx Data Lines (stereo)	Tx/Rx FIFO Depth	Use Case
SAI0	1/1	64/64	Apalis standard digital audio interface
SAI1	1/1	64/64	On-module audio codec, cannot be used externally. It is also connected internally to the MQS
SAI2	0/1	-/64	Input only, Available on module edge connector as an alternate function, not compatible with other modules
SAI3	0/1	-/64	Input only, Available on module edge connector as an alternate function, not compatible with other modules
HDMI SAI TX 0	4/0	64/-	SoC Internal connection to HDMI and DisplayPort output (4xStereo = 8 channels)
HDMI SAI RX 0	0/4	-/64	Internal connection to HDMI input (not available on module edge connector)
SAI6	1/1	64/64	Audio Mixer interface, SoC internal connection
SAI6	0/1	-/64	Audio Mixer interface, SoC internal connection

The SAI interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS). The interfaces can be used to connect an additional external audio codec. Please be aware that some Apalis modules may provide different codec standards such as HD Audio or just a subset of AC97 and I2S on this interface. The SAI on the Apalis iMX8 cannot be used as HD Audio interface.

Table 5-56 Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
202	DAP1_D_IN	SAI1_RXFS	AUD.SAI0.RXD	I	Data Input to i.MX 8
196	DAP1_D_OUT	SAI1_RXC	AUD.SAI0.TXD	O	Data Output from i.MX 8
204	DAP1_SYNC	SPI2_CS1	AUD.SAI0.TXFS	I/O	Field Select (Transmit Frame Sync)
200	DAP1_BIT_CLK	SPI0_CS1	AUD.SAI0.TXC	I/O	Serial Clock (Transmit Bit Clock)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
198	DAP1_RESET#	ESAI1_SCKT	LSIO.GPIO2.IO07	O	Audio codec reset (regular GPO)

Some codecs need an external master reference clock. According to the Apalis standard, the module edge connector pin number 194 should be used as the master clock. However, the Apalis iMX8 does not feature master clock output on pin 194. There is an audio master clock available on pin 215 as an alternate function of the SPDIF out signal. Using this pin means losing the compatibility with other Apalis module. In order to get a compatible solution, either an assembly option for pin 194 and 215 could be a solution or using an external oscillator instead.

For controlling the I²S codec, an additional I²C interface is required, and the generic I²C interface I2C1is recommended for this purpose.

Table 5-57 Additional Digital Audio Port Signals (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
215	SPDIF1_OUT	SPDIF0_TX	AUD.ACM.MCLK_OUT1	O	Audio master clock output for external codec
223	SPI1_MISO	SPI0_SDI	AUD.SAI0.RXD	I	Alternate Data Input to i.MX 8
225	SPI1_MOSI	SPI0_SDO	AUD.SAI0.TXD	O	Alternate Data Output from i.MX 8
221	SPI1_CLK	SPI0_SCK	AUD.SAI0.RXC	I/O	Field Select (Receive Frame Sync)
227	SPI1_CS	SPI0_CS0	AUD.SAI0.RXFS	I/O	Serial Clock (Receive Bit Clock)

Table 5-58 Additional Digital Audio Ports (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
35	SATA1_ACT#	ESAI1_TX0	AUD.SAI2.RXD	I	Data Input to i.MX 8
164	MMC1_CD#	ESAI1_TX1	AUD.SAI2.RXFS	I/O	Field Select (Receive Frame Sync)
198	DAP1_RESET#	ESAI1_SCKT	AUD.SAI2.RXC	I/O	Serial Clock (Receive Bit Clock)
17	GPIO8	MLB_DATA	AUD.SAI3.RXD	I	Data Input to i.MX 8
63	TS_1	MLB_CLK	AUD.SAI3.RXFS	I/O	Field Select (Receive Frame Sync)
15	GPIO7	MLB_SIG	AUD.SAI3.RXC	I/O	Serial Clock (Receive Bit Clock)

5.16.1 Synchronous Audio Interface used as I²S

The SAI can be used as I²S interfaces with the following features:

- Master or Slave
- Asynchronous 64x32 bit FIFO for each transmitter and receiver
- Word size from 8-bit to 32-bit

The following signals are used for the I²S interface:

Table 5-59 Synchronous Audio Interface used as Maser I²S

i.MX 8 Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_TXD	SDIN	O	Serial Data Output from i.MX 8
SAIx_RXD	SDOUT	I	Serial Data Input to i.MX 8
SAIx_TXFS	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx_TXC	SCK	I/O	Serial Continuous Clock

Table 5-60 Synchronous Audio Interface used as Slave I²S

i.MX 8 Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_RXD	SDOUT	I	Serial Data Input to i.MX 8
SAIx_TXD	SDIN	O	Serial Data Output from i.MX 8
SAIx_TXFS	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx_TXC	SCK	I/O	Serial Continuous Clock

5.16.2 Synchronous Audio Interface used as AC'97

The SAI interface can be configured as AC'97 compatible interface. The AC'97 Audio interface does not need an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97Audio codec does require a master reference clock, but instead a separate crystal/oscillator can be used. Please take care with the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host, and not to the signal direction.

Table 5-61 Synchronous Audio Interface used as AC'97

i.MX 8 Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx_RXD	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 8
SAIx_TXD	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 8
SAIx_TXFS	SYNC	O	AC'97 Audio Sync
SAIx_TXC	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.17 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with a variety of serial audio devices including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Apalis module standard.

Features

- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 6 transmitters and up to 4 receivers
- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20 or 24bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-62 ESAI Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
197	CAM1_HSYNC	ESAI0_SCKT	AUD.ESAI0.SCKT	I/O	TX serial bit clock

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
273	LCD1_G2	ESAI0_FST	AUD.ESAI0.FST	I/O	Frame sync for transmitters and receivers in the synchronous mode and for the transmitters only in asynchronous mode
195	CAM1_VSYNC	ESAI0_SCKR	AUD.ESAI0.SCKR	I/O	RX serial bit clock
271	LCD1_G1	ESAI0_FSR	AUD.ESAI0.FSR	I/O	RX frame sync signal in asynchronous mode
191	CAM1_PCLK	MCLK_IN0	AUD.ESAI0.RX_HF_CLK	I/O	RX high frequency clock
177	CAM1_D5	ESAI0_TX0	AUD.ESAI0.TX0	I/O	TX data 0
179	CAM1_D4	ESAI0_TX1	AUD.ESAI0.TX1	I/O	TX data 1
181	CAM1_D3	ESAI0_TX2_RX3	AUD.ESAI0.TX2_RX3	I/O	TX data 2 or RX data 3
183	CAM1_D2	ESAI0_TX3_RX2	AUD.ESAI0.TX3_RX2	I/O	TX data 3 or RX data 2
185	CAM1_D1	ESAI0_TX4_RX1	AUD.ESAI0.TX4_RX1	I/O	TX data 4 or RX data 1
187	CAM1_D0	ESAI0_TX5_RX0	AUD.ESAI0.TX5_RX0	I/O	TX data 5 or RX data 0

5.18 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

Features:

- Input sampling rate measurement
- CD Text
- S/PDIF receiver to S/PDIF transmitter bypass mode
- IEC 60958 consumer format
- Sampling rates from 32kHz to 192kHz

Table 5-63 S/PDIF Data Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
215	SPDIF1_OUT	SPDIF0_TX	AUD.SPDIF0.TX	O	Serial data output
217	SPDIF1_IN	SPDIF0_RX	AUD.SPDIF0.RX	I	Serial data input

5.19 Medium Quality Sound (MQS)

The medium quality sound interface can be used to generate medium quality audio via a standard GPIO. The PWM output signal does not require an external DAC or codec chip. The advantage over using the high quality analogue audio output of the on module SGTL5000 is the option to use a simple switching power amplifier circuit (Class-D amplifier).

The MQS is sourced by SAI1 with a 2 channel 16 bit 44.1 kHz or 48 kHz audio signals which is basically an I^2S signal. Since this is the same SAI channel that is used by the on module audio codec, it is not possible to use MQS simultaneous with the analogue audio output. The signal to noise ratio (SNR) is expected to be no more than 20 dB for signals below 10 kHz. For signals with higher frequencies, the SNR is even worse.

Table 5-64 MQS Interface Signals (incompatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
184	SD1_CLK	USDHC2_CLK	AUD.MQS.R	O	Left MQS Channel
217	SPDIF1_IN	SPDIF0_RX			
180	SD1_CMD	USDHC2_CMD	AUD.MQS.L	O	Right MQS Channel
215	SPDIF1_OUT	SPDIF0_TX			

5.20 Touch Panel Interface

The Apalis iMX8 offers a 4-wire resistive touch interface. The touch interface is implemented with a simple external circuit and makes use of the ADCs that are integrated in the i.MX 8 SoC. The external circuit allows drawing more current than the standard GPIO of the SoC would allow. This is necessary since some resistive touch panel require higher current. The standard Linux BSP contains the support of the resistive touch panel interface.

Since the ADC input pins of the i.MX 8 are only 1.8V rated, the touch interface is running on 1.8V as well.

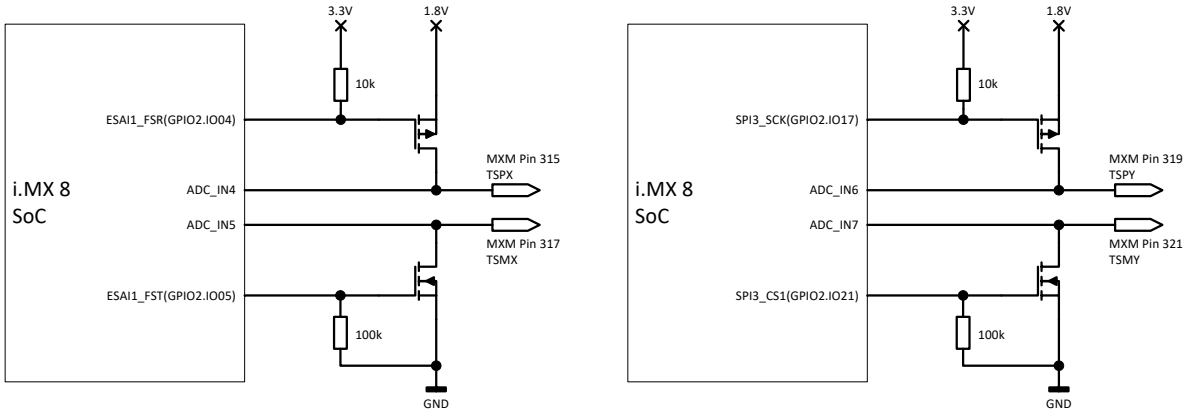

Figure 16: External Circuit for Touch Panel Interface

Table 5-65 Touch Interface Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Remarks
315	AN1_TSPX	ADC_IN4	DMA.ADC.IN4	I	ADC input for X+
		ESAI1_FSR	LSIO.GPIO2.IO04	O	FET gate driver for X+
317	AN1_TSMX	ADC_IN5	DMA.ADC.IN5	I	ADC input for X-
		ESAI1_FST	LSIO.GPIO2.IO05	O	FET gate driver for X-
319	AN1_TSPY	ADC_IN6	DMA.ADC.IN6	I	ADC input for Y+
		SPI3_SCK	LSIO.GPIO2.IO17	O	FET gate driver for Y+
321	AN1_TSMY	ADC_IN7	DMA.ADC.IN7	I	ADC input for Y-
		SPI3_CS1	LSIO.GPIO2.IO21	O	FET gate driver for Y-

If the touch panel interface is unused, leave the pins unconnected and disable the driver. Connecting the pins to ground (especially TSPX and TSPY) while having the driver still enabled could cause a short circuit if the driver turns on the high side FET.

5.21 Analogue Inputs

The Apalis module standard features four dedicated pins for analogue inputs. These analogue inputs are read by the ADCs that are located in the i.MX 8 SoC. The SoC features one ADC with totally up to eight channels that are available at the module edge connector. Only four of these eight channels are compatible with other Apalis modules, the other four channels are located on the touch interface pins. If the transistor drivers are disabled, these inputs can also be used.

Pay attention, the input voltage range is only 1.8V and not 3.3V as on other Apalis modules. On the module, there are 1k series resistors placed in the ADC lines (not on the touch interface pins) in order to protect the SoC input.

Features

- 12-bit ADC
- Linear successive approximation algorithm
- 0 to 1.8V (full scale)
- DMA support
- Trigger detection
- Automatic compare for less-than, greater-than, within rage, or out-of range with “store on true” and “repeat until true” option
- Interrupt support

Table 5-66 Analogue Inputs Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Remarks
305	AN1_ADC0	ADC_IN0	DMA.ADC.IN0	I	Dedicated ADC input
307	AN1_ADC1	ADC_IN1	DMA.ADC.IN1	I	Dedicated ADC input
309	AN1_ADC2	ADC_IN2	DMA.ADC.IN2	I	Dedicated ADC input
311	AN1_TSWIP_ADC3	ADC_IN3	DMA.ADC.IN3	I	Dedicated ADC input

Table 5-67 Additional Analogue Inputs Pins (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Remarks
315	AN1_TSPX	ADC_IN4	DMA.ADC.IN4	I	ADC input (primary used as touch interface)
317	AN1_TSMX	ADC_IN5	DMA.ADC.IN5	I	ADC input (primary used as touch interface)
319	AN1_TSPY	ADC_IN6	DMA.ADC.IN6	I	ADC input (primary used as touch interface)
321	AN1_TSMY	ADC_IN7	DMA.ADC.IN7	I	ADC input (primary used as touch interface)

5.22 Camera Interface

Even though the Apalis module standard reserves dedicated pins for parallel camera inputs, the Apalis iMX8 module does not feature such an interface. Nevertheless, the Apalis iMX8 features up to two MIPI/CSI-2 compatible camera inputs. The interfaces use the MIPI D-PHY as physical layer.

The CSI signals are located in the type-specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

Features

- Scalable data lane support, 1 to 4 Data Lanes

- Up to 1.5Gbps per lane, providing 4K30 capability for the 4 lanes
- Supports 10Mbps data rate in low power modes
- Implements all three CSI-2 MIPI layers (pixel to byte backing, low level protocol, and lane management)
- Unidirectional master operation supported

As the CSI is a high-speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is type specific. Please find the according information in the table below.

Table 5-68 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	750MHz (1.5GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-69 CSI interface signals

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	MIPI_CSI1_CLK_P	CSI1_CLK+	I	CSI interface 1 clock
161	TS_DIFF18-	MIPI_CSI1_CLK_N	CSI1_CLK-	I	
157	TS_DIFF17+	MIPI_CSI1_DATA0_P	CSI1_D1+	I/O	CSI interface 1 data lane 1
155	TS_DIFF17-	MIPI_CSI1_DATA0_N	CSI1_D1-	I/O	
151	TS_DIFF16+	MIPI_CSI1_DATA1_P	CSI1_D2+	I	CSI interface 1 data lane 2
149	TS_DIFF16-	MIPI_CSI1_DATA1_N	CSI1_D2-	I	
145	TS_DIFF15+	MIPI_CSI1_DATA2_P	CSI1_D3+	I	CSI interface 1 data lane 3
143	TS_DIFF15-	MIPI_CSI1_DATA2_N	CSI1_D3-	I	
139	TS_DIFF14+	MIPI_CSI1_DATA3_P	CSI1_D4+	I	CSI interface 1 data lane 4
137	TS_DIFF14-	MIPI_CSI1_DATA3_N	CSI1_D4-	I	
127	TS_DIFF12+	MIPI_CSI0_CLK_P	CSI3_CLK+	I	CSI interface 3 clock
125	TS_DIFF12-	MIPI_CSI0_CLK_N	CSI3_CLK-	I	
121	TS_DIFF11+	MIPI_CSI0_DATA0_P	CSI3_D1+	I/O	CSI interface 3 data lane 1
119	TS_DIFF11-	MIPI_CSI0_DATA0_N	CSI3_D1-	I/O	
115	TS_DIFF10+	MIPI_CSI0_DATA1_P	CSI3_D2+	I	CSI interface 3 data lane 2
113	TS_DIFF10-	MIPI_CSI0_DATA1_N	CSI3_D2-	I	
109	TS_DIFF9+	MIPI_CSI0_DATA2_P	CSI3_D3+	I	CSI interface 3 data lane 3
107	TS_DIFF9-	MIPI_CSI0_DATA2_N	CSI3_D3-	I	
103	TS_DIFF8+	MIPI_CSI0_DATA3_P	CSI3_D4+	I	CSI interface 3 data lane 4
101	TS_DIFF8-	MIPI_CSI0_DATA3_N	CSI3_D4-	I	

Some cameras require an external master reference clock. According to the Apalis standard, the module edge connector pin number 193 should be used as master clock. However, the Apalis iMX8 does not feature master clock output on pin 193. An external oscillator could be used instead.

Table 5-70 Additional Camera Interface Signals (Apalis Standard)

X1 Pin#	Apalis Signal Name	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
201	I2C3_SDA (CAM)	SIM0_POWER_EN	DMA.I2C3.SDA	I/O	Camera control I^2C
203	I2C3_SCL (CAM)	SIM0_PD	DMA.I2C3.SCL	O	Camera control I^2C

5.23 Clock Output

The Apalis standard reserves two pins (193 and 194) as reference clock outputs for an external audio codec or camera sensor. However, the Apalis iMX8 does not feature clock outputs on these two pins. There is an audio master clock output available on pin 215 as alternate function of the SPDIF output signal.

Table 5-71 Audio Master Clock Output (not compatible with other modules)

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
215	SPDIF1_OUT	SPDIF0_TX	AUD.ACM.MCLK_OUT1	O	Audio master clock output for external codec

The PCIe interface requires a 100MHz reference clock for all the peripherals and switches. The Apalis standard defines one differential pair for the reference clock. Zero delay clock buffers can be used if more than one reference clock sink is present on the carrier board. The reference clock is generated by a separate PCIe clock generator that meets the specifications for Gen3 PCIe.

Table 5-72 PCIe Reference clock Signals

X1 Pin#	Apalis Signal Name	DSC557-03 Ball Name	I/O	Description
55	PCIE1_CLK+	CLK1+	O	100MHz Reference clock differential pair.
53	PCIE1_CLK-	CLK1-	O	

5.24 Keypad

The i.MX 8 SoC would feature a dedicated keypad interface. Some of the are located as alternate functions of the ADC and touch interface pins. These pins are only 1.8V rated. Other pins of the dedicated keypad interface are having 3.3V logic level. Therefore, it is not recommended to use the dedicated keypad interface. However, you can use any free GPIOs to realize a matrix keypad interface.

5.25 Controller Area Network (CAN)

The i.MX 8 SoC features a total of three Flexible Controller Area Network (FlexCAN) interfaces. Two of these three FlexCAN interfaces are available on the Apalis standard pins. The third one is available as alternate functions of GPIO pins. The CAN protocol complies with the CAN 2.0B specification and ISO11898-1 standard. It supports both standard and extended message frames.

Features

- Bit rate up to 1Mb/s
- Standard and extended data frames
- Content-related addressing
- Flexible mailboxes of zero to eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-73 CAN Signal Pins

X1 Pin#	Apalis Signal Name	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
14	CAN1_TX	FLEXCAN0_TX	DMA.FLEXCAN0.TX	O	CAN port 1 transmit pin
12	CAN1_RX	FLEXCAN0_RX	DMA.FLEXCAN0.RX	I	CAN port 1 receive pin
18	CAN2_TX	FLEXCAN1_TX	DMA.FLEXCAN1.TX	O	CAN port 2 transmit pin
16	CAN2_RX	FLEXCAN1_RX	DMA.FLEXCAN1.RX	I	CAN port 2 receive pin

Table 5-74 Additional CAN interface (not compatible with other modules)

X1 Pin#	Apalis Signal Name	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
13	GPIO6	FLEXCAN2_TX	DMA.FLEXCAN2.TX	O	CAN port 3 transmit pin
11	GPIO5	FLEXCAN2_RX	DMA.FLEXCAN2.RX	I	CAN port 3 receive pin

5.26 Media Local Bus (MLB150)

The Media Local Bus is predominantly used in automotive for high-bandwidth audio video and control information transport. MLB is a standardized on-PCB, inter-chip communication bus for MOST (Media Oriented Systems Transport) based devices. As MLB is not part of the Apalis module specifications, the interface is not compatible with other Apalis modules. The i.MX 8 SoC features a 3-pin (single-ended) and a 6-pin (differential pair) interface for the MLB. However, only the single ended 3-pin variant is available on the module edge connector. The MLB interface might not be supported by the standard Toradex BSP.

Table 5-75 MLB Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
63	TS_1	MLB_CLK	CONN.MLB.CLK	I	Single ended clock
17	GPIO8	MLB_DATA	CONN.MLB.DATA	I/O	Single ended data
15	GPIO7	MLB_SIG	CONN.MLB.SIG	I/O	Single ended signal

5.27 Quad Serial Peripheral Interface (QuadSPI, QSPI)

The Quad Serial Peripheral Interface is an SPI interface with four bidirectional data lines instead of one transmit and one receive data line. The interface is mainly used for connecting to flash devices. The QuadSPI is incompatible with the Apalis family. The pins are located on the module edge connector as secondary functions.

Table 5-76 QSPI Signal Pins

X1 Pin#	Apalis Std Function	i.MX 8 Ball Name	i. MX 8 Function	I/O	Description
295	LCD1_B4	QSPI1A_SS0_B	LSIO.QSPI1A.SS0_B	O	Chip Select 0
299	LCD1_B6	QSPI1A_SS1_B	LSIO.QSPI1A.SS1_B	O	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
301	LCD1_B7	QSPI1A_SCLK	LSIO.QSPI1A.SCLK	O	Serial Clock
287	LCD1_B0	QSPI1A_DATA0	LSIO.QSPI1A.DATA0	I/O	Serial I/O for command, address, and data
289	LCD1_B1	QSPI1A_DATA1	LSIO.QSPI1A.DATA1	I/O	Serial I/O for command, address, and data
291	LCD1_B2	QSPI1A_DATA2	LSIO.QSPI1A.DATA2	I/O	Serial I/O for command, address, and data
293	LCD1_B3	QSPI1A_DATA3	LSIO.QSPI1A.DATA3	I/O	Serial I/O for command, address, and data
297	LCD1_B5	QSPI1A_DQS	LSIO.QSPI1A.DQS	I	Data Strobe signal, required on some high speed DDR devices

5.28 JTAG

The JTAG interface is not normally required for software development with the Apalis iMX8. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The location is standardised by the Apalis specification. Please be aware, the reference voltage for the interface is 1.8V. The RTCK signal is not provided by the SoC. The pad is left unconnected on the module. Do not connect the other test pad. They are used during production testing for validating the power supply.

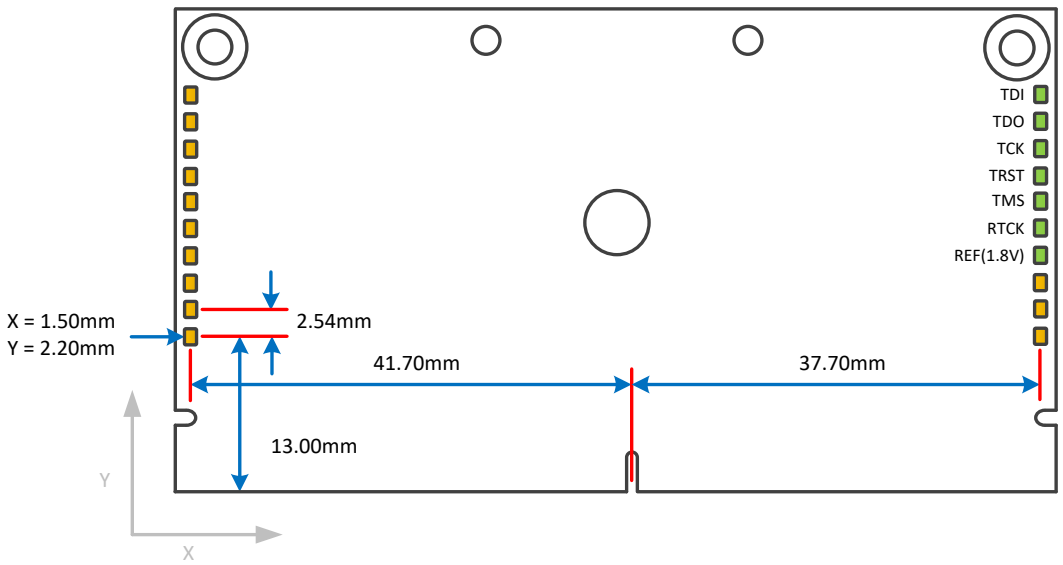

Figure 17 JTAG test point location on bottom side of module

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Apalis iMX8 even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in the recovery mode, the USBO1 interface is used to connect it to a host computer. You will find additional information at our Developer Center (http://developer.toradex.com).

In order to enter recovery mode, the recovery mode pads need to be shorted during the initial power on (cold boot) of the module. Figure 18 shows the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling **up** pin 63 of the module edge connector (TS_1) with a 1kΩ resistor while booting. This pin is located in the type-specific area. It is not guaranteed that other Apalis modules will be able to be placed into recovery mode in the same way.

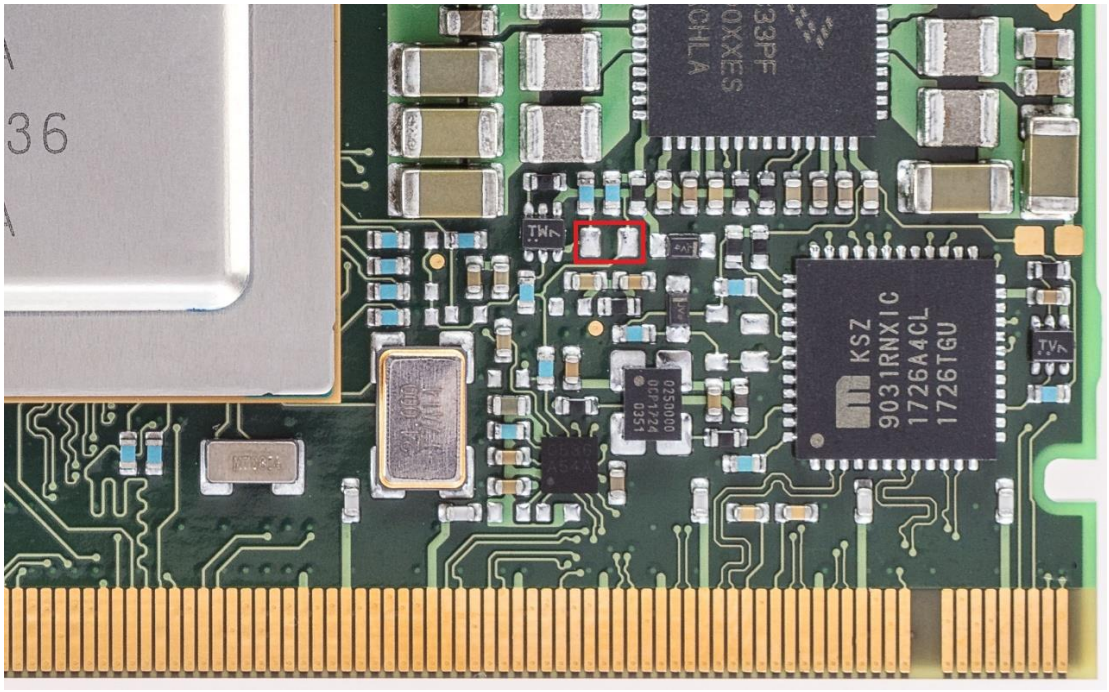

Figure 18 Location of recovery mode pads

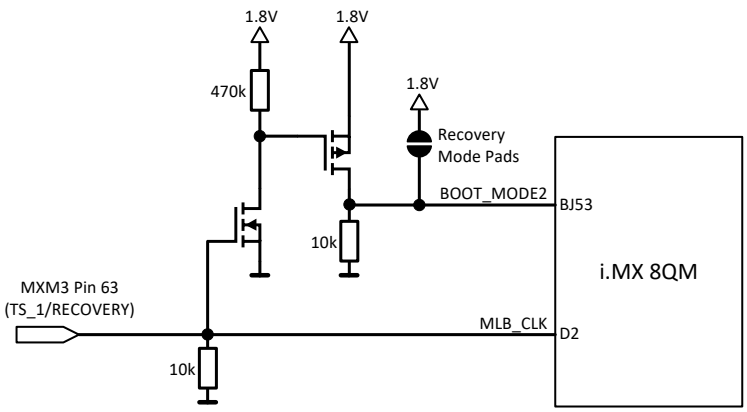

Figure 19: Recovery Mode Glue Logic

7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document which can be downloaded on our website at:

https://developer.toradex.com/products/apalis-som-family/modules/apalis-imx8#errata

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC	Main power supply	-0.3	3.6	V
Vmax_AVCC	Analogue power supply	-0.3	3.6	V
Vmax_VCC_BACKUP	RTC power supply	-0.3	4.3	V
Vmax_IO_3.3V	SoC IO pins with 3.3V logic level	-0.3	3.6	V
Vmax_AN1	ADC and touch analogue input	-0.5	2.1	V
Vmax USBO1_VBUS	Input voltage at USBO1_VBUS	-0.3	5.5	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3	3.465	V
AVCC	Analogue power supply	3.0	3.3	3.465	V
VCC_BACKUP	RTC power supply	2.5	3.3	3.6	V

8.3 Electrical Characteristics

Table 8-3 Typical Power Consumption

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	TBD	A
IDD_HIGHCPU	Maximal CPU Load, 3D-graphic test	TBD	A
IDD_HD	Full HD Video on HDMI (h.264 decoding, CPU full load)	TBD	A
IDD_SUSPEND	Module in Suspend State	TBD	mA
IDD_BACKUP	Current consumption of internal RTC	TBD	µA

These typical values are just for indication. The actual consumption varies between different modules and is temperature dependent. The current consumption can be higher than IDD_HIGHCPU, depending on the load of the GPU and the temperature.

8.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.

8.5 Mechanical Characteristics

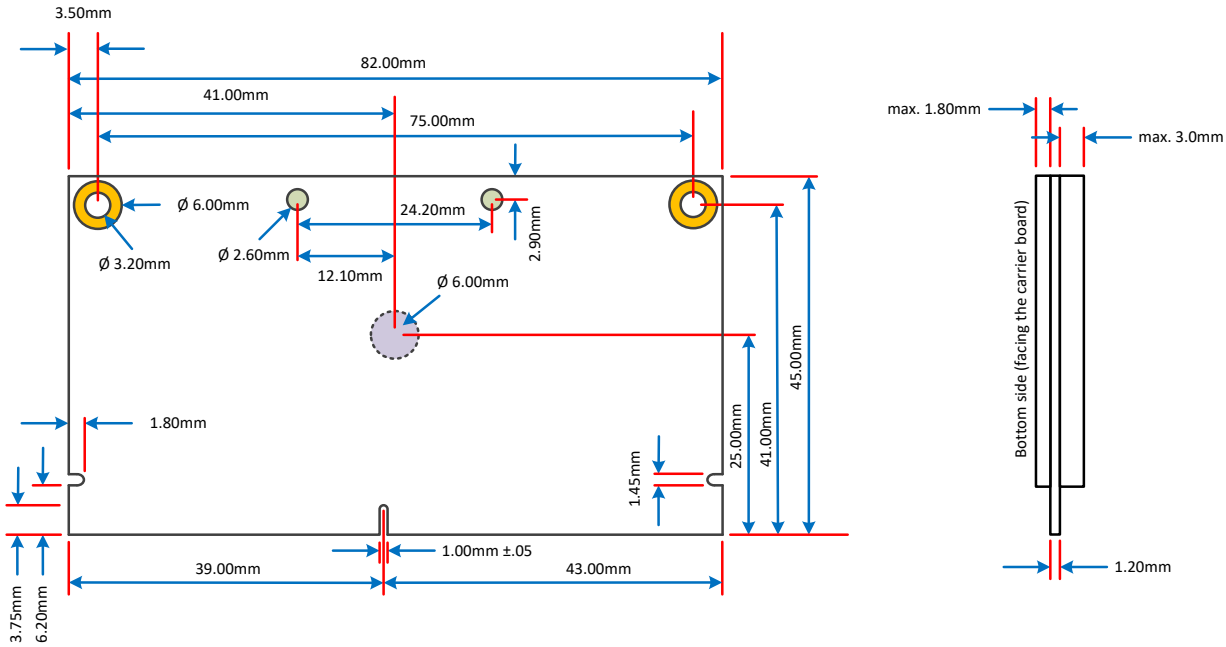

Figure 20 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

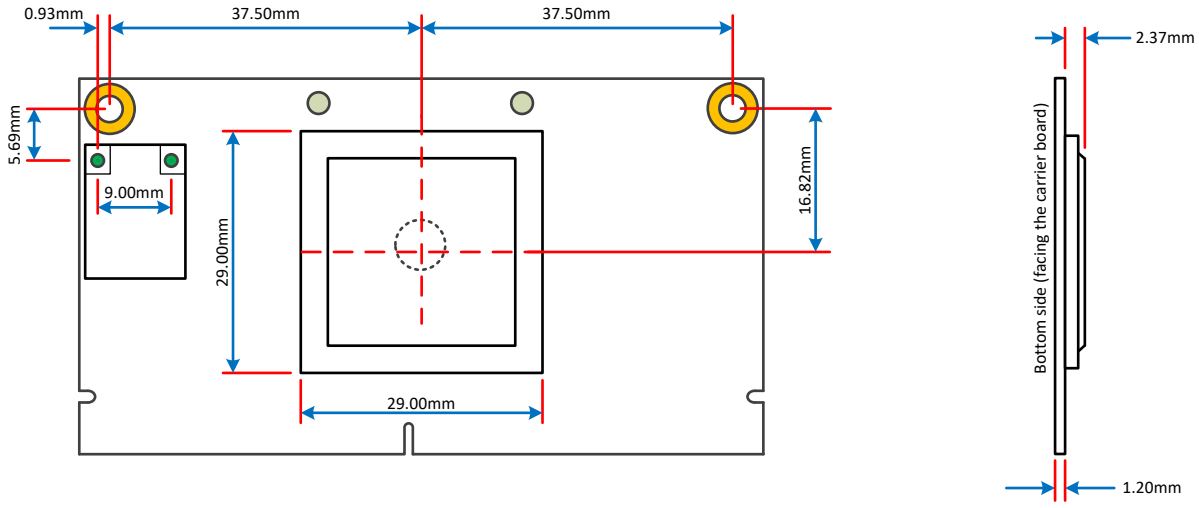

Figure 21 Mechanical position of i.MX 8 SoC (top view)
Tolerance for all measures: +/- 0.1mm

8.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board-to-board stacking heights from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314B1-2-R300 which has a board-to-board height of 3.0mm. This stacking height allows using the MXM SnapLock system for easy fixing of the module to the carrier board.

You can refer to a list of other MXM3 connectors on the developer website.

8.6 Thermal Specification

The Apalis iMX8 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The i.MX 8 SoC features DVFS on each of the CPU cluster independently, as well as independently on each of the two GPUs. This allows the Apalis iMX8 to deliver higher performance at lower average power consumption compared to other solutions. The big/LITTLE architecture with the two Cortex A72 (high speed) and four Cortex A53 (low power consumption) allows to optimize the workload for the lowest possible power consumption.

The Apalis iMX8 modules come with embedded temperature sensors. The sensors are measuring the die (junction) temperature and are used for determining whether the cores need to be throttled in order to prevent overheating. In the event that the temperature of the i.MX 8 reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- It is generally advised to use a heat sink on the Apalis iMX8
- If you need the full CPU/Graphics performance over a long period of time, we recommend well designing the whole heat dissipation solution of the system.
- Toradex provides a heatsink for the Apalis iMX8. This solution can be used passively as well as in combination with a fan. More information can be found here: http://developer.toradex.com/products/apalis-heatsink
- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents in idle. A die temperature increase from 25°C to 125°C will increase the leakage by a factor of 10
- The leakage of a single A72 core is roughly 4 times higher than a single A53. Therefore, the operating system should turn off the A72 cores in light load situations

In general, the more effective the thermal solution is, the more performance you can get out of the Apalis iMX8 Module.

Table 8-4 1.1 Thermal Specification Apalis iMX8QM 4GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8QM only. ($R_{\theta JA}$)[2]		11.7		°C/W
Thermal Resistance Junction-to-Top of i.MX 8QM chip case. ($R_{\theta JCtop}$)[2]		0.28		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

Table 8-5 1.1 Thermal Specification Apalis iMX8QM 4GB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C

Description	Min	Typ	Max	Unit
Thermal Resistance Junction-to-Ambient, i.MX 8QM only. ($R_{\theta JA}$)[2]		11.7		°C/W
Thermal Resistance Junction-to-Top of i.MX 8QM chip case. ($R_{\theta JCtop}$)[2]		0.28		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] All components are rated to run until -40°C.

Table 8-6 1.1 Thermal Specification Apalis iMX8QP 2GB WB

Description	Min	Typ	Max	Unit
Operating temperature range	-25[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8QP only. ($R_{\theta JA}$)[2]		11.7		°C/W
Thermal Resistance Junction-to-Top of i.MX 8QP chip case. ($R_{\theta JCtop}$)[2]		0.28		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The LPDDR4 RAM is limiting the minimum operating temperature. The rest of the components are capable to run until -40°C, except for the Wi-Fi module which limits to -30°C.

Table 8-7 1.1 Thermal Specification Apalis iMX8QP 2GB

Description	Min	Typ	Max	Unit
Operating temperature range	-25[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		125	°C
Thermal Resistance Junction-to-Ambient, i.MX 8QP only. ($R_{\theta JA}$)[2]		11.7		°C/W
Thermal Resistance Junction-to-Top of i.MX 8QP chip case. ($R_{\theta JCtop}$)[2]		0.28		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The LPDDR4 RAM is limiting the minimum operating temperature. The rest of the components are capable to run until -40°C

8.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance

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