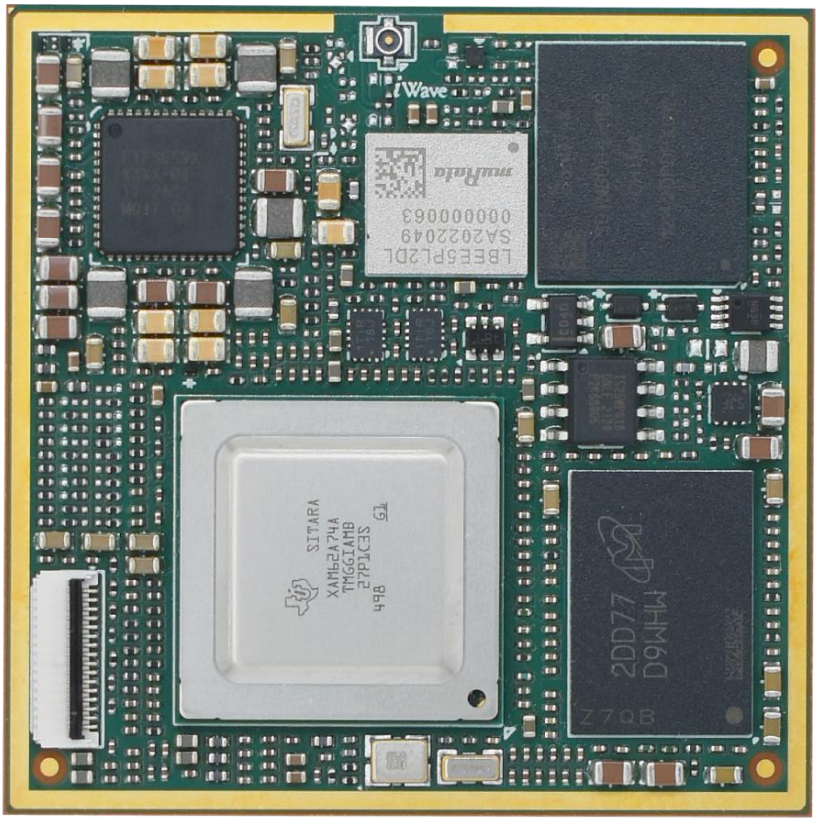
iW-RainboW-G55M
AM62Ax Quad/Dual/Solo OSM LGA Module Hardware User Guide



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DRAFT VERSION

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the TI's AM62Ax (Quad) Application processor based OSM V1.1 specification compatible LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the AM62Ax OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.1 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the following key characteristics like Completely machine processible during soldering, assembly and testing, Pre-tinned LGA package for direct PCB soldering without connector.

The OSM Module definition targeting application that requires low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

TI's AM62Ax SoC based OSM LGA Module is rich with AM62Ax features along with on SOM LPDDR4, eMMC, QSPI, Wi-Fi & BT module and comes in compact 45mm x 45mm form factor (Size L). The Module PCB has 662 contacts which can be mounted as LGA/BGA on OSM carrier card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BGA	Ball Grid Array
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DRAM	Dynamic Random Access Memory
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
EMS	Electronics manufacturing services
ESAI	Enhanced Serial Audio Interface
SPI	Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LGA	Land Grid Array
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
McASP	Multichannel Audio Serial Port
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System on Chip
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit
Wi-Fi	Wireless Fidelity
BT	Bluetooth

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Signal
USB HS	Universal Serial Bus High Speed differential pair signals
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM SOM.

1.5 References

- AM62Ax_DS_SPRSP77_6_17_2022.pdf
- AM62A Technical Reference Manual - SPRUJ16 - NDA - 23-Jul-2022 Draft.pdf
- OSM Specification V1.1

1.6 Important Note

In this document, wherever AM62Ax SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "Functionality Name"

  Example: QSPI0_CLK

  In this signal, ***QSPI0_CLK*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO0_37)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO0_37*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about AM62Ax OSM LGA Module SOM and Hardware architecture with high level block diagram.

2.1 AM62Ax OSM LGA Module Block Diagram

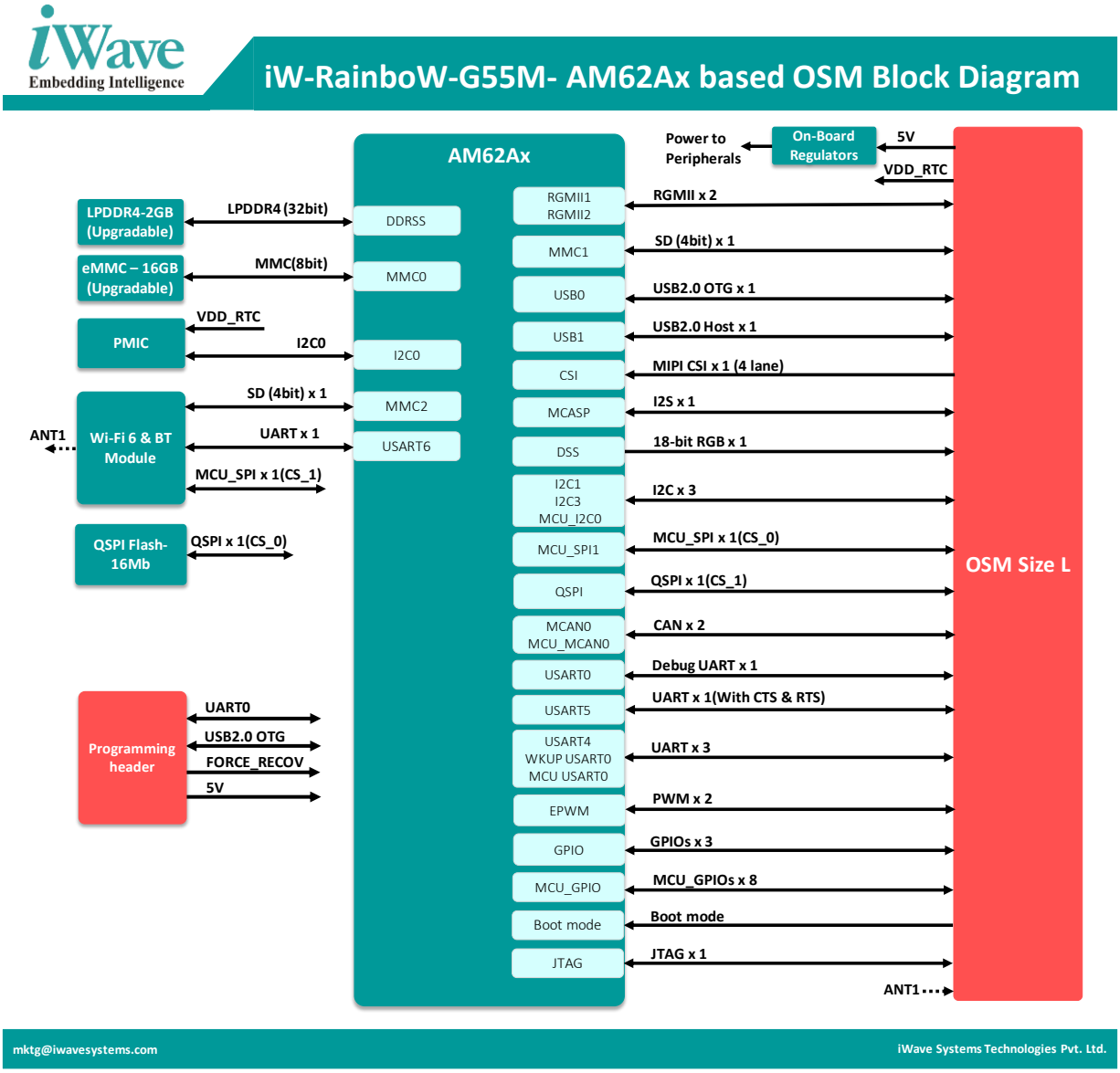

Figure 1: AM62Ax OSM LGA MODULE Block Diagram

2.2 AM62Ax SOM Features

AM62Ax OSM LGA Module supports the following features.

SoC

- AM62Ax Q/D/S Core Applications Processor:
  - AM62A74 Quad Core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
  - AM62A72 Dual Core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
  - AM62A34 Quad core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
  - AM62A32 Dual core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
  - AM62A31 Single core: 1 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS

Power

- TPS6593-Q1 PMIC

Memory

- LPDDR4 With Inline ECC - 2GB (Expandable up to 8GB)[1]
- eMMC Flash - 16GB (Expandable up to 128GB)[2]
- QSPI Flash – 16Mb

Other On-SOM Features

- IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + BT 5.3 + EEE802.15.4
- Programming Header

OSM LGA Interfaces

From SoC Domain:

- RGMII x 2
- SDIO x 1 (4-bit x 1)
- USB 2.0 x 2 Port
- MIPI CSI x 1 (4 Lane)
- SAI/I2S (Audio Interface) x 1 Port
- SPI x 1 Port
- QSPI x 1 Port (CS1)
- RGB x 1 (18 Bit)
- Data UART (with CTS & RTS) x 1 Port
- Data UART (without CTS & RTS) x 2 Port (One port can be used as Debug Port)
- GPIOs x 3
- MCAN x 1 Port
- I2C x 2 Ports

- JTAG x 1 Port
- PWM x 2
- Boot mode

From MCU Domain:

- CAN x 1 Port
- I2C x 1
- SPI x 1 (With 2 Chip select)
- Data UART x 1
- Wakeup UART x 1
- GPIOs x 8

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 45mm X 45mm (OSM V1.1 Specification)

1. *The AM62Ax supports up to 8GB (32-bit) if LPDDR4 chip is available.*
2. *Memory Size will differ based on iWave's SOM Product Part Number.*

2.3 AM62Ax SoC

iW-RainboW-G55M OSM LGA Module can support AM62Ax SoCs from TI. The AM62Ax Main domain consists of Quad core and MCU domain consists of dual core:

- AM62A74 Quad Core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
- AM62A72 Dual Core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
- AM62A34 Quad core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
- AM62A32 Dual core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
- AM62A31 Single core: 1 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS

The AM62Ax processors along with ARM core supports integrated single core Deep Learning Accelerator (C7x256v) of up to 2 TOPs, Image Signal Processor, 4Kp30 video encode and decode capable VPU, 1 x display controllers. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI, eMMC 5.1, SD 3.0, USB 2.0 and Dual core MCU domain integrated with FFI & Device Management.

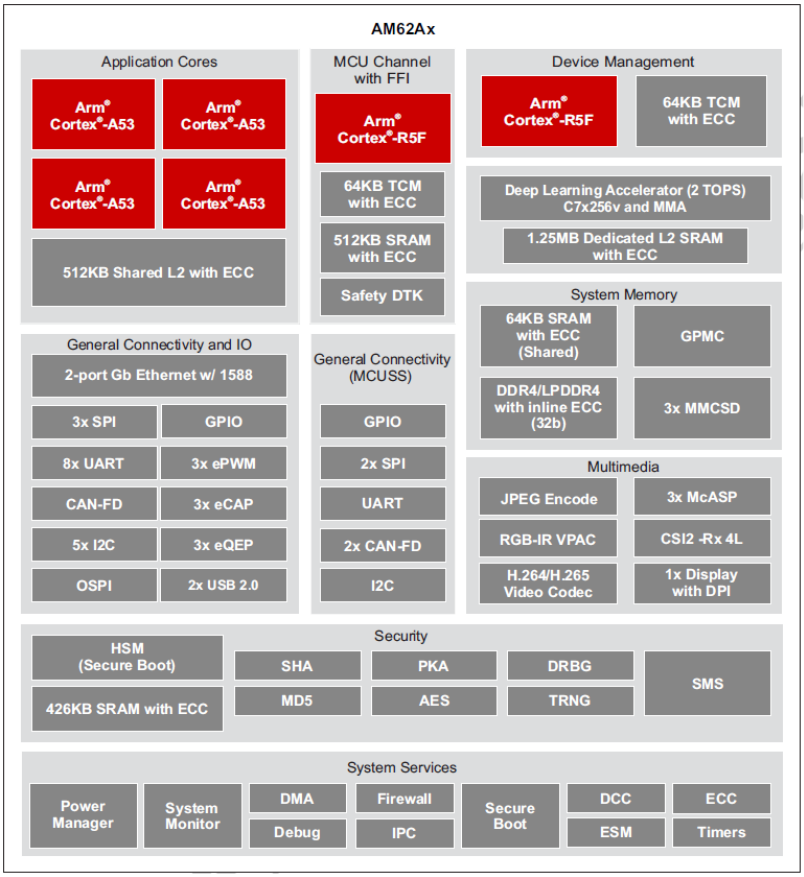

Figure 2: AM62Ax Block Diagram

Note: The AM62Ax processor offers numerous advanced features, please refer the latest AM62Ax Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 TPS6593-Q1 PMIC

The AM62Ax OSM LGA Module uses one TPS6593-Q1 PMIC (U5) for module power management. The TPS6593-Q1 features five high efficiency step-down regulators and four linear regulators. The TPS6593-Q1 includes a 32-KHz crystal oscillator, which generates an accurate 32-KHz clock for the integrated RTC module. A backup-battery management provides power to the crystal oscillator and the real-time clock (RTC) module from a coin cell battery or a super-cap in the event of power loss from the main supply. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The TPS6593-Q1 PMIC comes in 56pin 8x8 VQFN package and is placed on the top side of the SOM.

2.5 Memory

2.5.1 LPDDR4 RAM with Inline ECC

The AM62Ax OSM LGA Module supports 2GB LPDDR4 RAM memory by default using 32bit DDR_CH0 channel of AM62Ax SoC to support LPDDR4 up to 1600Mbps. LPDDR4 part U15 is placed on top side of the SOM. The RAM size can be expandable up to maximum of 8GB (if chips are available). To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The AM62Ax OSM LGA Module supports 16GB eMMC as default boot and storage device. This is directly connected to MMC0 controller of the AM62Ax SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) voltage levels.

The eMMC flash memory (U4) is physically located on top side of the LGA Module. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 QSPI Flash

The AM62Ax OSM LGA Module supports 16Mb QSPI using chip select 0 as optional boot and storage device. This is directly connected to OSPI controller of the AM62Ax SoC and operates at 1.8V (I/O supply).

The QSPI flash memory (U12) is physically located on top side of the LGA Module.

2.6 Network & Communiation

2.6.1 Wi-Fi and Bluetooth Interface

The AM62Ax OSM LGA Module is integrated with Murata's "LBES5PL2EL-SMP" based Wi-Fi+Bluetooth+IEEE802.15.4 module. LBES5PL2EL-SMP module is complaint with IEEE802.11a/b/g/n/ac/ax, SISO, Bluetooth specification v5.2 and IEEE802.15.4. It supports standard SDIO3.0 interface for WLAN, UART interfaces support for Bluetooth is Host Controller Interface (HCI) and SPI interface supports for IEEE802.15.4. Connection to a host processor is through SDIO, High-Speed UART interfaces and SPI.

The AM62Ax OSM LGA Module uses SoC UART6 interface for Bluetooth, MMC2 interface for Wi-Fi and MCU SPI With CS1 interface for IEEE802.15.4 in a default configuration. In the OSM LGA module, antenna pins of LBES5PL2EL-SMP Bluetooth and Wi-Fi is connected to J1 connector and optionally connected to A16th pin of OSM.

Wi-Fi + Bluetooth Antenna(J1)

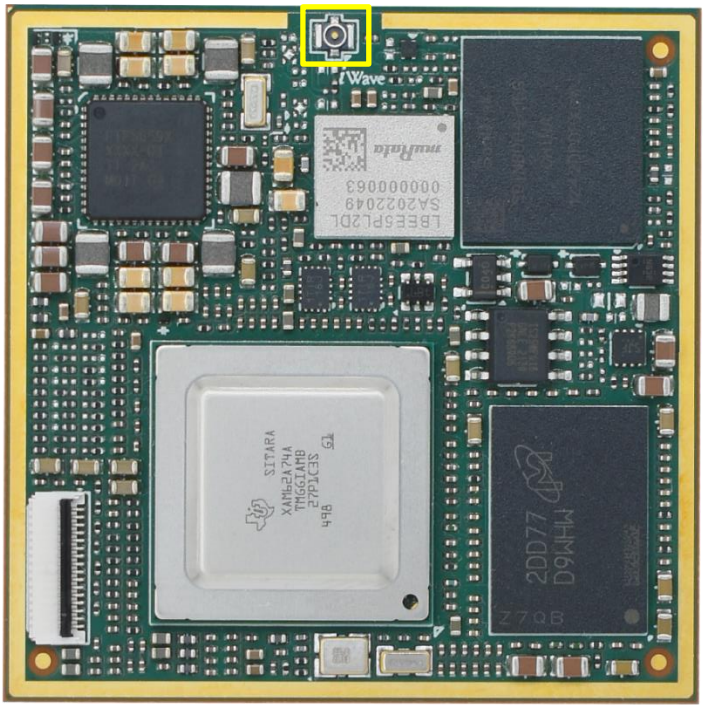

Figure 3: Wi-Fi + Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata.

Antenna Part Number - : 2042811100 from Molex.

2.7 OSM LGA/BGA Balls

OSM LGA/BGA Balls has standard pinout as per OSM Specification V1.1 The interfaces which are available at 662 contacts are explained in the following sections.

OSM LGA/BGA Balls (J3)

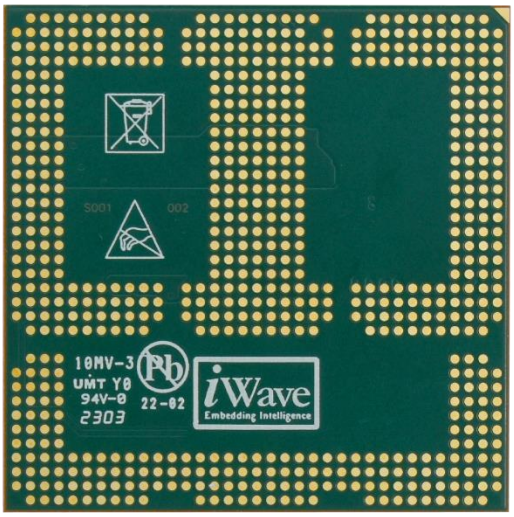

Figure 4: OSM LGA/BGA Balls

Number of contacts - : 662

Table 3: OSM Pinouts

OSM Pins	Signal
SIZE 0	
M18	NC
N18	NC
U19	BOOT_SEL0#
R18	BOOT_SEL1#
AB17	MCAN0_RX
AC17	MCAN0_TX
AB19	MCU_MCAN0_RXD
AC19	MCU_MCAN0_TXD
V17	CARRIER_PWR_ON
A15	GND
A16	OSM_ANT0
A17	GND
A18	GND
A19	GND
A20	NC
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NC
C17	NC
C19	NC
C21	NC
AC18	NC
F15	NC
E16	NC
R15	ENET_RGMII0_RXC
M15	ENET_RGMII0_RX_CTL
L16	NC
N15	ENET_RGMII0_RD2
P15	ENET_RGMII0_RD3
J15	ENET_RGMII0_TXC
K16	ENET_RGMII0_TX_CTL
K15	ENET_RGMII0_RD0
L15	ENET_RGMII0_RD1

OSM Pins	Signal
H15	ENET_RGMII0_TD0
G15	ENET_RGMII0_TD1
H16	ENET_RGMII0_TD2
G16	ENET_RGMII0_TD3
N16	NC
M17	ETH_IOPWR
T16	ENET_MDC
T15	ENET_MDIO
T17	FORCE_RECOV#
F16	GND
J16	GND
J20	GND
E21	GND
E15	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D18	GND
L18	GND
F20	GND
D17	OSM_GPIO_A_0(MCU_GPIO0_12)
E17	OSM_GPIO_A_1(MCU_GPIO0_2)
F17	OSM_GPIO_A_2(MCU_GPIO0_3)
G17	OSM_GPIO_A_3(MCU_GPIO0_4)
H17	OSM_GPIO_A_4(MCU_GPIO0_20)
J17	OSM_GPIO_A_5(MCU_GPIO0_23)
K17	OSM_GPIO_A_6(MCU_GPIO0_1)
L17	NC
D19	OSM_GPIO_B_0(GPIO1_13)
E19	OSM_GPIO_B_1(GPIO1_14)

OSM Pins	Signal
F19	OSM_GPIO_B_2(GPIO1_31)
G19	NC
H19	NC
J19	NC
K19	NC
L19	NC
AA15	I2C3_SCL(UART0_CSTN)
AA16	I2C3_SDA(UART0_RSTN)
AA20	MCU_I2C0_SCL
AA21	MCU_I2C0_SDA
V21	MCASP0_AXR2
W21	MCASP0_AXR3
V19	MCASP0_AXR0
W19	MCASP0_AXR1
W20	MCASP0_ACLKX
W18	MCASP0_AFSX
V18	NC
R19	JTAG_NTRST
P19	NC
N17	JTAG_TCK
P17	JTAG_TDI
R17	JTAG_TDO
N19	JTAG_TMS
E18	PWM_0(EXT_REFCLK1)
F18	PWM_1(SPI0_CS1)
G18	NC
H18	NC
J18	NC
K18	NC
T18	NC
T19	NC
Y13	NC
Y14	NC
AA13	NC
W17	VRTC_3V0
J21	MMC1_CD
F21	MMC1_CLK
E20	MMC1_CMD
G20	MMC1_DATA0
G21	MMC1_DATA1
H20	MMC1_DATA2

OSM Pins	Signal
H21	MMC1_DATA3
C20	SDIO_MMC1
D21	NC
D20	MMC1_WP
T21	NC
K20	NC
K21	NC
L20	NC
L21	NC
M21	NC
N20	NC
N21	NC
P20	NC
P21	NC
R21	NC
T20	NC
U21	NC
U20	NC
W15	QSPI0_D3
W16	QSPI0_D2
Y15	QSPI0_CS1
U16	QSPI0_CLK
U15	QSPI0_D0
V15	QSPI0_D1
AA23	MCU_SPI1_CS0(WKUP_UART0_CTSN)
Y21	MCU_SPI1_CLK(MCU_MCAN1_RX)
Y22	MCU_SPI1_MISO(MCU_UART0_RTSN)
Y23	MCU_SPI1_MOSI(MCU_UART0_CTSN)
U17	SYS_RST#
C18	NC
C14	UART5_CTSN(OSPI0_DQS)
C13	UART5_RTSN(OSPI0_LBCLK)
A14	UART5_RXD(OSPI0_CS2)
B13	UART5_TXD(OSPI0_CS3)
D16	NC
D15	NC
D14	MCU_UART0_RXD
D13	MCU_UART0_TXD
A22	WKUP_UART0_RXD
B23	WKUP_UART0_TXD
D22	UART0_RXD

OSM Pins	Signal
D23	UART0_TXD
C22	UART4_RXD(MMC2_SDCD)
C23	UART4_TXD(MMC2_SDWP)
AB13	USB0_DM
AC14	USB0_DP
AC16	USB0_DRVVBUS
AB14	GPIO_USB_A_ID(GPIO1_18)
AC15	USB_A_OC#
AB16	USB0_VBUS
AB23	USB1_DM
AC22	USB1_DP
AC20	USB1_DRVVBUS
AB22	GPIO_USB_B_ID(GPIO1_19)
AC21	USB_B_OC#
AB20	USB1_VBUS
AB18	NC
AA18	NC
M19	VDD_CORE
Y16	VDD_DDR_1V1
Y20	VCC_1V8
Y19	NC
Y17	VCC_IN_5V
U18	NC
B22	PMIC_ON_OFF
C16	SoC_RESET_OUT
P16	MCU_RESET_OUT
SIZE S	
C2	NC
G3	CAM_PWR(GPIO0_32)
G4	CAM_RST#(GPIO0_35)
B3	MIPI_CSI0_CLK_N
B4	MIPI_CSI0_CLK_P
C1	MIPI_CSI0_DATA0_N
B1	MIPI_CSI0_DATA0_P
A2	MIPI_CSI0_DATA1_N
A3	MIPI_CSI0_DATA1_P
A5	MIPI_CSI0_DATA2_N
A6	MIPI_CSI0_DATA2_P
B6	MIPI_CSI0_DATA3_N
B7	MIPI_CSI0_DATA3_P
AB8	NC

OSM Pins	Signal
AB7	NC
AB11	NC
AB10	NC
AC9	NC
AC8	NC
AC6	NC
AC5	NC
AB5	NC
AB4	NC
AA3	NC
E1	NC
D2	NC
P1	ENET_RGMII1_RXC
L1	ENET_RGMII1_RX_CTL
K2	NC
M1	ENET_RGMII1_RD2
N1	ENET_RGMII1_RD3
H1	ENET_RGMII1_TXC
J2	ENET_RGMII1_TX_CTL
J1	ENET_RGMII1_RD0
K1	ENET_RGMII1_RD1
G1	ENET_RGMII1_TD0
F1	ENET_RGMII1_TD1
G2	ENET_RGMII1_TD2
F2	ENET_RGMII1_TD3
C6	ENET_MDC
C7	ENET_MDIO
M2	NC
B5	GND
D8	GND
P4	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND
A4	GND

OSM Pins	Signal
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
AA4	GND
AA7	GND
R1	GND
D3	NC
D4	NC
E3	NC
E4	NC
F3	DISP_VDD_EN(GPIO0_43)
F4	DISP_BL_EN(GPIO0_44)
C4	I2C1_SCL
C3	I2C1_SDA
AB2	NC
AB1	NC
AC3	NC
AC2	NC
V2	NC
W2	NC
Y1	NC
W1	NC
R2	NC
T1	NC

OSM Pins	Signal
U1	NC
T2	NC
AA9	PMIC_ON_OFF
M4	VOUT0_PCLK
R4	VOUT0_DATA0(RGB_B0)
R3	VOUT0_DATA1(RGB_B1)
P3	VOUT0_DATA2(RGB_B2)
N3	VOUT0_DATA3(RGB_B3)
N4	VOUT0_DATA4(RGB_B4)
M3	VOUT0_DATA5(RGB_B5)
H3	GPIO0_42(GPMC0_CSN1)
J4	VOUT0_DE
K4	GPIO0_41(GPMC0_CSN0)
W4	VOUT0_DATA6(RGB_G0)
V3	VOUT0_DATA7(RGB_G1)
V4	VOUT0_DATA8(RGB_G2)
U3	VOUT0_DATA9(RGB_G3)
T3	VOUT0_DATA10(RGB_G4)
T4	VOUT0_DATA11(RGB_G5)
K3	VOUT0_HSYNC
Y7	VOUT0_DATA12(RGB_R0)
AA6	VOUT0_DATA13(RGB_R1)
Y6	VOUT0_DATA14(RGB_R2)
AA5	VOUT0_DATA15(RGB_R3)
Y5	GPMC0_AD8(RGB_R4)
Y4	GPMC0_AD9(RGB_R5)
J3	SOC_RESET_OUT_3V3
L3	VOUT0_VSYNC
AA2	NC
N2	NC
D11	NC
D10	NC
C10	NC
D9	NC
C8	NC
B11	NC
B10	NC
A9	NC
A8	NC
C9	NC
Y3	VPP_1V8

OSM Pins	Signal
C5	VCC_0V85
Y11	VCC_IN_5V
Y10	VCC_IN_5V
Y9	VCC_IN_5V
Y8	VCC_IN_5V
D6	MCU_RESET_IN
D7	POR_RESET_OUT
SIZE M	
C34	NC
C33	NC
D32	NC
D31	NC
D33	NC
C31	NC
A31	NC
A30	NC
B32	NC
B31	NC
A34	NC
A33	NC
B35	NC
B34	NC
H33	NC
G33	NC
F32	NC
E32	NC
G32	NC
E33	NC
E35	NC
D35	NC
F34	NC
E34	NC
H35	NC
G35	NC
J34	NC
H34	NC
AB35	NC
AC34	NC
W35	NC
T35	NC
U34	NC

OSM Pins	Signal
R35	NC
P35	NC
N35	NC
V34	NC
V35	NC
U35	NC
Y35	NC
AA35	NC
Y34	NC
AA34	NC
R34	NC
N33	NC
P33	NC
A26	GND
J33	GND
AC30	GND
AC33	GND
H32	GND
G34	GND
F35	GND
F33	GND
D34	GND
D28	GND
C35	GND
C32	GND
AC27	GND
AB34	GND
AB31	GND
AB28	GND
AA32	GND
AA28	GND
AA27	GND
AA26	GND
AA25	GND
W34	GND
T34	GND
N34	GND
M35	GND
K34	GND
C25	GND
A29	GND

OSM Pins	Signal
A32	GND
B27	GND
B28	GND
B30	GND
B33	GND
J35	GND
U32	NC
U33	NC
V32	NC
V33	NC
W32	NC
W33	NC
Y32	NC
Y33	NC
M34	NC
L34	NC
L35	NC
K35	NC
L33	NC
K33	NC
J32	NC
K32	NC
L32	NC
M32	NC
M33	NC
N32	NC
P32	NC
P34	NC
R32	NC
R33	NC
T32	NC
T33	NC
AB25	NC
AB26	NC
C30	NC
D29	NC
C29	NC
D30	NC
AC26	NC
AB27	NC
AC32	NC

OSM Pins	Signal
AC31	NC
AB33	NC
AB32	NC
AC29	NC
AC28	NC
AB30	NC
AB29	NC
D26	NC
D25	NC
C26	NC
D27	NC
C28	NC
B26	NC
B25	NC
A28	NC
A27	NC
C27	NC
AA33	VDD_CANUART
B29	CAN_IO_1V8
Y25	VCC_IN_5V
Y28	VCC_IN_5V
Y27	VCC_IN_5V
Y26	VCC_IN_5V
Y29	EMU0
Y30	EMU1
Y31	GPIO0_40(GPMC0_DIR)
AA29	PMIC_GPIO6
AA30	NC
AA31	NC
SIZE L	
AF3	NC
AE3	NC
AP1	NC
AL1	NC
AK2	NC
AM1	NC
AN1	NC
AH1	NC
AJ2	NC
AJ1	NC
AK1	NC

OSM Pins	Signal
AF1	NC
AG1	NC
AG2	NC
AF2	NC
AM2	NC
AR2	NC
AN4	NC
AN10	NC
AR8	NC
AP7	NC
AR9	NC
AR10	NC
AR5	NC
AP6	NC
AP3	NC
AP4	NC
AR6	NC
AR7	NC
AR3	NC
AR4	NC
AP9	NC
AP25	GND
AP28	GND
AP31	GND
AP34	GND
AR14	GND
AP19	GND
AR20	GND
AR26	GND
AR29	GND
AR32	GND
AP22	GND
AP16	GND
AE2	GND
AP13	GND
AP8	GND
AE34	GND
AP5	GND
AP2	GND
AN33	GND
AN21	GND

OSM Pins	Signal
AN18	GND
AR17	GND
AN15	GND
AF35	GND
AG3	GND
AH2	GND
AH34	GND
AJ35	GND
AK3	GND
AL2	GND
AL34	GND
AM13	GND
AM16	GND
AM19	GND
AM22	GND
AN11	GND
AN9	GND
AN6	GND
AN3	GND
AM35	GND
AF32	NC
AF33	NC
AG32	NC
AG33	NC
AH32	NC
AH33	NC
AJ32	NC
AJ33	NC
AN12	NC
AN13	NC
AP17	NC
AP18	NC
AR15	NC
AR16	NC
AP14	NC
AP15	NC
AP11	NC
AP12	NC
AN16	NC
AN17	NC
AM20	NC

OSM Pins	Signal
AM21	NC
AN19	NC
AN20	NC
AM17	NC
AM18	NC
AM14	NC
AM15	NC
AN23	NC
AN22	NC
AM11	NC
AM12	NC
AN14	NC
AP32	NC
AP33	NC
AP35	NC
AN35	NC
AL35	NC
AK35	NC
AH35	NC
AG35	NC
AR33	NC
AR34	NC
AN34	NC
AM34	NC
AK34	NC
AJ34	NC
AG34	NC
AF34	NC
AE33	NC
AR18	NC
AR19	NC
AR21	NC
AR22	NC
AP26	NC
AP27	NC
AP29	NC
AP30	NC
AP20	NC
AP21	NC
AP23	NC
AP24	NC

OSM Pins	Signal
AR27	NC
AR28	NC
AR30	NC
AR31	NC
AN32	NC
AL3	NC
AL4	NC
AM3	NC
AM4	NC
AM5	NC
AM6	NC
AM7	NC
AM8	NC
AM9	NC
AM10	NC
AM23	NC
AM24	NC
AM25	NC
AM26	NC
AM27	NC
AM28	NC
AM29	NC
AM30	NC
AM31	NC
AN2	NC
AN5	NC
AN7	NC
AN8	NC
AN24	NC
AN25	NC
AN26	NC
AN27	NC
AN28	NC
AN29	NC
AN30	NC
AP10	NC
AN31	NC
AE32	NC
AE4	VCC_IN_5V
AF4	VCC_IN_5V
AG4	VCC_IN_5V

OSM Pins	Signal
AH3	VCC_IN_5V
AH4	VCC_IN_5V
AJ3	VCC_IN_5V
AJ4	VCC_IN_5V
AK4	VCC_IN_5V
AK32	SOC_BOOT_MODE14
AK33	SOC_BOOT_MODE15
AL32	SOC_BOOT_MODE13
AL33	SOC_BOOT_MODE12
AM32	SOC_BOOT_MODE1
AM33	SOC_BOOT_MODE0

2.8 Device Main Domain :

This section describes the modules integrated in the device MAIN domain.

2.8.1 RGMII Interface

The AM62Ax OSM LGA Module supports RGMII interface on OSM LGA. AM62Ax provides two Ethernet Interfaces ENET0 and ENET1 with TSN support. The two RGMII lanes are connected to OSM LGA. Connection of the AM62Ax to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on ENET0 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ENET_RGMII0_TD0	RGMII1_TD0/ Y17	O, 1.8V CMOS	Transmit data bit 0 port A
G15	ETH_A_(S)(R)(G)MII_TXD1	ENET_RGMII0_TD1	RGMII1_TD1/ V16	O, 1.8V CMOS	Transmit data bit 1 port A
H16	ETH_A_(S)(R)(G)MII_TXD2	ENET_RGMII0_TD2	RGMII1_TD2/ Y16	O, 1.8V CMOS	Transmit data bit 2 port A
G16	ETH_A_(S)(R)(G)MII_TXD3	ENET_RGMII0_TD3	RGMII1_TD3/ AA17	O, 1.8V CMOS	Transmit data bit 3 port A
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ENET_RGMII0_TX_CTL	RGMII1_TX_CTL/ W16	O, 1.8V CMOS	Transmit enable (Error) port A
J15	ETH_A_(R)(G)MII_TX_CLK	ENET_RGMII0_TXC	RGMII1_TXC/ AB17	I/O, 1.8V CMOS	Transmit clock port A
K15	ETH_A_(S)(R)(G)MII_RXD0	ENET_RGMII0_RD0	RGMII1_RD0/ AB16	I, 1.8V CMOS	Receive data bit 0 (received first) port A
L15	ETH_A_(S)(R)(G)MII_RXD1	ENET_RGMII0_RD1	RGMII1_RD1/ V15	I, 1.8V CMOS	Receive data bit 1 port A
N15	ETH_A_(R)(G)MII_RXD2	ENET_RGMII0_RD2	RGMII1_RD2/ W15	I, 1.8V CMOS	Receive data bit 2 port A
P15	ETH_A_(R)(G)MII_RXD3	ENET_RGMII0_RD3	RGMII1_RD3/ V14	I, 1.8V CMOS	Receive data bit 3 port A
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ENET_RGMII0_RX_CTL	RGMII1_RX_CTL/ AA15	I, 1.8V CMOS	Receive data valid port A
R15	ETH_A_(R)(G)MII_RX_CLK	ENET_RGMII0_RXC	RGMII1_RXC/ AA16	I, 1.8V CMOS	Receive clock port A
T15	ETH_MDIO	ENET_MDIO	MDIO0_MDIO / V13	I/O, 1.8V CMOS	Management data
T16	ETH_MDC	ENET_MDC	MDIO0_MDC / V12	O, 1.8V CMOS	Management data clock

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M17	ETH_IOPWR	-	-	P, 1V8	ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces.

For more details on ENET1 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ENET_RGMII1_TD0	RGMII2_TD0/ AA19	O, 1.8V CMOS	Transmit data bit0 port B
F1	ETH_B_(S)(R)(G)MII_TXD1	ENET_RGMII1_TD1	RGMII2_TD1/ Y18	O, 1.8V CMOS	Transmit data bit1 port B
G2	ETH_B_(S)(R)(G)MII_TXD2	ENET_RGMII1_TD2	RGMII2_TD2/ AA18	O, 1.8V CMOS	Transmit data bit 2 port B
F2	ETH_B_(S)(R)(G)MII_TXD3	ENET_RGMII1_TD3	RGMII2_TD3/ W17	O, 1.8V CMOS	Transmit data bit 3 port B
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ENET_RGMII1_TX_CTL	RGMII2_TX_CTL/ Y19	O, 1.8V CMOS	Transmit enable (Error) port B
H1	ETH_B_(R)(G)MII_TX_CLK	ENET_RGMII1_TXC	RGMII2_TXC / AB19	I/O, 1.8V CMOS	Transmit clock port B
J1	ETH_B_(S)(R)(G)MII_RXD0	ENET_RGMII1_RD0	RGMII2_RD0/ AA21	I, 1.8V CMOS	Receive data bit 0 port B
K1	ETH_B_(S)(R)(G)MII_RXD1	ENET_RGMII1_RD1	RGMII2_RD1/ Y20	I, 1.8V CMOS	Receive data bit1 port B
M1	ETH_B_(R)(G)MII_RXD2	ENET_RGMII1_RD2	RGMII2_RD2/ AB21	I, 1.8V CMOS	Receive data bit 2 port B
N1	ETH_B_(R)(G)MII_RXD3	ENET_RGMII1_RD3	RGMII2_RD3/ AB20	I, 1.8V CMOS	Receive data bit 3 port B
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ENET_RGMII1_RX_CTL	RGMII2_RX_CTL/ W18	I, 1.8V CMOS	Receive clock port B
P1	ETH_B_(R)(G)MII_RX_CLK	ENET_RGMII1_RXC	RGMII2_RXC/ AA20	I, 1.8V CMOS	Receive clock port B
C7	ETH_B_MDIO	ENET_MDIO	MDIO0_MDIO / V13	I/O, 1.8V CMOS	Management data IO for Port B
C6	ETH_B_MDC	ENET_MDC	MDIO0_MDC / V12	O, 1.8V CMOS	Management data clock for Port B

2.8.2 USB 2.0 Interface

The AM62Ax OSM LGA Module supports two USB2.0 interface.

AM62Ax SoC's USB controller supports two independent instances of USB subsystem to support this operation. It supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps). Either of which can be independently configured to act as a USB Host or a USB Device.

Device. For more details on USB 2.0 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB13	USB_A_D_N	USB0_DM	USB0_DM/ AA10	IO, USB	USB 2.0 Port0 Data Negative.
AC14	USB_A_D_P	USB0_DP	USB0_DP/ AA9	IO, USB	USB 2.0 Port0 Data Positive.
AB14	USB_A_ID	GPIO_USB_A_ID(GPIO1_18)	SPI0_D0/ B15	I, 1.8V CMOS/ 10K PU	USB 2.0 Port0 ID.
AC15	USB_A_OC#	NC	NA	NC/ 1.8V 10K PU	USB 2.0 Port0 Over Current Indicator.
AB16	USB_A_VBUS	USB0_VBUS	NA	I, 5V Power	USB 2.0 Port0 OTG VBUS Power for detection.
AC16	USB_A_EN	USB0_DRVVBUS	USB0_DRVVBUS /C20	0, 1.8V CMOS	USB 2.0 Port0 Power Enable.
AB23	USB_B_D_N	USB1_DM	USB1_DM/ Y11	IO, USB	USB 2.0 Port1 Data Negative.
AC22	USB_B_D_P	USB1_DP	USB1_DP/ Y10	IO, USB	USB 2.0 Port1 Data Positive.
AB22	USB_B_ID	GPIO_USB_B_ID(GPIO1_19)	SPI0_D1/ E15	I, 1.8V CMOS/ 10K PU	USB 2.0 Port1 ID.
AC21	USB_B_OC#	USB_A_OC#	NA	NC/1.8V 10K PU	USB 2.0 Port1 Over Current Indicator.
AB30	USB_A_VBUS	USB1_VBUS	NA	I, 5V Power	USB 2.0 Port1 OTG VBUS Power for detection.
AC20	USB_B_EN	USB1_DRVVBUS	USB1_DRVVBUS /D19	0, 1.8V CMOS	USB 2.0 Port1 Power Enable.

2.8.3 MIPI CSI Interface

The AM62Ax SoC supports one 4-lane camera interfaces, the CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification v1.3 and implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The CSI-2 Rx Controller module supports up to 16 virtual channels per input (partial MIPI CSI v2.0 feature). The Programmable formats including YUV420, YUV422, RGB, Raw, and User Defined (over 25 different formats supported). The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus. The AM62Ax SoC also supports ISP for providing aggregate performance and HDR processing. The AM62Ax OSM LGA Module supports 4 lane MIPI CSI camera interface via OSM BGA along with the other controlling signals. For more details on MIPI CSI OSM pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C1	CSI_DATA0_N	MIPI_CSI0_DATA0_N	CSI0_RXN0 / W12	I, MIPI	MIPI CSI differential data lane 0 negative.
B1	CSI_DATA0_P	MIPI_CSI0_DATA0_P	CSI0_RXP0 / W13	I, MIPI	MIPI CSI differential data lane 0 positive.
A2	CSI_DATA1_N	MIPI_CSI0_DATA1_N	CSI0_RXN1 / Y13	I, MIPI	MIPI CSI differential data lane 1 negative.
A3	CSI_DATA1_P	MIPI_CSI0_DATA1_P	CSI0_RXP1 / Y14	I, MIPI	MIPI CSI differential data lane 1 positive.
A5	CSI_DATA2_N	MIPI_CSI0_DATA2_N	CSI0_RXN2 / AA13	I, MIPI	MIPI CSI differential data lane 2negative.
A6	CSI_DATA2_P	MIPI_CSI0_DATA2_P	CSI0_RXP2 / AA12	I, MIPI	MIPI CSI differential data lane 2 positive.
B6	CSI_DATA3_N	MIPI_CSI0_DATA3_N	CSI0_RXN3 / AB11	I, MIPI	MIPI CSI differential data lane 3 negative.
B7	CSI_DATA3_P	MIPI_CSI0_DATA3_P	CSI0_RXP3 / AB10	I, MIPI	MIPI CSI differential data lane 3 positive.
B3	CSI_CLOCK_N	MIPI_CSI0_CLK_N	CSI0_RXCLKN/ AB14	I, MIPI	MIPI CSI differential Clock negative.
B4	CSI_CLOCK_P	MIPI_CSI0_CLK_P	CSI0_RXCLKP/ AB13	I, MIPI	MIPI CSI differential Clock positive.
C3	I2C_CAM_SDA / CSI_TX_N	I2C1_SDA	I2C1_SDA/ E17	IO, 1.8V CMOS/4.7K PU	MIPI CSI I2C Data.
C4	I2C_CAM_SCL / CSI_TX_P	I2C1_SCL	I2C1_SCL/ C17	IO, 1.8V CMOS/4.7K PU	MIPI CSI I2C Clock.
G3	CAM_PWR / GPIO_C_6	GPIO_CAM_PWR(GPIO0_32)	GPMC0_ADVN_ALE/ L18	O, 1.8V CMOS	MIPI CSI Camera power enable.
G4	CAM_RST# / GPIO_C_7	GPIO_CAM_RST#(GPIO0_35)	GPMC0_BE0N_CLE/ L19	O, 1.8V CMOS	MIPI CSI Camera Reset.

2.8.4 SDIO(4bit) Interface

The AM62Ax SoC OSM SOM supports one SD interface port on OSM Edge. AM62Ax SoC MMC1 controller is used for SD interface. It supports 1-bit or 4-bit transfer mode for SD memory/SDIO and works up to SDR104 class transfer rate at max. 108 Mbytes/s @ 208 MHz. AM62Ax SoC supports SDIO card detect function & write protect function and connected from OSM Edge.

The AM62Ax SoC OSM SOM supports configurable IO voltage levels for MMC1 lines which can be controlled through SoC GPIO1_15. If GPIO1_15 is set to low, then 1.8V IO level is selected for MMC1 lines. If GPIO1_15 is set to high, then 3.3V IO level is selected for MMC1 lines.

For more details on SDIO interface pinouts on OSM Edge connector, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
F21	SDIO_A_CLK	MMC1_CLK	MMC1_CLK/ E22	O, 1.8V/3.3V CMOS/ 49.9K PD	SDIO_A Clock
E20	SDIO_A_CMD	MMC1_CMD	MMC1_CMD/ C21	IO, 1.8V/3.3V CMOS	SDIO_A Command.
G20	SDIO_A_D0	MMC1_DATA0	MMC1_DATA0/ B22	IO, 1.8V/3.3V CMOS	SDIO_A Data0.
G21	SDIO_A_D1	MMC1_DATA1	MMC1_DATA1/ D21	IO, 1.8V/3.3V CMOS	SDIO_A Data1.
H20	SDIO_A_D2	MMC1_DATA2	MMC1_DATA2/ C22	IO, 1.8V/3.3V CMOS	SDIO_A Data2.
H21	SDIO_A_D3	MMC1_DATA3	MMC1_DATA3/ D22	IO, 1.8V/3.3V CMOS	SDIO_A Data2.
J21	SDIO_A_CD#	MMC1_CD	MMC1_CD/ D18	I, 1.8V/3.3V OD CMOS	SDIO_A Card detect.
D20	SDIO_A_WP	MMC1_WP	MMC1_WP/ E18	I, 1.8V/3.3V OD CMOS	SDIO_A Card Write protect.
C20	SDIO_A_IOPWR	SDIO_MMC1	NA	O, Power	SDIO_A Voltage. It is used to provide the IO Voltage Level

2.8.5 Audio Interface

The AM62Ax OSM LGA Module supports I2S_A & B of OSM Edge connector from SoC's McASP(Multichannel Audio Serial Port) channel. The McASP module can operate in both transmit and receive modes and McASP peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, S/SPDIF, TDM and other similar bit-stream format. The McASP module has Independent serializer for each AXRx channel and Out up-sampled data at 96 kHz or 192 kHz. The McASP general features are including transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits. Only Transmitter Clock and Transmitter Left-Right Clock (LRCK) is supported as per OSM specification.

In AM62Ax OSM LGA Module the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio interface pinouts on OSM Edge connector, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
W21	I2S_A_DATA_OUT	MCASP0_AXR3	MCASP0_AXR3/ C19	O, 1.8V CMOS	Serial Audio Interface Channel A Data Output
V21	I2S_A_DATA_IN	MCASP0_AXR2	MCASP0_AXR2/ B19	I, 1.8V CMOS	Serial Audio Interface Channel A Data Input
W20	I2S_BITCLK	MCASP0_ACLKX	MCASP0_ACLKX /A19	O, 1.8V CMOS	Serial Audio Interface Channel Bit Clock
W18	I2S_LRCLK	MCASP0_AFSX	MCASP0_AFSX/ A20	O, 1.8V CMOS	Serial Audio Interface Channel Left/Right Clock
W19	I2S_B_DATA_OUT	MCASP0_AXR1	MCASP0_AXR1/ B18	O, 1.8V CMOS	Serial Audio Interface Channel B Data Output
V19	I2S_B_DATA_IN	MCASP0_AXR0	MCASP0_AXR0/ B20	I, 1.8V CMOS	Serial Audio Interface Channel B Data Input

2.8.6 QSPI Interface

The AM62Ax OSM LGA Module supports SPI_A of OSM Edge connector from SoC's QSPI Module with Chip select 1, Chip select 0 of the same QSPI is connected to on SOM QSPI Flash and this QSPI can also configure as SPI. This QSPI/SPI supports boot media option. The QSPI Features Memory mapped 'direct' mode of operation for performing flash data transfers and executing code from flash memory and Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.

For more details on QSPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y15	SPI_A_CS#	QSPI0_CS1	OSPI0_CSN1/ G19	O, 1.8V CMOS	QSPI0 Chip Select 0
U16	SPI_A_SCK	QSPI0_CLK	OSPI0_CLK/ L22	O, 1.8V CMOS	QSPI0 Clock
U15	SPI_A_SDI_(IO0)	QSPI0_D0	OSPI0_D0/ J21	IO, 1.8V CMOS	QSPI0 Data0
V15	SPI_A_SDO_(IO1)	QSPI0_D1	OSPI0_D1/ J18	IO, 1.8V CMOS	QSPI0 Data1
W16	SPI_A_/WP_(IO2)	QSPI0_D2	OSPI0_D2/ J19	IO, 1.8V CMOS	QSPI0 Data2
W15	SPI_A_/HOLD_(IO 3)	QSPI0_D3	OSPI0_D3/ H18	IO, 1.8V CMOS	QSPI0 Data3

2.8.7 Data UART

The AM62Ax OSM supports three UART channels where one channels UART_A is with CTS and RTS and two channels UART_D is without and a console UART port. UART5 and UART4 from AM62Ax SoC is connected to UART_A and UART_D channels of OSM LGA respectively. UART0 is connected to UART Console port of OSM.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	UART5_RXD (OSPI0_CS2)	OSPI0_CSn2/ K20	I, 1.8V CMOS	UART2 Receiver.
B13	UART_A_TX	UART5_TXD (OSPI0_CS3)	OSPI0_CSN3/ G20	O, 1.8V CMOS	UART2 Transmitter.
C13	UART_A_RTS	UART5_RTSn(OSPI0_LBCLK)	OSPI0_LBCLKO/ K22	O, 1.8V CMOS	UART2 Clear to Send.
C14	UART_A_CTS	UART5_CTSn(OSPI0_DQS)	OSPI0_DQS/ L21	I, 1.8V CMOS	UART2 Request to Send.
C22	UART_D_RX	UART4_RXD (MMC2_SDCD)	MMC2_SDCD / F22	I, 1.8V CMOS	UART3 Transmitter.
C23	UART_D_TX	UART4_TXD (MMC2_SDWP)	MMC2_SDWP / E21	O, 1.8V CMOS	UART3 Receiver.
D22	UART_CON_RX	UART0_RXD	UART0_RXD / E14	I, 1.8V CMOS	Debug UART Transmitter. *Optionally connected to on SOM programming header.*
D23	UART_CON_TX	UART0_TXD	UART0_TXD / D15	O, 1.8V CMOS	Debug UART Receiver. *Note: Optionally connected to on SOM programming header.*

2.8.8 MCAN Interface

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the ISO 11898-1:2015 standard and CAN 2.0 Part A, B protocol specifications. The AM62Ax SoC Supports one CAN from main domain which supporting both classic CAN and CAN FD (CAN with Flexible Data-Rate) specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The CAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the CAN module.

For more details of main domain CAN pinouts on OSM Edge connector, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	MCAN0_TX	MCAN0_TX/ B17	O, 1.8V CMOS	CAN 1 Transmitter.
AB17	CAN_A_RX	MCAN0_RX	MCAN0_RX/ C18	I, 1.8V CMOS	CAN 1 Receiver.

2.8.9 I2C Interface

The AM62Ax SoC OSM supports two I2C from main domain, AM62Ax SoC main domain I2C features compliance with the Philips I2C-bus specification version 2.1, Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps) and 7-bit and 10-bit device addressing modes.

For more details of I2C pinouts on OSM Edge connector, refer below table:

OSM Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	I2C3_SCL(UART0_CSTN)	UART0_CTSN/ F14	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Clock.
AA16	I2C_A_SDA	I2C3_SDA(UART0_RSTN)	UART0_RTSN/ C15	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Data.
C3	I2C_CAM_SDA / CSI_TX_N	I2C1_SDA	I2C1_SDA/ E17	IO, 1.8V CMOS/4.7K PU	MIPI CSI I2C Data.
C4	I2C_CAM_SCL / CSI_TX_P	I2C1_SCL	I2C1_SCL/ C17	IO, 1.8V CMOS/4.7K PU	MIPI CSI I2C Clock.

2.8.10 RGB Interface

The AM62Ax SoC OSM SOM supports 8-bit, 16-bit, 18-bit parallel display.

For more details of RGB pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y7	RGB_R0	VOUT0_DATA12(RGB_R0)	VOUT0_DATA12/ W20	O, 3.3V CMOS	Red data bit 0
AA6	RGB_R1	VOUT0_DATA13(RGB_R1)	VOUT0_DATA13/ W19	O, 3.3V CMOS	Red data bit 1
Y6	RGB_R2	VOUT0_DATA14(RGB_R2)	VOUT0_DATA14/ Y21	O, 3.3V CMOS	Red data bit 2
AA5	RGB_R3	VOUT0_DATA15(RGB_R3)	VOUT0_DATA15/ Y22	O, 3.3V CMOS	Red data bit 3
Y5	RGB_R4	GPMC0_AD8(RGB_R4)	GPMC0_AD8/ P22	O, 3.3V CMOS	Red data bit 4
Y4	RGB_R5	GPMC0_AD9(RGB_R5)	GPMC0_AD9/ R19	O, 3.3V CMOS	Red data bit 5
W4	RGB_G0	VOUT0_DATA6(RGB_G0)	VOUT0_DATA6/ V22	O, 3.3V CMOS	Green data bit 0
V3	RGB_G1	VOUT0_DATA7(RGB_G1)	VOUT0_DATA7/ V21	O, 3.3V CMOS	Green data bit 1
V4	RGB_G2	VOUT0_DATA8(RGB_G2)	VOUT0_DATA8/ V19	O, 3.3V CMOS	Green data bit 2
U3	RGB_G3	VOUT0_DATA9(RGB_G3)	VOUT0_DATA9/ V18	O, 3.3V CMOS	Green data bit 3
T3	RGB_G4	VOUT0_DATA10(RGB_G4)	VOUT0_DATA10/ W22	O, 3.3V CMOS	Green data bit 4
T4	RGB_G5	VOUT0_DATA11(RGB_G5)	VOUT0_DATA11/ W21	O, 3.3V CMOS	Green data bit 5
R4	RGB_B0	VOUT0_DATA0(RGB_B0)	VOUT0_DATA0	O, 3.3V CMOS	Blue data bit 0
R3	RGB_B1	VOUT0_DATA1(RGB_B1)	VOUT0_DATA1/ U21	O, 3.3V CMOS	Blue data bit 1
P3	RGB_B2	VOUT0_DATA2(RGB_B2)	VOUT0_DATA2/ U20	O, 3.3V CMOS	Blue data bit 2
N3	RGB_B3	VOUT0_DATA3(RGB_B3)	VOUT0_DATA3/ U19	O, 3.3V CMOS	Blue data bit 3
N4	RGB_B4	VOUT0_DATA4(RGB_B4)	VOUT0_DATA4/ T19	O, 3.3V CMOS	Blue data bit 4
M3	RGB_B5	VOUT0_DATA5(RGB_B5)	VOUT0_DATA5/ U18	O, 3.3V CMOS	Blue data bit 5
M4	RGB_(PIXEL)CLK	VOUT0_PCLK	VOUT0_PCLK/ AA22	O, 3.3V CMOS	Pixel clock signal
L3	RGB_VSYNC	VOUT0_VSYNC	VOUT0_VSYNC/ V17	O, 3.3V CMOS	Vertical synch
K3	RGB_HSYNC	VOUT0_HSYNC	VOUT0_HSYNC/ T18	O, 3.3V CMOS	Horizontal synch

J3	RGB_RESET#	SoC_RESET_OUT_3V3	RESETSTATZ/ F19	O, 3.3V CMOS	Global Reset
J4	RGB_DE	VOUT0_DE	VOUT0_DE/ U17	O, 3.3V CMOS	Data Enable
K4	RGB_DISP	GPIO0_41(GPMC0_CSn0)	GPMC0_CSN0/ M19	O, 3.3V	Display ON/OFF
H3	RGB_CS#	GPIO0_42(GPMC0_CSn1)	GPMC0_CSN1/ M21	O, 3.3V	Chip select
F3	GPIO_C_4 / DISP_VDD_EN	DISP_VDD_EN(GPIO0_4 3)	GPMC0_CSN2/ M22	O, 1.8V	Display power enable, active high
F4	GPIO_C_5 / DISP_BL_EN	DISP_BL_EN(GPIO0_44)	GPMC0_CSN3/ M20	O, 1.8V	Display backlight enable, active high
E18	DISP_BL_PWM / PWM_0	PWM_0(EXT_REFCLK1)	EXT_REFCLK1/ B16	O, 1.8V	Brightness control through pulse width modulation

2.8.11 OSM GPIOs

The AM62Ax OSM supports GPIOs on OSM LGA as per OSM V1.1. AM62Ax SoC's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. AM62Ax OSM V1.1 supports 3 GPIOs from main domain & 8 GPIOs from MCU domain, which can be used for any general-purpose application and are listed below.

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D19	GPIO_B_0	OSM_GPIO_B_0(GPIO1_13)	MCASP0_AFSR/ B21	IO, 1.8V CMOS	OSM General Purpose Input/output B0.
E19	GPIO_B_1	OSM_GPIO_B_1(GPIO1_14)	MCASP0_ACLKR/ A21	IO, 1.8V CMOS	OSM General Purpose Input/output B1.
F19	GPIO_B_2	OSM_GPIO_B_2(GPIO1_31)	EXTINTn/ F17	IO, 1.8V CMOS	OSM General Purpose Input/output B2.

2.8.12 Control Signals

OSM V1.1 specification supports control Signals, for more details on OSM Control Signals pinouts on OSM Edge connector, refer below table:

OSM Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U17	SYS_RST#	SYS_RST#	RESET_REQZ/ E19	I, 1.8V CMOS 10K PU	Main domain (SoC) Hard RESET Input to SOM.
AA9	PWR_BTN#	PMIC_ON_OFF	NA	I, 5V CMOS 10K PU	Power ON /OFF Input to SOM.
V17	CARRIER_PWR_EN	CARRIER_PWR_ON	NA	O, 1.8V CMOS 10K PU	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.

2.8.13 Boot Select

The AM62Ax OSM LGA Module supports one Boot Select pins as per OSM V1.1 specification. AM62Ax OSM LGA Module supports booting from On-SOM QSPI, eMMC and OSM SD, USB (from carrier board). Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

Also, AM62Ax OSM LGA Module supports active low FORCE_RECOV# functionality pin in OSM LGA. By pulling low on this pin puts AM62Ax SoC in serial download mode where the SoC boot media can be programmed through AM62Ax SoC's USB0 controller USB 2.0 interface which is connected to USB_A port of OSM LGA.

OSM Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	**BOOT_MODE (1:0)** **00** - On SOM QSPI Boot **11** - On SOM eMMC boot **10** - USB boot
R18	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS 10K PU	
T17	FORCE_RECOVERY#	FORCE_RECOVERY#	NA	I, 1.8V CMOS 10K PU	If low on carrier board module enters recovery mode. *Note: In recovery mode media selection switch should be in USB mode.* **BOOT_MODE (1:0)** **10** - USB Mode **FORCE_RECOVERY#** **0** - USB DFU Mode 1 - USB Boot mode

2.8.14 Miscellaneous Pins

For more details of miscellaneous pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
B22	VENDOR DEFINED1	PMIC_ON_OFF	NA	I, 5V CMOS 10K PU	Power ON /OFF Input to SOM.
C16	VENDOR DEFINED2	SoC_RESET_OUT	RESETSTATZ/ F19	O, 1.8V CMOS 10K PD	Main domain Hard RESET Out to Carrier.
P16	VENDOR DEFINED3	MCU_RESET_OUT	MCU_RESETSTATZ/ D14	O, 1.8V CMOS 10K PD	MCU domain (SoC) Hard RESET Out to Carrier.
D6	VENDOR DEFINED6	MCU_RESET_IN	MCU_RESETZ/ C12	I, 1.8V CMOS 10K PU	MCU domain Hard RESET Input to SOM.
D7	VENDOR DEFINED7	POR_RESET_OUT	PORZ_OUT/ F18	O, 1.8V CMOS 10K PD	POWER ON RESET Out to Carrier
Y29	VENDOR DEFINED8	EMU0	EMU0/ C13	IO, 1.8V CMOS 10K PU	Emulation Control 0
Y30	VENDOR DEFINED9	EMU1	EMU1/ E10	IO, 1.8V CMOS 10K PU	Emulation Control 1
Y31	VENDOR DEFINED10	GPIO0_40(GPMC 0_DIR)	GPMC0_DIR/ K18	IO, 3.3V CMOS	GPIO0_40
AA29	VENDOR DEFINED11	PMIC_GPIO6	NA	IO, 1.8V CMOS	PMIC GPIO6
A16	COM_AREA_02	OSM_ANT0	-	-	Main Antenna *Optinally connected to Wi-Fi Bluetooth antenna*

2.8.15 Power and GND

The AM62Ax OSM LGA Module works with 5V power input (VCC) from OSM LGA and generates all other required powers internally On-SOM itself. AM62Ax OSM LGA Module also supports coin cell power input (VDD_RTC) from OSM LGA to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on OSM LGA, refer the below table.

OSM Pin No.	OSM Edge Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y8,Y9,Y10,Y11,Y17 Y25,Y26,Y27,Y28 AE4,AF4,AG4,AH3,AH4, AJ3,AJ4,AK4	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Supply Voltage.
M19	VCC_2_TEST	VDD_CORE	NA	0.75V POWER	Module power voltage test point
Y16	VCC_3_TEST	VDD_DDR_1V1	NA	1.1V POWER	Module power voltage test point
Y20	VCC_4_TEST	VCC_1V8	NA	1.8V POWER	Module power voltage test point
Y3	VCC_5_TEST	VPP_1V8	NA	1.8V POWER	Module power voltage test point
C5	VCC_6_TEST	VCC_0V85	NA	0.85V POWER	Module power voltage test point
AA33	VCC_7_TEST	VDD_CANUART	NA	0.85V POWER	Module power voltage test point
B29	VCC_8_TEST	CAN_IO_1V8	NA	I,1V8 POWER	Module power voltage test point
A4,A7,A10,B2,B5,B8,B9, C11,D1,D5,D8,E2,H2,H4 ,L2,L4,P2,P4,R1,U2,U4, V1,W3,Y2,AA1,AA4,AA 7,AA8,AA10,AA11,AB3, AB6,AB9,AC4,AC7,AC10 ,A26,A29,A32,B27,B28, B30,B33,C25,C32,C35,D 28,D34,F33,F35,G34,H3 2,J33,J35,K34,M35,N34, T34,W34,AA25,AA26,A A27,AA28,AA32,AB28,A B31,AB34,AC27,AC30,A C33,AE2,AE34,AF35,AG 3,AH2,AH34,AJ35,AK3, AL2,AL34,AM13,AM16, AM19,AM22,AM35,AN 3,AN6,AN9,AN11,AN15, AN18,AN21,AN33,AP2, AP25,AP28,AP31,AP34, AR14,AR17,AR20,AR26,	GND	GND	NA	Power	Ground.

OSM Pin No.	OSM Edge Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AR29,AR32					
W17	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.9 Device MCU Domain :

This section describes the modules integrated in the device MCU domain.

2.9.1 SPI Interface

The AM62Ax OSM LGA Module supports SPI_B of OSM Edge connector from MCU SPI1 Module with Chip select 0, Chip select 1 of the same SPI is connected to on SOM Low-rate wireless area network module (EEE802.15.4) and OSM L17 Pin optionally.

For more details on SPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA23	SPI_B_CS0#	MCU_SPI1_CS0(WKUP_UART0_CTSn)	WKUP_UART0_CTSN/C10	O, 1.8V CMOS	SPI_B Chip Select 0
Y21	SPI_B_SCK	MCU_SPI1_CLK(MCU_MCAN1_RX)	MCU_SPI1_CLK(MCU_MCAN1_RX)/B9	O, 1.8V CMOS/0E	SPI_B Clock
Y22	SPI_B_SDI	MCU_SPI1_MISO(MCU_UART0_RTSn)	MCU_UART0_RTSN/D10	I, 1.8V CMOS	SPI_B Master IN Slave Out
Y23	SPI_B_SDO	MCU_SPI1_MOSI(MCU_UART0_CTSn)	MCU_UART0_CTSN/B11	O, 1.8V CMOS	SPI_B Master Out Slave In
L17	GPIO_A_7 / SPI_B_CS1#	NC	NC	O, 1.8V CMOS	NC. *Note : Optionally SPI_B Chip Select 1 supported*

2.9.2 Data UART

The AM62Ax OSM supports one Data UART channels where one channels UART_B is without CTS and RTS. UART0 from AM62Ax MCU domain is connected to UART_B channels of OSM LGA respectively.

For more details on MCU Data UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D14	UART_B_RX	MCU_UART0_RXD	MCU_UART0_RXD/D8	I, 1.8V CMOS	UART_B Receiver.
D13	UART_B_TX	MCU_UART0_TXD	MCU_UART0_TXD/F8	O, 1.8V CMOS	UART_B Transmitter.

2.9.3 Wakeup UART

The AM62Ax OSM supports one Wakeup UART channels where one channels UART_C is without CTS and RTS. Wakeup UART0 from AM62Ax MCU domain is connected to UART_C channels of OSM LGA respectively.

For more details on MCU Wakeup UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A22	UART_C_RX	WKUP_UART0_RXD	WKUP_UART0_RXD/C9	I, 1.8V CMOS	UART_B Receiver.
B23	UART_C_TX	WKUP_UART0_TXD	WKUP_UART0_TXD/E9	O, 1.8V CMOS	UART_B Transmitter.

2.9.4 CAN Interface

The AM62Ax SoC Supports one CAN from MCU domain which supporting both classic CAN and CAN FD (CAN with Flexible Data-Rate) specification.

For more details of main domain CAN pinouts on OSM Edge connector, refer below table:

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC19	CAN_B_TX	MCU_MCAN0_TXD	MCU_MCAN0_TXD/ C7	O, 1.8V CMOS	CAN_B Transmitter.
AB19	CAN_B_RX	MCU_MCAN0_RXD	MCU_MCAN0_RXD/ E8	I, 1.8V CMOS	CAN_B Receiver.

2.9.5 I2C Interface

The AM62Ax SoC OSM supports one I2C from MCU domain, AM62Ax SoC MCU domain I2C features compliance with the Philips I2C-bus specification version 2.1, Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps) and 7-bit and 10-bit device addressing modes and the same I2C is connected PMIC for support watch dog functionality.

For more details of I2C pinouts on OSM Edge connector, refer below table:

OSM Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA20	I2C_B_SCL	MCU_I2C0_SCL	MCU_I2C0_SCL/ E12	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Clock.
AA21	I2C_B_SDA	MCU_I2C0_SDA	MCU_I2C0_SDA/ D9	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Data.

2.9.6 OSM GPIOs

The AM62Ax OSM supports GPIOs on OSM LGA as per OSM V1.1. AM62Ax SoC's MCU GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. AM62Ax OSM V1.1 supports 8 GPIOs from MCU domain, which can be used for any general-purpose application and are listed below.

Pin No.	OSM Pin Name	OSM Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	OSM_GPIO_A_0(MCU_GPIO0_12)	WKUP_UART0_RTSN/ C8	IO, 1.8V CMOS	OSM General Purpose Input/output A0.
E17	GPIO_A_1	OSM_GPIO_A_1(MCU_GPIO0_2)	MCU_SPI0_CLK/ B13	IO, 1.8V CMOS	OSM General Purpose Input/output A1.
F17	GPIO_A_2	OSM_GPIO_A_2(MCU_GPIO0_3)	MCU_SPI0_D0/ A15	IO, 1.8V CMOS	OSM General Purpose Input/output A2.
G17	GPIO_A_3	OSM_GPIO_A_3(MCU_GPIO0_4)	MCU_SPI0_D1/ B12	IO, 1.8V CMOS	OSM General Purpose Input/output A3.
H17	GPIO_A_4	OSM_GPIO_A_4(MCU_GPIO0_20)	WKUP_I2C0_SDA/ E13	IO, 1.8V CMOS	OSM General Purpose Input/output A4.
J17	GPIO_A_5	OSM_GPIO_A_5(MCU_GPIO0_23)	WKUP_CLKOUT0/ B10	IO, 1.8V CMOS	OSM General Purpose Input/output A5.
K17	GPIO_A_6 / SPI_A_CS1#	OSM_GPIO_A_6(MCU_GPIO0_1)	MCU_SPI0_CS1/ C11	IO, 1.8V CMOS	OSM General Purpose Input/output A6.
L17	GPIO_A_7 / SPI_B_CS1#	NC	NA	IO, 1.8V CMOS	NC. *Optionally connected to L17 and also to SOM low rate Wifi SPI interface.*

2.9.7 JTAG

The AM62Ax OSM supports JTAG interface for SoC debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security.

For more details on JTAG pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM LGA Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	JTAG_TCK	TCK/ A14	I, 1V8 CMOS 10K PU	JTAG test Clock.
N19	JTAG_TMS(SWDIO)	JTAG_TMS	TMS/ B14	I, 1V8 CMOS 10K PU	JTAG test mode select.
P17	JTAG_TDI	JTAG_TDI	TDI/ A16	I, 1V8 CMOS 10K PU	JTAG test data input.
R17	JTAG_TDO(SWO)	JTAG_TDO	JTAG_TDO/ C14	O, CMOS 1V8	JTAG test data output.
R19	JTAG_NTRST	JTAG_TRSTN	TRSTN/ F15	I, 1V8 CMOS 10K PD	JTAG test RESET output.

2.10 Other Features

2.10.1 Programming Header

The AM62Ax OSM LGA Module supports 16 pin programming header for testing the on-module features. The programming header is used for Flashing the board and has DATA UART for getting the boot prints.

Number of Pins - 16

Connector Part - 503480-1600 from Molex

Table 4: Programming header Pin assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_IN_5V	NA	Power	Supply voltage
2	VCC_IN_5V	NA	Power	Supply voltage
3	VCC_IN_5V	NA	Power	Supply voltage
4	VCC_IN_5V	NA	Power	Supply voltage
5	VCC_IN_5V	NA	Power	Supply voltage
6	GND	NA	Power	Ground
7	USB0_DM	USB0_DM/AA10	IO, USB	USB 2.0 OTG High Speed Data Positive.
8	USB0_DP	USB0_DP/AA9	IO, USB	USB 2.0 OTG High Speed Data Negative
9	GND	NA	Power	Ground
10	USB0_VBUS	USB0_VBUS /V8	I, Power	USB 2.0 OTG VBUS power for detection.
11	GND	NA	Power	Ground
12	UART0_RXD	UART0_RXD/E14	O, 1.8V CMOS	Debug UART Transmitter.
13	UART0_TXD	UART0_TXD/D15	I, 1.8V CMOS	Debug UART Receiver.
14	GND	NA	Power	Ground
15	GND	NA	Power	Ground
16	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	If low on carrier board module enters recovery mode.

2.11 AM62Ax Pin Multiplexing on OSM BGA

The AM62Ax SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the AM62Ax SoC's IO pins can be configured as GPIO if required. The below table provides the details of AM62Ax SoC pin connections to the OSM edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring TI's AM62Ax Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the OSM SOM Edge connector for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

Table 5: AM62Ax SoC IOMUX for OSM Edge Connector interfaces

Interface/ Function	OSM Edge Pin Number	AM62Ax SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Default
MIPI CSI0	B3	AB14	CSI0_RXCLKN											CSI0_RXCLKN
	B4	AB13	CSI0_RXCLKP											CSI0_RXCLKP
	C1	W12	CSI0_RXN0											CSI0_RXN0
	B1	W13	CSI0_RXP0											CSI0_RXP0
	A2	Y13	CSI0_RXN1											CSI0_RXN1
	A3	Y14	CSI0_RXP1											CSI0_RXP1
	A5	AA13	CSI0_RXN2											CSI0_RXN2
	A6	AA12	CSI0_RXP2											CSI0_RXP2
	B6	AB11	CSI0_RXN3											CSI0_RXN3
	B7	AB10	CSI0_RXP3											CSI0_RXP3
	C3	C17	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD		I2C1_SCL
	C4	E17	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO			GPIO1_29	EHRPWM2_B	MMC2_SDWP		I2C1_SDA
	G3	L18	GPMC0_ADVn_ALE	GPMC0_ADVn_ALE		MCASP1_AXR2				TRC_DATA7	GPIO0_32			GPIO0_32
	G4	L19	GPMC0_BE0n_CLE	GPMC0_BE0n_CLE		MCASP1_ACLKX				TRC_DATA10	GPIO0_35			GPIO0_35
RGMI1	K16	W16	RGMII1_TX_CTL	RMII1_TX_EN						GPIO0_73				RGMII1_TX_CTL
	J15	AB17	RGMII1_TXC	RMII1_CRS_DV						GPIO0_74				RGMII1_TXC
	H15	Y17	RGMII1_TD0	RMII1_TXD0						GPIO0_75				RGMII1_TD0
	G15	V16	RGMII1_TD1	RMII1_TXD1						GPIO0_76				RGMII1_TD1
	H16	Y16	RGMII1_TD2							GPIO0_77				RGMII1_TD2
	G16	AA17	RGMII1_TD3	CLKOUT0						GPIO0_78				RGMII1_TD3
	K16	AA15	RGMII1_RX_CTL	RMII1_RX_ER						GPIO0_79				RGMII1_RX_CTL
	R15	AA16	RGMII1_RXC	RMII1_REF_CLK						GPIO0_80				RGMII1_RXC
	K15	AB16	RGMII1_RD0	RMII1_RXD0						GPIO0_81				RGMII1_RD0
	L15	V15	RGMII1_RD1	RMII1_RXD1						GPIO0_82				RGMII1_RD1
	N15	W15	RGMII1_RD2							GPIO0_83				RGMII1_RD2
	P15	V14	RGMII1_RD3							GPIO0_84				RGMII1_RD3
MDIO	T15/C7	V13	MDIO0_MDIO							GPIO0_85				MDIO0_MDIO
	T16/C6	V12	MDIO0_MDC							GPIO0_86				MDIO0_MDC
RGMI2	L1	W18	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3					GPIO1_1				RGMII2_RX_CTL
	P1	AA20	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1					GPIO1_2				RGMII2_RXC
	J1	AA21	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2					GPIO1_3				RGMII2_RD0
	K1	Y20	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR			MCASP2_AXR7		GPIO1_4				RGMII2_RD1
	M1	AB21	RGMII2_RD2		MCASP2_AXR0					GPIO1_5	EQEP2_A			RGMII2_RD2
	N1	AB20	RGMII2_RD3		AUDIO_EXT_REFCLK0					GPIO1_6	EQEP2_B			RGMII2_RD3

Interface/ Function	OSM Edge Pin Number	AM62Ax SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Default
	J2	Y19	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR 4					GPIO0_87				RGMII2_TX_CTL
	H1	AB19	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR 5					GPIO0_88				RGMII2_TXC
	G1	AA19	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR 6					GPIO0_89				RGMII2_TD0
	F1	Y18	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLK R			MCASP2_AX R8		GPIO0_90				RGMII2_TD1
	G2	AA18	RGMII2_TD2		MCASP2_AFSX					GPIO0_91	EQEP2_I			RGMII2_TD2
	F2	W17	RGMII2_TD3	CLKOUT0	MCASP2_ACLK X					GPIO1_0	EQEP2_S			RGMII2_TD3
SD Interface	G20	B22	MMC1_DAT0	CP_GEMAC_CPTS 0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_AP WM_OUT			GPIO1_45				MMC1_DAT0
	G21	D21	MMC1_DAT1	CP_GEMAC_CPTS 0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_AP WM_OUT			GPIO1_44				MMC1_DAT1
	H20	C22	MMC1_DAT2	CP_GEMAC_CPTS 0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43				MMC1_DAT2
	H21	D22	MMC1_DAT3	CP_GEMAC_CPTS 0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42				MMC1_DAT3
	F21	E22	MMC1_CLK		TIMER_IO4	UART3_RXD				GPIO1_46				MMC1_CLK
	E20	C21	MMC1_CMD		TIMER_IO5	UART3_TXD				GPIO1_47				MMC1_CMD
	J21	E18	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48				MMC1_SDCD
	D20	D18	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				GPIO1_49				MMC1_SDWP
QSPI	U15	J21	OSPI0_D0							GPIO0_3				OSPI0_D0
	V15	J18	OSPI0_D1							GPIO0_4				OSPI0_D1
	W16	J19	OSPI0_D2							GPIO0_5				OSPI0_D2
	W15	H18	OSPI0_D3							GPIO0_6				OSPI0_D3
	U16	L22	OSPI0_CLK							GPIO0_0				OSPI0_CLK
	Y15	G19	OSPI0_CSn1							GPIO0_12				OSPI0_CSn1
USB0	AC14	AA9	USB0_DP											USB0_DP
	AB13	AA10	USB0_DM											USB0_DM
	AB16	V8	USB0_VBUS											USB0_VBUS
	AB14	B15	SPI0_D0	CP_GEMAC_CPTS 0_HW1TSPUSH	EHRPWM1_B					GPIO1_18				GPIO1_18
	AC16	C20	USB0_DRVVBUS							GPIO1_50				USB0_DRVVBUS
USB1	AC22	Y10	USB1_DP											USB1_DP
	AB23	Y11	USB1_DM											USB1_DM
	AB20	V6	USB1_VBUS											USB1_VBUS
	AB22	E15	SPI0_D1	CP_GEMAC_CPTS 0_HW2TSPUSH	EHRPWM_TZn _IN0					GPIO1_19				SPI0_D1
	AC20	D19	USB1_DRVVBUS							GPIO1_51				USB1_DRVVBUS
UART5	A14	K20	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_ OUT1	MCASP1_AFSR	MCASP1_AXR 2	UART5_RXD		GPIO0_13				UART5_RXD
	B13	G20	OSPI0_CSn3	OSPI0_RESET_OU T0	OSPI0_ECC_FA IL	MCASP1_ACLKR	MCASP1_AXR 3	UART5_TXD		GPIO0_14				UART5_TXD
	C14	L21	OSPI0_DQS					UART5_CTSn		GPIO0_2				UART5_CTSn
	C13	K22	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1				UART5_RTSn
UART4	D14	F22	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				GPIO0_71				UART4_RXD
	D13	E21	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				GPIO0_72				UART4_TXD
UART0	D23	D15	UART0_TXD	ECAP2_IN_APWM _OUT	SPI2_D1	EHRPWM2_B				GPIO1_21				UART0_TXD
	D22	E14	UART0_RXD	ECAP1_IN_APWM _OUT	SPI2_D0	EHRPWM2_A				GPIO1_20				UART0_RXD

Interface/ Function	OSM Edge Pin Number	AM62Ax SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Default
Audio MCASP0	V21	B19	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD		ECAP2_IN_APWM_OUT		GPIO1_8	EQEP0_B			MCASP0_AXR2
	W21	C19	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD		ECAP1_IN_APWM_OUT		GPIO1_7	EQEP0_A			MCASP0_AXR3
	W19	B18	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT				EHRPWM1_A	GPIO1_9	EQEP0_S			MCASP0_AXR1
	V19	B20	MCASP0_AXR0		AUDIO_EXT_REFCLK0				EHRPWM1_B	GPIO1_10	EQEP0_I			MCASP0_AXR0
	W20	A19	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A			MCASP0_ACLKX
	W18	A20	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B			MCASP0_AFSX
CAN	AC17	B17	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I		GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3		MCAN0_TX
	AB17	C18	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S		GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4		MCAN0_RX
RGB	K3	T18	VOUT0_HSYNC	GPMC0_A16			UART3_RTSn			GPIO0_61				VOUT0_HSYNC
	J4	U17	VOUT0_DE	GPMC0_A17			UART3_CTSn			GPIO0_62				VOUT0_DE
	L3	V17	VOUT0_VSYNC	GPMC0_A18			UART2_RTSn			GPIO0_63				VOUT0_VSYNC
	M4	AA22	VOUT0_PCLK	GPMC0_A19			UART2_CTSn			GPIO0_64				VOUT0_PCLK
	R4	U22	VOUT0_DATA0	GPMC0_A0			UART2_RXD			GPIO0_45				VOUT0_DATA0
	R3	U21	VOUT0_DATA1	GPMC0_A1			UART2_TXD			GPIO0_46				VOUT0_DATA1
	P3	U20	VOUT0_DATA2	GPMC0_A2			UART3_RXD			GPIO0_47				VOUT0_DATA2
	N3	U19	VOUT0_DATA3	GPMC0_A3			UART3_TXD			GPIO0_48				VOUT0_DATA3
	N4	T19	VOUT0_DATA4	GPMC0_A4			UART4_RXD			GPIO0_49				VOUT0_DATA4
	M3	U18	VOUT0_DATA5	GPMC0_A5			UART4_TXD			GPIO0_50				VOUT0_DATA5
	W4	V22	VOUT0_DATA6	GPMC0_A6			UART5_RXD			GPIO0_51				VOUT0_DATA6
	V3	V21	VOUT0_DATA7	GPMC0_A7			UART5_TXD			GPIO0_52				VOUT0_DATA7
	V4	V19	VOUT0_DATA8	GPMC0_A8			UART6_RXD			GPIO0_53				VOUT0_DATA8
	U3	V18	VOUT0_DATA9	GPMC0_A9			UART6_TXD			GPIO0_54				VOUT0_DATA9
	T3	W22	VOUT0_DATA10	GPMC0_A10			UART6_RTSn			GPIO0_55				VOUT0_DATA10
	T4	W21	VOUT0_DATA11	GPMC0_A11			UART6_CTSn			GPIO0_56				VOUT0_DATA11
	Y7	W20	VOUT0_DATA12	GPMC0_A12			UART5_RTSn			GPIO0_57				VOUT0_DATA12
	AA6	W19	VOUT0_DATA13	GPMC0_A13			UART5_CTSn			GPIO0_58				VOUT0_DATA13
	Y6	Y21	VOUT0_DATA14	GPMC0_A14			UART4_RTSn			GPIO0_59				VOUT0_DATA14
	AA5	Y22	VOUT0_DATA15	GPMC0_A15			UART4_CTSn			GPIO0_60				VOUT0_DATA15
	Y5	P22	GPMC0_AD8	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0				GPIO0_23			GPIO1_120	VOUT0_DATA16
	Y4	R19	GPMC0_AD9	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1				GPIO0_24			GPIO1_121	VOUT0_DATA17
	K4	M19	GPMC0_CSn0			MCASP2_AXR14			TRC_DATA15	GPIO0_41				GPIO0_41
	H3	M21	GPMC0_CSn1			MCASP2_AXR15			TRC_DATA16	GPIO0_42				GPIO0_42
I2C3	AA16	C15	UART0_RTSn	UART0_RTSn	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1		GPIO1_23	MCASP2_ACLKX		I2C3_SDA
	AA15	F14	UART0_CTSn	UART0_CTSn	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0		GPIO1_22	MCASP2_AFSX		I2C3_SCL
Mian domain GPIOs	D19	B21	MCASP0_AFSR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I	SPI2_CLK		GPIO1_14
	E19	A21	MCASP0_ACLKR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S	SPI2_CS0		GPIO1_13
	F19	F17	EXTINTn							GPIO1_31				GPIO1_31
MCU GPIOs	D17	C8	WKUP_UART0_RTSn	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12				MCU_GPIO0_12
	E17	B13	MCU_SPI0_CLK							MCU_GPIO0_2				MCU_GPIO0_2
	F17	A15	MCU_SPI0_D0							MCU_GPIO0_3				MCU_GPIO0_3
	G17	B12	MCU_SPI0_D1							MCU_GPIO0_4				MCU_GPIO0_4
	H17	E13	WKUP_I2C0_SDA							MCU_GPIO0_20				MCU_GPIO0_20
	J17	B10	WKUP_CLKOUT0							MCU_GPIO0_23				MCU_GPIO0_23

Interface/ Function	OSM Edge Pin Number	AM62Ax SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Default
	K17	C11	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1				MCU_GPIO0_1
	L17	D7	MCU_MCAN1_TX	MCU_TIMER_IO2	MCU_SPI1_CS1		MCU_EXT_REFCLK0			MCU_GPIO0_15				MCU_GPIO0_15
MCU SPI1	Y21	B9	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16				MCU_SPI1_CLK
	Y23	B11	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7				MCU_SPI1_D0
	Y22	D10	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8				MCU_SPI1_D1
	AA23	C10	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11				MCU_SPI1_CS0
MCU CAN0	AC19	C7	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13				MCU_MCAN0_TX
	AB19	E8	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14				MCU_MCAN0_RX
MCU UART0	D13	F8	MCU_UART0_TXD							MCU_GPIO0_6				MCU_UART0_TXD
	D14	D8	MCU_UART0_RXD							MCU_GPIO0_5				MCU_UART0_RXD
WKUP UART0	A22	C9	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9				WKUP_UART0_RXD
	B23	E9	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10				WKUP_UART0_TXD
MCU I2C0	AA20	E12	MCU_I2C0_SCL							MCU_GPIO0_17				MCU_I2C0_SCL
	AA21	D9	MCU_I2C0_SDA							MCU_GPIO0_18				MCU_I2C0_SDA
Miscellaneous	C16	F19	RESETSTATz											
	P16	D14	MCU_RESETSTATz							MCU_GPIO0_21				MCU_RESETSTATz
	Y31	K18	GPMC0_DIR			MCASP2_AXR13			TRC_DATA14	GPIO0_40	EQEP2_S			GPIO0_40

3. TECHNICAL SPECIFICATION

This section provides detailed information about the AM62Ax OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the seventeen VCC_IN_5V in Size-L Module and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VCC_IN_5V that may vary over the 4.5V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.5V to 5.25V.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of AM62Ax OSM LGA Module.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V[1]	4.5V[1]	5V	5.25V	±50mV
2	VDD_RTC [2]	2.8V	3V	3.3V	±20mV

[1] AM62Ax OSM LGA Module is designed to work with VCC_IN_5V input power rail from OSM only. VCC_IN_5V can be as low as 3.0V with sufficient current if fan is not used.

[2]AM62Ax OSM LGA Module use this voltage as backup power source to RTC controller when VCC_IN_5V is off.

3.1.2 Power Input Sequencing

The AM62Ax OSM LGA Module ’s Power Input sequence requirement is explained below.

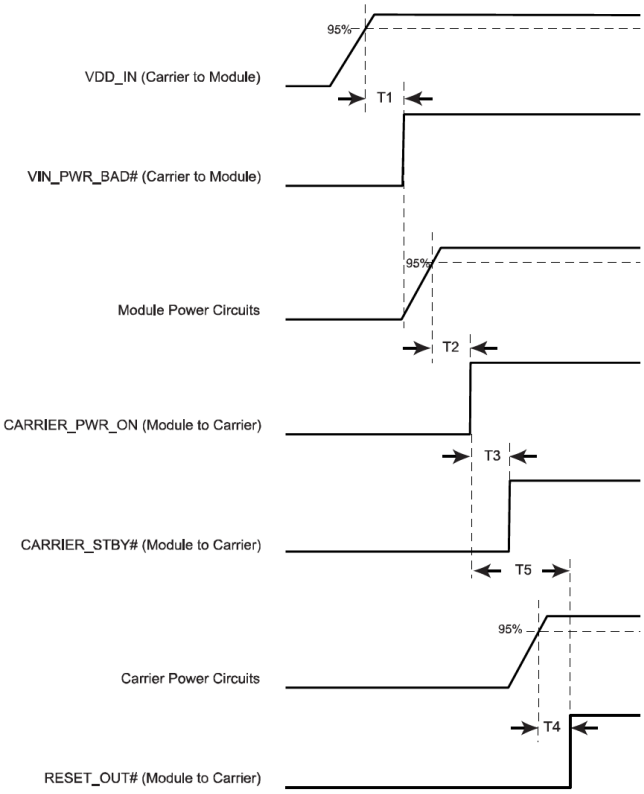

Figure 5: Power Input Sequencing

Table 7: Power Sequence Timing

Item	Description	Value
T1	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T2	VIN_PWR_BAD# rise time to SOM Power rise time	≥ 0 ms
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	≥ 0 ms
T4	Carrier power circuits are up to RESET_OUT# rise	≥ 0 ms
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 to 500ms

3.1.3 Power Consumption

Table 8: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Video run in RGB display (Gstreamer)	VDD_IN	TBD
Play Video run in RGB display (Gplay)	VDD_IN	TBD
Camera Streaming	VDD_IN	TBD
Play Audio	VDD_IN	TBD
Ping Bluetooth	VDD_IN	TBD
Ping Wi-Fi	VDD_IN	TBD
Ping Ethernet (Eth0 and Eth1)	VDD_IN	TBD
eMMC to Standard SD file transfer	VDD_IN	TBD
eMMC to USB2.0 file transfer	VDD_IN	TBD
Bluetooth file transfer	VDD_IN	TBD
Wi-Fi file transfer	VDD_IN	TBD
Ethernet Streaming (Video Play)	VDD_IN	TBD
Dhrystone	VDD_IN	TBD
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in RGB display (Gplay) • Camera Streaming • Ethernet (eth0 & eth1) Run the ping (65500 packet size) • Wi-Fi- Run the ping teston back ground • FileTransfer - Transfer the 1GB files in storage devices • Run the dry2 application on back ground	VDD_IN	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VDD_IN	TBD
Deep Sleep Mode.	VDD_IN	TBD
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	TBD

[1] *Power consumption measurements are done in iWave 's AM62Ax SoC based OSM Development platform with iWave's TBD.*

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of AM62Ax OSM LGA Module.

Table 9: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution & Heat sink/ Heat Spreader refer the following section.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink Solution for AM62Ax OSM LGA Module. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

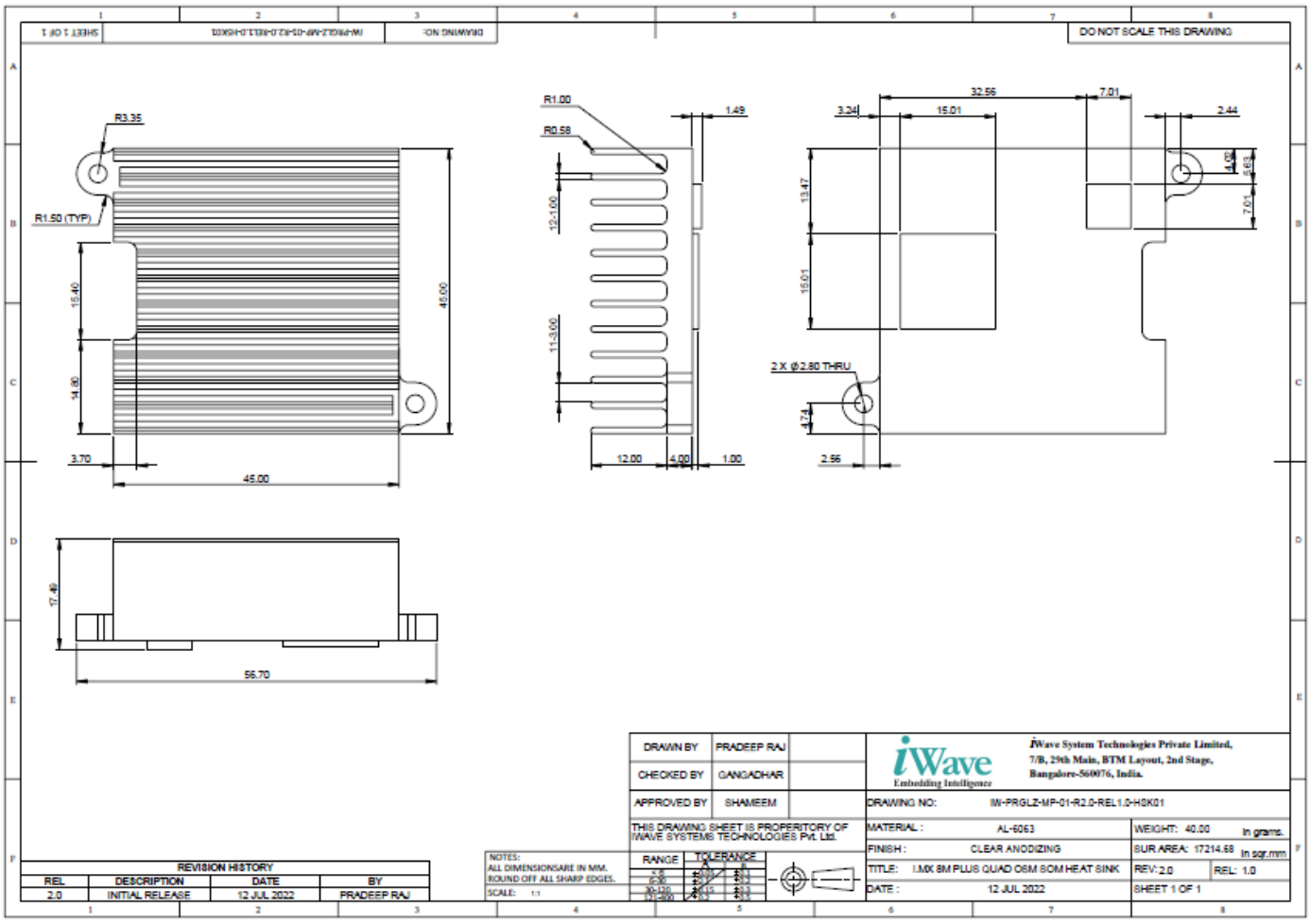

Figure 6: Mechanical dimension of heat Sink

3.2.3 RoHS Compliance

iWave's AM62Ax OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's AM62Ax OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 AM62Ax OSM LGA Module Mechanical Dimensions

AM62Ax OSM LGA Module PCB size is 45 mm x 45 mm The AM62Ax OSM LGA Module PCB thickness is 1.38mm±0.15mm**,** top side maximum height component is 2.41mm (SoC).

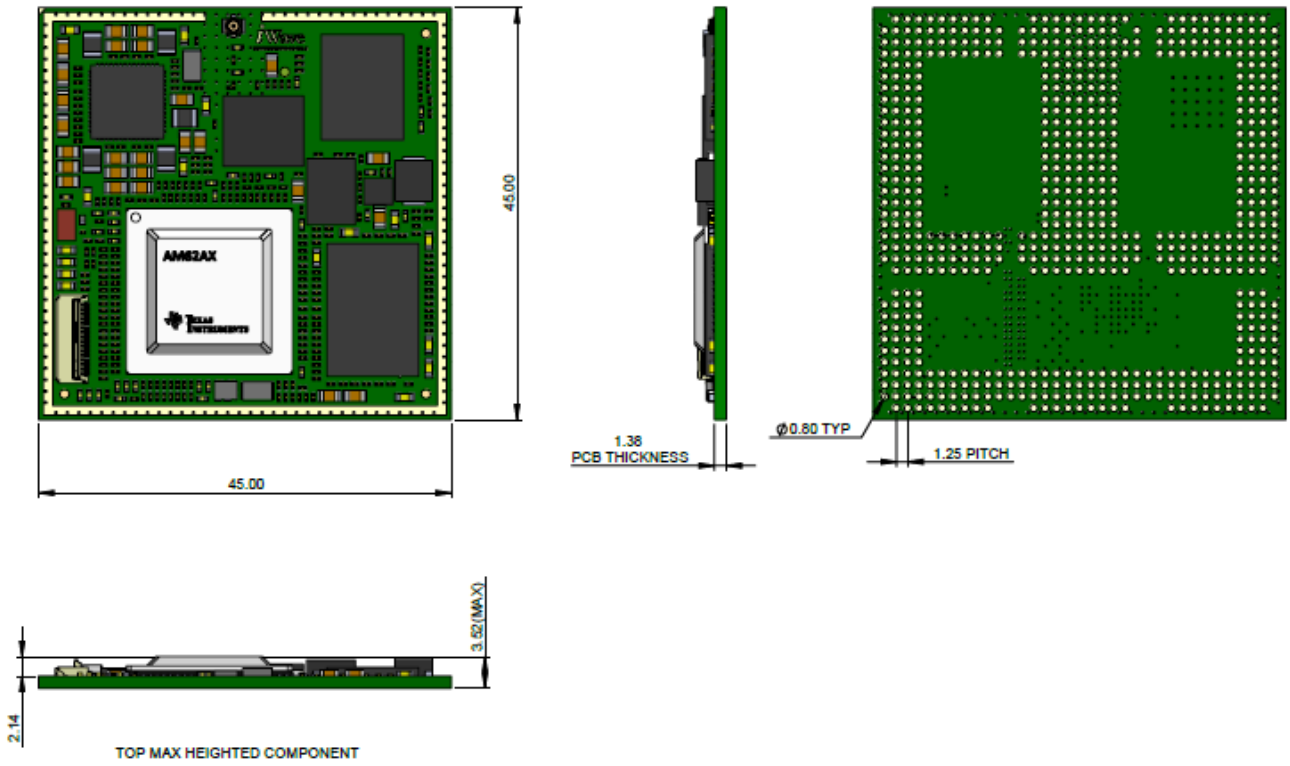

Figure 7: Mechanical dimensions of AM62Ax OSM LGA Module

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different AM62Ax OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 10: Orderable Product Part Numbers

Product Part Number	Description	Temperature
With Wi-Fi/BT Configuration		
iW-G55M-OL74-4L002G-E016G-BIA	AM62A74 CPU, 2GB LPDDR4, 16GB eMMC, Wi-Fi/BT OSM SOM	-40°C to 85°C
iW-G55M-OL74-4L001G-E008G-BIA	AM62A74 CPU, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT OSM SOM	-40°C to 85°C
iW-G55M-OL34-4L002G-E016G-BIA	AM62A34 CPU, 2GB LPDDR4, 16GB eMMC, Wi-Fi/BT OSM SOM	-40°C to 85°C
iW-G55M-OL34-4L001G-E008G-BIA	AM62A34 CPU, 1GB LPDDR4, 8GB eMMC, Wi-Fi/BT OSM SOM	-40°C to 85°C
Without Wi-Fi/BT Configuration		
iW-G55M-OL74-4L002G-E016G-BIB	AM62A74 CPU, 2GB LPDDR4, 16GB eMMC, OSM SOM	-40°C to 85°C
iW-G55M-OL74-4L001G-E008G-BIB	AM62A74 CPU, 1GB LPDDR4, 8GB eMMC, OSM SOM	-40°C to 85°C
iW-G55M-OL34-4L002G-E016G-BIB	AM62A34 CPU, 2GB LPDDR4, 16GB eMMC, OSM SOM	-40°C to 85°C
iW-G55M-OL34-4L001G-E008G-BIB	AM62A34 CPU, 1GB LPDDR4, 8GB eMMC, OSM SOM	-40°C to 85°C

Note: Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.

5. APPENDIX

5.1.1 AM62Ax OSM Development Platform

iWave Systems supports iW-RainboW-G55S-AM62Ax Development Platform which is targeted for quick validation of AM62Ax SoC based OSM SOM and its features. Being a PICO-ITX form factor with 100mm x 72mm size, the OSM Development Platform is highly packed with all necessary interfaces & on-board connectors to validate complete OSM supported features.

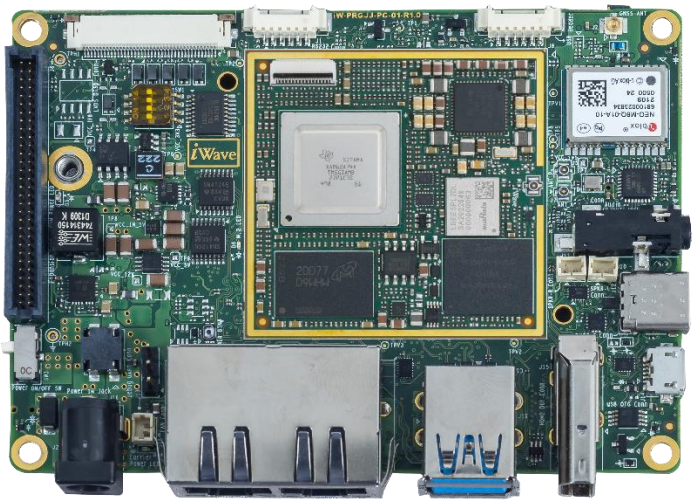

Figure 8: AM62Ax OSM Development Platform


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