DK_START_GW5A-LV25UG324_V1.1

User Guide

DBUG416-1.0E, 08/18/2023

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Revision History

Date	Version	Description
08/18/2023	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_START_GW5A-LV25UG324_V1.1 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pinout

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1103, GW5A series of FPGA Products Data Sheet
- UG985, GW5A-25 Pinout
- UG1101, GW5A series of FPGA Products Package and Pinout User Guide
- UG290, Gowin FPGA Products Programming and Configuration Guide
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ADC	Analog-to-digital Converter
DDR	Double Data Rate
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

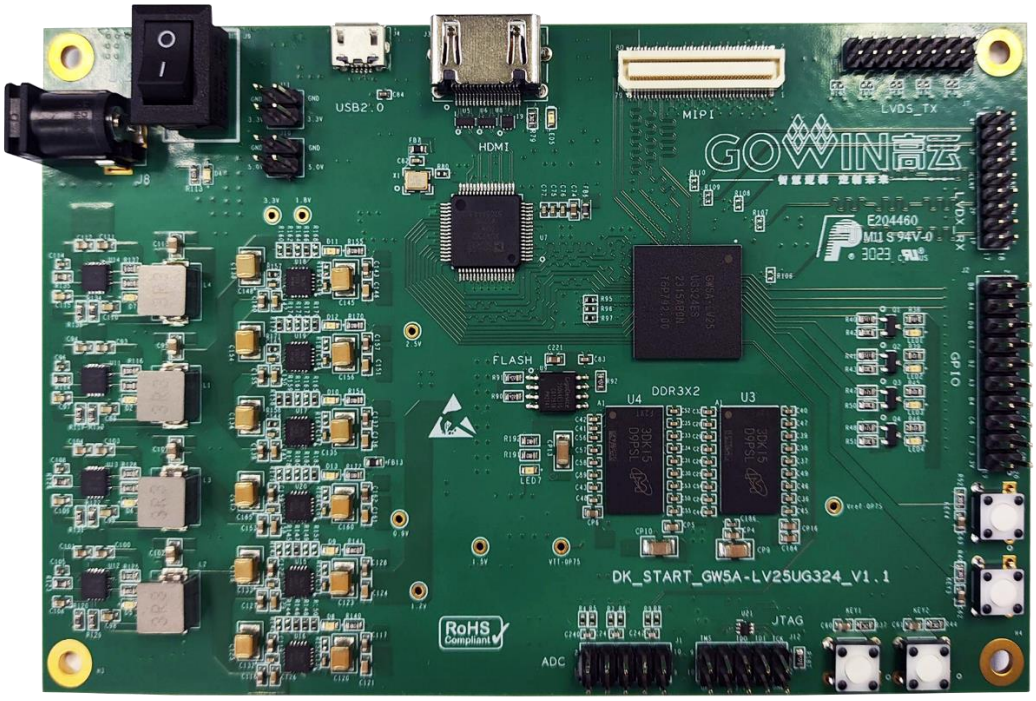
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5A-LV25UG324_V1.1 Development Board



DK_START_GW5A-LV25UG324_V1.1 development board applies to DDR3 high-speed data storage, MIPI, LVDS high-speed communication, ADC, HDMI_TX communication, hardware verification, and software learning and debugging, etc.

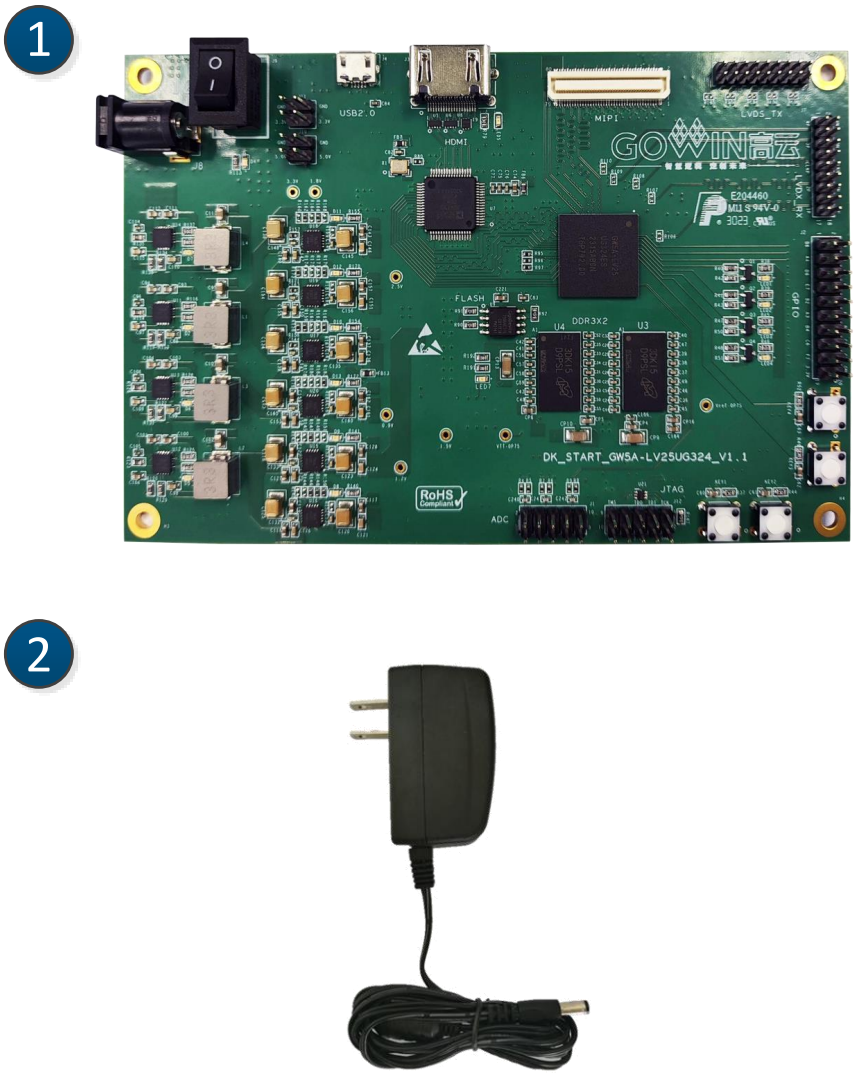
The development board adopts Gowin GW5A-LV25UG324 FPGA device. For the internal resources of the chip, see *DS1103, GW5A series of FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5A-LV25UG324_V1.1 development board
2. 12V power (Input: 100-240V~50/60Hz 0.6A, output: DC 12V 2A)

Figure 2-2 A Development Kit



① DK_START_GW5A-LV25UG324_V1.1 development board

② 12V power supply adapter

2.3 PCB Components

Figure 2-3 PCB Components

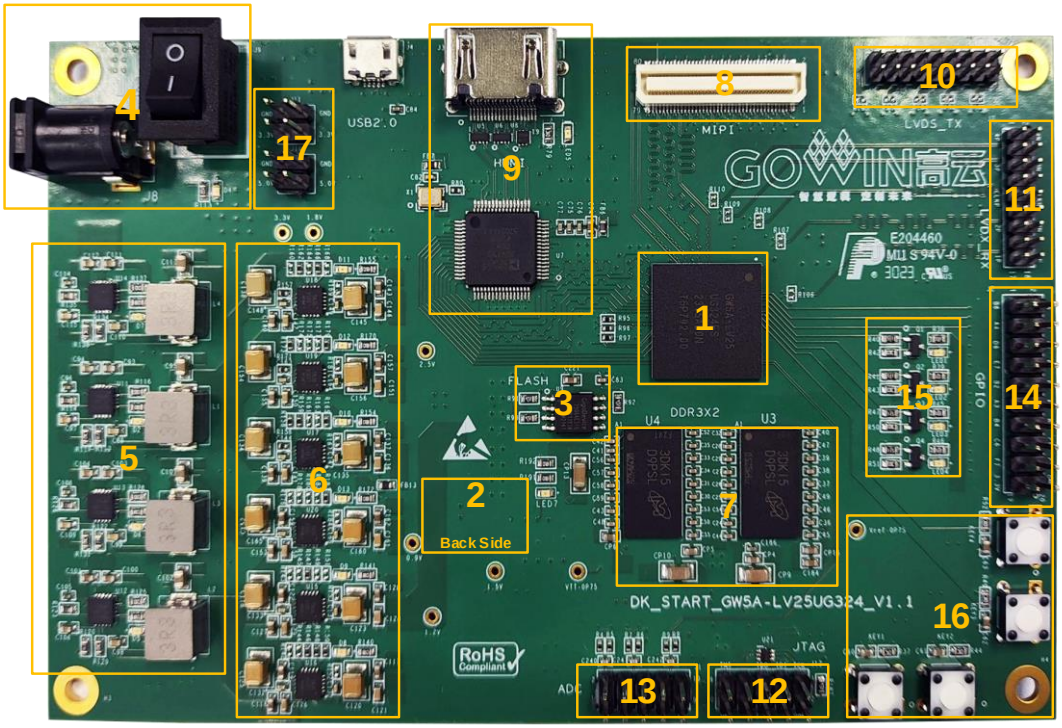


Table 2-1 PCB Components

No.	Description
1	GW5A-LV25UG324, FPGA
2	OT322550MJBA4SL, 50M clock crystal oscillator
3	GD25Q64ESIG, 64M SPI flash
4	+12V power supply
5	TPS54622, DC-DC power conversion chip
6	TPL930, LDO power conversion chip
7	2 DDR3 Memory, MT41J128M16JT-125:K
8	AXK580137YG, including MIPI_RX/TX hard core, MIPI_RX soft core, MIPI_TX soft core interfaces
9	HDMI_TX interface
10	4 lanes + 1 clk, LVDS_TX interface
11	4 lanes + 1 clk, LVDS_RX interface
12	JTAG download interface

No.	Description
13	ADC input interfaces
14	18 GPIOs with 1.5V power supply interface
15	4*LED
16	4*Switch
17	5.0V to external power supply, 3.3V to external power supply interface

2.4 Features

The key features are as follows:

- FPGA Device
  - The development board adopts GW5A-LV25UG324 FPGA device, which is the fifth generation products of Gowin Arora family.
  - Max. user I/O: 240
- Download and Boot
  - The programs can be downloaded by connecting Gowin downloader to the JTAG interface on the board.
  - External SPI Flash boot
  - The DONE light is on after loading
- Power
  - External DC 12V/2A Power
  - The POWER light is on after power on
  - The board generates 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V voltage.
- System Clock
  - 50MHz clock
- Memory Device
  - 2Gbit DDR3 SDRAM
  - 64Mbit Quad SPI Flash Memory
- LVDS Interface
  - LVDS_TX (4 lanes + 1 clk)
  - LVDS_RX (4 lanes + 1 clk)
- MIPI Interface
  - MIPI_RX/TX hard core (4 lanes + 1 clk)
  - MIPI_RX soft core (4 lanes + 1 clk)
  - MIPI_TX soft core (4 lanes + 1 clk)
  - 4 GPIOs
  - 5.0V power supply

  - 3.3V power supply
  - Use connector with 80 contacts and 0.5mm pitch
- ADC
  - The interface uses 2x5Pin pins.
  - 3 ADCs, the differential input is designed with an anti-aliasing filter.
- Key & LED
  - 4 keys
  - 4 LEDs
- HDMI_TX Interface
  - Interface of HDMI transmitter chip ADV7513BSWZ
- GPIO Interface
  - 18 1.5V GPIOs

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5A series of FPGA Products, refer to *DS1103, GW5A series of FPGA products*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG1101, GW5A Series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is 100-240V~50/60MHz 0.6A, and the output parameter is DC +12V 2A.

Four TPS54622 (DC-DC) power supply chips are used to convert the adapter's 12V to 1.2V, 2.1V, 3.6V, and 5.0V, respectively, each with a maximum output current of 6A.

Then the generated 1.2V, 2.1V, and 3.6V power is provided to six TPL930 (LDO) power supply chips to generate 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V power supplies. The maximum output current is 3A.

The power supply output from the TPL930 power supply chip is used as the input of the TPS51200 power supply chip, which outputs 0.75V to power the DDR3.

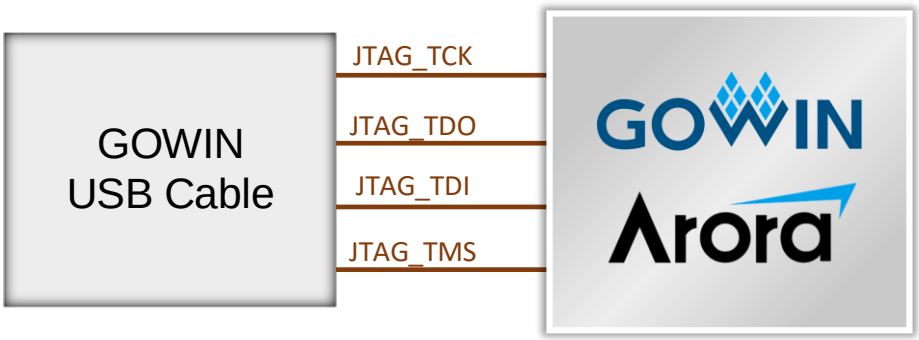
3.3 JTAG Interface

3.3.1 Introduction

The DK_START_GW5A-LV25UG324_V1.1 development board has a JTAG download port (J12) reserved for download and debugging. The interface type is 2x5 pin headers with 2.54mm double-row pitch, which is equipped with ESD protection circuit.

The program can be programmed to an external SPI Flash or downloaded to an SRAM by connecting Gowin downloader to the JTAG download port (J12) on the board. The connection diagram of JTAG is shown in Figure 3-1.

Figure 3-1 Connection Diagram of JTAG



3.3.2 Pinout

Table 3-1 JTAG Pinout

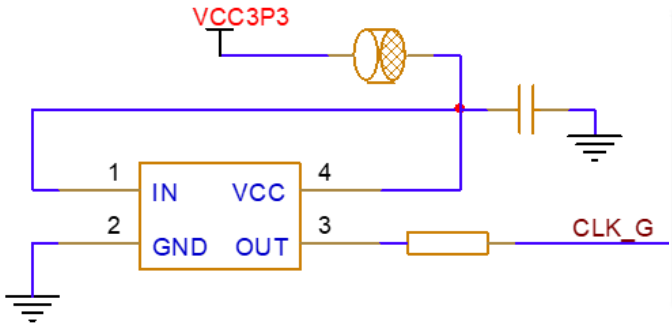
Signal Name	FPGA(U1) Pin No.	BANK	I/O Level	Description
JTAG_TCK	A17	10	3.3V	JTAG Signal
JTAG_TDO	D16	10	3.3V	
JTAG_TDI	D15	10	3.3V	
JTAG_TMS	B18	10	3.3V	

3.4 Clock

3.4.1 Introduction

FPGA clock source, single-ended clock signal introduction, crystal oscillator model: OT322550MJBA4SL. The clock pinout is as shown in Table 3-2.

Figure 3-2 Clock Connection Diagram



3.4.2 Pinout

Table 3-2 Clock Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_G	T9	4	3.3V	Frequency 50MHz

3.5 DDR3

3.5.1 Introduction

DK_START_GW5A-LV25UG324_V1.1 development board includes two 2Gbit DDR3 chip, with the model number of MT41J128M16JT-125:K. The signal of DDR3 chip is connected to the BANK1, BANK2, and BANK3 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

Table 3-3 DDR3 Configuration

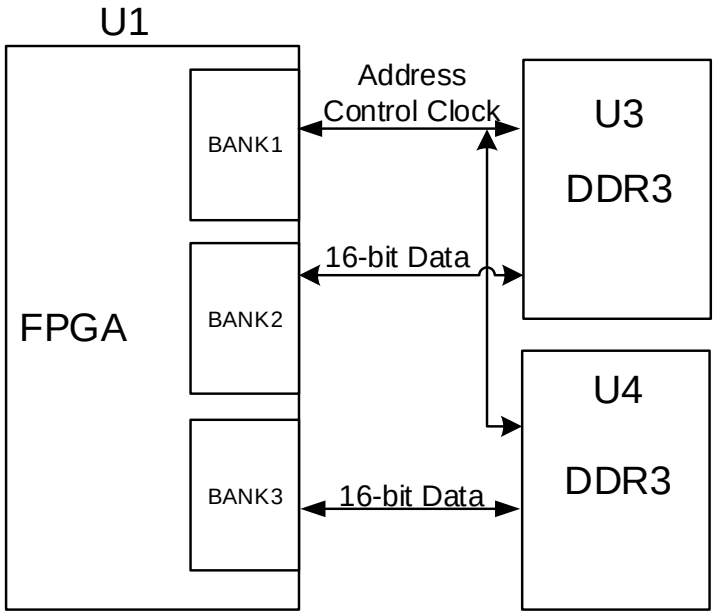
Designator	Model	Capacity
U3	MT41J128M16JT-125:K	128M x 16bit
U4	MT41J128M16JT-125:K	128M x 16bit

DDR3 hardware design requires strict consideration of signal integrity.

In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-3.

Figure 3-3 Hardware Connection Diagram of DDR3



3.5.2 Pinout

Table 3-4 DDR3 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	B11	1	1.5V	Address
DDR3_A1	A10	1	1.5V	Address
DDR3_A2	C11	1	1.5V	Address
DDR3_A3	F11	1	1.5V	Address
DDR3_A4	A14	1	1.5V	Address
DDR3_A5	G11	1	1.5V	Address
DDR3_A6	C12	1	1.5V	Address
DDR3_A7	F10	1	1.5V	Address
DDR3_A8	A12	1	1.5V	Address
DDR3_A9	C10	1	1.5V	Address
DDR3_A10	F12	1	1.5V	Address
DDR3_A11	A11	1	1.5V	Address

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A12	D12	1	1.5V	Address
DDR3_A13	G9	1	1.5V	Address
DDR3_BA0	B14	1	1.5V	Bank address
DDR3_BA1	E12	1	1.5V	Bank address
DDR3_BA2	D11	1	1.5V	Bank address
DDR3_CS#	E13	1	1.5V	Chip select
DDR3_CAS#	F13	1	1.5V	Column address strobe
DDR3_CKE	A13	1	1.5V	Clock Enable
DDR3_ODT	E11	1	1.5V	On-Die Termination Enable
DDR3_RAS#	C15	1	1.5V	Row address strobe
DDR3_RESET	F9	1	1.5V	Reset
DDR3_WE#	C13	1	1.5V	Write enable
DDR3_CLK0_N	C14	1	1.5V	Differential clock
DDR3_CLK0_P	D14	1	1.5V	Differential clock
DDR3_DQ0	E18	2	1.5V	Data
DDR3_DQ1	F15	2	1.5V	Data
DDR3_DQ2	E16	2	1.5V	Data
DDR3_DQ3	F14	2	1.5V	Data
DDR3_DQ4	H13	2	1.5V	Data
DDR3_DQ5	C17	2	1.5V	Data
DDR3_DQ6	F16	2	1.5V	Data
DDR3_DQ7	C18	2	1.5V	Data
DDR3_DQ8	G16	2	1.5V	Data
DDR3_DQ9	K12	2	1.5V	Data
DDR3_DQ10	F17	2	1.5V	Data
DDR3_DQ11	L12	2	1.5V	Data
DDR3_DQ12	G18	2	1.5V	Data
DDR3_DQ13	L13	2	1.5V	Data

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ14	F18	2	1.5V	Data
DDR3_DQ15	K13	2	1.5V	Data
DDR3_LDM	G14	2	1.5V	Data input mask
DDR3_UDM	H15	2	1.5V	Data input mask
DDR3_LDQSp	D17	2	1.5V	Data Clock
DDR3_LDQSn	D18	2	1.5V	Data Clock
DDR3_UDQSp	J13	2	1.5V	Data Clock
DDR3_UDQSn	K14	2	1.5V	Data Clock
DDR3_DQ16	L18	3	1.5V	Data
DDR3_DQ17	L15	3	1.5V	Data
DDR3_DQ18	M18	3	1.5V	Data
DDR3_DQ19	J16	3	1.5V	Data
DDR3_DQ20	L17	3	1.5V	Data
DDR3_DQ21	H18	3	1.5V	Data
DDR3_DQ22	M16	3	1.5V	Data
DDR3_DQ23	H17	3	1.5V	Data
DDR3_DQ24	P17	3	1.5V	Data
DDR3_DQ25	T17	3	1.5V	Data
DDR3_DQ26	N17	3	1.5V	Data
DDR3_DQ27	N14	3	1.5V	Data
DDR3_DQ28	P18	3	1.5V	Data
DDR3_DQ29	U17	3	1.5V	Data
DDR3_DQ30	N18	3	1.5V	Data
DDR3_DQ31	U18	3	1.5V	Data
DDR3_LDM_1	L16	3	1.5V	Data input mask
DDR3_UDM_1	T18	3	1.5V	Data input mask
DDR3_LDQSp_1	K17	3	1.5V	Data Clock
DDR3_LDQSn_1	K18	3	1.5V	Data Clock
DDR3_UDQSp_1	N15	3	1.5V	Data Clock
DDR3_UDQSn_1	N16	3	1.5V	Data Clock

3.6 SPI Flash

3.6.1 Introduction

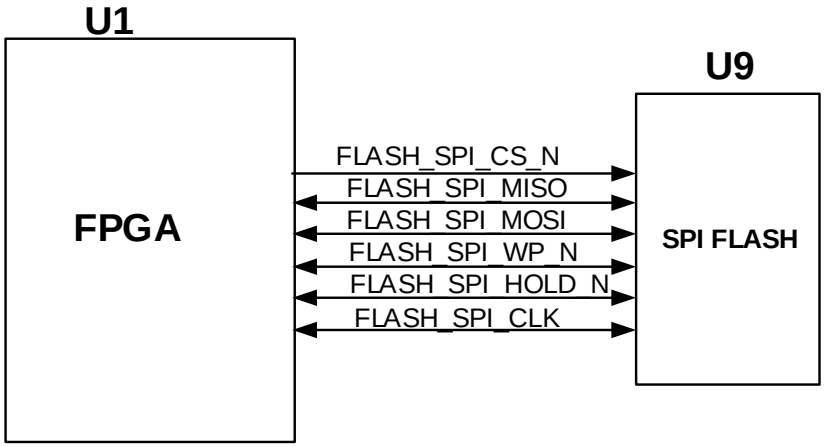
The DK_START_GW5A-LV25UG324_V1.1 development board includes an SPI Flash memory chip. The chip model is GD25Q64ESIG and the memory capacity of 64Mbit. The FPGA program is programmed into the SPI FLASH and the FPGA chip loads the program in the SPI Flash through the MSPI interface when powered up. The specific models and related parameters of SPI FLASH are as shown in Table 3-5.

Table 3-5 Specific Model and Related Parameters of SPI Flash

Designator	Model	Capacity
U9	GD25Q64ESIG	64M Bit

The SPI Flash is connected to the dedicated pins in BANK4 on the FPGA chip. Figure 3-4 is the hardware connection diagram of SPI Flash.

Figure 3-4 Hardware Connection Diagram of SPI Flash



3.6.2 Pinout

Table 3-6 Flash Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level
FLASH_SPI_CLK	R15	4	3.3V
FLASH _SPI_CS_N	V3	4	3.3V
FLASH_SPI_MISO	R13	4	3.3V
FLASH_SPI_MOSI	T13	4	3.3V

Signal Name	FPGA Pin No.	BANK	I/O Level
FLASH_SPI_WP_N	T14	4	3.3V
FLASH_SPI_HOLD_N	V14	4	3.3V

3.7 LED, Key

3.7.1 Introduction

The DK_START_GW5A-LV25UG324_V1.1 development board includes four user LEDs. The user LEDs are connected to the IO of BANK0 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low.

There are four user keys on the development board. The user keys are respectively connected to the general IO of FPGA BANK0. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed.

3.7.2 Pinout

Table 3-7 LED Pinout

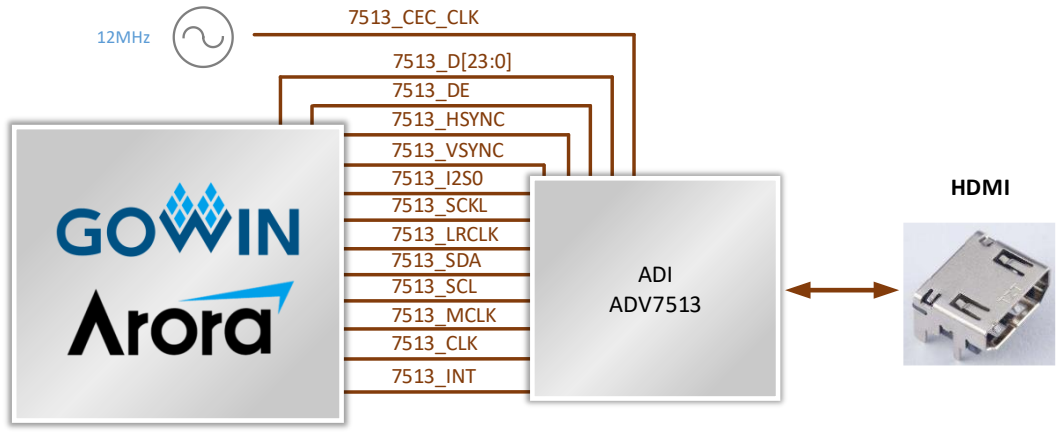
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	A7	0	1.5V	LED
LED2	A8	0	1.5V	LED
LED3	B8	0	1.5V	LED
LED 4	C8	0	1.5V	LED
KEY1	D9	0	1.5V	Key
KEY2	C9	0	1.5V	Key
KEY3	B9	0	1.5V	Key
KEY4	A9	0	1.5V	Key

3.8 HDMI_TX Interface

3.8.1 Introduction

The DK_START_GW5A-LV25UG324_V1.1 Development Board includes HDMI_TX interface. The HDMI_TX interface uses ADI decoding chip of ADV7513BSWZ. The connection diagram is as shown in Figure 3-5.

Figure 3-5 FPGA and HDMI2 Interface Connection Diagram



3.8.2 Pinout

Table 3-8 HDMI_TX Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_CLK	N8	5	3.3V	The RGB data row locks the output clock
7513_D0	T3	5	3.3V	RGB data signal
7513_D1	T4	5	3.3V	RGB data signal
7513_D2	T5	5	3.3V	RGB data signal
7513_D3	T6	5	3.3V	RGB data signal
7513_D4	P7	4	3.3V	RGB data signal
7513_D5	T7	4	3.3V	RGB data signal
7513_D6	P8	5	3.3V	RGB data signal
7513_D7	N9	5	3.3V	RGB data signal
7513_D8	M11	5	3.3V	RGB data signal
7513_D9	N11	5	3.3V	RGB data signal

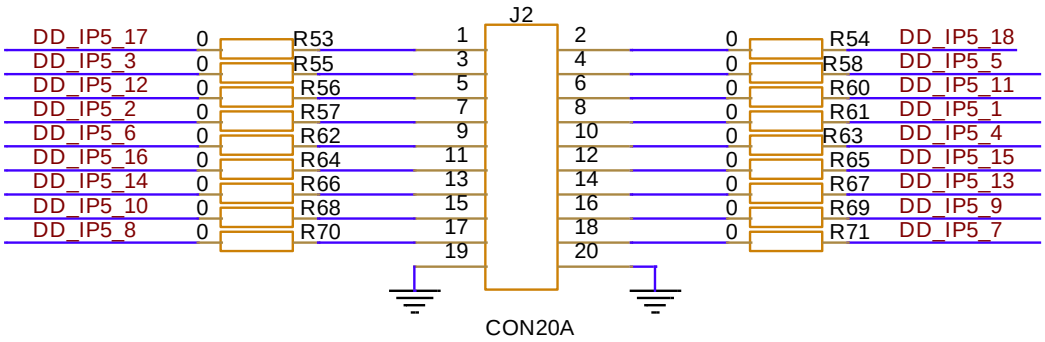
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_D10	U5	4	3.3V	RGB data signal
7513_D11	V5	4	3.3V	RGB data signal
7513_D12	V6	5	3.3V	RGB data signal
7513_D13	U7	5	3.3V	RGB data signal
7513_D14	V7	5	3.3V	RGB data signal
7513_D15	U8	5	3.3V	RGB data signal
7513_D16	V8	5	3.3V	RGB data signal
7513_D17	M10	5	3.3V	RGB data signal
7513_D18	T11	5	3.3V	RGB data signal
7513_D19	R11	5	3.3V	RGB data signal
7513_D20	V12	4	3.3V	RGB data signal
7513_D21	V13	4	3.3V	RGB data signal
7513_D22	V16	4	3.3V	RGB data signal
7513_D23	U16	4	3.3V	RGB data signal
7513_VSYNC	P6	5	3.3V	Vertical Sync output signal
7513_HSYNC	R7	5	3.3V	Horizontal Sync output signal
7513_DE	M8	5	3.3V	RGB Data Enable
7513_SCLK	R3	5	3.3V	Audio Serial Clock
7513_LRCLK	N5	5	3.3V	Audio left/right clock
7513_MCLK	R5	5	3.3V	Audio master clock
7513_I2S0	N6	5	3.3V	Audio output pin
7513_SCL	V15	4	3.3V	I2C serial interface clock
7513_SDA	U13	5	3.3V	I2C serial interface data
7513_INT	U15	4	3.3V	Interrupt signal

3.9 GPIO

3.9.1 Introduction

The DK_START_GW5A-LV25UG324_V1.1 development board routes out 18 1.5V GPIOs through the double-row pin header with 2.54mm pitch.

Figure 3-6 Schematic Connection Diagram of GPIO



3.9.2 Pinout

Table 3-9 GPIO Pinout

Signal Name	FPGA Pin No.	BANK	IO Level
DD_IP5_1	B6	0	1.5V
DD_IP5_2	A4	0	1.5V
DD_IP5_3	D6	0	1.5V
DD_IP5_4	E7	0	1.5V
DD_IP5_5	B2	0	1.5V
DD_IP5_6	A3	0	1.5V
DD_IP5_7	B4	0	1.5V
DD_IP5_8	C6	0	1.5V
DD_IP5_9	F7	0	1.5V
DD_IP5_10	C7	0	1.5V
DD_IP5_11	C5	0	1.5V
DD_IP5_12	B3	0	1.5V
DD_IP5_13	A2	0	1.5V
DD_IP5_14	E8	0	1.5V
DD_IP5_15	E6	0	1.5V

Signal Name	FPGA Pin No.	BANK	IO Level
DD_IP5_16	C4	0	1.5V
DD_IP5_17	A6	0	1.5V
DD_IP5_18	A5	0	1.5V

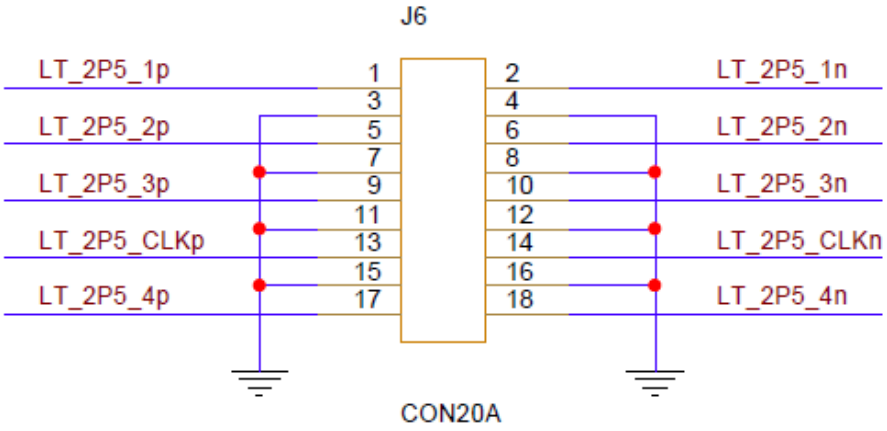
3.10 LVDS Connector

3.10.1 Introduction

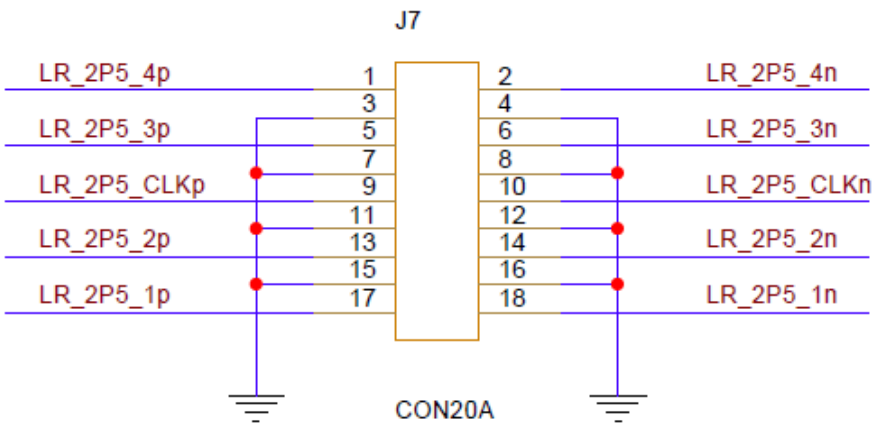
The DK_START_GW5A-LV25UG324_V1.1 development board includes an LVDS transceiver connector with two parts, both in the form of 2x10 pin headers with 2.0mm pitch. LVDS_TX contains: 4 lanes + 1 clk; LVDS_RX contains: 4 lanes + 1 clk.

Figure 3-7 LVDS Schematic Connection Diagram

LVDS_TX:



LVDS_RX:



3.10.2 Pinout

Table 3-10 LVD_TX Pinout

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level
LT_2P5_1p	E4	7	2.5V
LT_2P5_1n	D3	7	2.5V
LT_2P5_2p	D2	7	2.5V
LT_2P5_2n	D1	7	2.5V
LT_2P5_CLKp	F4	7	2.5V
LT_2P5_CLKn	F3	7	2.5V
LT_2P5_3p	E3	7	2.5V
LT_2P5_3n	E1	7	2.5V
LT_2P5_4p	J7	7	2.5V
LT_2P5_4n	J6	7	2.5V

Table 3-11 LVD_RX Pinout

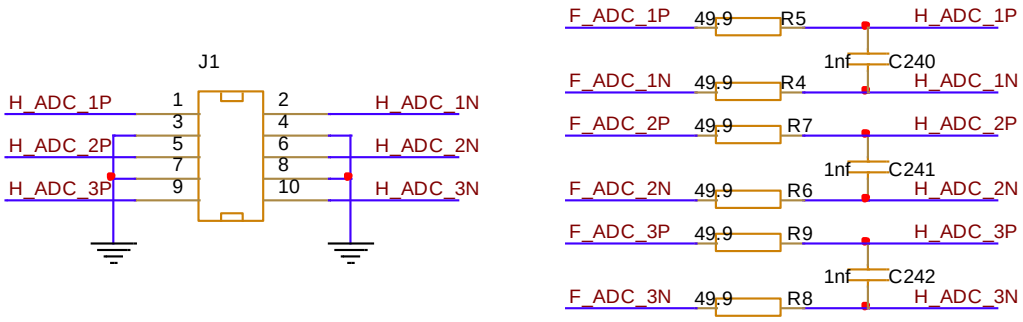
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level
LR_2P5_1p	F6	7	2.5V
LR_2P5_1n	F5	7	2.5V
LR_2P5_2p	C2	7	2.5V
LR_2P5_2n	C1	7	2.5V
LR_2P5_CLKp	H2	6	2.5V
LR_2P5_CLKn	H1	6	2.5V
LR_2P5_3p	K4	6	2.5V
LR_2P5_3n	K3	6	2.5V
LR_2P5_4p	L4	6	2.5V
LR_2P5_4n	L3	6	2.5V

3.11 ADC Interface

3.11.1 Introduction

The DK_START_GW5A-LV25UG324_V1.1 development board reserves input interfaces for ADC signal. The connector uses a 2x5 pin header with 2.54mm pitch.

Figure 3-8 ADC Schematic



3.11.2 Pinout

Table 3-12 ADC Signal Input Pin Distribution

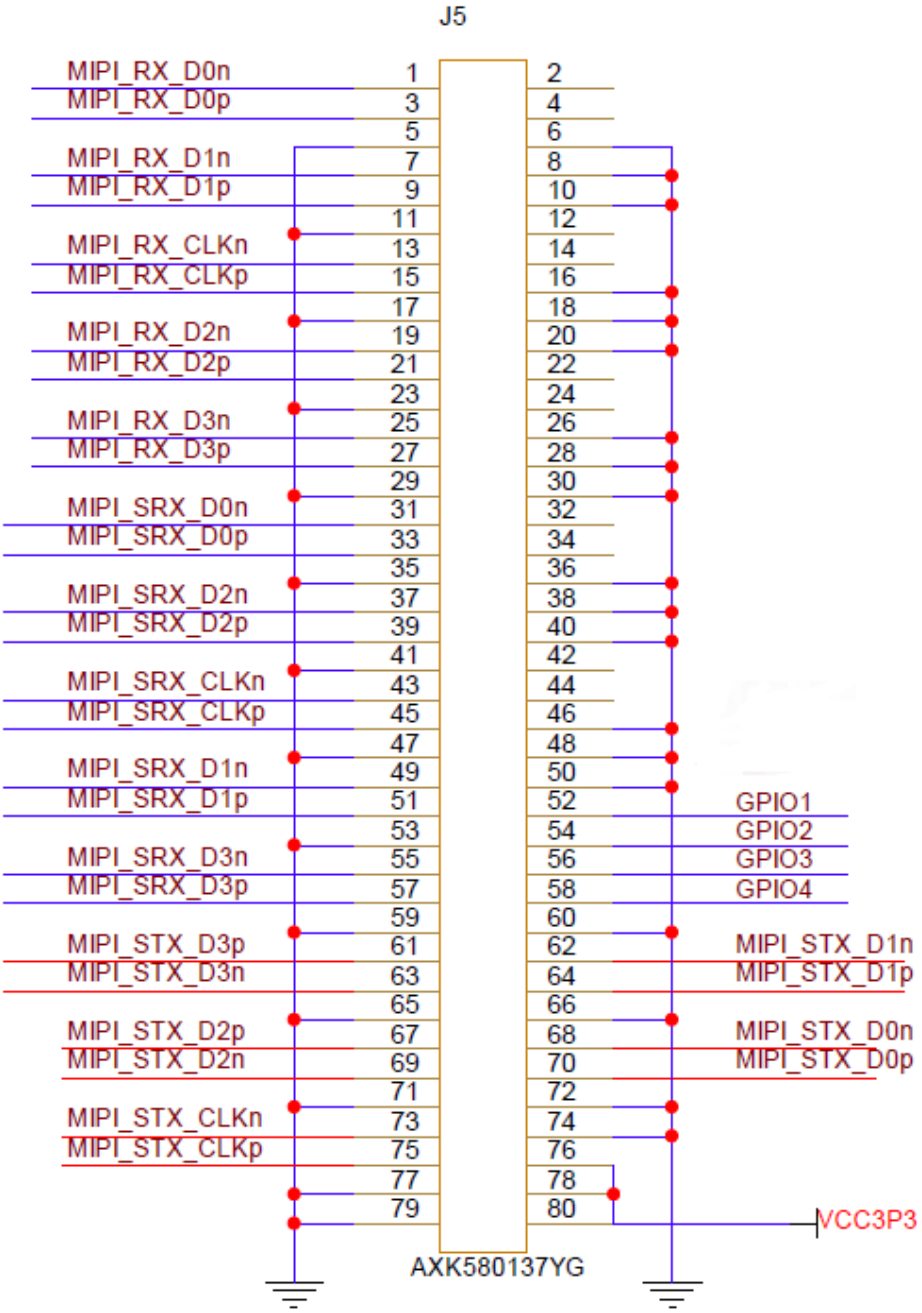
Signal Name	FPGA Pin No.	BANK	IO Level
F_ADC_3P	L14	3	1.5V
F_ADC_3N	M13	3	1.5V
F_ADC_2P	K15	2	1.5V
F_ADC_2N	K16	2	1.5V
F_ADC_1P	B16	1	1.5V
F_ADC_1N	A16	1	1.5V

3.12 MIPI

3.12.1 Introduction

The MIPI interface on the development board uses 80pin AXK580137YG connectors with 0.5mm pitch. The MIPI_RX/TX hard core signal routed from FPGA (4 lanes + 1 clk); MIPI_RX signal (4 lanes + 1 clk); MIPI_TX soft core (4 lanes + 1 clk). The connector also provides 3.3V and 5.0V power. The schematice circuit is as shown in Figure 3-9.

Figure 3-9 Schematic Circuit of MIPI Interface



3.12.2 Pinout

Table 3-13 MIPI Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	J5 Socket Pin No.
MIPI_SRX_D3p	L5	7	2.5V	-
MIPI_SRX_D3N	K5	7	2.5V	-
MIPI_SRX_D2p	G3	7	2.5V	-
MIPI_SRX_D2n	G1	7	2.5V	-
MIPI_SRX_D1p	H7	7	2.5V	-
MIPI_SRX_D1n	G6	7	2.5V	-
MIPI_SRX_D0p	F2	7	2.5V	-
MIPI_SRX_D0n	F1	7	2.5V	-
MIPI_SRX_CLKp	H4	7	2.5V	-
MIPI_SRX_CLKn	H3	7	2.5V	-
MIPI_STX_D3p	K2	6	2.5V	-
MIPI_STX_D3n	K1	6	2.5V	-
MIPI_STX_D2p	L2	6	2.5V	-
MIPI_STX_D2n	L1	6	2.5V	-
MIPI_STX_D1p	N2	6	2.5V	-
MIPI_STX_D1n	N1	6	2.5V	-
MIPI_STX_D0p	P2	6	2.5V	-
MIPI_STX_D0n	P1	6	2.5V	-
MIPI_STX_CLKp	M3	6	2.5V	-
MIPI_STX_CLKn	M1	6	2.5V	-
MIPI_RX_CLKp	L6	MIPI	1.2V	15
MIPI_RX_CLKn	M5	MIPI	1.2V	13
MIPI_RX_D0p	T2	MIPI	1.2V	3
MIPI_RX_D0n	T1	MIPI	1.2V	1
MIPI_RX_D1p	U2	MIPI	1.2V	9
MIPI_RX_D1n	U1	MIPI	1.2V	7
MIPI_RX_D2p	N4	MIPI	1.2V	21

Signal Name	FPGA Pin No.	BANK	I/O Level	J5 Socket Pin No.
MIPI_RX_D2n	N3	MIPI	1.2V	19
MIPI_RX_D3p	P4	MIPI	1.2V	27
MIPI_RX_D3n	P3	MIPI	1.2V	25
GPIO1	J1	6	2.5V	52
GPIO2	H5	7	2.5V	54
GPIO3	K6	7	2.5V	56
GPIO4	L7	7	2.5V	58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