DK-START-GW2AR18

User Guide

DBUG359-1.1E, 9/12/2019

Disclaimer

Revision History

Date	Version	Description
1/15/2019	1.0E	Initial version published.
9/12/2019	1.1E	One precaution added.

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1 About This Guide

1.1 Purpose

The DK-START-GW2AR18 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the hardware circuits functions, circuit, and pins distribution;
3. Precautions to be taken when using the development board;
4. Introduction to the use of the FPGA development software.

1.2 Supported Products

The information in the guide applies to GW1N2AR series of FPGA products: GW2AR-18.

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW2AR series of FPGA Products Data Sheet
2. GW2AR series of FPGA Products Package and Pinout
3. GW2AR-18 Pinout
4. Gowin FPGA Products Programming and Configuration User Guide
5. Gowin YunYuan Software User Guide

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
SIP	System in Package
SDRAM	Synchronous Dynamic RAM
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
TDM	Time Division Multiplexing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
EQ144	EQFP144

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

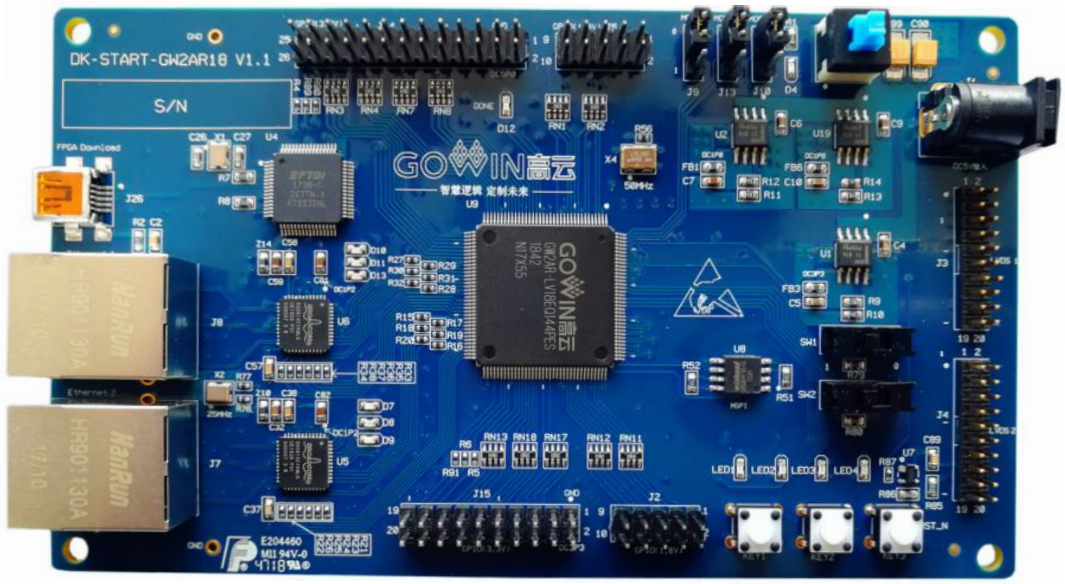
E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2 Development Board Description

2.1 Overview

Figure 2-1 DK-START-GW2AR18



DK-START-GW2AR18 adopts the GW2AR-18 device. 64Mbit PSRAM is embedded in this device. The GW2AR series of FPGA products are the first generation products of the Arora® family. They offer one form of SIP chip. The main difference between the GW2A series and the GW2AR series is that the GW2AR series integrates abundant memories. The GW2AR series also provides high-performance DSP resources, a high-speed LVDS interface, and abundant BSRAM resources. These embedded resources in combination with a streamlined FPGA architecture with 55nm process make the GW2AR series of FPGA products suitable for high-speed and low-cost applications.

The development board offers abundant external interfaces, including

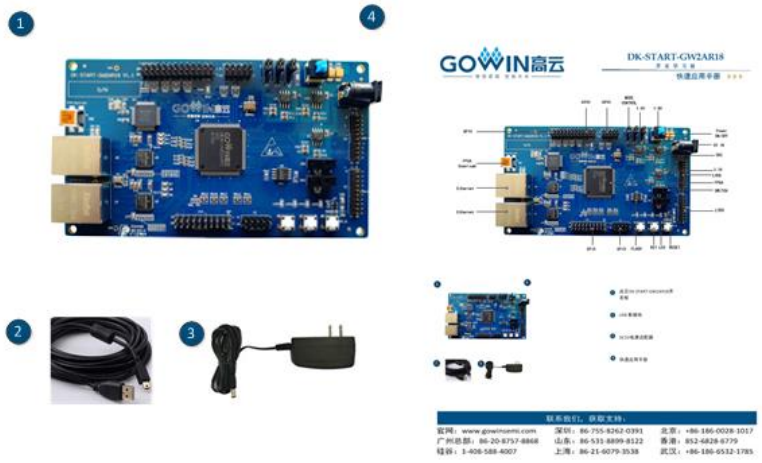
LVDS interfaces, GPIO interfaces, slide switches, key switches, LED, reset, clock resources, etc.

2.2 A Development Board Suite

A development board suite includes the following items:

- DK-START-GW2AR18
- USB cable
- Quick Start Guide

Figure 2-2 A Development Board Suite



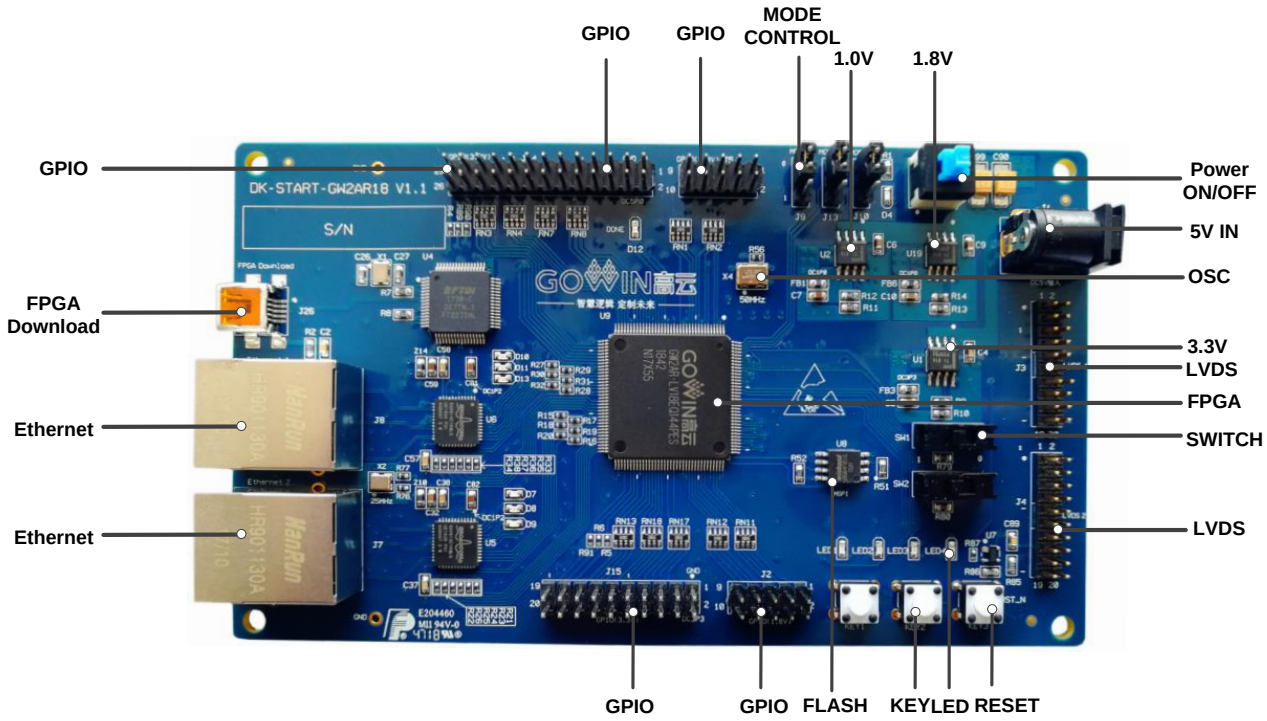
① DK-START-GW2AR18

② USB Cable

③ Quick Start Guide

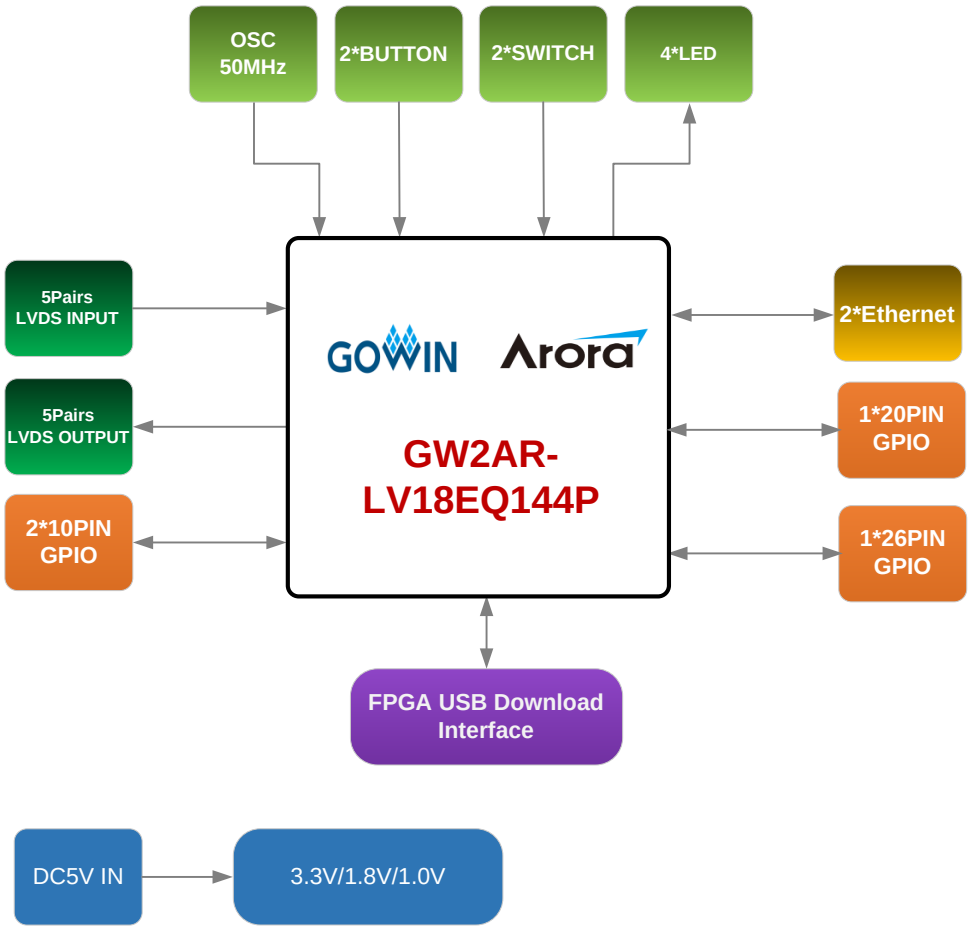
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Architecture

Figure 2-4 System Architecture



2.5 Features

The structure and features of the development board are as follows:

1. FPGA
- EQFP144 package
- Up to 120 user I/O
- Abundant LUT4 resources
- Multiple modes and capacities of B-SRAM

2. FPGA Configuration Mode
- JTAG
- MSPI

- Multi BOOT

3. Clock resource

50MHz Clock Crystal Oscillator

4. Key switch and slide switch

- One reset button
- Two key switches
- Two slide switches

5. LED

- One power indicator (green)
- One DONE indicator (green)
- Four LEDs (green)

6. Memory

64Mbit built-in PSRAM

7. LVDS

5 pairs of LVDS differential input; 5 pairs of LVDS differential output

8. GPIO

50 I/O expansion resources

9. Ethernet

2 Ethernet interfaces

10. LDO Power

Supports 3.3 V, 1.8V, and1.0V.

2.6 Development Board Specification

Table 2-1 Development Board Specification

No.	Item	Functions	Technical Conditions	Remarks
1	FPGA	Core chip	–	–
2	Download	Support an USB interface; Support JTAG, MSPI, and Multi BOOT	USB-JTAG module on board	–
3	Power Supply	3.3 V, 1.8V and 1.0 V output via LDO circuit	● Input power: 5V ● Provide power for FPGA, download circuit and other circuits via 5V–3.3 V circuit; ● Provide power for FPGA PSRAM via 5V–1.8V circuit; ● Provide power for FPGA via 5 V–1.0 V circuit.	–
4	Slide Switches	Available for testing	2	–
5	Key Switches	Available for testing	2	–
6	Reset button	Reset for FPGA	1	–
7	LED	Test indicator, DONE indicator, Power indicator	● Four Test indicators, green ● One DONE indicator, green ● One Power indicator, green	–
8	Crystal Oscillator	Provide 50MHz clock for FPGA	Package5032	–
9	Memory	Offers PSRAM	64Mbit built-in PSRAM	–
10	GPIO	I/O, convenient for user extension and test	50	–
11	LVDS	LVDS, used for testing	5 pairs of input, 5 pairs of output	–
12	Ethernet	For design use.	2 Ethernet interfaces	–
13	Protection	USB interface: ESD protection; Power interface: Inverse current and over current protection	● USB interface ESD protection: ±15kV non-contact discharge, ± 8kV contact discharge; ● Schottky diode is connected between positive and negative anodes of power	–

No.	Item	Functions	Technical Conditions	Remarks
			outlet; ● 2A self-recovery fuses are connected at power inlet	
14	Voltage	–	Input Voltage: 5V	–
15	Humidity	–	95%	–
16	Temperature	–	Operating range: –20°~70°	–

3 Development Board Circuit

3.1 FPGA Module

3.1.1 Overview

The resources of GW1N2AR series of FPGA products are set out in Table 3-1.

Table 3-1 GW2AR-18 FPGA Resources List

Device	GW2AR-18
LUT4	20,736
Flip-Flop (FF)	15,552
Shadow SRAM S-SRAM (bits)	41,472
Block SRAM B-SRAM (bits)	828K
B-SRAM quantity B-SRAM	46
PSRAM(bits)	64M
18 x 18 Multiplier	48
Maximum[1](PLLs+DLLs)	4+4
Total number of I/O banks	8
Max. user I/O[2]	140
Core voltage	1.0V

Note!

See *GW2AR series of FPGA Products Data Sheet* for further details.

3.1.2 I/O BANK Introduction

There are four I/O Banks in the GW2AR series of FPGA products, as shown in Figure 3-1.

Figure 3-1 GW2AR I/O Bank Distribution

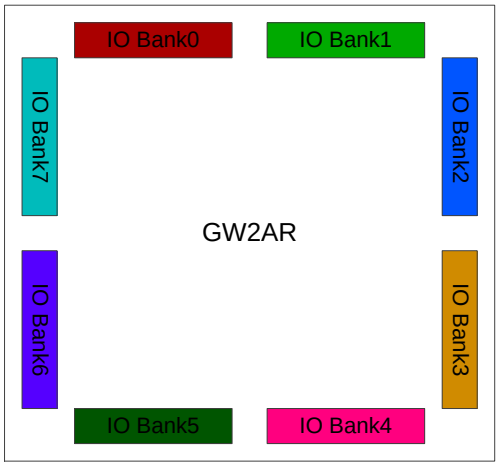


Figure 3-2 View of GW2AR-18 EQ144 Pins Distribution (Top View)

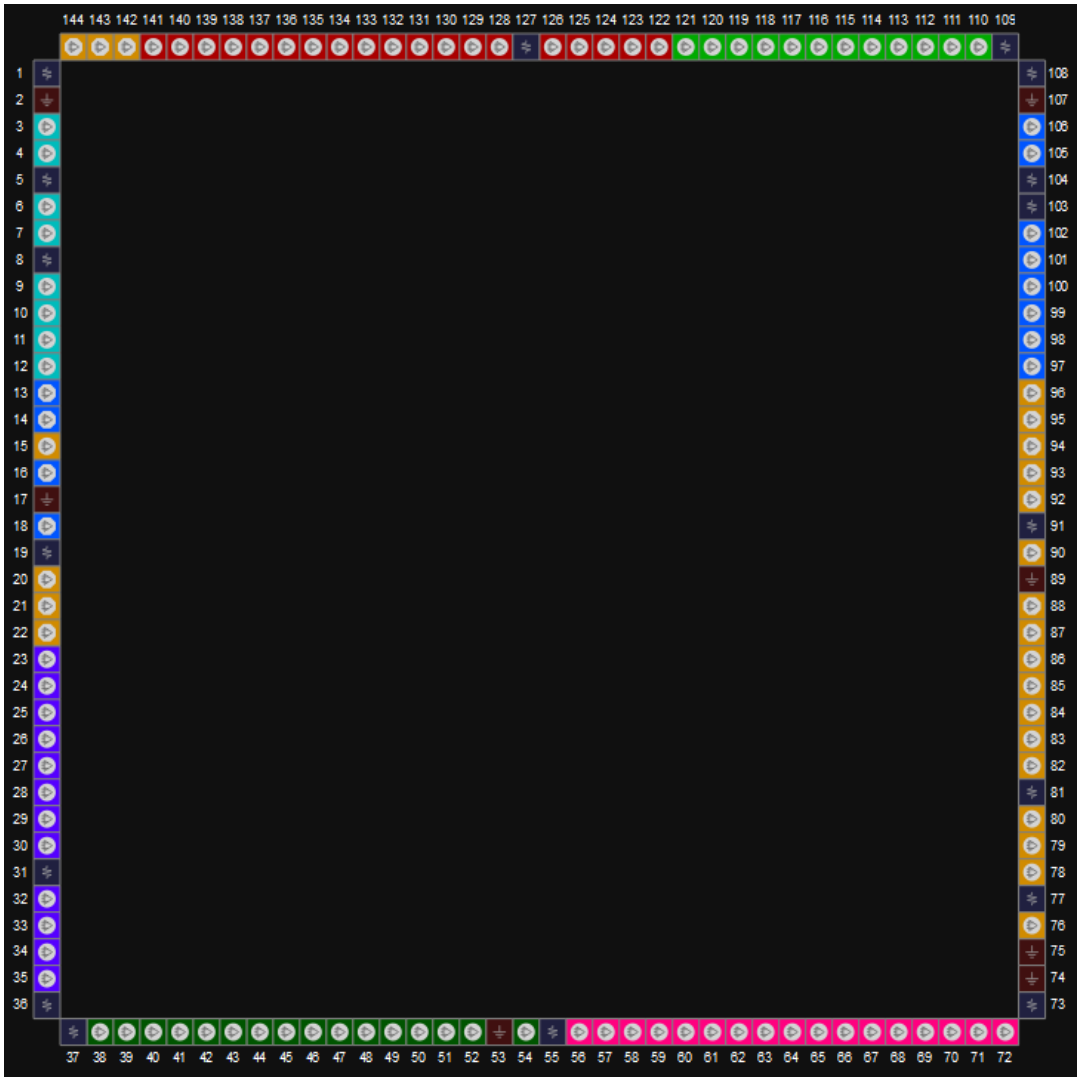


Table 3-2 FPGA I/O Pins Distribution

I/O BANK No.	Signals
I/O BANK0	Pins used for download mode selection LVDS differential input LED&Reset&Slide switch&Key switch GPIO
I/O BANK1	LVDS differential input LVDS differential output
I/O BANK2	JTAG GPIO
I/O BANK3	DONE&RECONFIG_N&READY MSPI GPIO
I/O BANK4	Ethernet
I/O BANK5	GPIO Ethernet

I/O BANK No.	Signals
I/O BANK6	GPIO
I/O BANK7	50MHz clock input GPIO

3.2 Download

3.2.1 Overview

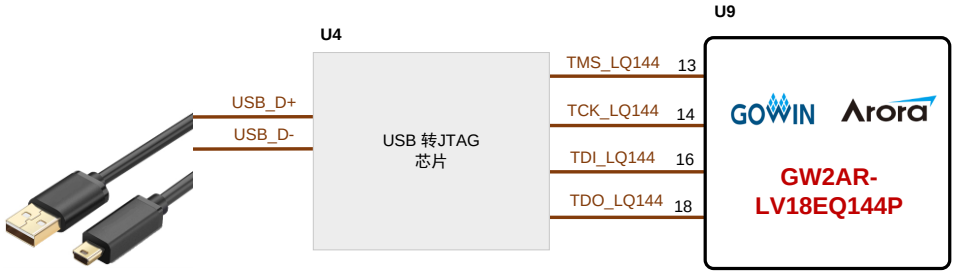
The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, or the external flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is power down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-3 Connection Diagram for FPGA USB Downloading



3.2.3 Download Flow

1. FPGA SRAM Download Mode:
   Plug the USB cable to the USB interface (J26) on the development board. Power on. Open the Programmer, select SRAM mode, and then select the bitstream file you required.
2. FPGA MSPI Download Mode:
   Plug the USB cable to the USB interface (J26) on the development board. Set J13 to "0", and set J9 and J10 to "1". Power on. Open the Programmer, select External Flash mode, and then select the bitstream file you required. Turn off the power after downloading. Set J13, J9, and J10 to "0", power on, and then the device will import the bitstream file to SRAM from the external Flash.

3.2.4 Pins Distribution

Table 3-3 FPGA Download and Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
TMS	13	2	JTAG Signal	1.8V
TCK	14	2	JTAG Signal	1.8V
TDI	16	2	JTAG Signal	1.8V
TDO	18	2	JTAG Signal	1.8V
MODE0	144	0	One Mode selection pin	3.3V
MODE1	142	0	One Mode selection pin	3.3V
MODE2	143	0	One Mode selection pin	3.3V
RECONFIG_N	20	3	RECONFIG_N	3.3V
DONE	21	3	One DONE indicator	3.3V
READY	22	3	READY	3.3V

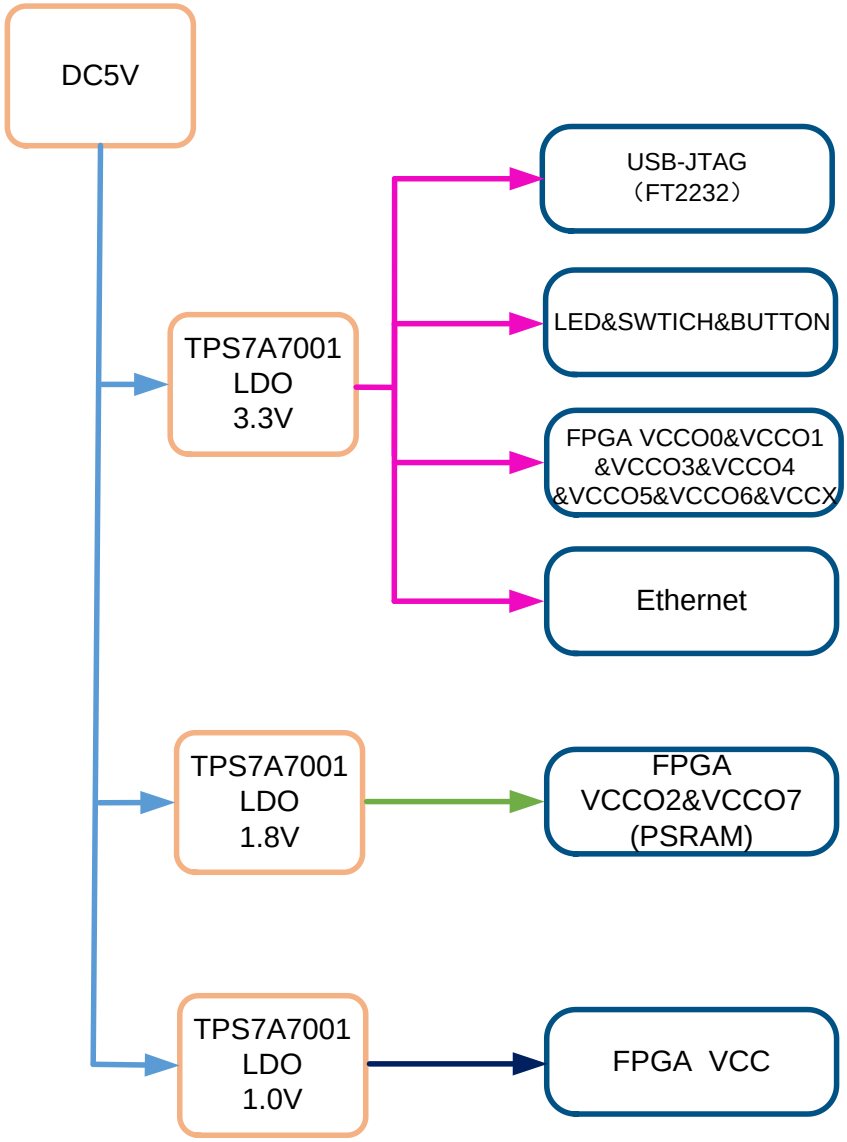
3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 1.8V and 1.0V, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-4 Power System Distribution



3.3.3 FPGA Power Pins Distribution

Table 3-4 FPGA Power Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
VCCO0	127	0	I/O Bank Power	3.3V
VCCO1	109	1	I/O Bank Power	3.3V
VCCO2	103	2	I/O Bank Power	1.8V

Signal Name	Pin No.	BANK	Description	I/O
VCCO3	77, 91	3	I/O Bank Power	3.3V
VCCO4	55	4	I/O Bank Power	3.3V
VCCO5	37	5	I/O Bank Power	3.3V
VCCO6	31	6	I/O Bank Power	3.3V
VCCO7	5, 19	7	I/O Bank Power	1.8V
VCCPLLL0	8	-	PLLL0 power	1.0V
VCCPLLR0	104	-	PLLR0 power	1.0V
VCCPLLR1	81	-	PLLR1 power	1.0V
VCCPLL1	36	-	PLLL1 power be internal short circuited.	1.0V
VCCX	31, 55	-	Auxiliary voltage The auxiliary voltage and VCCO4, VCCO6 are internal short circuited.	3.3V
VCC	1, 36, 73, 108	-	Core voltage	1.0V
VSS	2, 17, 53, 74, 89, 107	-	GND	-

3.4 Clock, Reset

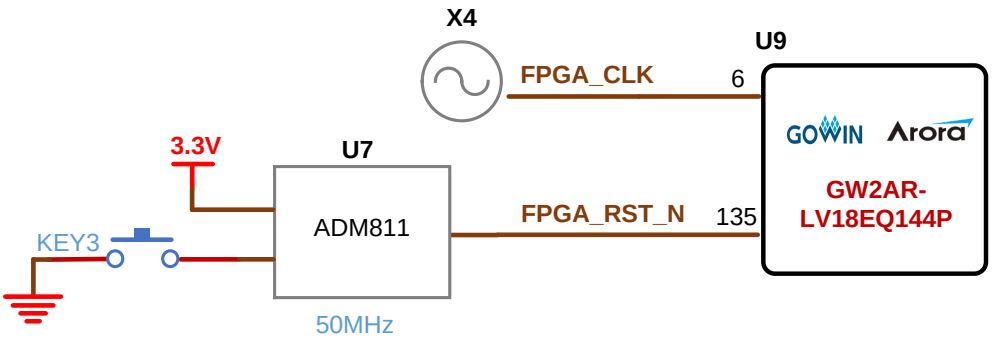
3.4.1 Overview

A 50MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

For easier debugging, one reset signal is added on the development board. It's low active.

3.4.2 Clock, Reset

Figure 3-5 Clock, Reset



3.4.3 Pins Distribution

Table 3-5 FPGA Clock and Reset Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
FPGA_CLK	6	7	50MHz crystal oscillator Input	3.3V
FPGA_RST_N	135	0	Reset signal, active low	1.8V

3.5 LED

3.5.1 Overview

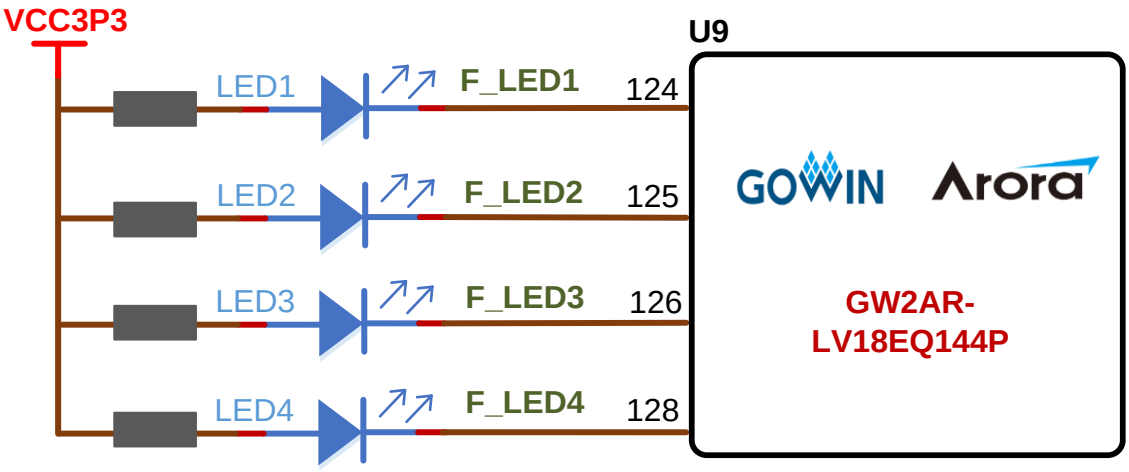
Four green LEDs are incorporated into the development board and are used to display the required status. In addition, two LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on;
- If the logic is high, LED is off.

3.5.2 LED Circuit

Figure 3-6 LED Circuit



3.5.3 Pins Distribution

Table 3-6 LED Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_LED1	124	0	LED1	3.3V
F_LED2	125	0	LED2	3.3V
F_LED3	126	0	LED3	3.3V
F_LED4	128	0	JESD 4	3.3V

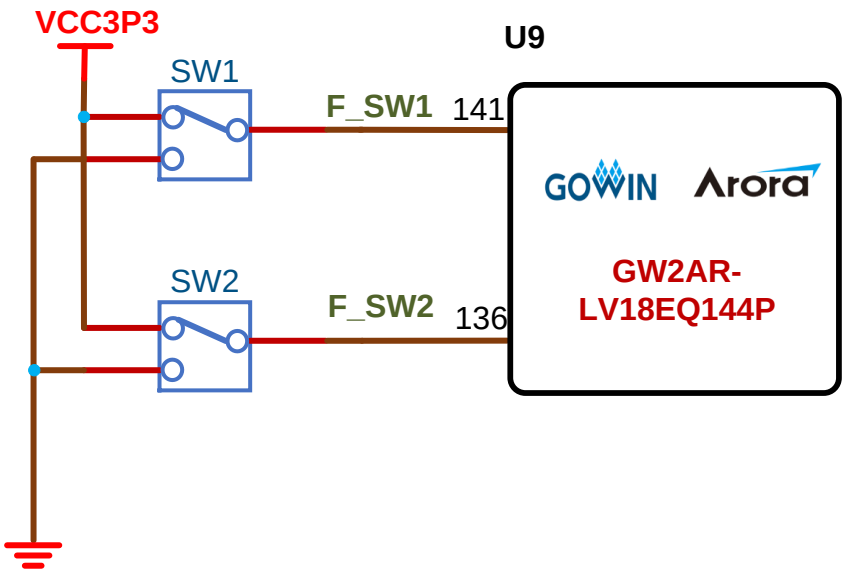
3.6 Switches

3.6.1 Overview

Two Slide switches are incorporated into the development board. These are used to input the 0/1 signal during testing.

3.6.2 Switch Circuit

Figure 3-7 Switch Circuit



3.6.3 Pins Distribution

Table 3-7 Clock Circuit Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_SW1	141	0	Slide Switch1	3.3V
F_SW2	136	0	Slide Switch2	3.3V

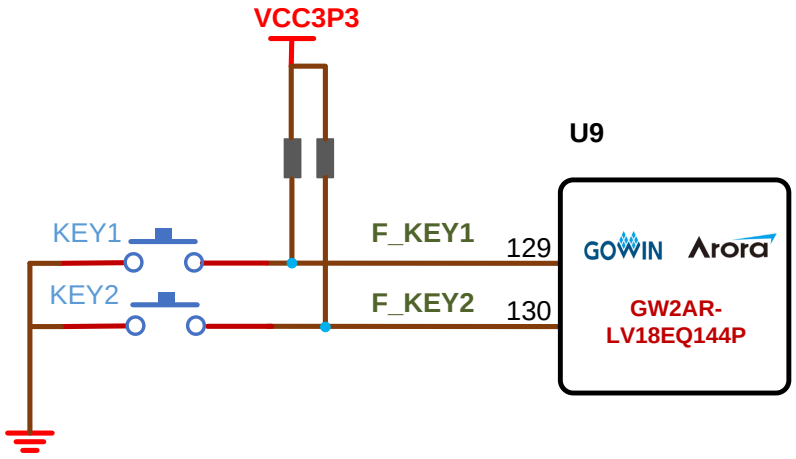
3.7 Key

3.7.1 Overview

Two key switches are embedded in the development board. Users can manually input the 0/1 signal to the corresponding FPGA pins for testing purposes. Press the key to input 0; Input 1 when the key is up.

3.7.2 Key Circuit

Figure 3-8 Key Circuit Diagram



3.7.3 Pins Distribution

Table 3-8 Key Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
F_KEY1	129	0	KEY1	3.3V
F_KEY2	130	0	KEY2	3.3V

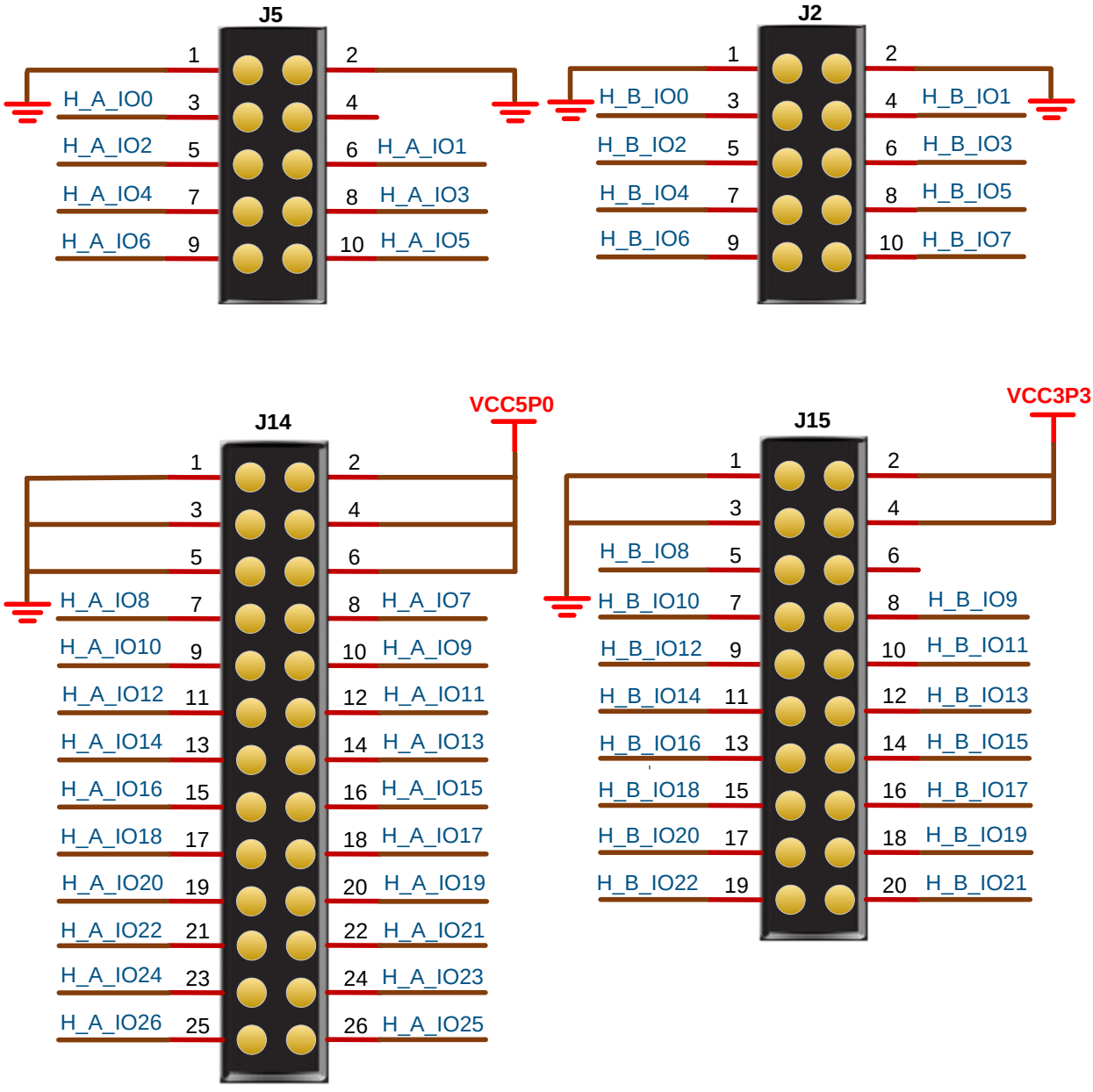
3.8 GPIO

3.8.1 Overview

Two 2.54mm DC3-10P sockets, one 2.54mm DC3-20P socket, and one 2.54mm DC3-26P socket are reserved on the development board for user function extension and testing purposes.

3.8.2 GPIO Circuit

Figure 3-9 GPIO Circuit



3.8.3 Pins Distribution

Table 3-9 J5 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
GND	-	1	-	GND	-
GND	-	2	-	GND	-
H_A_IO0	4	3	7	General I/O	1.8V
-	-	4	-	-	-
H_A_IO2	9	5	7	General I/O	1.8V
H_A_IO1	3	6	7	General I/O	1.8V
H_A_IO4	11	7	7	General I/O	1.8V
H_A_IO3	7	8	7	General I/O	1.8V
H_A_IO6	15	9	6	General I/O	3.3V
H_A_IO5	10	10	7	General I/O	1.8V

Table 3-10 J14 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
GND	-	1	-	GND	-
VCC5P0	-	2	-	5V Output	5V
GND		3	0	GND	-
VCC5P0		4	0	5V Output	5V
GND		5	0	GND	-
VCC5P0		6	0	5V Output	5V
H_A_IO8	24	7	6	General I/O	3.3V
H_A_IO7	12	8	7	General I/O	1.8V
H_A_IO10	26	9	6	General I/O	3.3V
H_A_IO9	23	10	6	General I/O	3.3V
H_A_IO12	28	11	6	General I/O	3.3V
H_A_IO11	25	12	6	General I/O	3.3V
H_A_IO14	30	13	6	General I/O	3.3V
H_A_IO13	27	14	6	General I/O	3.3V
H_A_IO16	33	15	6	General I/O	3.3V
H_A_IO15	29	16	6	General I/O	3.3V
H_A_IO18	35	17	6	General I/O	3.3V
H_A_IO17	32	18	6	General I/O	3.3V
H_A_IO20	39	19	5	General I/O	3.3V

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
H_A_IO19	34	20	6	General I/O	3.3V
H_A_IO22	41	21	5	General I/O	3.3V
H_A_IO21	38	22	5	General I/O	3.3V
H_A_IO24	43	23	5	General I/O	3.3V
H_A_IO23	40	24	5	General I/O	3.3V
H_A_IO26	44	25	5	General I/O	3.3V
H_A_IO25	42	26	5	General I/O	3.3V

Table 3-11 J2 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
GND	-	1	-	GND	-
GND	-	2	-	GND	-
H_B_IO0	105	3	2	General I/O	1.8V
H_B_IO1	106	4	2	General I/O	1.8V
H_B_IO2	101	5	2	General I/O	1.8V
H_B_IO3	102	6	2	General I/O	1.8V
H_B_IO4	99	7	2	General I/O	1.8V
H_B_IO5	100	8	2	General I/O	1.8V
H_B_IO6	97	9	2	General I/O	1.8V
H_B_IO7	98	10	2	General I/O	1.8V

Table 3-12 J15 GPIO Pins Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
GND	-	1	-	GND	-
VCC3P3	-	2	-	3.3V Output	3.3V
GND		3	-	GND	-
VCC3P3		4	-	3.3V Output	3.3V
H_B_IO8	122	5	0	General I/O	3.3V
-	-	6	-	-	-
H_B_IO10	90	7	3	General I/O	3.3V
H_B_IO9	123	8	0	General I/O	3.3V
H_B_IO12	87	9	3	General I/O	3.3V
H_B_IO11	92	10	3	General I/O	3.3V
H_B_IO14	85	11	3	General I/O	3.3V
H_B_IO13	88	12	3	General I/O	3.3V
H_B_IO16	83	13	3	General I/O	3.3V
H_B_IO15	86	14	3	General I/O	3.3V
H_B_IO18	80	15	3	General I/O	3.3V
H_B_IO17	84	16	3	General I/O	3.3V
H_B_IO20	78	17	3	General I/O	3.3V
H_B_IO19	82	18	3	General I/O	3.3V
H_B_IO22	76	19	3	General I/O	3.3V
H_B_IO21	79	20	3	General I/O	3.3V

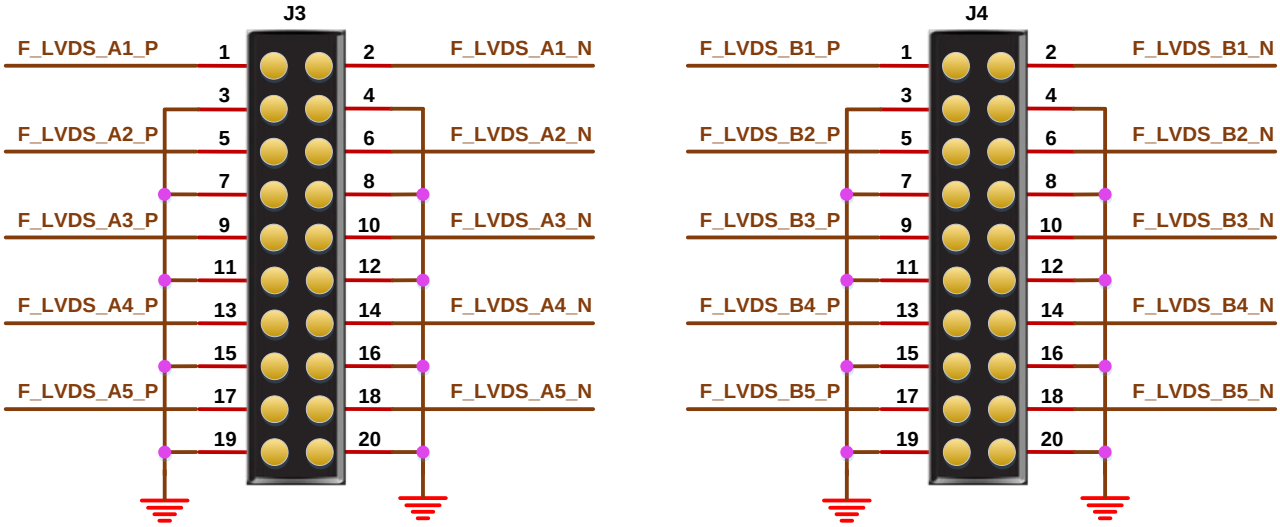
3.9 LVDS

3.9.1 Overview

Two 2.0 mm DC3-20P sockets are reserved on the development board for LVDS input/output testing and data communication.

3.9.2 LVDS Circuit

Figure 3-10 LVDS Circuit



3.9.3 Pins Distribution

Table 3-13 J3 FPGA Pin Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
F_LVDS_A1_P	140	1	0	A Channel 1+	3.3V
F_LVDS_A1_N	139	2	0	A Channel 1-	3.3V
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A2_P	138	5	0	A Channel 2+	3.3V
F_LVDS_A2_N	137	6	0	A Channel 2–	3.3V
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_A3_P	134	9	0	A Channel 3+	3.3V
F_LVDS_A3_N	133	10	0	A Channel 3–	3.3V
GND	-	11	-	-	

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
GND	-	12	-	-	
F_LVDS_A4_P	132	13	0	A Channel 4+	3.3V
F_LVDS_A4_N	131	14	0	A Channel 4–	3.3V
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_A5_P	121	17	1	A Channel 5+	3.3V
F_LVDS_A5_N	120	18	1	A Channel 5–	3.3V
GND	-	19	-	-	
GND	-	20	-	-	

Table 3-14 J4 FPGA Pin Distribution

Signal Name	Pin No.	Socket Pin No.	BANK	Description	I/O
F_LVDS_B1_P	119	1	1	B Channel 1	3.3V
F_LVDS_B1_N	118	2	1	B Channel 1–	3.3V
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B2_P	117	5	1	B Channel 2+	3.3V
F_LVDS_B2_N	116	6	1	B Channel 2–	3.3V
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_B3_P	115	9	1	B Channel 3+	3.3V
F_LVDS_B3_N	114	10	1	B Channel 3–	3.3V
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_B4_P	113	13	1	B Channel 4+	3.3V
F_LVDS_B4_N	112	14	1	B Channel 4–	3.3V
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_B5_P	110	17	1	B Channel 5+	3.3V
F_LVDS_B5_N	110	18	1	B Channel 5–	3.3V
GND	-	19	-	-	-
GND	-	20	-	-	-

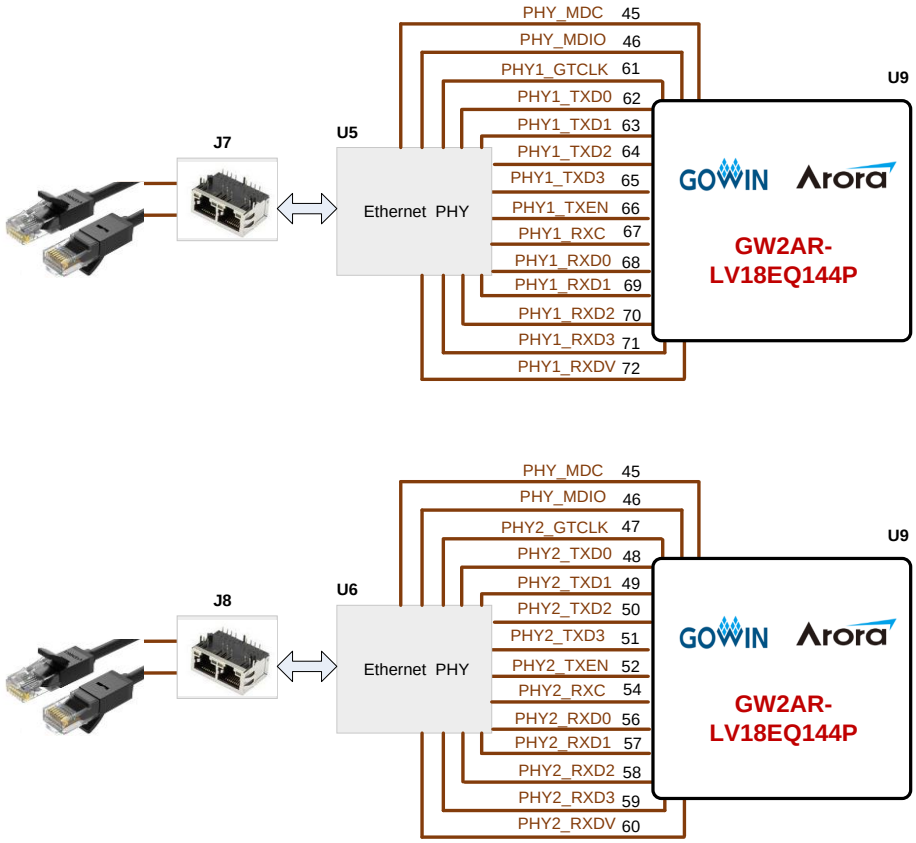
3.10 Ethernet

3.10.1 Overview

Two Ethernet interfaces are reserved for FPGA to communicate with PC or the other external devices.

3.10.2 Ethernet Circuit

Figure 3-11 Ethernet Download Connection



3.10.3 Pins Distribution

Table 3-15 Ethernet1 Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
PHY_MDC	45	5	PHY1 management interface clock	3.3V
PHY_MDIO	46	5	PHY1 management interface data	3.3V
PHY1_GTCLK	61	4	RGMII/MII transmitter clock	3.3V
PHY1_TXD0	62	4	RGMII/MII transmitter data	3.3V
PHY1_TXD1	63	4	RGMII/MII transmitter data	3.3V
PHY1_TXD2	64	4	RGMII/MII transmitter data	3.3V
PHY1_TXD3	65	4	RGMII/MII transmitter data	3.3V
PHY1_TXEN	66	4	RGMII/MII transmitting enable	3.3V
PHY1_RXC	67	4	RGMII/MII receive clock	3.3V
PHY1_RXD0	68	4	RGMII/MII receive data	3.3V
PHY1_RXD1	69	4	RGMII/MII receive data	3.3V
PHY1_RXD2	70	4	RGMII/MII receive data	3.3V
PHY1_RXD3	71	4	RGMII/MII receive data	3.3V
PHY1_RXDV	72	4	RGMII/MII receive enable	3.3V

Table 3-16 Ethernet2 Pins Distribution

Signal Name	Pin No.	BANK	Description	I/O
PHY_MDC	45	5	PHY2 management interface clock	3.3V
PHY_MDIO	46	5	PHY2 management interface data	3.3V
PHY2_GTCLK	47	5	RGMII/MII transmitter clock	3.3V
PHY2_TXD0	48	5	RGMII/MII transmitter data	3.3V
PHY2_TXD1	49	5	RGMII/MII transmitter data	3.3V
PHY2_TXD2	50	5	RGMII/MII transmitter data	3.3V
PHY2_TXD3	51	5	RGMII/MII transmitter data	3.3V
PHY2_TXEN	52	5	RGMII/MII transmitting enable	3.3V
PHY2_RXC	54	5	RGMII/MII receive clock	3.3V
PHY2_RXD0	56	4	RGMII/MII receive data	3.3V
PHY2_RXD1	57	4	RGMII/MII receive data	3.3V
PHY2_RXD2	58	4	RGMII/MII receive data	3.3V
PHY2_RXD3	59	4	RGMII/MII receive data	3.3V
PHY2_RXDV	60	4	RGMII/MII receive enable	3.3V

4 Precautions

Precautions to be taken when using the development board:

1. Handle with care and pay attention to electrostatic protection;
2. When you program the external FLASH, please refer to the MODE value in *Gowin FPGA products programming and configuration Guide*;
3. When the LVDS differential signal is used as input, the built-in 100Ω terminating resistor needs to be enabled.

5 Gowin YunYuan Software

Please refer to *Gowin Software User Guide* for details.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