Surface Mount Dual Matched MMIC Amplifier MGVA-82+

50 Ω DC to 5.2 GHz

The Big Deal

- Gain, 14.1 dB typ. at 2 GHz
- Dual matched amplifier for push-pull & balanced amplifiers
- High dynamic range

Product Overview

MGVA-82+ (RoHS compliant) is an advanced wideband amplifier fabricated using InGaP HBT technology and offers high dynamic range over a broad frequency range. In addition, the MGVA-82+ has good input and output return loss over a broad frequency range without the need for external matching components. Lead finish is Matte-Tin and is enclosed in a 3.5 x 2.5 mm, 16-lead MCLP package for good thermal performance.

Feature	Advantages
Broadband	Covers many communication bands including cellular, cable TV, PCS, SATCOM, WiMAX, and more.
Excellent Gain Flatness: ±0.6 dB over 0.05-2GHz	Requires no gain compensation in most wideband applications.
Matched pair for use in high IP3 and IP2 amplifiers. Gain match: \pm 0.2 dB typ. Phase match: \pm 3° typ. to 3 GHz	Enables it to be used in push-pull amplifiers resulting in outstanding IP2.
High IP3, up to 41 dBm	Ideal for suppressing unwanted intermodulation in the presence of multiple carriers, now common in many communication systems.
High P1dB: Up to 17.6 dBm	High P1dB enables the amplifier to operate in linear region in the presence of strong interfering signals.
Medium Noise Figure: 6.7-7.7 dB typ.	Together with High OIP3/P1dB, results in high dynamic range

Key Features



CASE STYLE: JV2579

Surface Mount Dual Matched MMIC Amplifier

DC - 5.2GHz

Product Features

- Two matched amplifiers in one package
- High IP3, +36 dBm at 2 GHz
- High IP2, +44 dBm at 2 GHz in push-pull configuration
- Gain, 14.1 dB typ at 2 GHz
- Excellent Gain flatness, ±0.6 dB (0.05-2 GHz)
- P1dB, +20 dBm typ at 2 GHz

Typical Applications

- SATCOM
- CATV
- FTTH
- Optical networks
- Base station infrastructure
- Balanced amplifiers

General Description



CASE STYLE: JV2579

+RoHS Compliant The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

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simplified schematic (each of A1, A2) and pad description



Function	Pad Number	Description
RF-IN1	2	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation. (see Characterization Test Circuit, Fig 1.)
RF-OUT1 & DC-IN	12	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in "Characterization Test Circuit", Fig 1
RF-IN2	4	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation. (see Characterization Test Circuit, Fig 1.)
RF-OUT2 & DC-IN	10	RF output and bias pin. DC voltage is present on this pin; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in "Characterization Test Circuit", Fig 1
GND	1,3,5,6,8,9,11,13,1416 & paddle	Connections to ground. Use via holes as shown in "Suggested Layout for PCB Design" to reduce ground path inductance for best performance.
N/C	7,15	No Connection

* Enhancement mode pseudomorphic High Electron Mobility Transistor.



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Electrical Specifications¹ at 25°C, Zo=50 Ω and Device Voltage 5V, unless noted (Specifications (other than Matching or where defined as push-pull) are for each of the two matched amplifiers in the package)

Parameter		Condition (MHz)	Min.	Тур.	Max.	Units
requency Range			DC		5.2	GHz
Gain		50	13.8	15.3	16.8	dB
		1000		14.9	_	
		2000	12.2	14.1	15.5	
		3000	_	13.2	_	
		4000	9.8	12.1	13.3	
		5200	_	9.9		
Gain Flatness		50 - 2000		±0.6	_	dB
Input Return Loss		50		32.4		dB
input neturn 2055		1000		23.5		UD UD
		2000		17.7		
		3000		15.4		
		4000		13.0		
		5200		9.4		
Output Return Loss		50		16.2		dB
		1000		14.7		
		2000		11.7		
		3000		10.5		
		4000		9.1		
		5200		6.9		
Output power @ 1 dB Comp	ression	50		20.2		dBm
		1000		20.3		
		2000		20.2		
		3000		19.8		
		4000		19.5		
		5200		18.3		
Output IP3		50		41		dBm
Output IF3			_		_	UDIII
		1000		38	_	
		2000	33	36	-	
		3000	-	35	-	
		4000	-	33	-	
		5200		32	-	
Output IP2		50	-	55	-	dBm
		1000		55	-	
		2000	40	44	-	
		3000		41	-	
		4000	_	38	_	
		5200	_	37	_	
Noise Figure		50		6.7		dB
		1000		6.8		
		2000		7.0		
		3000		7.0		
		4000		7.3		
		5200		7.7		
		50		0.1		dB
		1000		0.1		
	Amplitude Unbalance	2000		0.1		
		3000		0.2		
		4000		0.2		
		5200		0.3		
Matching between A1, A2		50		0.1		deg
		1000		1.1		
		2000		1.9		
	Phase Unbalance	3000		3.4		
		4000		6.7		
		5200		9.4		
Device operating voltage			4.8	5.0	5.2	V
Device operating current			_	100	120	mA
Device current variation	vs. temperature ⁴			70.5		
	vs. temperature ⁴			70.5 0.038		μΑ/°C mA/m\

Measured on Mini-Circuits Test Board TB-1002+, see characterization circuit, Fig 1.
 Ojc= (Junction Temperature – Ground Pad Temperature) / (Voltage X sum of current in A1 & A2)



Absolute Maximum Ratings for each Amplifier⁽³⁾

Parameter	Ratings
Operating Temperature ⁴	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Operating Current at 5V	160 mA
Power Dissipation	0.84 W
Input Power (CW)	20 dBm
DC Voltage (pads 10, 12)	5.8V

(3) Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.
 (4) Defined with reference to ground pad temperature.

Characterization Test Circuit

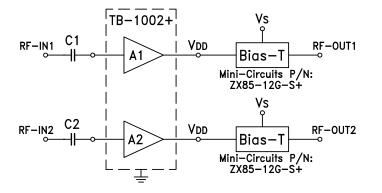


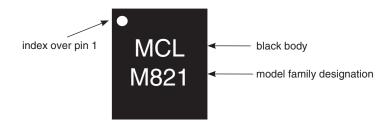
Fig 1. Block Diagram of Test Circuit used for characterization. (DUT tested in Mini-Circuits Test board TB-1002+). Gain, Return loss, Output Power at 1dB compression (P1 dB), output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X micro-wave network analyzer.

Conditions:

1. Gain and Return loss: Pin= -25dBm

2. Output IP3 (OIP3) & Output IP2 (OIP2): Two tones, spaced 1MHz apart, 0 dBm/tone at output. Note: C1&C2 are PNA built-in DC Blocks.

Product Marking



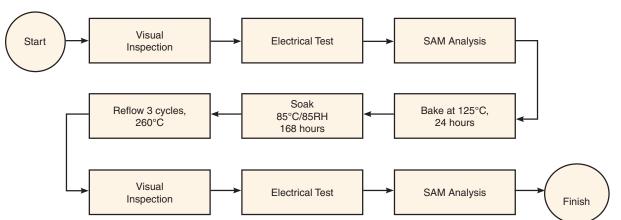
Marking may contain other features or characters for internal lot control



Additional Detailed Technical Information additional information is available on our dash board. To access this information <u>click here</u>			
	Data Table		
Performance Data	Swept Graphs		
	S-Parameter (S4P Files) Data Set (.zip file)		
Case Style	JV2579 Plastic package, exposed paddle lead finish: Matte-Tin plate		
Tape & Reel	F104		
Standard quantities available on reel	7" reels with 2K devices		
Suggested Layout for PCB Design	PL-582		
Evaluation Board	TB-1002+		
Environmental Ratings	ENV08T2		

ESD Rating

Human Body Model (HBM): Class 1C (1000 to <2000V) in accordance with ANSI/ESD STM 5.1 - 2001** ** Tested as a single ended amplitier in SOT-89 pacakge.



MSL Test Flow Chart

Additional Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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