Key Design Features

- Synthesizable, technology independent VHDL Core
- 16-bit signed input/output data samples[1]
- Digital oscillator with > 100 dB SFDR
- Digital oscillator phase resolution of $2\pi/2^{16}$
- Digital oscillator frequency resolution of $Fs/2^{32}$
- Integrated FIR decimation filter with configurable decimation factors from 0 to 2^N
- Highly optimized design requiring only 12 multipliers per decimate-by-2 stage
- Each decimate-by-2 filter stage has 80 dB of stop-band attenuation[2]
- Typical FPGA sample rates of up to 250 MHz[3]

Applications

- Digital I/Q Demodulators
- Compatible with any digital modulation scheme - e.g. QPSK, BPSK, QAM, WiMAX, WCDMA, COFDM etc.
- Conversion of IF signals to baseband frequencies for subsequent processing

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Sample clock (F_S)	rising edge
reset	in	Asynchronous reset	low
en	in	Input clock enable (rate F_S)	high
en_out	out	Output clock enable (rate F_S/N)	high
phase_inc [31:0]	in	Phase increment as an unsigned 32-bit number (controls osc frequency)	data
i_in [15:0]	in	Complex input (Real part) as 16-bit signed (rate F_S)	data
q_in [15:0]	in	Complex input (Imag part) as 16-bit signed (rate F_S)	data
i_out [15:0]	out	Complex output (Real part) as 16-bit signed (rate F_S/N)	data
q_out [15:0]	out	Complex output (Imag part) as 16-bit signed (rate F_S/N)	data

1 Data sample width may be modified on request
2 Filter characteristic may be modified on request
3 Xilinx Virtex 6 FPGA used as a benchmark

Block Diagram

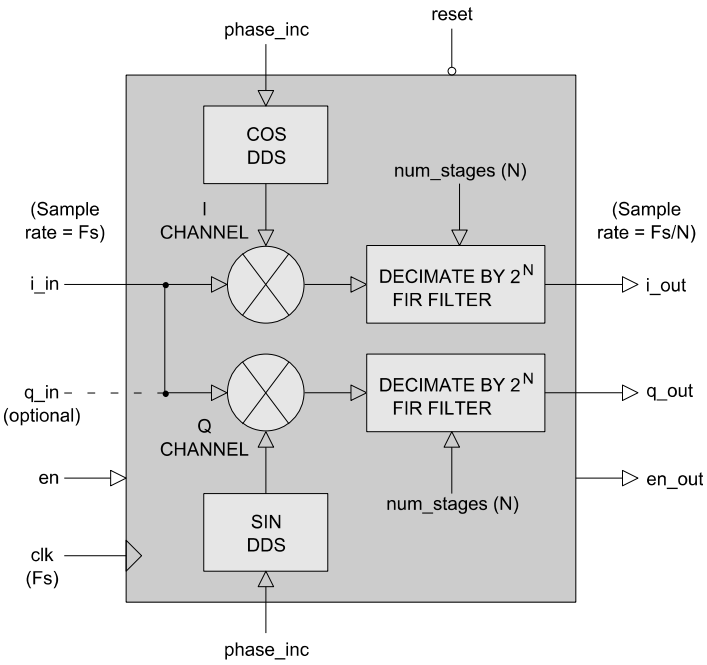

Figure 1: DDC simplified architecture

Generic Parameters

Generic name	*Description*	*Type*	*Valid range*
num_stages	Number of decimate-by-2 stages	integer	≥ 0
dithering	Enable phase dither	boolean	TRUE/FALSE
lutsize	16/12-bit LUT select	integer	16 or 12
seed	Seed for random number generator	std_logic vector	0 < seed < 2^{32}

General Description

DDC_DEC (Figure 1) is a complex-valued digital down-converter with a configurable number of decimation stages. The design is ideal for high sample-rate applications and permits a digital input signal to be mixed-down and re-sampled at a lower data rate. The DDC is suitable for the down-conversion of any digitally modulated signal to baseband – an essential step before digital processing.

The DDC features a high-precision 16-bit DDS oscillator for the digital mixing stage. This oscillator is fully programmable and offers excellent phase and frequency resolution. The digital mixing stage is a complex multiplier that allows the mixing of both real and imaginary (I/Q) inputs. If only real inputs are required, then the imaginary input (*q_in*) should be tied low.

The output decimation stage features a configurable decimate-by-2^N poly-phase filter for both I and Q channels. Each filter stage is highly optimized to use only 12 multipliers while still achieving 80 dB of stop-band attenuation.

The design features two clock-enable signals. The signal *en* is the global clock-enable and may be used to enable/disable sampling for the whole circuit. The output clock-enable signal *en_out* is only asserted when the decimated output samples are active. For instance, when decimating by a factor of 2, then this signal will have a 50% duty cycle. When decimating by a factor of 4 it will have a 25% duty cycle and so on.

Complex digital mixer

The digital mixing process performs a complex multiplication between the input samples *i_in* and *q_in* and the samples from the internal DDS modules. For any given frequency component in the input signal, the frequency component of the output signal has two components F_{out1} and F_{out2} given by the following relationship:

$$F_{out1} = F_1 - F_2 \quad , \quad F_{out2} = F_1 + F_2$$

F_1 is the frequency component of the input signal and F_2 is the oscillator frequency. It can be seen that by choosing a suitable oscillator frequency, then the signal of interest may be mixed-down to baseband so that the centre frequency is positioned at 0Hz. Normally the higher frequency mixer product (F_{out2}) is unwanted and will be attenuated by the decimation filter output stages.

Figure 2. below shows the basic mixing principal in which a generic input signal is shifted to baseband using a 20MHz oscillator frequency.

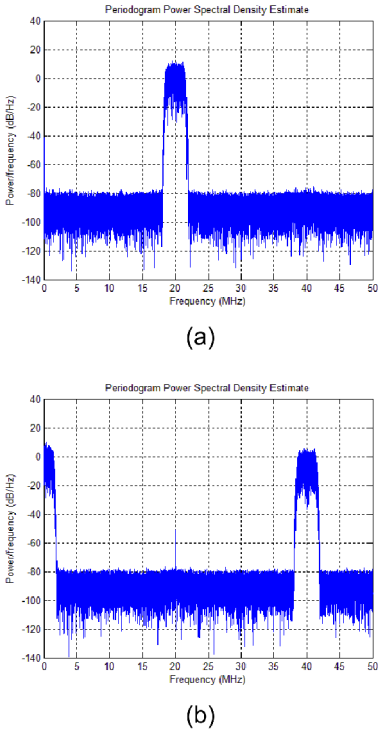

Figure 2: Mix-down of a 4MHz B/W signal to baseband. (a) Source signal, (b) Baseband signal after mixing (decimation filter disabled)

Digital oscillator (DDS)

The frequency of the DDS output waveform is controlled by the phase increment (*phase_inc*) on a clock-by-clock basis. The phase increment may be calculated using the formula:

$$\Phi_{inc} = \left(F_{out} * 2^{32}\right) / F_s + 0.5$$

F_{out} is the desired oscillator frequency and F_S is the system sampling frequency. Note that the phase increment must be adjusted to the nearest *integer* value. The minimum and maximum frequencies the oscillator can generate are given by the following formulas:

$$F_{min} = F_s / 2^{32} \quad , \quad F_{max} < F_s / 2$$

The process of phase quantization introduces noise on the phase signal and it produces unwanted spurious spectral components in the DDS output signal (referred to as *spurs*). The difference between the carrier level and the maximum level of spurs is called the *Spurious Free Dynamic Range* (SFDR). By setting the generic parameter *dithering* to *true*, then the incidence and magnitude of these spurs can be reduced significantly. The dithering function uses a random number generator with the starting *seed* specified in the generic parameter.

Decimation filter

The decimation filter allows the output from the mixer to be decimated by any power of 2. Each decimate-by-2 stage has a magnitude response as shown in Figure 3. below.

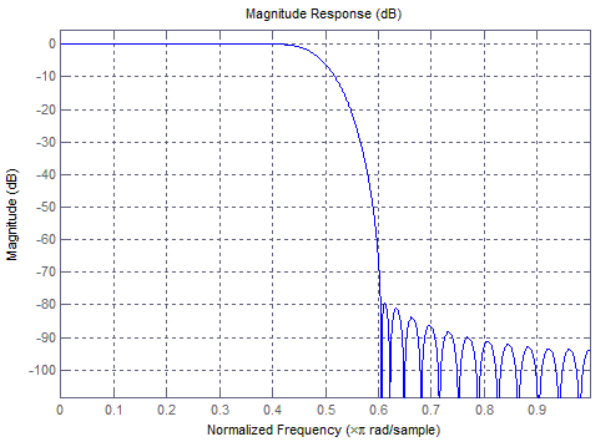

Figure 3: Decimation filter magnitude response for a single decimate-by-2 stage

The number of decimate-by-2 stages is specified by the generic parameter *num_stages*. For instance, setting this parameter to 2 will decimate the output samples by a factor of 4. Setting the parameter to 0 will eliminate all decimation and will output the signals directly from the digital mixer. Figure 4. demonstrates the result of mixing and decimating a generic 4MHz wideband signal by various stages.

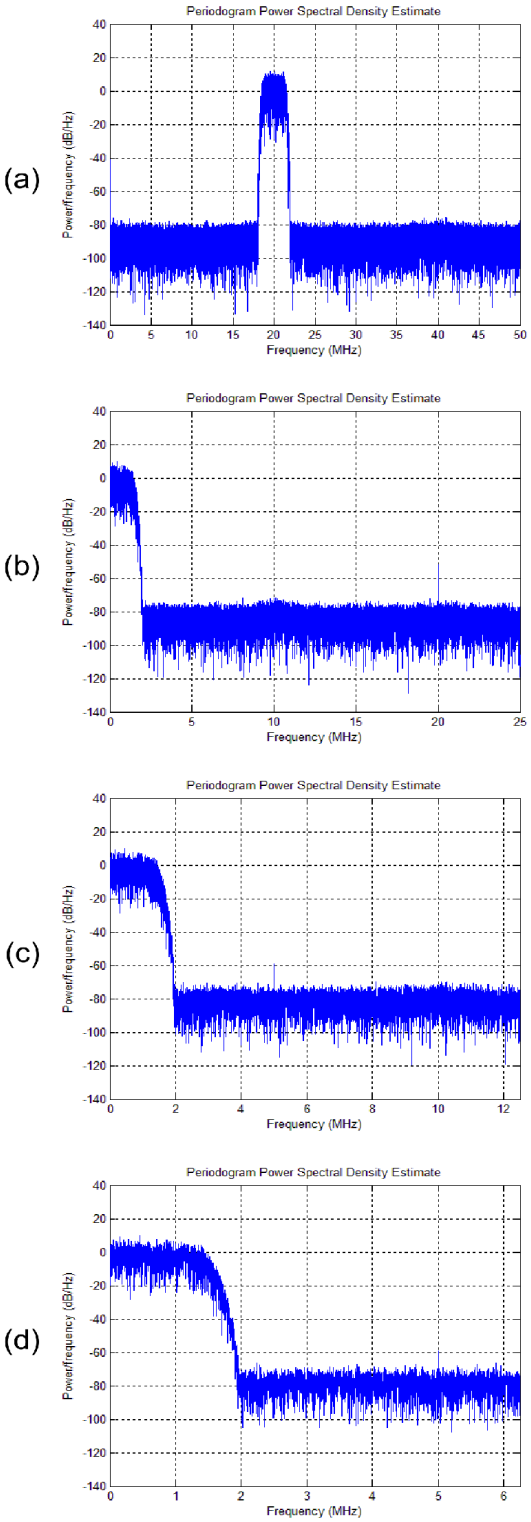

Figure 4: Digital down-conversion of a generic signal to baseband. (a) Source signal, (b) Decimate by 2, (c) Decimate by 4, (d) Decimate by 8

Functional Timing

The DDC generates output samples depending on the decimation factor. Figure 5. below, shows the timing of the input and output samples for a decimation by 2. Note that the output samples are valid on the rising-edge of *clk* when *en_out* is high. In this case, for a down-sample by 2 then the output clock-enable has a 50% duty cycle.

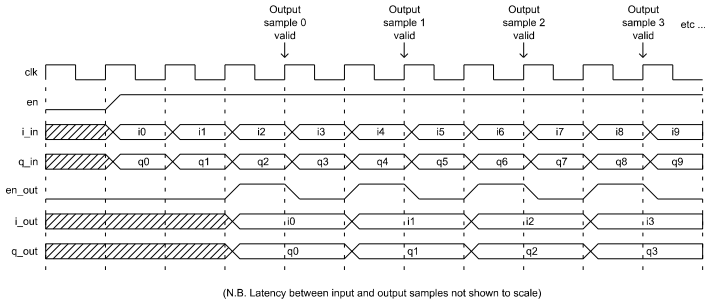

Figure 5: Timing waveform - decimation by 2

Figure 6. shows a similar picture, but this time for a decimation by 4. in this case, the output samples are valid every 4th clock cycle. Likewise, successive decimation factors of 8, 16, 32, etc. have similar timing waveforms with the *en_out* signal being asserted every 8th, 16th and 32nd clock cycle respectively.

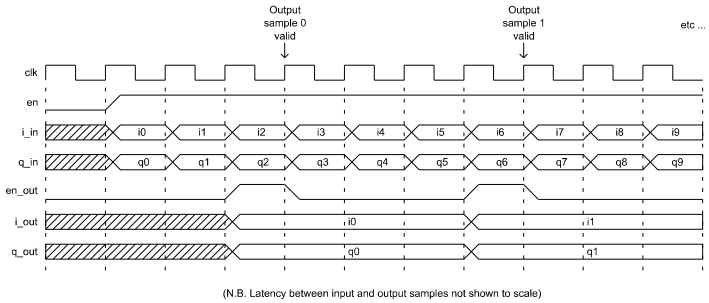

Figure 6: Timing waveform – decimation by 4

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
fir_dec_pack.vhd	Package containing decimation filter parameters
fir_dec_mad.vhd	Multiply-add block
fir_dec_mad_centre.vhd	Multiply-add block - centre tap
fir_dec_mad_zero.vhd	Multiply-add block - zero coeffs
fir_dec_rnd.vhd	Filter rounding block
fir_dec_sat_vhd	Filter saturation block
fir_dec_s0.vhd	Filter polyphase section 0
fir_dec_s1.vhd	Filter polyphase section 1
fir_dec.vhd	Decimate-by-2 filter
fir_dec_n.vhd	Top-level component
sincos_lut.vhd	SIN/COS look-up table
dds.vhd	DDS oscillator
ddc.vhd	Digital down-converter mixer
ddc_file_reader.vhd	Text file reader for I/Q input samples
ddc_dec.vhd	Top-level component
ddc_dec_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is the same as that outlined in the source file description above.

The VHDL testbench instantiates the DDC_DEC component and the user may modify the phase increment and generic parameters accordingly. In the test provided, the sample-frequency is set to 100MHz with an oscillator frequency of 20 MHz. The decimation factor is set to '2'. The input samples for the test are provided in the file 'ddc_stim.txt'. These samples are for a generic signal of 4MHz bandwidth and a centre frequency of 20MHz as per Figure 4(a).

The simulation must be run for at least 10 ms during which time the DDC will output the I and Q samples to a file called 'ddc_out.txt'. The power spectral density of the output samples should correspond to that of Figure 4(b).[4]

4 Matlab® scripts to generate power-spectral density plots are available on request. Please contact Zipcores..

Synthesis

The files required for synthesis and the design hierarchy is shown below:

- ddc_dec.vhd
  - ddc.vhd
    - dds.vhd
      - sincos_lut.vhd
  - fir_dec_pack.vhd
  - fir_dec_n.vhd
    - fir_dec.vhd
      - fir_dec_s0.vhd
      - fir_dec_s1.vhd
        - fir_dec_mad.vhd
        - fir_dec_mad_centre.vhd
        - fir_dec_mad_zero.vhd
      - fir_dec_rnd.vhd
      - fir_dec_sat_vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx® Virtex 6 and Spartan 6 FPGA devices. Synthesis results for other FPGAs and technologies can be provided on request.

Generally, for each decimate-by-2 stage an extra 24 H/W multipliers are added to the design - 12 for each I/Q channel.

Setting the lutsize to 12-bits will result in a much smaller LUT implementation and will greatly reduce the internal RAM resources required. Likewise, the implementation will be smaller if the dithering function is disabled.

Trial synthesis results are shown with the generic parameters set to: num_stages = 1, lutsize = 12, dithering = true, seed = 0xffd45101.

Resource usage is specified after Place and Route.

VIRTEX 6

Resource type	Quantity used
Slice register	1153
Slice LUT	1103
Block RAM	1
DSP48	32
Occupied slices	340
Clock frequency (approx)	250 MHz

SPARTAN 6

Resource type	Quantity used
Slice register	745
Slice LUT	904
Block RAM	2
DSP48	32
Occupied slices	314
Clock frequency (approx)	150 MHz

Revision History

Revision	*Change description*	*Date*
1.0	Initial revision	22/05/2008
1.1	Modified key design features	15/09/2009
2.0	Major revision. Digital mixer and decimation filter now combined in one top-level module	22/07/2011
2.1	Added 12-bit LUT option. Updated synthesis results for Xilinx® 6 series FPGAs	08/06/2012

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