Key Design Features

- Synthesizable, technology independent VHDL IP Core
- Conversion of pixels between 4:4:4 and 4:2:2 YCbCr formats
- Supports 10-bit Luma and Chroma samples
- Fully pipelined architecture with simple flow control
- Features VSYNC and HSYNC sideband flags to keep track of video frame and line boundaries
- Output 1 x pixel per clock
- Small implementation size
- Support for 400 MHz+ operation on basic FPGA devices

Applications

- Digital video and image processing
- Interfacing between different video processing and video transceiver ICs that use different colour formats

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Synchronous clock	rising edge
reset	in	Asynchronous reset	low
pixin_y [9:0]	in	Luma Component	data
pixin_cb [9:0]	in	Chroma (Blue) component	data
pixin_cr [9:0]	in	Chroma (Red) component	data
pixin_c [9:0]	in	Multiplexed Chroma value (4:2:2 formats)	data
pixin_vsync	in	Vertical sync flag in	high
pixin_hsync	in	Horizontal sync flag in	high
pixin_val	in	Input pixel valid	high
pixin_rdy	out	Input pixel ready	high
pixout_y [9:0]	out	Luma Component	data
pixout_cb [9:0]	out	Chroma (Blue) component	data
pixout_cr [9:0]	out	Chroma (Red) component	data
pixout_c [9:0]	out	Multiplexed Chroma value (4:2:2 formats)	data
pixout_vsync	out	Vertical sync flag out	high
pixout_hsync	out	Horizontal sync flag out	high
pixout_val	out	Output pixel valid	high
pixout_rdy	in	Output pixel ready	high

Block Diagram

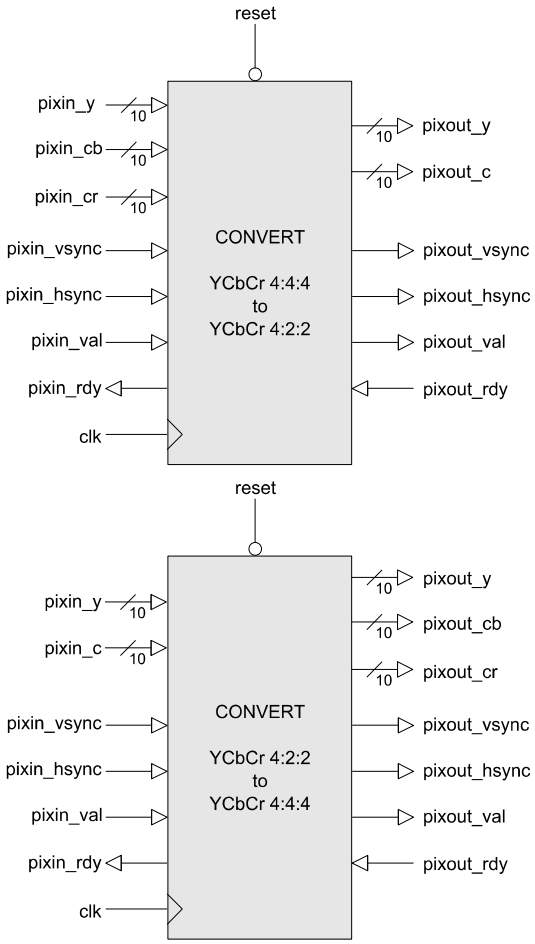

Figure 1: Chroma resampler architecture

General Description

The CONV_YC IP Core (Figure 1) is a fully pipelined chroma resampler that converts pixels between 4:4:4 and 4:2:2 formats in the YCbCr colour space. In total, the IP Core package contains two distinct modules – one module that converts from 4:4:4 to 4:2:2 and the other that performs the reciprocal operation from 4:2:2 to 4:4:4.

Pixels flow into the design in accordance with the valid ready pipeline protocol[1]. Input pixels and syncs are sampled on the rising edge of *clk* when *pixin_val* and *pixin_rdy* are both high. At the output interface, pixels and syncs are sampled on a the rising edge of *clk* when *pixout_val and pixout_rdy* are high. The input and output sync signals are coincident with the first pixel of a frame and the first pixel of a line. These are useful to identify the video frame and line boundaries. The *pixin_hsync* signal is also used to ensure that pixels are aligned correctly at the converter inputs.

Note that if no flow control is required in the design and the output interface can always accept pixels, then the *pixout_rdy* signal may be tied high. Likewise, the *pixin_rdy* flag may be ignored in this case.

1 See Zipcores application note: app_note_zc001.pdf for more examples of how to use the valid-ready pipeline protocol

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