Hardware User Guide

Zipcores FMC-BRK Mezzanine Card

ZIP-FMC-BRK Rev. A.1
March 2023

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Overview

Introduction

The Zipcores FMC-BRK Mezzanine card is a versatile FMC breakout-board and prototyping platform that conforms to the ANSI/VITA 57.1 FMC™ mezzanine standard. The card is compatible with a wide range of base-boards and FMC-compliant systems. Examples include evaluation boards from Xilinx®, Intel®, Avnet® and Digilent®. The card provides passive connectivity to all 160 signals on the FMC (LPC) connector via 4 x standard 0.100" pitch (2.54 mm) headers. This includes 34 x differential LVDS pairs (LA00:33) or 68 x single-ended signals. The differential pairs are balanced for track length and impedance-matched for 100Ω LVDS termination. The ground pins of the FMC are also connected to an independent ground plane to offer the best possible signal integrity and noise immunity.

The card is ideal for the development high-speed LVDS and other high-speed differential interfaces such as those required in displays, cameras, image sensors, ADCs, DACs and general purpose serial connectivity. The FMC card also provides access to the 2 x Gigabit Transceiver Pairs (GTP), GTP clock, 2 x user clock pairs, I^2C, JTAG, state flags, power supplies and ground pins. As well as breaking out all the FMC pins, the card also provides easy access to the FMC power supplies as separate PCB through-hole vias. All power pins are independently de-coupled with a 100nF capacitor to the ground plane.

Other features on the card include: 8 x indicator LEDs, 4 x push-button switches (with RC de-bouncing) and a single-ended 100 MHz clock oscillator. The LEDs, buttons and oscillator may be powered by either the VADJ or 3.3V supply on the card. In this way, the component I/O can be made compatible with the desired I/O voltage. Finally, the FMC-BRK card provides a standard pitch 0.100" (2.54 mm) prototyping area of 12 x 22 through-holes. This area is ideal for implementing custom circuitry and extending the functionality of the card for different user applications. Figures (1) and (2) show the general board layout and the distribution of main board components.

Board layout

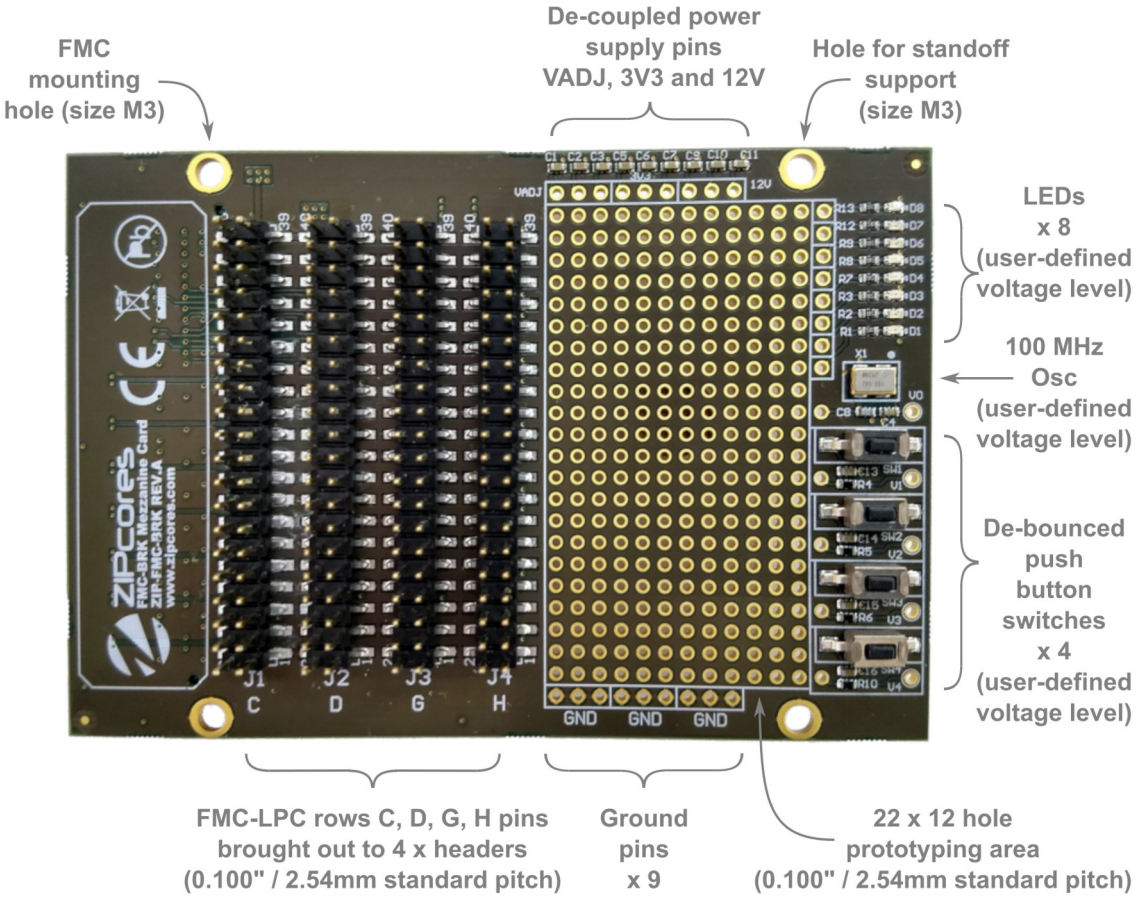

Figure 1: ZIP-FMC-BRK Rev. A board (top view)

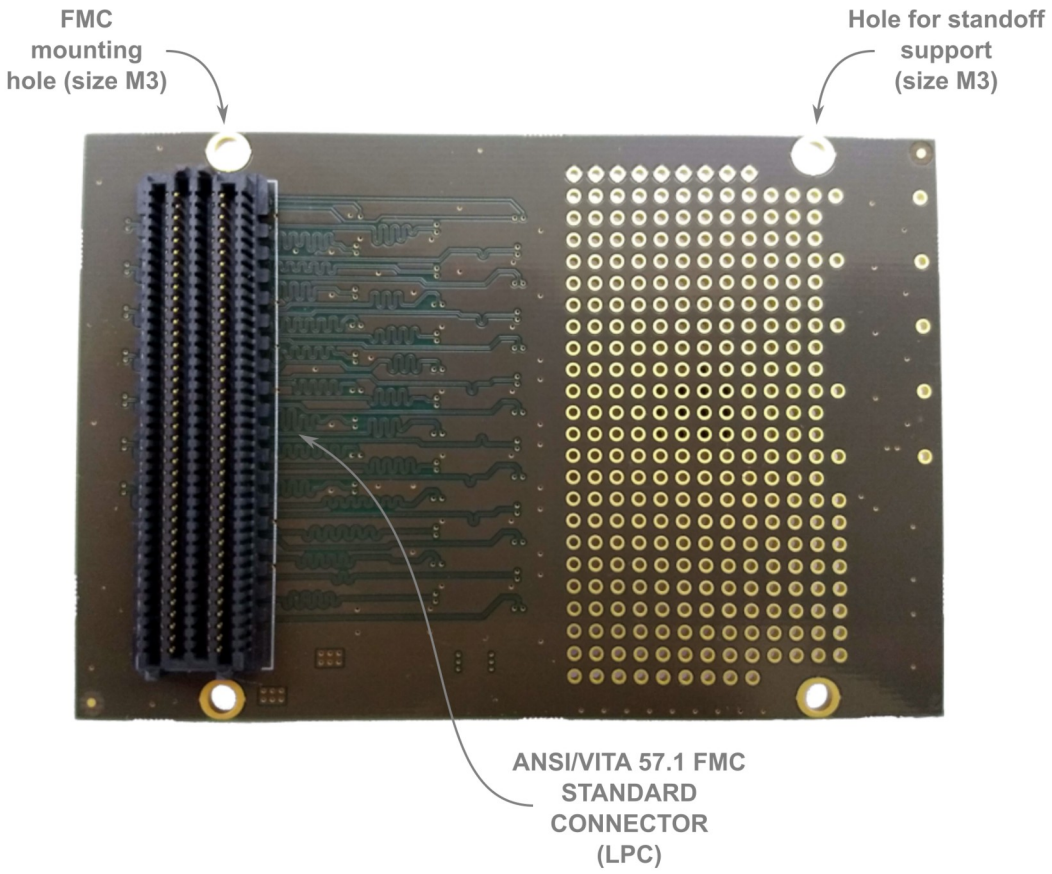

Figure 2: ZIP-FMC-BRK Rev. A board (bottom view)

Key features

- Standard ANSI/VITA 57.1 FMC™ LPC connector
- Also compatible with FMC HPC (but only LPC pins used)
- 4 x headers provide passive connectivity to all 160 pins on the FMC connector (rows C, D, G and H)
- All pin and through-hole spacings are standard 0.100” pitch or 2.54 mm
- Access to 34 x differential pairs (LA00:33), 68 x single-ended signals or a mixture of either
- Access to 2 x GTP transceiver pairs including GTP clock
- Access to 2 x user-clock differential pairs
- Access to the I^2C, JTAG and FMC state flags
- Access to the VADJ, 3.3V and 12V FMC power supplies
- All differential pairs routed with the same track lengths
- All differential signals impedance-matched for LVDS 100Ω termination
- Dimensions approx 10 x 6.7 cm
- Separate VADJ, 3.3V, 12V and GND through-hole vias
- Separate power pins de-coupled to ground with 100 nF capacitors
- Separate PCB ground-plane for improved signal integrity and noise immunity
- Features large 22 x 12 prototyping area for custom circuitry and user-defined functions
- 8 x user LEDs with 332Ω series resistors
- 4 x user push-buttons with RC de-bouncing circuit
- 100 MHz low-jitter single-ended clock oscillator
- 2 x M3 mounting holes for securing the FMC connector
- 2 x M3 mounting holes for supporting standoff ‘legs’
- Compatible with a wide range of FMC base-boards and FMC-compliant systems

Detailed description

FMC header connectors

The 160 x FMC signals are routed to four (2 x 20) header connectors as shown in Figure (3) below. A separate 40-pin header is allocated to each row of the FMC connector such that row C maps to J1, row D maps to J2, row G maps to J3 and row H maps to J4. The pin numbering also *exactly* matches the signal numbering in the VITA 57.1 specification. So, for instance, row C pin 10 on connector J1 is the signal 'LA06_P' which corresponds to signal C10 of the VITA specification. A full list of the FMC connector pinouts are also given in Appendix B at the end of this document.

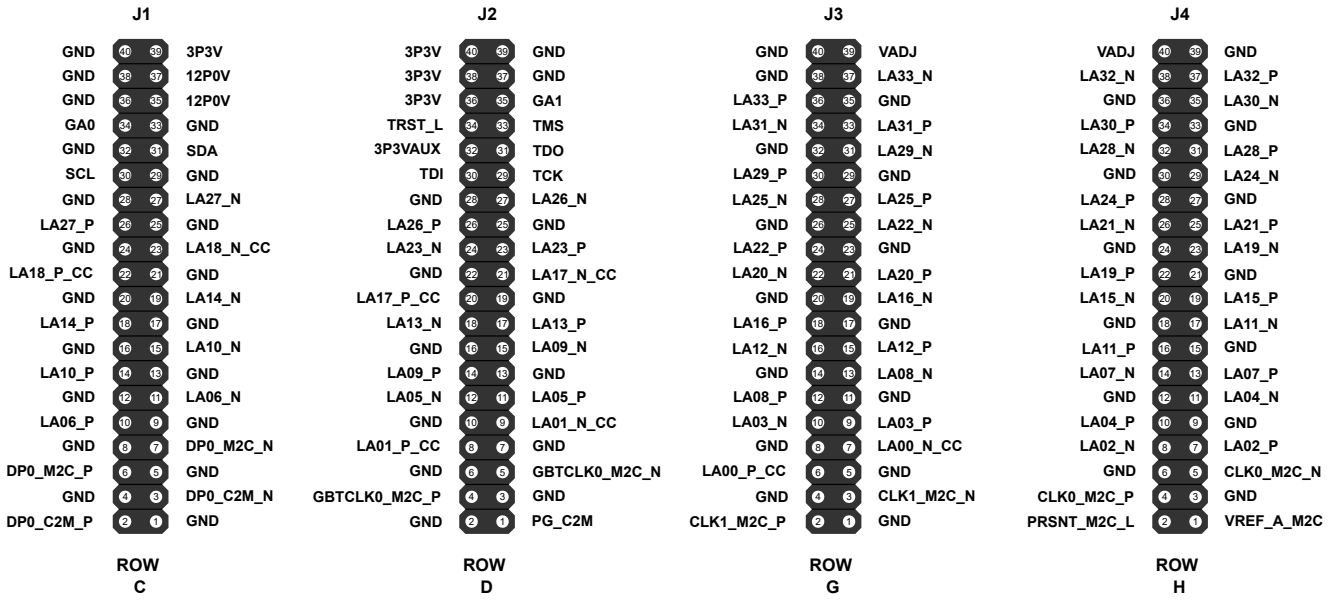

Figure 3: FMC signals mapped to 4 x 40-pin header connectors

User LEDs

The FMC card provides 8 x general purpose indicator LEDs. Each LED is in series with a 332Ω resistor to ground. The input to the LED circuit is a through-hole on the card that allows the LED to be driven using a simple hook-up wire or soldered connection. The maximum recommended driving voltage is 3.3V. Figure (4) below shows the LED circuit of which there are 8 in total.

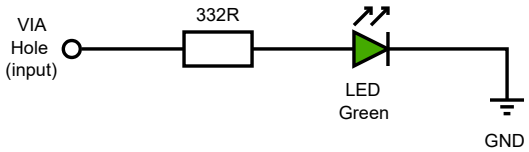

Figure 4: General purpose LED indicator circuit (active high LED on)

User push-button switches

The card features 4 x push-button switches for general purpose use. Each switch is de-bounced with a passive RC circuit. The switches are designed as active-low switches with a button press driving the output low. As with the LED circuits, the switch outputs must be connected using hook-up wire or a soldered connection.

The switches may be powered by either the VADJ or 3.3V supply on the card. Again, the switch power supply must be provided by a hook-up wire or soldered connection to the power vias. The power vias for each switch are labelled V1, V2, V3 and V4 on the FMC card. Figure (5) shows the push-button circuit of which there are 4 in total.

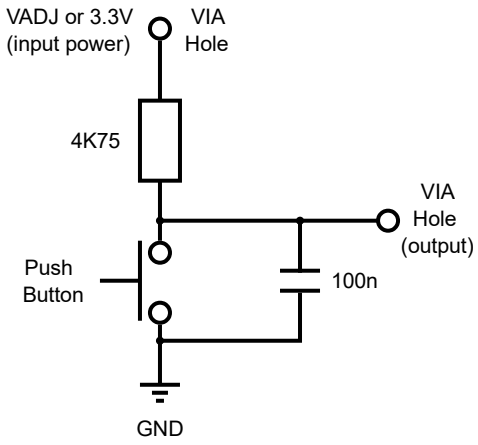

Figure 5: Push-button switches (active low button press)

User 100 MHz clock oscillator

A precision single-ended clock oscillator is provided on the board part number: SG-8018CB from EPSON. As with the other user circuits on the card, the IC power supply and output are connected using a through-hole via. The 100 MHz oscillator power supply voltage can be anything from 1.62 V to 3.63 V. This means that either the VADJ or 3.3V supply on the FMC card may be used to power the device. Figure (6) shows the circuit diagram of the oscillator[1].

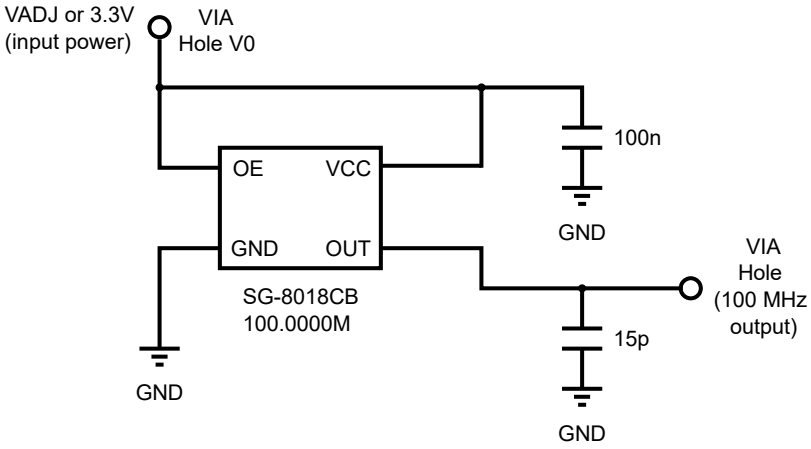

Figure 6: 100 MHz precision clock oscillator circuit

1 Note: on some boards the oscillator is replaced by a 50 MHz version of equivalent specification. Part number: SG-8018CB 50.0000M

FMC power supplies

All the FMC standard power pins are made available on the FMC-BRK mezzanine card. As well as routing power to the FMC breakout header connectors, the card provides the VADJ, 3.3V and 12V power supplies as separate through-hole vias. These extra supplies are de-coupled with 100 nF capacitors to the ground plane. In addition to the separate power pins, a row of 9 x ground pins are provided on the card to allow for easy prototyping.

User prototyping area

The user prototyping area is a grid of 22 x 12 through-holes on the card. The prototyping area is idea for designing custom circuits and adding extra functionality to the FMC-card or main base-board. The area is large enough to support other small development boards, extra connectors or custom connectivity between external peripherals. The holes in the prototyping area are standard 0.100” pitch or 2.54 mm.

ANSI/VITA 57.1 FMC™ connector

The mezzanine card uses a standard ANSI/VITA 57.1 FMC connector. The pinouts of the connector are configured with the Low-Pin-Count (LPC) option occupying rows D/C and G/H. Although the pinouts are designed for the LPC connector, the mezzanine card is also compatible with the High-Pin-Count connector (HPC). Note that in the case of HPC then rows A/B, E/F and K/J will be left unconnected. A detailed specification of the FMC connector may be found on the Samtec® website just here:

www.samtec.com/standards/vita/fmc

The FMC standard connector is used in a wide selection of FPGA development boards from vendors such as Xilinx®, Intel®, Avnet® and Digilent®. Xilinx in particular have adopted the FMC standard in all their FPGA and SoC development boards. Appendix A gives some examples of FMC-compatible base-boards. More information can be found on the Xilinx website just here:

www.xilinx.com/products/boards-and-kits/fmc-cards.html

A full description of the FMC connector pinout with the mezzanine card is given in Appendix B.

Appendices

Appendix A: Examples of supported FMC base-boards

ZYNQ-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
ZedBoard www.zedboard.org/product/zedboard	Digilent/Avnet	1 x LPC	1.8V, 2.5V, 3.3V
MicroZed FMC Carrier Card www.zedboard.org/product/microzed-fmc-carrier	Avnet	1 x LPC	1.8V, 2.5V, 3.3V
PicoZed FMC Carrier Card V2 www.zedboard.org/product/picozed-fmc-carrier-card-v2	Avnet	1 x LPC	1.8V, 2.5V, 3.3V
Xilinx Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit www.xilinx.com/products/boards-and-kits/zcu104.html	Xilinx/Avnet	1 x LPC	1.2V, 1.5V, 1.8V
Xilinx Zynq-7000 SoC ZC702 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc702-g.html	Xilinx/Avnet	2 x LPC	2.5V fixed
Xilinx Zynq-7000 SoC ZC706 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html	Xilinx/Avnet	1 x LPC + 1 x HPC	2.5V fixed

GENERAL FPGA-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
Spartan-7 SP701 FPGA Evaluation Kit www.xilinx.com/products/boards-and-kits/sp701.html	Xilinx/Avnet	1 x LPC	1.8, 2.5V, 3.3V
Nexys Video Artix-7 FPGA www.store.digilentinc.com/nexys-video-artix-7-fpga-trainer-board-for-multimedia-applications/	Digilent	1 x LPC	1.2V, 1.8V, 2.5V, 3.3V
Xilinx Artix-7 FPGA AC701 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html	Xilinx/Avnet	1 x HPC	1.8V, 2.5V, 3.3V
Xilinx Kintex-7 FPGA KC705 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-k7-kc705-g.html	Xilinx/Avnet	1 x LPC + 1 x HPC	1.8V, 2.5V, 3.3V
Genesys 2 Kintex-7 FPGA Development Board www.store.digilentinc.com/genesys-2-kintex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V
NetFPGA-1G-CML Kintex-7 FPGA Development Board www.store.digilentinc.com/netfpga-1g-cml-kintex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V
Xilinx Virtex-7 FPGA VC707 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html	Xilinx/Avnet	2 x HPC	1.2V, 1.5V, 1.8V
Xilinx Virtex-7 FPGA VC709 Connectivity Kit www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html	Xilinx/Avnet	2 x HPC	1.8V fixed
NetFPGA-SUME Virtex-7 FPGA Development Board www.store.digilentinc.com/netfpga-sume-virtex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V

ULTRASCALE-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit www.xilinx.com/products/boards-and-kits/kcu105.html	Xilinx/Avnet	1 x LPC + 1 x HPC	1.2V, 1.5V, 1.8V
Xilinx Kintex UltraScale FPGA KCU1250 Characterization Kit www.xilinx.com/products/boards-and-kits/ck-u1-kcu1250-g.html	Xilinx/Avnet	3 x HPC	1.8V fixed
Xilinx Kintex UltraScale+ FPGA KCU116 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html	Xilinx/Avnet	1 x HPC (partial)	1.8V fixed
Xilinx Virtex UltraScale FPGA VCU108 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html	Xilinx/Avnet	2 x HPC	1.2V, 1.5V, 1.8V
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit www.xilinx.com/products/boards-and-kits/vcu118.html	Xilinx/Avnet	1 x HPC	1.2V, 1.5V, 1.8V

Appendix B: FMC Connector pinout (rows H, G, D, C)

FMC pin	*VITA net name*	*FMC pin*	*VITA net name*	*FMC pin*	*VITA net name*	*FMC pin*	*VITA net name*
H1	VREF_A_M2C	G1	GND	D1	PG_C2M	C1	GND
H2	PRSNT_M2C_L	G2	CLK1_M2C_P	D2	GND	C2	DP0_C2M_P
H3	GND	G3	CLK1_M2C_N	D3	GND	C3	DP0_C2M_N
H4	CLK0_M2C_P	G4	GND	D4	GBTCLK0_M2C_P	C4	GND
H5	CLK0_M2C_N	G5	GND	D5	GBTCLK0_M2C_N	C5	GND
H6	GND	G6	LA00_P_CC	D6	GND	C6	DP0_M2C_P
H7	LA02_P	G7	LA00_N_CC	D7	GND	C7	DP0_M2C_N
H8	LA02_N	G8	GND	D8	LA01_P_CC	C8	GND
H9	GND	G9	LA03_P	D9	LA01_N_CC	C9	GND
H10	LA04_P	G10	LA03_N	D10	GND	C10	LA06_P
H11	LA04_N	G11	GND	D11	LA05_P	C11	LA06_N
H12	GND	G12	LA08_P	D12	LA05_N	C12	GND
H13	LA07_P	G13	LA08_N	D13	GND	C13	GND
H14	LA07_N	G14	GND	D14	LA09_P	C14	LA10_P
H15	GND	G15	LA12_P	D15	LA09_N	C15	LA10_N
H16	LA11_P	G16	LA12_N	D16	GND	C16	GND
H17	LA11_N	G17	GND	D17	LA13_P	C17	GND
H18	GND	G18	LA16_P	D18	LA13_N	C18	LA14_P
H19	LA15_P	G19	LA16_N	D19	GND	C19	LA14_N
H20	LA15_N	G20	GND	D20	LA17_P_CC	C20	GND
H21	GND	G21	LA20_P	D21	LA17_N_CC	C21	GND
H22	LA19_P	G22	LA20_N	D22	GND	C22	LA18_P_CC
H23	LA19_N	G23	GND	D23	LA23_P	C23	LA18_N_CC
H24	GND	G24	LA22_P	D24	LA23_N	C24	GND
H25	LA21_P	G25	LA22_N	D25	GND	C25	GND
H26	LA21_N	G26	GND	D26	LA26_P	C26	LA27_P
H27	GND	G27	LA25_P	D27	LA26_N	C27	LA27_N
H28	LA24_P	G28	LA25_N	D28	GND	C28	GND
H29	LA24_N	G29	GND	D29	TCK	C29	GND
H30	GND	G30	LA29_P	D30	TDI	C30	SCL
H31	LA28_P	G31	LA29_N	D31	TDO	C31	SDA
H32	LA28_N	G32	GND	D32	3P3VAUX	C32	GND
H33	GND	G33	LA31_P	D33	TMS	C33	GND
H34	LA30_P	G34	LA31_N	D34	TRST_L	C34	GA0
H35	LA30_N	G35	GND	D35	GA1	C35	12P0V
H36	GND	G36	LA33_P	D36	3P3V	C36	GND
H37	LA32_P	G37	LA33_N	D37	GND	C37	12P0V
H38	LA32_N	G38	GND	D38	3P3V	C38	GND
H39	GND	G39	VADJ	D39	GND	C39	3P3V
H40	VADJ	G40	GND	D40	3P3V	C40	GND

Appendix C: List of supporting design files

The FMC-BRK card has a number of supporting design files and documents that may be downloaded from the Zipcores website at: www.zipcores.com/downloads.html. Most of the design files are source-code files that are required for building and running the example demo as described in Appendix D. A list of these files and a brief description is given below:

Folders and important files	***Description***
docs/ zip_fmc_brk_user_guide.pdf zip_fmc_brk_safety_info.pdf zip_fmc_brk_schematic.pdf zip_fmc_brk_assembly.pdf zip_fmc_brk_gerber.pdf zip_fmc_brk_bom.pdf	Folder containing various design documents. FMC-BRK hardware user guide (this document). FMC-BRK regulatory compliance and safety information. FMC-BRK design schematics. FMC-BRK assembly drawings. FMC-BRK gerber summary. FMC-BRK bill of materials.
const/ fmc_brk_top.xdc	Folder containing the physical constraints for the Xilinx Vivado project. Example master 'XDC' file that defines all the top-level pinouts and design constrains for the FMC-BRK card when connected to the Xilinx® AC701 base-board. This file may be adapted for use with all Xilinx FPGAs.
vivado/ FMC_BRK_TOP.xpr	This folder contains the Vivado project environment for the demo. Vivado project setup file (double click to invoke project).
vhdl/ fmc_brk_top.vhd fmc_brk_top_bench.vhd	This folder contains the top-level VHDL source-code files for the example demo. The main top-level files are: The top-level synthesizable component. The top-level testbench for the VHDL simulation.
modelsim/ FMC_BRK_TOP.mpf	This folder contains the Modelsim® simulation environment in order to run a VHDL hardware simulation of the demo. You will need to obtain a copy of Mentor Graphics Modelsim in order to use these files. Modelsim project setup file (double click to invoke project).
misc/	This folder contains various data sheets, schematics and design notes for the components on the FMC-BRK card.

Zipcores offers a wide range of IP Cores and custom solutions for the FMC-BRK development board. As well as Xilinx FPGAs, we can provide IP for other FPGAs or SoCs on request. If you have a specific requirement or simply want to discuss a potential solution then please get in touch. Further details may be found by visiting our website or contacting us at: www.zipcores.com/help.php.

Appendix D: Running the example demo

A simple demo is provided to get started with the FMC-BRK card. The demo generates a series of active-high pulses on the differential output pairs of the card. The pulses are at LVCMOS25 levels and are generated such that LAXX_P and LAXX_N signals are inverted versions of each other. The period of each pulse is also defined according to the pin-number such that: LA00_P/N has a 1.0us period, LA01_P/N has a 1.1us period, LA02_P/N has a 1.2us period etc. In this way, it's easy to locate each LA pin on the card by its waveform. In order to run the demo, the following basic lab setup is recommended:

- Oscilloscope for measuring the output pulse waveforms. (E.g. Tektronix MDO3014).
- Hook-up wire (optional) to easily connect the scope probe to the header pins.
- Xilinx Artix-7 FPGA AC701 Evaluation Kit (www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html). This will be used as the base board on which the FMC-BRK mezzanine card will be mounted. (Note: other base boards may be supported on request. Please contact us for more details).
- Spacers (10 mm) and screws (size M2.5) in order to secure the FMC-BRK card to the base-board.
- Xilinx Vivado Software (rev. 2018.3 or later) together with the Xilinx AC701 board definition files.
- USB cable for programming the AC701 board.

Once the equipment is set up then the user should invoke the Vivado software and load the project environment 'FMC_BRK_TOP.xpr' which is in the 'vivado' folder as described in Appendix C above. The same directory structure should be maintained so that the links and dependencies are correctly resolved. If the project loads correctly, the initial project layout should look something like Figure (7) below:

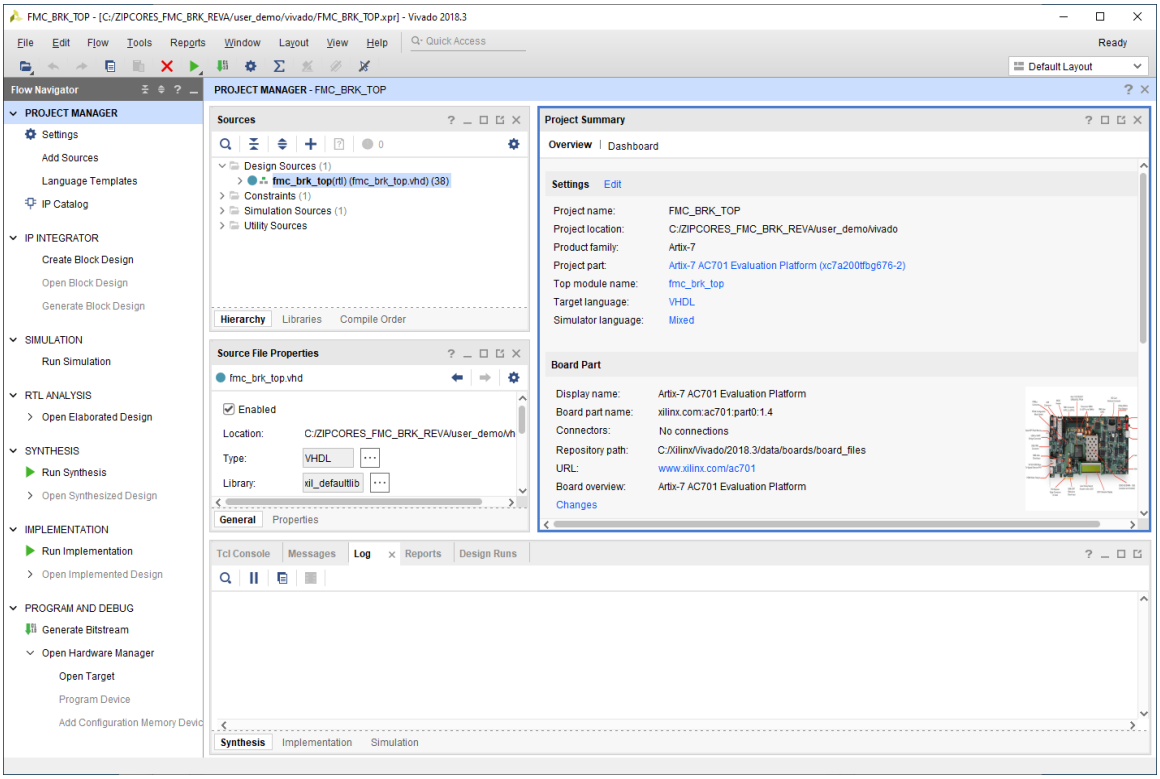

Figure 7: Initial Vivado project startup for demo

Once the project is loaded then the next step is to build the bitstream for programming the FPGA. Click on 'Generate Bitstream' in the project manager window and wait for the compile process to complete. After the bitstream is generated then open the hardware manager and program the AC701 board.

Figure (8) below shows an example bench setup with the LA32_P and LA32_N pins (H37/H38) being probed on the FMC header connector. Notice that the pulse period is exactly 4.2 us and the pulse trains are inverted versions of each other.

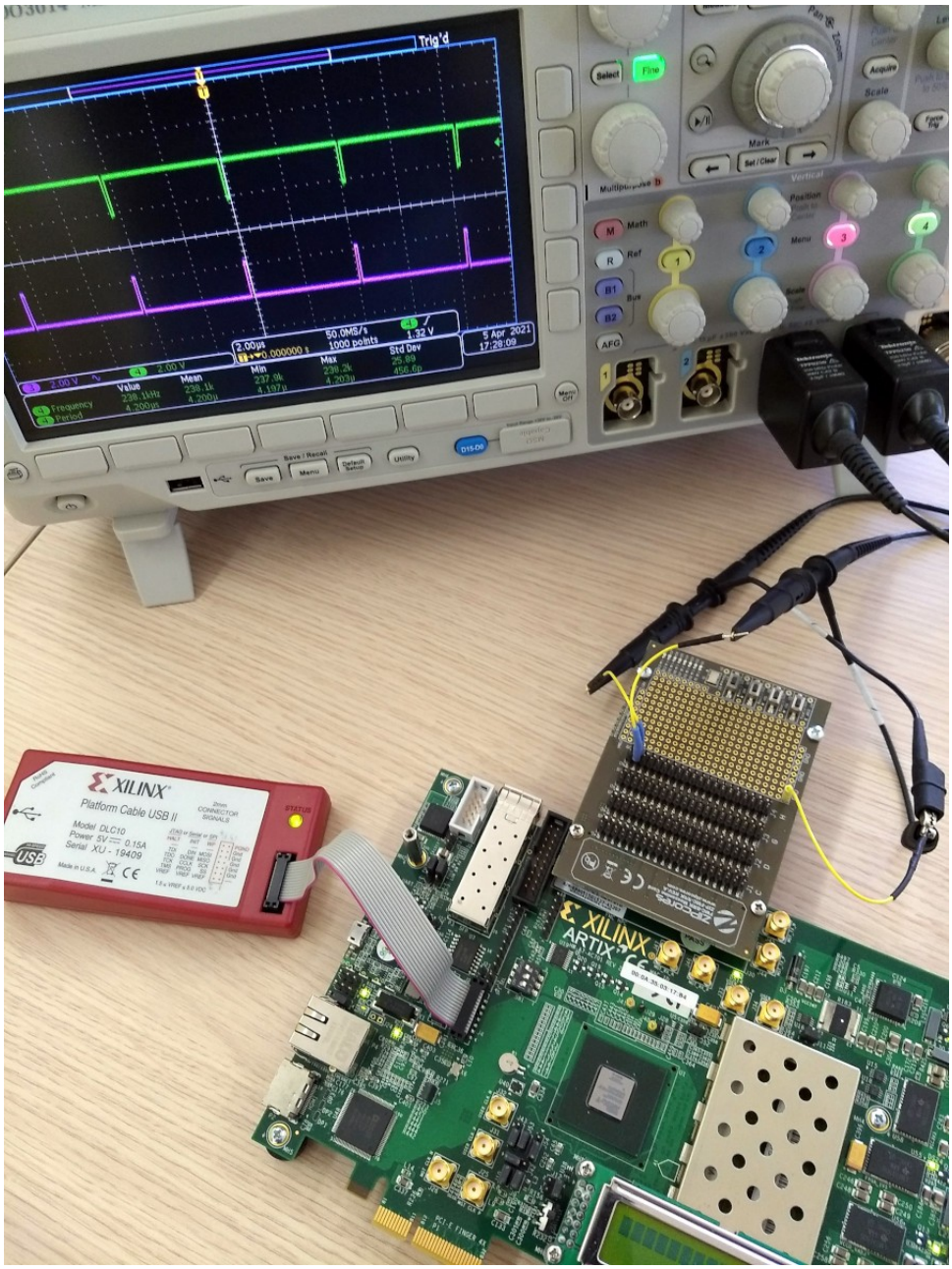

Figure 8: Bench setup showing FMC-BRK card connected to the Xilinx AC701 board

Revision history

Revision	*Change description*	*Date*
A.0	Initial revision	25/11/2021
A.1	Fixed typo in description of pin C39 that was incorrectly labelled (Figure 3). Now correctly labelled as 3P3V. Added gerber file description in Appendix C.	01/03/2023

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