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NORA-W10 series

Stand-alone multiradio modules

Data sheet

Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for NORA-W10 series modules.

Supporting Wi-Fi 4 (802.11b/g/n) and Bluetooth Low Energy v5.0, NORA-W10 standalone, multiradio modules offer a host-less, open CPU configuration that allows customer applications to run on the module itself – with no need for a supporting host MCU. NORA-W10 series modules are ideal for Internet of Things (IoT) devices, telematics, low-power sensors, connected buildings (appliances and surveillance), point-of-sales, health devices, AI, facial recognition, and other design solutions that demand top-grade security.

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Mass production / End of life	Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Hardware version	PCN reference	Product status
NORA-W101	NORA-W101-00B-00	04	N/A	Initial production
NORA-W106	NORA-W106-00B-00	04	N/A	Initial production
NORA-W106	NORA-W106-10B-00	14	N/A	Initial production

Contents

1 Functional description

1.1 Overview

The NORA-W10 series comprises small, stand-alone, multiradio modules that integrate a powerful microcontroller (MCU) and a radio for wireless communication. The open CPU architecture allows customers to develop advanced applications running on the dual core 32-bit MCU. The radio provides support for Wi-Fi 802.11b/g/n in the 2.4 GHz ISM band and Bluetooth v5.0 (Bluetooth Low Energy communications).

These compact modules include the wireless MCU, flash memory, crystal, and other components for matching, filtering, antenna, decoupling, and antenna operation. Supporting integrated cryptographic hardware accelerators, NORA-W10 series modules are ideal for Internet of Things (IoT) devices, telematics, low power sensors, connected factories, connected buildings (appliances and surveillance), point-of-sales, health devices, artificial intelligence, facial recognition, and other design solutions that demand top-grade security.

NORA-W10 is based on the Espressif ESP32-S3 chip [3]. It is the second generation of u-blox modules residing on the Espressif ESP32 series Wi-Fi and Bluetooth chip. The first generation is NINA-W1/B2 series modules. The simple device design allows developers to use an external antenna (NORA-W101) or utilize the internal antenna (NORA-W106) in the application design.

As the mechanical design of NORA-W10 is based on the NORA form factor, applications can be migrated to and from NORA-B1 [7].

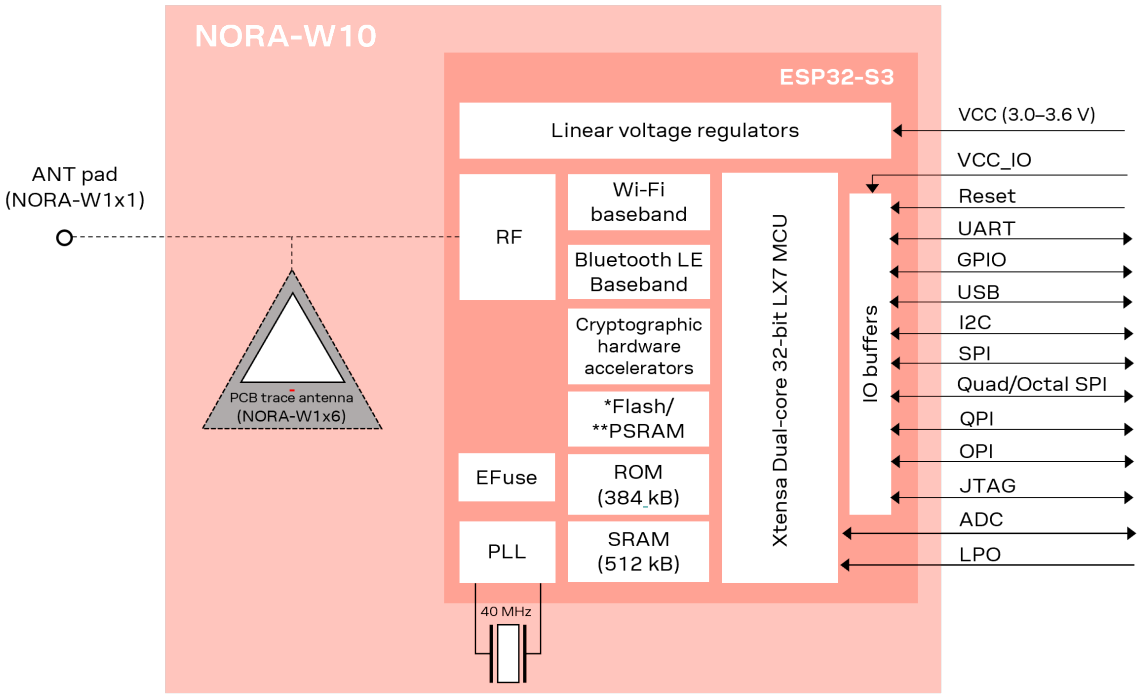
NORA-W10 modules are compliant with the Radio Equipment Directive (RED) and are also certified in the following countries: Great Britain (UKCA), US (FCC), Canada (IC / ISED RSS), Japan (MIC), Taiwan (NCC), South Korea (KCC), Australia / New Zealand (ACMA), Brazil (Anatel), and South Africa (ICASA). The modules are also qualified according to u-blox qualification policy, based on AEC-Q104 standard for professional grade operation and supports temperature range of –40 °C to +85 °C. The -10B variant is specified to 85 °C and professional grade with the PSRAM ECC function is enabled. See also, Operating temperature range.

1.2 Applications

NORA-W10 series are suitable for a wide range of applications, including:

- Wi-Fi networks
- Internet of Things (IoT)
- Bluetooth low energy applications
- Telematics
- Point-of-sales
- Medical and industrial networks
- Access to laptops, mobile phones, and similar consumer devices
- Home/building automation apps
- Wireless gateways
- Artificial intelligence (AI)
- Facial recognition

1.3 Block diagram



* Only on NORA-W101-00B and NORA-W106-00B
** Only on NORA-W106-10B

Figure 1: NORA-W10 series block diagram

1.4 Product variants

NORA-W10 modules have an open CPU architecture that is tailored towards OEMs that want to embed Wi-Fi and Bluetooth LE support into their own application.

1.4.1 NORA-W101

1.4.1.1 NORA-W101-00B

NORA-W101-00B has a dedicated antenna RF pin to be used for an external antenna or antenna connector. There is no internal antenna on the module. See also the list of approved antennas in the NORA-W10 system integration manual [1]. NORA-W101-00B includes an embedded flash of 8 MB with quad SPI. NORA-W101-00B includes no embedded PSRAM.

NORA-W101-00B has an outline of 10.4 (length) x 14.3 mm (width) x 1.9 mm (height).

1.4.2 NORA-W106

1.4.2.1 NORA-W106-00B

NORA-W106-00B is equipped with an internal PCB trace antenna, using antenna technology licensed from Abracon. The RF signal is not connected to any module pin. NORA-W106-00B includes an embedded flash of 8 MB with quad SPI. NORA-W106-00B includes no embedded PSRAM.

NORA-W106-00B has an outline of 10.4 (length) x 14.3 mm (width) x 1.9 mm (height).

1.4.2.2 NORA-W106-10B

NORA-W106-10B is equipped with an internal PCB trace antenna, using antenna technology licensed from Abracon. The RF signal is not connected to any module pin. NORA-W106-10B includes an embedded PSRAM of 8 MB, replacing the 8 MB flash. The octal SPI of the PSRAM additionally occupies five GPIO pins on top of the quad SPI, see Table 5.

NORA-W106-10B has an outline of 10.4 (length) x 14.3 mm (width) x 1.9 mm (height).

⚠ The NORA-W106-10B variant is specified at 85 °C with the PSRAM ECC enabled. See also Operating temperature range.

1.5 Radio performance

NORA-W10 series (NORA-W101, and NORA-W106) modules support Wi-Fi and are conformant with IEEE 802.11b/g/n single-band 2.4 GHz operation and Bluetooth LE specifications, as shown in Table 1.

Wi-Fi	Bluetooth Low Energy
IEEE 802.11b/g/n	Bluetooth 5.0 Bluetooth LE dual-mode
Band support Station mode: 2.4 GHz, channel 1-13* Access Point mode: 2.4 GHz, channel 1-13*	Band support 2.4 GHz, 40 channels
Typical conducted output power : 17 dBm	Typical conducted output power 7 dBm
Typical radiated output power: 20 dBm EIRP**	Typical radiated output power 10 dBm EIRP**
Conducted sensitivity -97 dBm	Conducted sensitivity -98 dBm
Data rates: IEEE 802.11b: 1 / 2 / 5.5 / 11 Mbit/s IEEE 802.11g: 6 / 9 / 12 / 18 / 24 / 36 / 48 / 54 Mbit/s IEEE 802.11n: MCS 0-7, HT20 (72 Mbit/s, Max), HT40 (150 Mbit/s, Max)	Data rates: 1 / 2 Mbit/s 125 / 500 Kbit/s

* Depending on the location (country or region), channels 12-13 must be limited or disabled. Consequently, the software implementation must support country determination algoritms when using channels 12-13. For example, algorithms must be be supported on these channels to comply with 802.11d amendment standard. For further information, see the NORA-W10 series system integration manual [1].

** RF power including maximum antenna gain (3 dBi)

Table 1: NORA-W10 series Wi-Fi and Bluetooth characteristics

1.6 CPU

NORA-W10 series modules have a dual-core system with two Harvard Architecture Xtensa LX7 CPUs operating at a maximum 240 MHz internal clock frequency.

The main features of the internal NORA-W10 memory include:

- 384 KB ROM for booting and core functions.
- 512 KB SRAM for data and instruction.

- 8 MB FLASH (NORA-W101-00B and NORA-W106-00B) for code storage, including hardware encryption to protect programs. 8 MB PSRAM (NORA-W106-10B).
- 4 kbit EFUSE (non-erasable memory) for MAC addresses, module configuration, flash encryption, and chip ID.

NORA-W10 has no software but includes an Open CPU architecture that allows customers to develop advanced applications running on the dual core 32-bit MCU. The radio provides support for Wi-Fi 802.11b/g/n in the 2.4 GHz ISM band, and Bluetooth LE communication.

NORA-W10 Open CPU also support external PSRAM/Flash memory depending upon the module variant.

The customer is responsible for the NORA-W10 certification and configuration, as described in Country approvals.

NORA-W10 series modules can be used to design solutions with top-grade security. Including integrated cryptographic hardware accelerators, the modules feature secure boot functionality that ensures that the module can only be restarted with authenticated software.

1.6.1 Software upgrade

For information about upgrading NORA-W10 series software, see the NORA-W10 system integration manual [1] .

1.7 MAC addresses

For information about MAC addresses, see https://docs.espressif.com/projects/esp-idf/en/v4.4.2/esp32s3/api-reference/system/system.html#mac-address.

1.8 Power modes

NORA-W10 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when they are not needed, and complex wake up events can be generated from different external and internal inputs.

For the lowest current consumption modes an external LPO clock or low frequency crystal is required. See also Low frequency clock.

For more information about power modes, see the Espressif ESP32-S3 Datasheet [3].

2 Interfaces

2.1 Power supply

The power for NORA-W10 series modules is supplied through **VCC** and **VCC_IO** pins by DC voltage.

⚠ As the current drawn from **VCC** and **VCC_IO** can vary significantly based on Wi-Fi power consumption profiles, the system power supply circuit must be able to support peak power.

2.1.1 Module supply input (VCC)

NORA-W10 series modules use an integrated Linear Voltage converter to transform and stabilize the supply voltage applied to the **VCC** pin.

2.1.2 Digital I/O interfaces reference voltage (VCC_IO)

All NORA-W10 series modules have an additional supply input for setting the I/O voltage level. Currently, NORA-W10 modules support a 3.3 V IO voltage level.

2.2 Low frequency clock

NORA-W10 series modules do not have an internal low power oscillator (LPO) or low frequency crystal (LFXTAL), which is required for low power modes. If low power modes are required, a 32.768 kHz clock signal can be supplied externally.

2.3 Module reset

NORA-W10 series modules can be reset (rebooted) with a low-level input on the **RESET_N** pin. The logic level of this pin is normally set high using an internal pull-up resistor. The low-level input triggers a “hardware reset” of the module. The **RESET_N** signal should be driven by an open drain, open collector, or contact switch.

2.4 Boot strap pins

Several module pins related to the boot configuration must be strapped correctly using either pull-up or pull-down resistors, as shown in Table 2.

⚠ Boot strap pins should be avoided if other GPIO pins can be used instead. Note that all module pins configured to their default state internally in the ESP32-S3 chip (shown in bold) must NOT be configured externally.

Pin	ESP32-S3 GPIO	State during boot	Default	Behavior	Description
F7, H7	GPIO0, GPIO46	00		Download Boot	Booting Mode
		01		Invalid, do not use	
		10	Pull-up*, Pull-down*	Normal Boot from internal Flash	
		11		Normal Boot from internal Flash	
J9	GPIO3	0	N/A	*EFUSE_DIS_USB_JTAG = 0, EFUSE_DIS_PAD_JTAG = 0, EFUSE_STRAP_JTAG_SEL = 1* JTAG signal from on-chip JTAG pins	JTAG Signal Selection
		1		*EFUSE_DIS_USB_JTAG = 0, EFUSE_DIS_PAD_JTAG = 0, EFUSE_STRAP_JTAG_SEL = 1* JTAG signal from USB Serial/JTAG controller	

Pin	ESP32-S3 GPIO	State during boot	Default	Behavior	Description
		D/C		*EFUSE_DIS_USB_JTAG = 0,* *EFUSE_DIS_PAD_JTAG = 0,* *EFUSE_STRAP_JTAG_SEL=0* JTAG signal from USB Serial/JTAG controller	

*About 45 kΩ.

Table 2: NORA-W10 series boot strapping pins

2.5 RF antenna interface

NORA-W10 modules include an RF antenna interface that supports Wi-Fi, and Bluetooth LE on the same antenna. The different communication protocols are time divided on the antenna and are switched between the Bluetooth and Wi-Fi data. Although communication using these different protocols is (more or less) transparent in the application, these protocols are never active at exactly the same time as they are in the module antenna.

NORA-W10 series modules support either a single internal antenna (NORA-W106) or external antennas connected through a dedicated antenna pin (NORA-W101). For an overview of the different antenna types (internal, integrated, and external) described in this section, see also the system integration manual [1].

2.5.1 Internal antenna

NORA-W106 modules have internal antennas that are specifically designed and optimized for NORA modules. NORA-W101 modules do not support an internal antenna.

NORA-W106 is equipped with a 2.4 GHz PCB trace antenna that is ideally placed in the middle of the module – along the side edge of the host PCB. For further information about antenna placement, see the system integration manual [1].

In NORA-W106 designs, keep a minimum clearance of 5 mm between the antenna and the casing. Also, keep at least 10 mm of free space around the metal antenna including the area directly below it. If a metal enclosure is required, use NORA-W101 and an external antenna.

It is beneficial to have a large solid ground plane on the host PCB with a good grounding on the module. A 50 x 50 mm ground plane is recommended but its size should be no less than 24x30 mm.

For more information about antenna-related design, see also the NORA-W10 series system integration manual [1].

⚠ The **ANT** solder pin (K9) on NORA-W106 modules is not available for connecting an external antenna.

2.5.2 External RF antenna interface

NORA-W101 has an antenna signal (**ANT**) pin with a characteristic impedance of 50 Ω for using an external antenna. The antenna signal supports both Tx and Rx.

An SMD antenna, or any other antenna featured in the pre-approved antennas list [1], can be employed as an external antenna or an integrated antenna on the host PCB. An antenna connector, for use with an external antenna through a coaxial cable, could also be implemented in the application design. A cable antenna might be necessary if the module is mounted in a shielded enclosure such as a metal box or cabinet.

An external antenna connector (U.FL. connector) features in the NORA-W10 reference design shown in the NORA-W10 series system integration manual [1]). The reference design must be followed to comply with regulatory approvals.

See also the list of pre-approved antennas in the NORA-W10 system integration manual [1].

2.6 IO signals

NORA-W10 modules have 82 pins in total. In NORA-W101 modules 38 pins can be used for both input and output. The pins can be used as GPIO signals are also multiplexed with the digital and analog interfaces.

It is also possible to multiplex all interfaces to any pin through an IO MUX, but the speed is limited. See also Digital pins.

2.6.1 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) functionality can, for example, be used to control the intensity of LEDs and driving digital motors. The controller consists of PWM timers, the PWM operator, and a dedicated capture sub-module. Each timer provides timing in synchronous or independent form, and each PWM operator generates the waveform for one PWM channel.

The PWM controller has eight channels, which can generate independent waveforms that can be used to drive RGB LED devices. For maximum flexibility, the high-speed and low-speed channels can be driven from one of four timers. The PWM controller can also automatically increase or decrease the duty cycle gradually, which allows for fades without any processor interference. The PWM signals can be configured to be available on any of the GPIO pins through the IO MUX.Data interfaces.

2.6.2 UARTs

NORA-W10 modules have three UART interfaces, UART0 to UART2. Each interface provides asynchronous communication support for RS232, RS485, and IrDA standards (with external drivers).

UART0 serves as the primary interface port. The maximum speed for all UART interfaces is 4 Mbit/s.

All UART interfaces can be routed to any GPIO pin through the IO MUX. But, as firmware upgrades are performed through the default pins on UART0, it is recommended that this interface specifically is NOT routed to the other pins. For further information about the default pins, see also Pin-out.

All UART interfaces provide hardware management of the CTS and RTS signals and software flow control (XON and XOFF).

2.6.3 SPI

Four SPI interfaces are available for the application.

On NORA-W101-00B and NORA-W106-00B, SPI0 (quad SPI) is configured to internal flash storage and is controlled using chip select CS0. Additional flash cannot be connected to SPI0 interface, but an external PSRAM can be connected. CS1 will be the chip select for PSRAM.

On NORA-W106-10B, SPI0/1 (octal SPI) is configured to internal PSRAM and is controlled using chip select CS1. Additional PSRAM cannot be connected to SPI0/1 interface, but an external Flash can be connected. CS0 will be the chip select for Flash.

It is possible to connect the remaining SPI interfaces to other pins via the IO MUX but the maximum speed will be reduced. It is also possible to configure the SPI interface as a dual or quad SPI (2 or 4-bit bidirectional data signals). See also Dual/Quad SPI.

2.6.4 Dual/Quad SPI

The dual/quad SPI (2 or 4 bi-bidirectional data signals) can be used for connecting an additional external PSRAM/Flash. The SPI to dual/quad SPI signal mappings is shown in Table 3.

SPI signal	Dual SPI signal	Quad SPI signal
MOSI	IO0	IO0
MISO	IO1	IO1
WP	-	IO2
HD	-	IO3
CS	CS	CS
CLK	CLK	CLK

Table 3: SPI to dual/quad SPI signal mapping

2.6.5 I2C

Two I2C interfaces can be routed over any GPIO pin.

NORA-W10 modules can operate as both the master and slave on the I2C bus, using both standard (100 kbit/s) and fast (400 kbit/s) transmission speeds. The interface uses the **SCL** signal to clock instructions and data on the **SDA** signal.

2.6.6 I2S

Two I2S interfaces can be routed over any GPIO pin.

NORA-W10 modules can operate with an 8-bit, 16-bit, 24-bit, or 32-bit resolution, master mode and slave mode I2S interface. NORA-W10 allows half duplex and full duplex communication mode, with the clock frequency of 10 KHz up-to 40 MHz.

2.6.7 SDIO

SDIO is multiplexed with the JTAG interface and the SPI_H interface. It is possible to connect the SDIO interfaces to other pins via the IO MUX but the speed is limited. See also Digital pins. Only SDIO host is supported (not SDIO slave).

2.6.8 LCD

NORA-W10 modules support parallel 8–16 bit LCD integration.

2.6.9 TWAI

NORA-W10 modules support the Two-Wire Automotive Interface (TWAI) communication protocol (ISO 118981, parts 1 and 2) with inherent message priorities and arbitration. It provides multi-master and multi-cast communication with error detection and signaling. The TWAI master can operate with a 1 Kbit/s to 1 Mbit/s bit rate along with a 64-byte FIFO receiver. It also supports CAN specification 2.0

2.7 Debug interfaces

2.7.1 JTAG debug interfaces

NORA-W10 modules support the JTAG debug interface (**JTAG_TMS**, **JTAG_CLK**, **JTAG_TDI** and **JTAG_TDO**). The JTAG interface is multiplexed with the SDIO and SPI_H interface.

2.8 Analog interfaces

2.8.1 Analog to digital converters

NORA-W10 modules support two, 12-bit, SAR, Analog to Digital Converters (ADC). Any analog capable pin can be used for ADC applications. All appropriate analog pins are shown in the Pin-out.

For lower power consumption, NORA-W101, NORA-W106 modules can measure voltages in sleep mode and threshold settings can be used to wake the CPU.

☞ Analog pins cannot be re-routed to other pins through the IO MUX.

3 Pin definition

3.1 Input and output pins

All NORA-W10 modules have 82 pins. For NORA-W101-00B and NORA-W106-00B, 38 pins can be used for either General Purpose input or output (GPIO). For NORA-W106-10B, 33 pins can be used for either General Purpose input or output (GPIO).

3.2 NORA-W10 pin assignment

Figure 2 shows the multiplexed pin-out for NORA-W101 and NORA-W106 Open CPU modules. These, and several additional interfaces not shown here, are described in Pin-out.

Although it is also possible to multiplex all interfaces through an IO MUX using any pin, the maximum speed is limited. See also Digital pins.

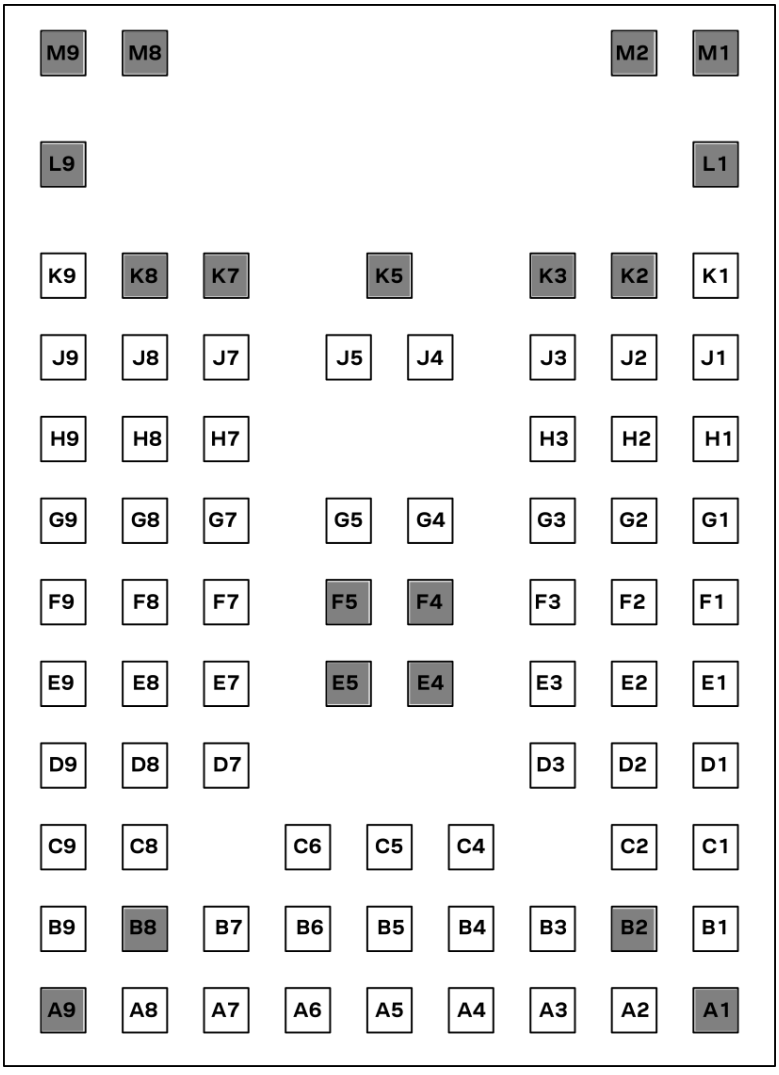


Figure 2: NORA-W101/W106 pin numbering (top view)

All gray pins located on the module are GND pins.

Pins A7, A8, B7, and J3 can only be used as input signals – regardless of the selected function/interface.

☞ The signals for several pins are boot strapped. It is important that these signals, shown in Pin-out, are set in the correct state during startup. See also Boot strap pins.

3.3 Pin-out

3.3.1 NORA-W101-00B and NORA-W106-00B

Table 4 describes the common pin-out for NORA-W101-00B and NORA-W106-00B series modules.

No.	NORA function	I/O[1]	Description	ESP32-S3 function	Remarks
A2	FSPIWP / GPIO38	I/O	SPI2 Write Protect / General Purpose I/O	FSPIWP / GPIO38	
A3	GPIO17	I/O	General Purpose I/O	GPIO17	Analog-capable pin
A4		NC			
A5	FSPIDQS / GPIO14	I/O		FSPIDQS / GPIO14	Analog-capable pin, Touch button input
A6	FSPIIO7 / GPIO13	I/O	SPI2 IO7 / General Purpose I/O	FSPIIO7 / GPIO13	Analog-capable pin, Touch button input
A7	VCCIO	I	Module I/O level voltage input		VIO voltage supply.
A8	VCC	I	Module supply voltage input		3.0-3.6 V module voltage supply.
B1	FSPICLK / GPIO36	I/O	SPI2 clock / General Purpose I/O	FSPICLK / GPIO36	
B3	FSPICS0 / GPIO34	I/O	SPI2 Chip select / General Purpose I/O	FSPICS0 / GPIO34	
B4	GPIO18	I/O	General Purpose I/O	GPIO18	Analog-capable pin
B5		NC			
B6	XTAL_32K_N /LPO_IN GPIO16	I/O	32KHz external clock input / Low Power Oscillator Input / General Purpose I/O	GPIO16	Analog-capable pin
B7	VCCIO	I	Module I/O level voltage input		VIO voltage supply.
B9		NC			
C1	FSPIQ / GPIO37	I/O	SPI2 Master Input Slave Output / General Purpose I/O	FSPIQ / GPIO37	
C2	FSPID / GPIO35	I/O	SPI2 Master Output Slave Input / General Purpose I/O	FSPID / GPIO35	
C4	SPICS0	I/O	SPI0 Chip select	SPICS0 / GPIO29	CS to internal flash. Do not connect
C5		NC			
C6	XTAL_32K_P / GPIO15	I/O	32KHz external clock input / General Purpose I/O	GPIO15	Analog-capable pin. If external LPO is used at LPO_IN, put decoupling capacitor to GND on this pin only.
C8	GPIO21	I/O	General Purpose I/O	GPIO21	
C9	USB_P / GPIO20	I/O	USB differential data signal / General Purpose I/O	USB_D+ / GPIO20	Analog-capable pin. Default drive capability of this pin is ~40mA
D1	SPIWP	I/O	SPI0 Write Protect	SPIWP / GPIO28	Connected to internal Flash. Do not connect. If required, connect only for external PSRAM.
D2	SPID	I/O	SPI0 Master Output Slave Input	SPID /	Connected to internal Flash.

[1] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AI/AO=Analog Input/Output, NC=Not Connected

No.	NORA function	I/O[1]	Description	ESP32-S3 function	Remarks
				GPIO32	Do not connect. If required, connect only for external PSRAM.
D3	FSPIHD / GPIO33	I/O	SPI2 Hold / General Purpose I/O	FSPIHD / GPIO33	
D7		NC			
D8	GPIO4	I/O	General Purpose I/O	GPIO4	Analog-capable pin, Touch button input
D9	USB_N / GPIO19	I/O	USB differential data signal / General Purpose I/O	USB_D- / GPIO19	Analog-capable pin. Default drive capability of this pin is ~40mA
E1	SPICS1	I/O	SPI Chip select / General Purpose I/O	SPICS1 / GPIO26	CE if external PSRAM is connected to SPI0.
E2	SPIQ	I/O	SPI0 Master Input Slave Output	SPIQ / GPIO31	Connected to internal Flash. Do not connect. If required, connect only for external PSRAM.
E3	SPICLK_N / GPIO48	I/O	SPI Differential clock / General Purpose I/O	SPICLK_N / GPIO48	
E7	GPIO9	I/O	General Purpose I/O	GPIO9	Analog-capable pin, Touch button input
E8	GPIO1	I/O	General Purpose I/O	GPIO1	Analog-capable pin, Touch button input
E9	GPIO7	I/O	General Purpose I/O	GPIO7	Analog-capable pin, Touch button input
F1	SPICLK	I/O	SPI0 clock	SPICLK / GPIO30	Connected to internal Flash. Do not connect. If required, connect only for external PSRAM.
F2	SPIHD	I/O	SPI0 Hold	SPIHD / GPIO27	Connected to internal Flash. Do not connect. If required, connect only for external PSRAM.
F3	SPICLK_P / GPIO47	I/O	SPI Differential clock / General Purpose I/O	SPICLK_P / GPIO47	
F7	GPIO0/ Boot	I/O	General Purpose I/O	GPIO0/ Boot	
F8	GPIO45	I/O	General Purpose I/O	GPIO45	
F9	GPIO6	I/O	General Purpose I/O	GPIO6	Analog-capable pin, Touch button input
G1	MTDO / GPIO40	I/O	JTAG Test Data Out /	MTDO / GPIO40	
G2	FSPIIO6 / GPIO12	I/O	SPI2 IO6 / General Purpose I/O	FSPIIO6 / GPIO12	Analog-capable pin, Touch button input
G3	FSPIIO5 / GPIO11	I/O	SPI2 IO5 / General Purpose I/O	FSPIIO5 / GPIO11	Analog-capable pin, Touch button input
G4		NC			
G5		NC			
G7		NC			
G8	U0TXD / GPIO43	I/O	UART data output / General Purpose I/O	U0TXD / GPIO43	
G9	U0RXD / GPIO44	I/O	UART data input / General Purpose I/O	U0RXD / GPIO44	
H1	JTAG_TDI / GPIO41	I/O	JTAG Test Data In (debug interface) / General Purpose I/O	MTDI / GPIO41	
H2	JTAG_TMS /	I/O	JTAG Test Mode Select /	MTMS /	

No.	NORA function	I/O[1]	Description	ESP32-S3 function	Remarks
	GPIO42		General Purpose I/O	GPIO42	
H3	FSPII04 / GPIO10	I/O	SPI2 IO5 / General Purpose I/O	FSPII04 / GPIO10	Analog-capable pin, Touch button input
H7	GPIO46	I/O	General Purpose I/O	GPIO46	
H8	GPIO2	I/O	General Purpose I/O	GPIO2	Analog-capable pin, Touch button input
H9	GPIO8	I/O	General Purpose I/O	GPIO8	Analog-capable pin, Touch button input
J1	VDD_SPI	O	SPI power supply: 3.3 V	VDD_SPI	
J2	JTAG_TCK / GPIO39	I/O	JTAG Test clock / General Purpose I/O	MTCK / GPIO39	
J3	RESET_N	I	External system reset input.	RESET	Active low
J4		NC			
J5		NC			
J7		NC			
J8	GPIO5	I/O	General Purpose I/O	GPIO5	Analog-capable pin, Touch button input
J9	GPIO3	I/O	General Purpose I/O	GPIO3	Analog-capable pin, Touch button input
K1		NC			
K9	ANT	I/O	Antenna Tx/Rx interface	LNA_IN	50 Ω nominal characteristic impedance, only used with NORA-W101 modules. NC for NORA-W106
	EGP	-	Exposed Ground Pins		Exposed scattered grey pins on the module should be connected to GND
L1-M9	EAGP	-	Exposed Antenna Ground Pins		Exposed pins underneath the antenna area should be connected to GND

Table 4: NORA-W10x-00B pin-out

3.3.2 NORA-W106-10B

Table 5 describes the common pin-out for NORA-W106-10B module.

No.	NORA function	I/O[2]	Description	ESP32-S3 function	Remarks
A2	FSPIWP / GPIO38	I/O	SPI2 Write Protect / General Purpose I/O	FSPIWP / GPIO38	
A3	GPIO17	I/O	General Purpose I/O	GPIO17	Analog-capable pin
A4		NC			
A5	FSPIDQS / GPIO14	I/O		FSPIDQS / GPIO14	Analog-capable pin, Touch button input
A6	FSPIIO7 / GPIO13	I/O	SPI2 IO7 / General Purpose I/O	FSPIIO7 / GPIO13	Analog-capable pin, Touch button input
A7	VCCIO	I	Module I/O level voltage input		VIO voltage supply.
A8	VCC	I	Module supply voltage input		3.0-3.6 V module voltage supply.
B1	FSPICLK / GPIO36	I/O	SPI2 clock / General Purpose I/O	FSPICLK / GPIO36	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
B3	FSPICS0 / GPIO34	I/O	SPI2 Chip select / General Purpose I/O	FSPICS0 / GPIO34	Connected to internal PSRAM. Do not connect.

[2] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AI/AO=Analog Input/Output, NC=Not Connected

No.	NORA function	I/O[2]	Description	ESP32-S3 function	Remarks
					If required, connect only for external flash.
B4	GPIO18	I/O	General Purpose I/O	GPIO18	Analog-capable pin
B5		NC			
B6	XTAL_32K_N /LPO_IN GPIO16	I/O	32KHz external clock input / Low Power Oscillator Input / General Purpose I/O	GPIO16	Analog-capable pin
B7	VCCIO	I	Module I/O level voltage input		VIO voltage supply.
B9		NC			
C1	FSPIQ / GPIO37	I/O	SPI2 Master Input Slave Output / General Purpose I/O	FSPIQ / GPIO37	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
C2	FSPID / GPIO35	I/O	SPI2 Master Output Slave Input / General Purpose I/O	FSPID / GPIO35	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
C4	SPICS0	I/O	SPI0 Chip select	SPICS0 / GPIO29	CS, if external Flash is connected to SPI0.
C5		NC			
C6	XTAL_32K_P / GPIO15	I/O	32KHz external clock input / General Purpose I/O	GPIO15	Analog-capable pin. If external LPO is used at LPO_IN, put decoupling capacitor to GND on this pin only.
C8	GPIO21	I/O	General Purpose I/O	GPIO21	
C9	USB_P / GPIO20	I/O	USB differential data signal / General Purpose I/O	USB_D+ / GPIO20	Analog-capable pin. Default drive capability of this pin is ~40mA
D1	SPIWP	I/O	SPI0 Write Protect	SPIWP / GPIO28	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
D2	SPID	I/O	SPI0 Master Output Slave Input	SPID / GPIO32	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
D3	FSPIHD / GPIO33	I/O	SPI2 Hold / General Purpose I/O	FSPIHD / GPIO33	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
D7		NC			
D8	GPIO4	I/O	General Purpose I/O	GPIO4	Analog-capable pin, Touch button input
D9	USB_N / GPIO19	I/O	USB differential data signal / General Purpose I/O	USB_D- / GPIO19	Analog-capable pin. Default drive capability of this pin is ~40mA
E1	SPICS1	I/O	SPI Chip select / General Purpose I/O	SPICS1 / GPIO26	CE to internal PSRAM. Do not connect
E2	SPIQ	I/O	SPI0 Master Input Slave Output	SPIQ / GPIO31	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
E3	SPICLK_N / GPIO48	I/O	SPI Differential clock / General Purpose I/O	SPICLK_N / GPIO48	
E7	GPIO9	I/O	General Purpose I/O	GPIO9	Analog-capable pin, Touch button input
E8	GPIO1	I/O	General Purpose I/O	GPIO1	Analog-capable pin, Touch button input

No.	NORA function	I/O[2]	Description	ESP32-S3 function	Remarks
E9	GPIO7	I/O	General Purpose I/O	GPIO7	Analog-capable pin, Touch button input
F1	SPICLK	I/O	SPI0 clock	SPICLK / GPIO30	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
F2	SPIHD	I/O	SPI0 Hold	SPIHD / GPIO27	Connected to internal PSRAM. Do not connect. If required, connect only for external flash.
F3	SPICLK_P / GPIO47	I/O	SPI Differential clock / General Purpose I/O	SPICLK_P / GPIO47	
F7	GPIO0/ Boot	I/O	General Purpose I/O	GPIO0/ Boot	
F8	GPIO45	I/O	General Purpose I/O	GPIO45	
F9	GPIO6	I/O	General Purpose I/O	GPIO6	Analog-capable pin, Touch button input
G1	MTDO / GPIO40	I/O	JTAG Test Data Out /	MTDO / GPIO40	
G2	FSPIIO6 / GPIO12	I/O	SPI2 IO6 / General Purpose I/O	FSPIIO6 / GPIO12	Analog-capable pin, Touch button input
G3	FSPIIO5 / GPIO11	I/O	SPI2 IO5 / General Purpose I/O	FSPIIO5 / GPIO11	Analog-capable pin, Touch button input
G4		NC			
G5		NC			
G7		NC			
G8	U0TXD / GPIO43	I/O	UART data output / General Purpose I/O	U0TXD / GPIO43	
G9	U0RXD / GPIO44	I/O	UART data input / General Purpose I/O	U0RXD / GPIO44	
H1	JTAG_TDI / GPIO41	I/O	JTAG Test Data In (debug interface) / General Purpose I/O	MTDI / GPIO41	
H2	JTAG_TMS / GPIO42	I/O	JTAG Test Mode Select / General Purpose I/O	MTMS / GPIO42	
H3	FSPII04 / GPIO10	I/O	SPI2 IO5 / General Purpose I/O	FSPII04 / GPIO10	Analog-capable pin, Touch button input
H7	GPIO46	I/O	General Purpose I/O	GPIO46	
H8	GPIO2	I/O	General Purpose I/O	GPIO2	Analog-capable pin, Touch button input
H9	GPIO8	I/O	General Purpose I/O	GPIO8	Analog-capable pin, Touch button input
J1	VDD_SPI	O	SPI power supply: 3.3 V	VDD_SPI	Output voltage pin to be used only for external Flash/PSRAM. Otherwise, NC.
J2	JTAG_TCK / GPIO39	I/O	JTAG Test clock / General Purpose I/O	MTCK / GPIO39	
J3	RESET_N	I	External system reset input.	RESET	Active low
J4		NC			
J5		NC			
J7		NC			
J8	GPIO5	I/O	General Purpose I/O	GPIO5	Analog-capable pin, Touch button input
J9	GPIO3	I/O	General Purpose I/O	GPIO3	Analog-capable pin, Touch button input
K1		NC			

No.	NORA function	I/O[2]	Description	ESP32-S3 function	Remarks
K9	ANT	I/O	Antenna Tx/Rx interface	LNA_IN	50 Ω nominal characteristic impedance, only used with NORA-W101 modules. NC for NORA-W106
	EGP	-	Exposed Ground Pins		Exposed scattered grey pins on the module should be connected to GND
L1-M9	EAGP	-	Exposed Antenna Ground Pins		Exposed pins underneath the antenna area should be connected to GND

Table 5: NORA-W106-10B pin-out

4 Electrical specifications

⚠ Stressing the device above one or more of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC/ VCC_IO	Module supply voltage	Input DC voltage at VCC and VCC_IO pins	-0.3	3.6	V
$I_{VCC\ MAX}$ + $I_{VCC\_IO\ MAX}$	Absolute maximum power consumption			500	mA
DPV	Digital pin voltage	Input DC voltage at any digital I/O pin	-0.3	3.6	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		0	dBm
Tstr	Storage temperature		-40	+85	°C

Table 6: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification shown in Table 6 must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

Parameter	Min.	Typical	Max.	Unit	Remarks
ESD immunity			±8*	kV	Indirect discharge according to IEC 61000-4-2
ESD sensitivity, tested for all pins except ANT and RSVD pins #11, #15, #33			2.5	kV	Human body model according to JEDEC JS001

* Tested on EVK-NORA-W10 evaluation board.

Table 7: Maximum ESD ratings

⚠ NORA-W10 series modules are Electrostatic Sensitive Devices, which means that some special precautions must be observed when handling them. See also ESD precautions.

4.2 Operating conditions

⚠ Operation beyond the specified operating conditions is not recommended and extended exposure beyond them can affect device reliability.

☞ Unless otherwise specified, all operating condition specifications are at an ambient temperature of 25 °C and at a supply voltage of 3.3 V.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Operating temperature	-40	+85	°C
Operating temperature (NORA-W10x-10B) [1]	-40	+65	°C

[1] Enabling the PSRAM ECC function reduces the size of PSRAM by 1/16 and extends maximum ambient temperature is 85°C.

Table 8: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC	Input supply voltage	Ambient temperature -40 °C to +85 °C	3.00	3.30	3.60	V
VCC_IO	I/O reference voltage	Ambient temperature -40 °C to +85 °C	3.00	3.30	3.60	V

Table 9: Input characteristics of voltage supply pins

4.2.3 RESET_N pin

Figure 3 shows the conditions for **VCC** and **RESET_N** timing during start-up and reset duration. The pin characteristics are described in Table 10.

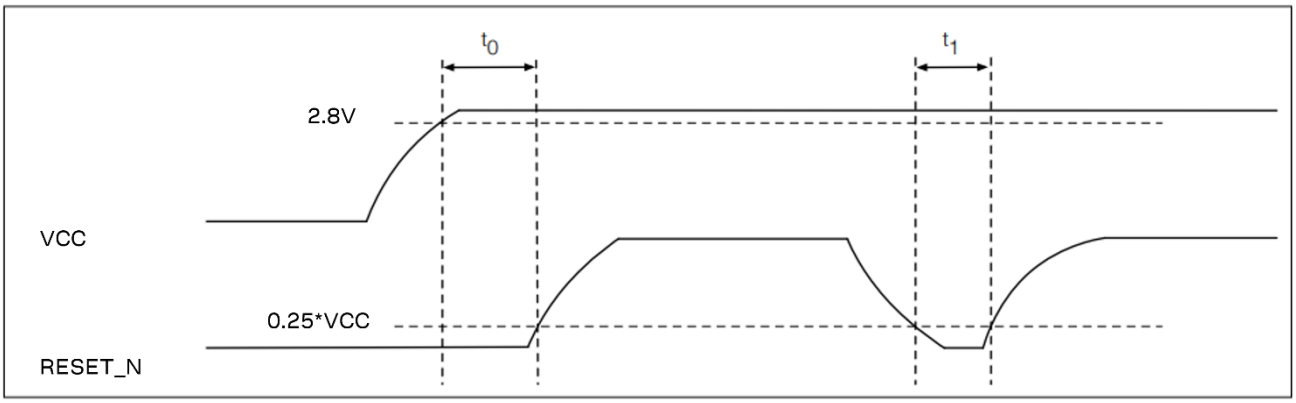


Figure 3: Module power-up and reset timing

Pin name	Parameter	Min	Typ	Max	Unit
RESET_N	Low-level input	-0.3		0.3*VCC	V
	Internal pull-up resistance		45		kΩ
	Internal capacitance		10		nF
t_0	Time from VCC valid input level 2.8 V to RESET_N release reaches 0.25*VCC	50	1000		µs
t_1	Duration of RESET_N pin < low level input 0.25*VCC, to trigger hardware reset	50			µs

Table 10: RESET_N pin characteristics.

☞ In case of slow ramp-up, frequent power on and off, or unstable power supply (e.g., battery charging, photovoltaic systems) consider using an external reset chip or a watchdog timer IC set to around 3.0 V to boot correctly.

4.2.4 LPO clock

NORA-W10 series modules do not have an internal low power oscillator (LPO) or crystal for low power modes. If low power modes are required, the LPO signal can be supplied to the **LPO_IN** pin from an external oscillator. Alternatively, an external low frequency crystal can also be attached to **XTAL_32K_N** and **XTAL_32K_P** pins. The amplitude range is 0.6 V < Vpp < **VCC_IO**. If the input signal is square wave the bottom voltage should be higher than 200 mV.

Symbol	Parameter	Min	Typ	Max	Unit
LPO	Input clock frequency		32.768		kHz
	Input slow clock accuracy (Initial + temp + aging)			±150	ppm
Tr/Tf	Input transition time Tr/Tf -10% to 90%			100	ns
	Frequency input duty cycle	20	50	80	%

Symbol	Parameter	Min	Typ	Max	Unit
VIH	Input voltage limits (Square wave, DC-coupled)			VCC_IO	V
VIL		0		0.6	V
	Input capacitance			10	pF

Table 11: External LPO clock characteristics

4.2.5 Digital pins

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
Any digital pin	Input characteristic: Low-level input	0		0.3*VCC_IO	V	
	Input characteristic: high-level input	0.7*VCC_IO		VCC_IO	V	
	Output characteristic: Low-level output	0		0.4	V	
	Output characteristic: High-level output	VCC_IO-0.4		VCC_IO	V	
	Drive capability			20	mA	Source/Sink
	Pull-up/pull-down resistance		45		kΩ.	
Signals rerouted through the IO MUX	Output signal speed			20	MHz	
	Input signal speed			10	MHz	The GPIO matrix delays the input signals by two cycles of the AHB clock, which typically introduces an 80 MHz -> 25 ns delay.

Table 12: Digital pin characteristics

4.2.6 Current consumption

The typical current consumption of a NORA-W10 module is shown in Table 13. The current consumption is highly dependent on the application implementation. All measurements taken with 3.3 V supply at 25 °C.

☞ The current consumption figures are inherited from the Espressif ESP 32-S3 data sheet [3].

Power mode	Activity	Typ	Unit	Remarks
Wi-Fi	Wi-Fi Tx 802.11b 1Mbps @ 20 dBm	340	mA	100% duty cycle
	Wi-Fi Tx 802.11g 54Mbps @ 17 dBm	291	mA	
	Wi-Fi Tx 802.11n HT20 MCS7 @ 16.5 dBm	286	mA	
	Wi-Fi Rx 802.11b/g/n HT20	88	mA	
Bluetooth LE	Bluetooth Tx Pout 0 dBm	220	mA	100% duty cycle
	Bluetooth Rx and listening	76	mA	
Modem-sleep mode	CPU speed 240 MHz, dual core	66.2	mA	Immediate wake-up
	CPU speed 160 MHz, dual core	49.6	mA	
	CPU speed 80 MHz, dual core	33.1	mA	
Light-sleep mode	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high impedance.	240	µA	
Deep-sleep mode	RTC memory and RTC peripherals are powered on	8	µA	
	RTC memory is powered on. RTC peripherals are powered off	7	µA	
Power off mode	CHIP_PU is set to low level. The chip is powered off	1	µA	

Table 13: Current consumption during typical use cases

4.2.7 Wi-Fi characteristics and absolute maximum radio performance

V_{CC} = 3.3 V, T_{amb} = 25 °C

Parameter	Operating mode	Specification	Unit
RF frequency range	802.11b/g/n	2.400 – 2.484	GHz
Modulation	802.11b	CCK and DSSS	
	802.11g/n	OFDM	
Supported data rates	802.11b	1, 2, 5.5, 11	Mbit/s
	802.11g	6, 9, 12, 18, 24, 36, 48, 54	Mbit/s
	802.11n	MCS0 – MCS7	
Supported bandwidth	802.11n	20,40	MHz
Supported guard interval	802.11n	400, 800	ns

Table 14: Wi-Fi radio characteristics

⚠ NORA-W10 series modules support Wi-Fi 802.11b/g/n operation in the 2.4 GHz band. Maximum transmitter output power values are supported only in certain regions – depending upon the certification approval. For typical radio performance data, see Radio performance.

Table 15 shows the maximum (conducted) transmitter output power and receiver sensitivity for supported modes of operation.

Parameter	Operating mode	Data rate	Specification (dBm)	Bandwidth	802.11 EVM limit (dBm)
Conducted Transmit Power	802.11b	1 Mbit/s	20* ± 1	20 MHz	-21 dBm
		11 Mbit/s	20* ± 1		-21 dBm
	802.11g	6 Mbit/s	19* ± 1	20 MHz	-20 dBm
		54 Mbit/s	16* ± 1		-26.5 dBm
	802.11n	MCS0	19* ± 1	20 MHz	-21.5 dBm
		MCS7	16* ± 1		-28.5 dBm
		MCS0	19* ± 1	40 MHz	-23.5 dBm
		MCS7	16* ± 1		-28.5 dBm
Receiver Sensitivity	802.11b	1 Mbit/s	-97.5 ± 2	20 MHz	N/A
		11 Mbit/s	-88.5 ± 2		N/A
	802.11g	6 Mbit/s	-93 ± 2	20 MHz	N/A
		54 Mbit/s	-76 ± 2		N/A
	802.11n	MCS0	-92.5 ± 2	20 MHz	N/A
		MCS7	-74 ± 2		N/A
		MCS0	-90 ± 2	40 MHz	N/A
		MCS7	-71 ± 2		N/A

* There is lower output power on band edge channels

Table 15: Wi-Fi radio maximum transmitter and receiver power parameter

⚠ Maximum transmitter output power values are supported only in certain regions – depending upon the certification approval. For typical radio performance data, see Radio performance.

4.2.8 Bluetooth Low Energy characteristics and absolute maximum radio performance

V_{CC} = 3.3 V, T_{amb} = 25 °C

Parameter	Specification	Unit
RF Frequency Range	2.400 – 2.4835	GHz
Supported Modes	Bluetooth v5.0	
Number of channels	40	
Modulation	GFSK	
Transmit Power (conducted)	20 ± 1	dBm
Receiver Sensitivity	-98 ± 2	dBm

Table 16: Bluetooth Low Energy characteristics

⚠ Maximum transmitter output power value is only supported in certain regions, depending upon the certification approval. For typical radio performance data, see Radio performance.

4.2.9 Antenna radiation patterns

Figure 4 provides an overview of the measurement procedure and describes how the NORA-W106 module is aligned to the XYZ-coordinate system. A measurement is taken at every dotted position above the module image (shown left). Each measurement is represented as a grid point in the radiation pattern (shown right).

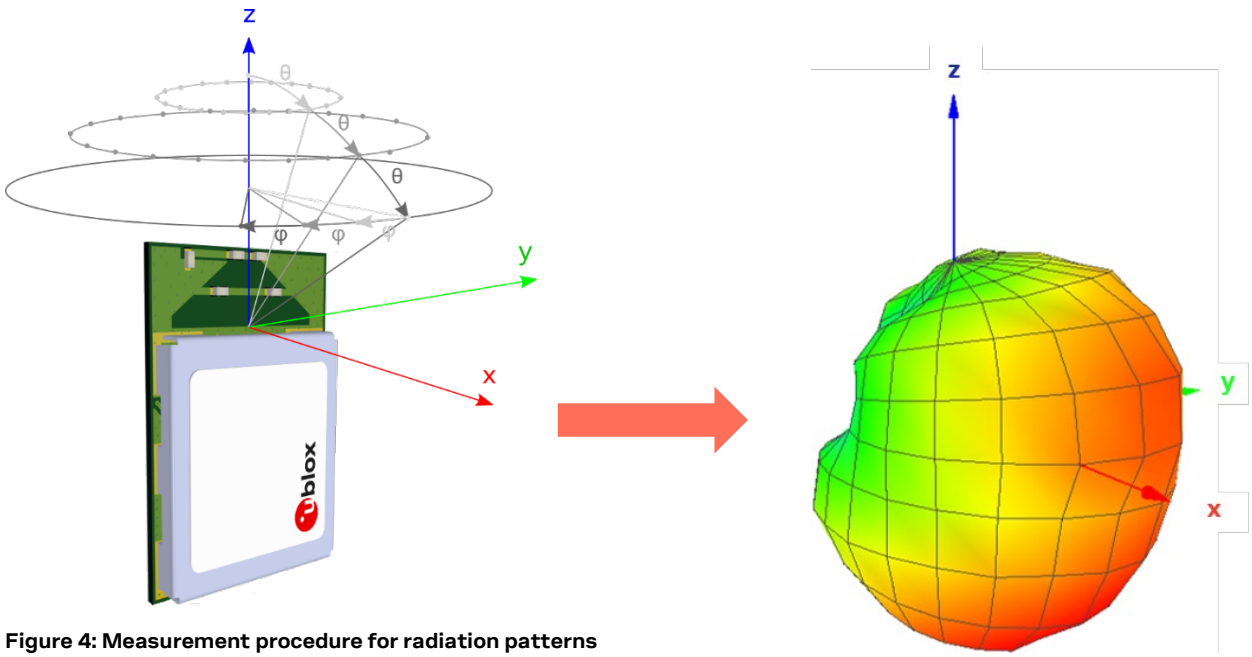
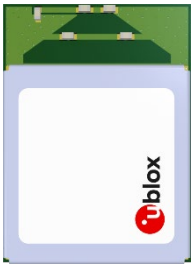
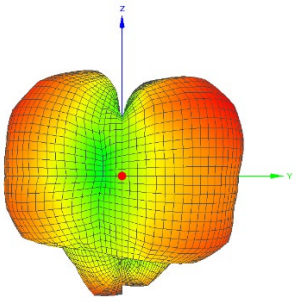
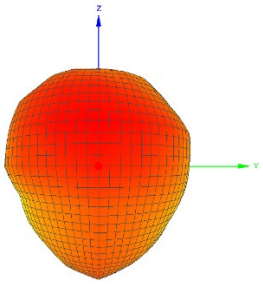
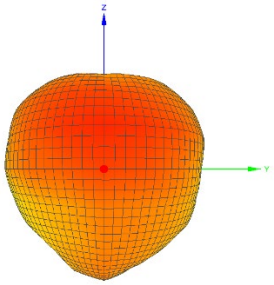
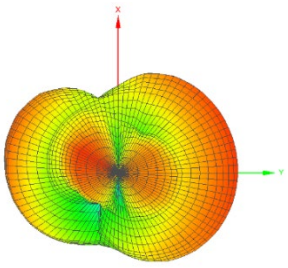
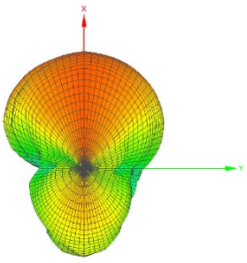
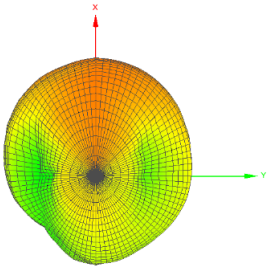
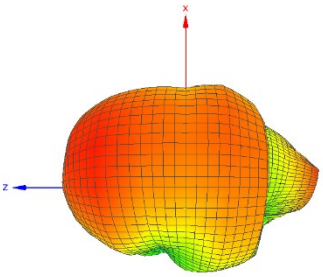
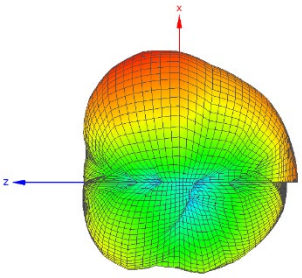
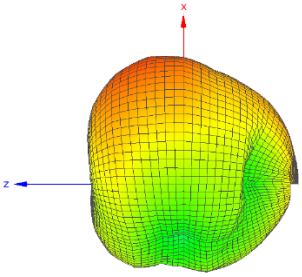


Figure 4: Measurement procedure for radiation patterns

Table 17 shows the displayed radiation patterns of the internal PCB trace antenna on NORA-W106.

View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 - -10 -2,5 5		
Top view, YZ plane positive X direction 			
Side view, XY plane negative Z direction 			
Side view, XZ plane negative Y direction 			
	Antenna Gain (dBi) -25 - -10 -2,5 5		

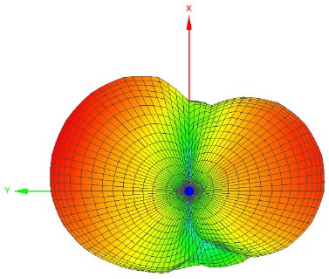
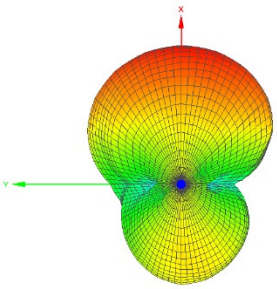
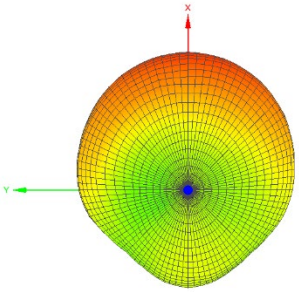
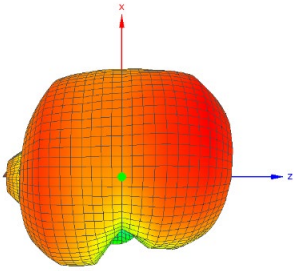
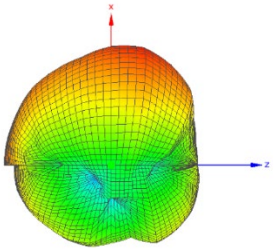
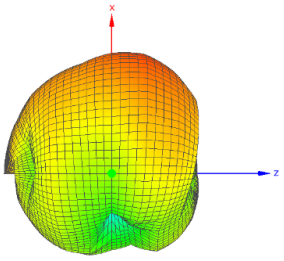
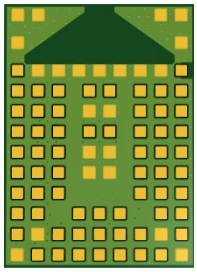
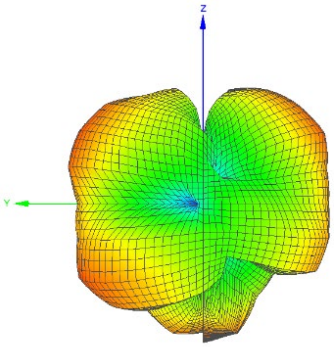
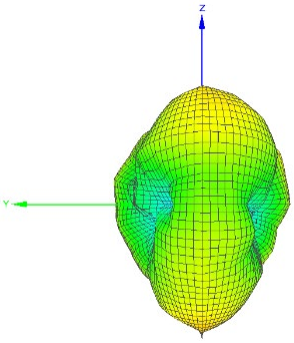
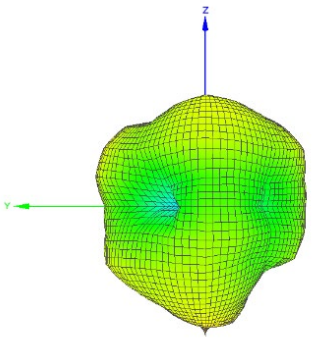
View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
Side view, XY plane positive Z direction 			
Side view, XZ plane positive Y direction 			
Bottom view, YZ plane negative X direction 			

Table 17: NORA-W106 antenna radiation patterns

5 Mechanical specifications

5.1 NORA-W101/W106 mechanical specifications

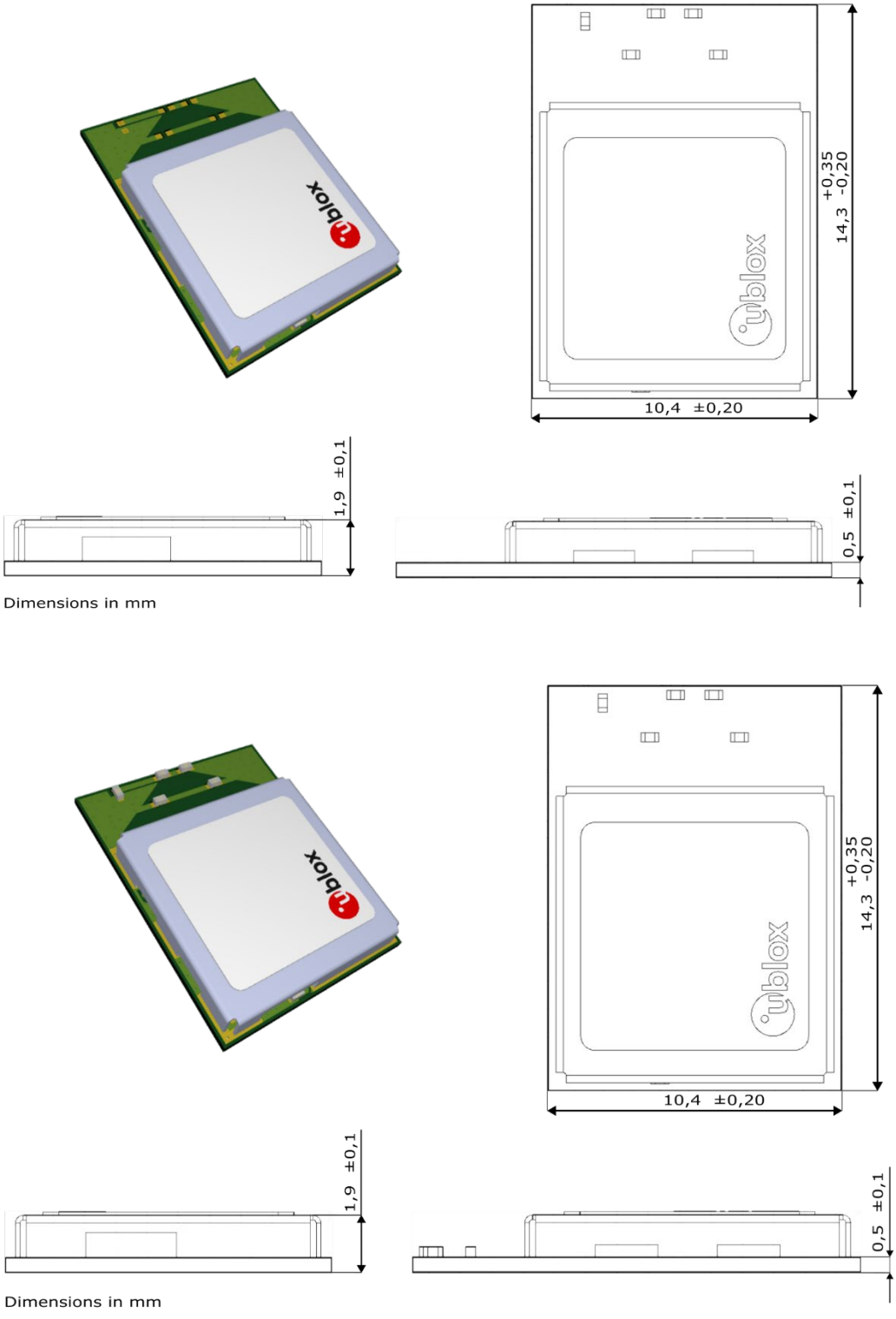


Figure 5: NORA-W106 and NORA-W101 dimensions

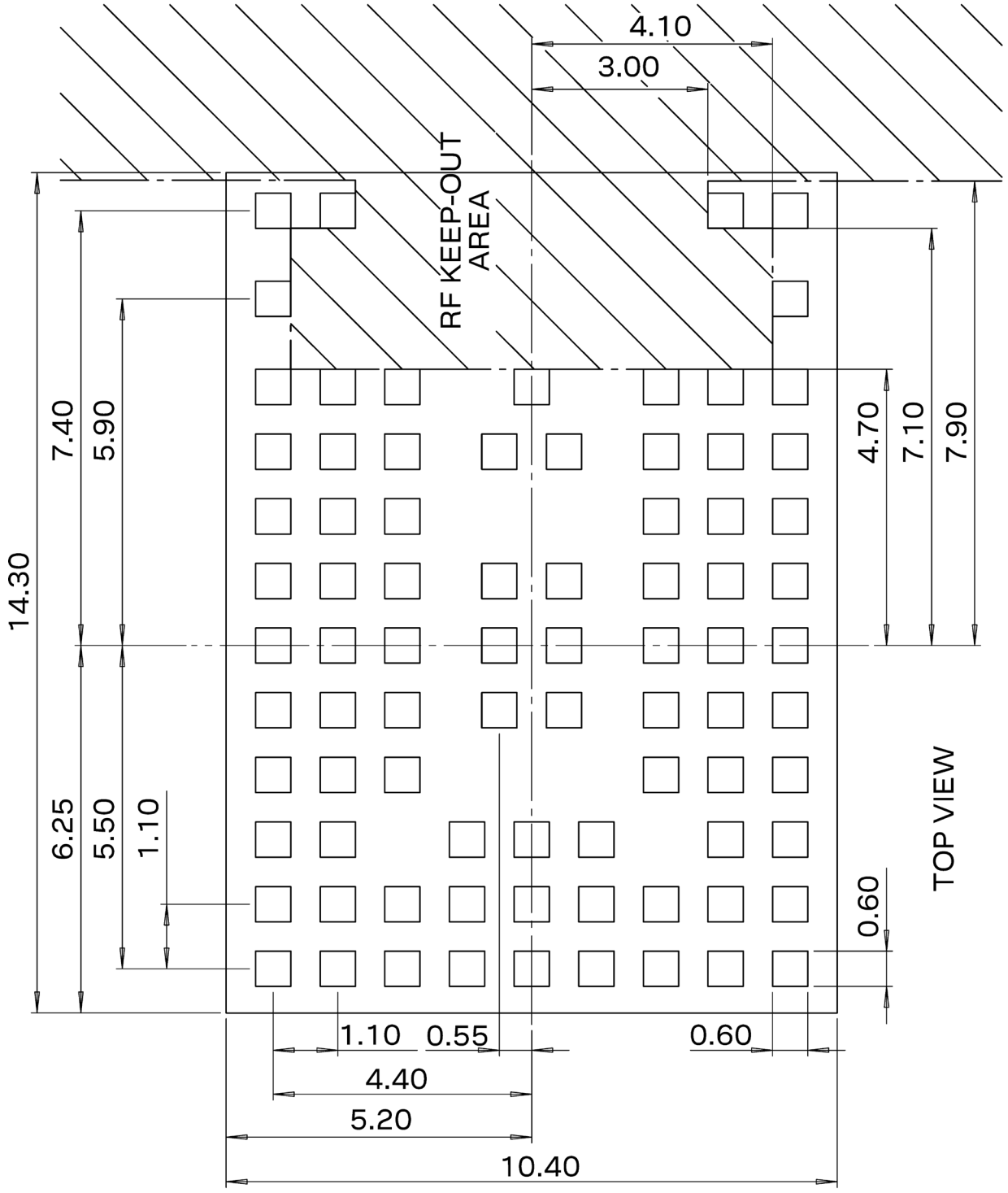


Figure 6: NORA-W101 mechanical outline

6 Qualification and approvals

6.1 Country approvals

The NORA-W10 module series will be certified for use in the following countries/regions:

Country/region	NORA-W101	NORA-W106
Europe (RED)	Approved	Approved
Great Britain (UKCA)	Approved	Approved
USA (FCC)	Approved	Approved
Canada (IC)	Approved	Approved
Japan (MIC)	Approved	Approved
Taiwan (NCC)	Pending	Pending
South Korea (KCC)	Approved	Approved
Brazil (ANATEL)	Approved	Approved
Australia and New Zealand (ACMA)	Approved	Approved
South Africa (ICASA)	Pending	Pending

Table 18: Country approvals for NORA-W10

For detailed information about the regulatory requirements that must be met when using NORA-W10 modules in an end product, see the NORA-W10 system integration manual [1].

6.2 Bluetooth qualification information

End products must be qualified and listed with the Bluetooth Special Interest Group (SIG). Product declarations are submitted through the SIG Bluetooth Launch Studio website.

NORA-W10 module series are qualified as a Controller Subsystem in accordance with the Bluetooth 5.0 specification and are registered with the SIG Qualified Design IDs (QDID) shown in Table 19.

To list your product that integrates NORA-W101 or NORA-W106 with no additional testing required, combine the QDID for the Bluetooth stack implemented in the Host Subsystem with the QDID of the pre-qualified Controller Subsystem shown in Table 19.

Model	Product type	QDID	Listing date
NORA-W101, NORA-W106	Controller subsystem	198070	14-Nov-2022

Table 19: NORA-W101/NORA-W106 Bluetooth QD ID

The Espressif IoT development framework for ESP-IDF currently supports two host Bluetooth stacks: Bluedroid and Apache NimBLE for Bluetooth LE. For further listing information, search the Bluetooth Launch Studio website.

7 Product handling

7.1 Packaging

NORA-W10 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. See also the Product packaging guide [2].

7.1.1 Reels

NORA-W10 modules are delivered in quantities of 500 pieces on a reel. The reel types for NORA-W10 modules are shown in Table 20. See also the Product packaging guide [2].

Model	Reel type
NORA-W101	A3
NORA-W106	A3

Table 20: Reel types for different NORA-W10 series modules

7.1.2 Tapes

Figure 7 and Figure 8 show the position and orientation of NORA-W10 modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 7 and Figure 8.

Figure 7: NORA-W101 module on tape orientation

Figure 8: NORA-W106 module on tape orientation

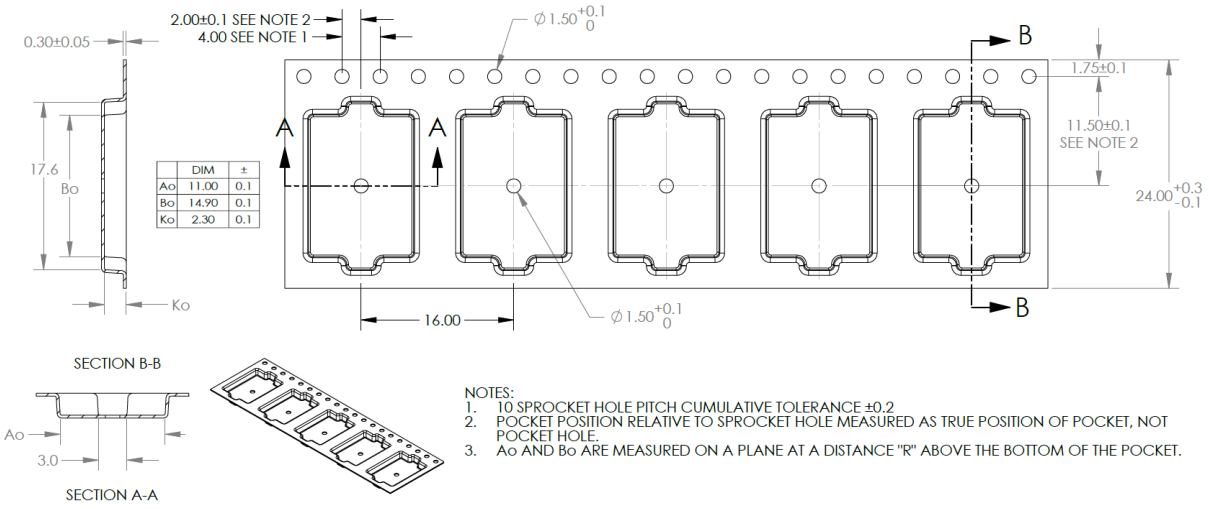


Figure 9: NORA-W101/NORA-W106 tape dimensions

7.2 Moisture sensitivity levels

NORA-W10 modules are rated as Moisture Sensitivity Level (MSL) Level 4 devices in accordance with the IPC/JEDEC J STD-020 standard. For more information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 168 hours in factory conditions of maximum 30 °C/60% RH or must be stored at less than 10% RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033 standard.

For more information regarding MSL (Moisture Sensitivity Level), labeling, and storage, see also the Product packaging guide [2].

7.3 Reflow soldering

NORA-W10 modules are approved for single reflow processes only.

⚠ Reflow profiles must be selected in accordance with u-blox soldering recommendations described in the NORA-W10 system integration manual [1]. Failure to observe these recommendations can result in severe damage to the device.

7.4 ESD precautions

NORA-W10 modules are Electrostatic Sensitive Devices (ESD) that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the module. ESD precautions are also relevant when handling the application board on which the module is mounted.

For further information about the handling of NORA-W10 modules, see also the system integration manual [1].

8 Labeling and ordering information

8.1 Product labeling

The labels (8x8 mm) of the NORA-W10 series modules described in the section include important product information.

Figure 10 shows the label of all the NORA-W10 series modules, which includes product type number and revision, production date, and data matrix that bears a unique serial number and the u-blox logo.

All units in mm unless specified otherwise stated.

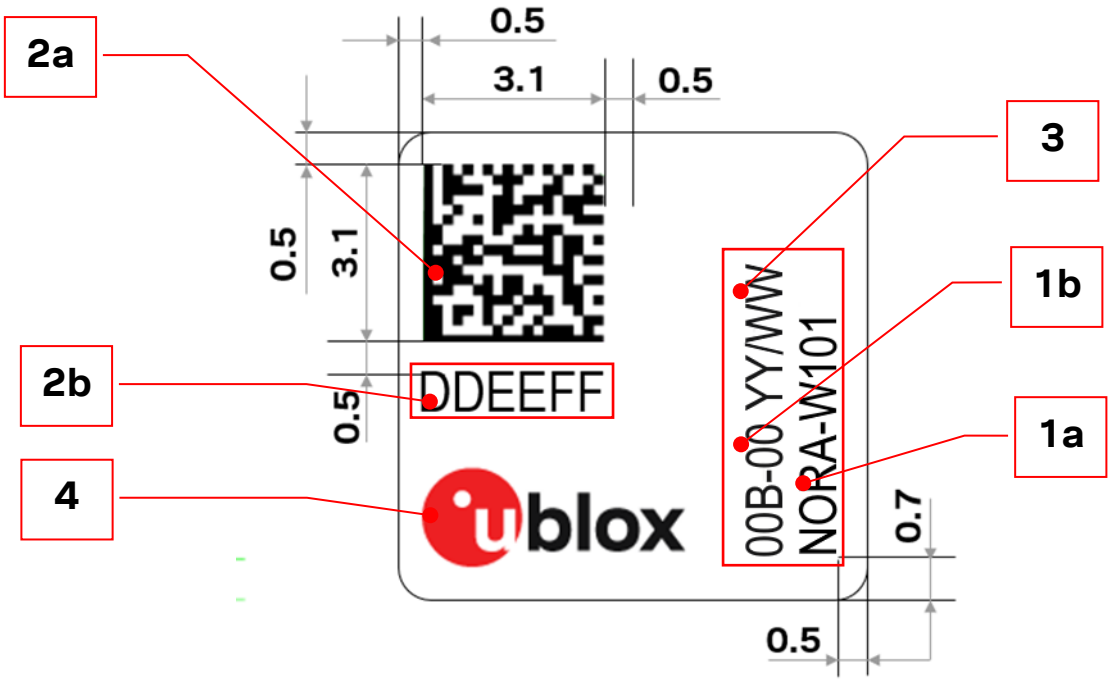


Figure 10: Location of product type number on the NORA-W10 series module label

Reference	Description
1a	Text box containing Product Name and approval ID:s (Applicable model names: NORA-W1xx).
1b	Product type number.
2a	Data Matrix with unique serial number comprising 19 alphanumeric digits: (product identifier, serial number, datacode) • Product identifier: 3 digits, used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant • Serial number: 12 digits, Unique MAC address assigned during module production. • Datacode: 4 digits, Represent the hardware and firmware version encoded.
2b	The six last hex symbols of the MAC address (AABBCC**DDEEFF**).
3	Date of production encoded YY/WW (year/week).
4	u-blox logo. The red dot also indicates pin 1.

Table 21: NORA-W10 series label description

8.2 Product identifiers

Table 22 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade	PPPP-TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 22: Product code formats

8.3 Identification codes

Table 23 describes the individual identification codes represented in each product identifier.

Code	Meaning	Example
PPPP	Form factor	NORA
TG	Platform (Technology and Generation) T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth G – Generation	W1: Wi-Fi Generation 1
VV	Variant based on the same platform; range [00…99]	01: product with antenna pin
TT	Major Product Version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 23: Part identification code

8.4 Ordering information

Ordering code	Product
NORA-W101-00B	Module with antenna pin. Open CPU version. Using ESP32-S3FN8.
NORA-W106-00B	Module with internal PCB trace antenna. Open CPU version integrating ESP32-S3FN8. This version includes 8 MB embedded flash and Quad SPI.
NORA-W106-10B	Module with internal PCB trace antenna. Open CPU version integrating ESP32-S3R8. This version includes embedded 8 MB PSRAM and octal SPI. It is also specified for operating temperatures up to 85°C – with PSRAM ECC enabled.

Table 24: Product ordering codes

See also Product variants.

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
BPF	Band Pass Filter
BR/EDR	Basic rate/Enhanced data rate
CAN	Controller Area Network
CTS	Clear To Send
DAC	Digital to Analog Converter
DC	Direct Current
D/C	Don't Care
DSR	Data Set Ready
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Industry Canada
LCD	liquid crystal display
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
LPO	Low Power Oscillator
MCU	Micro Controller Unit
MDIO	Management Data Input / Output
MII	Media-Independent Interface
MIMO	Multi-Input Multi-Output
MRD	Market Requirement Document
MSD	Moisture Sensitive Device
N/A	Not Applicable
PCN	Product Change Notification
RTS	Request To Send
RXD	Receive Data
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SPI	Serial Peripheral Interface
TBD	To Be Defined
TWAI	Two-wire Automotive Interface
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter

Table 25: Explanation of the abbreviations and terms used

Related documents

[1] NORA-W10 series system integration manual, UBX-17005730
[2] u-blox package information guide, UBX-14001652
[3] Espressif System ESP32-S3 Datasheet, version 3.6
[4] NORA-W10 EU declaration of conformity, UBX-18007184
[5] NORA-W10 UKCA declaration of conformity, UBX-22040048
[6] NORA-W10 series product summary, UBX-17051775
[7] NORA-B1 data sheet, UBX-20027119

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	03-May-2021	asoh	Initial release of the Data Sheet for NORA-W10 series with open CPU architecture.
R02	09-Mar-2023	asoh, hekf	Added TX/RX output power, current consumption and Total Radiated Power updates in Wi-Fi radio characteristics and absolute maximum radio performance. Revised Bluetooth Low Energy characteristics and absolute maximum radio performance. Added table data for RESET_N pin. Revised Disclosure restriction class and product status in Document information. Revised table data in Boot strap pins and Country approvals, and included other miscellaneous changes throughout. Updated Mechanical specifications, Product labeling and contact information. Included typical values for Current consumption.
R03	22-Jun-2023	hekf	Added product NORA-W106-10B in Document information and in Ordering information. Added NORA-W106-10B description in Product variants with table data describing the Operating temperature range for each variant.
R04	19-Dec-2023	hekf	Updated Country approvals.

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

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NORA-W106-00B NORA-W101-00B NORA-W106-10B