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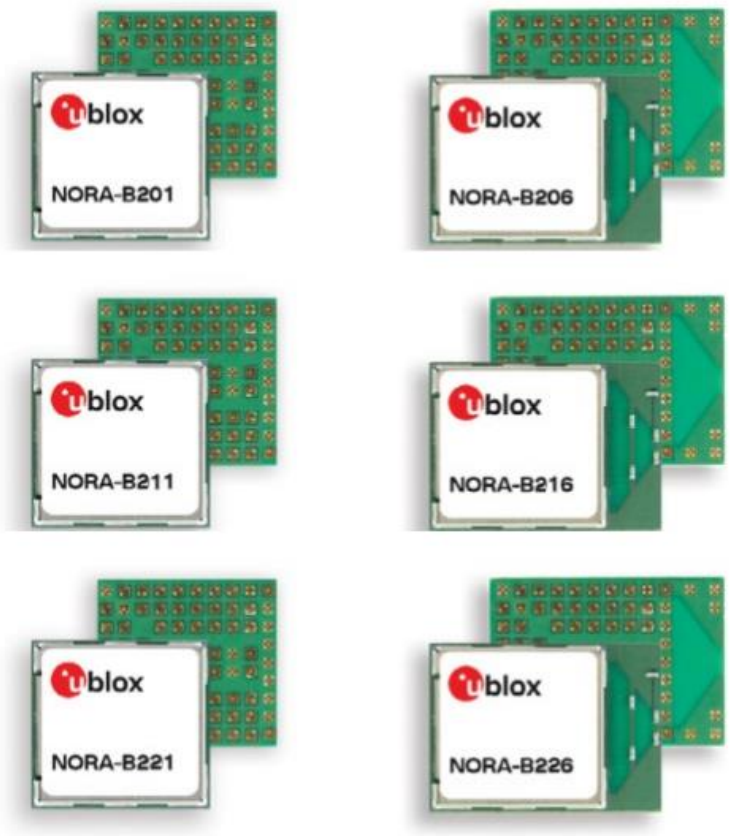
NORA-B2 series

Stand-alone Bluetooth® Low Energy and IEEE 802.15.4 module

Data sheet



Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for the NORA-B2 series stand-alone Bluetooth® Low Energy and IEEE 802.15.4 modules. OEMs can embed their own application in conjunction with the Zephyr RTOS (Real -Time Operating System) integrated into the Nordic Semiconductor nRF Connect SDK.

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Mass production/ End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product Status
NORA-B201	NORA-B201-00B-00	N/A	N/A	Engineering sample
NORA-B206	NORA-B206-00B-00	N/A	N/A	Engineering sample
NORA-B211	NORA-B211-00B-00	N/A	N/A	Engineering sample
NORA-B216	NORA-B216-00B-00	N/A	N/A	Engineering sample
NORA-B221	NORA-B221-00B-00	N/A	N/A	Engineering sample
NORA-B226	NORA-B226-00B-00	N/A	N/A	Engineering sample

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1 Functional description

1.1 Overview

Based on the Nordic Semiconductor nRF54L15, nRF54L10 ,and nRF54L05 Bluetooth® LE System on Chip (SoC), the NORA-B2 series of small stand-alone modules includes Arm® Cortex®-M33 processor, which provides a floating-point unit (FPU), digital signal processor (DSP) instruction set, and CryptoCell™-312 security architecture. It also features a 128 MHz RISC-V coprocessor and scalable memory configurations of up to 1.5 MB NVM and up to 256 KB RAM.

Supporting a 2.4 GHz radio, NORA-B2 features Bluetooth® Channel Sounding, LE Audio, and 802.15.4-2020 standards such as Thread, Matter, and Zigbee. It also supports a proprietary 2.4 GHz operational mode that provides up to 4 Mbps for higher throughput. NORA-B2 is tested and verified against Bluetooth® 6.0 Core.

Offering high-speed communication for multiple connected peripherals over SPI, QSPI, TWI, ADC, and PWM interfaces, NORA-B2 series operate at ambient temperatures of up to 85 °C.

The modules offer multiple antenna options, including antenna pin and on-board PCB trace antenna options. For more information about the antennas that are approved for use with the NORA-B2 series, see also the system integration manual [1].

1.2 Applications

NORA-B2 series modules provide scalable solutions for a broad range of market segments, including smart cities and buildings, industrial automation, telematics, medical, and healthcare.

Specific application areas include:

- Industrial automation
- Advanced wearables
- Smart buildings and cities
- Low-power sensors
- Wireless-connected and configurable equipment
- Point-of-sale
- Medical and health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking

1.3 Block diagram

Figure 1 shows the integration of the nRF54Lxx and other logical components in NORA-B2 modules.

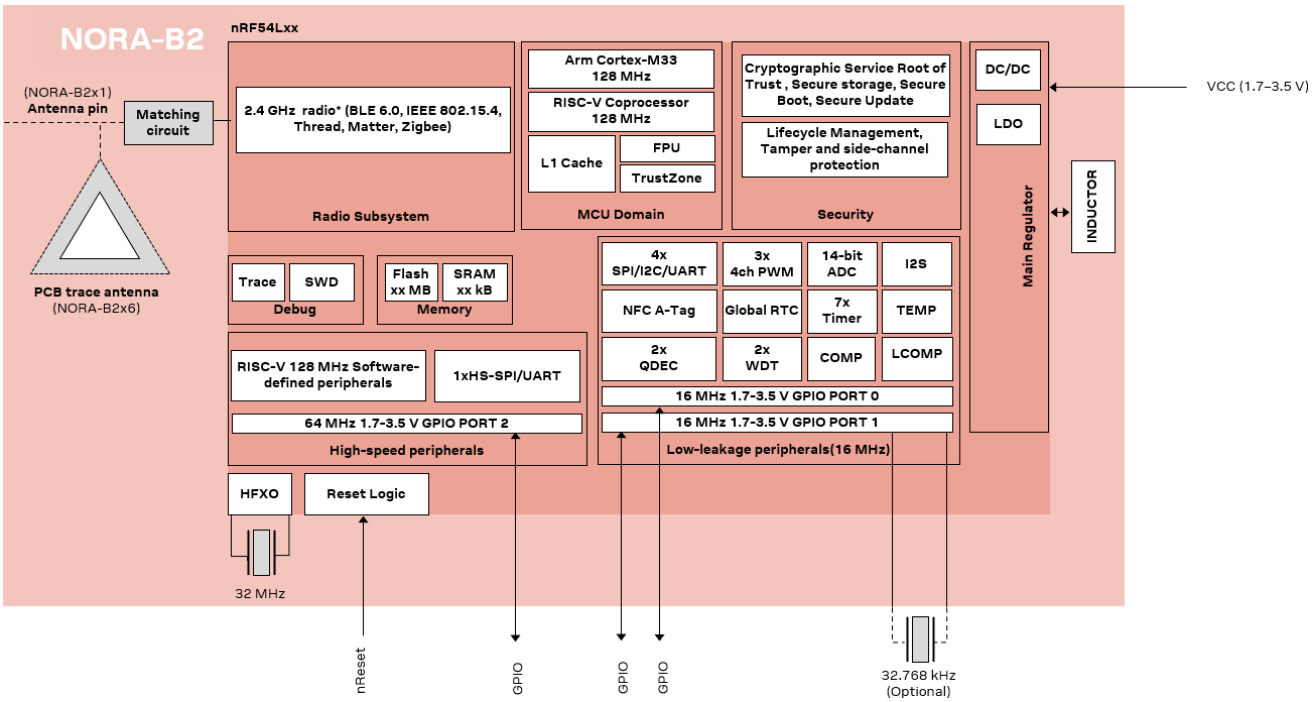


Figure 1: Block diagram of NORA-B2 series

1.4 Product variants

The NORA-B2 series modules come with two different antenna options. NORA-B2x1 supports an antenna pin for use with external antennas, while NORA-B2x6 includes an integrated PCB antenna. All product variants are professional grade.

Table 1 describes the main differences between the NORA-B2 various module variants.

Variants	CPU	Antenna	RAM	Flash	Weight [g]	Dimensions [mm]
NORA-B201	nRF54L15	Pin	256 kB	1.5 MB	<1	11.2 x 10.4 x 1.9
NORA-B206	nRF54L15	PCB trace	256 kB	1.5 MB	<1	14.3 x 10.4 x 1.9
NORA-B211	nRF54L10	Pin	192 kB	1.0 MB	<1	11.2 x 10.4 x 1.9
NORA-B216	nRF54L10	PCB trace	192 kB	1.0 MB	<1	14.3 x 10.4 x 1.9
NORA-B221	nRF54L05	Pin	96 kB	0.5 MB	<1	11.2 x 10.4 x 1.9
NORA-B226	nRF54L05	PCB trace	96 kB	0.5 MB	<1	14.3 x 10.4 x 1.9

Table 1: NORA-B2 variants exact characteristics summary

1.5 Product Description

Table 2 describes the common characteristics supported by all NORA-B2 module variants.

Item	NORA-B2xx-00B
CPU	Nordic Semiconductor nRF54Lxx
Operating temperature	–40 to +85 °C
Operating voltage	+1.7 to +3.5 VDC
Available GPIO	31 pins
Core	Arm Cortex-M33 with TrustZone technology
Operating speed	128 MHz or 64 MHz
Floating point unit (FPU)	Single precision with DSP instructions
Debug	Data Watchpoint and Trace (DWT), Embedded Trace Microcells (ETM), Instrumentation Trace Macrocell (ITM), Cross Trigger Interface (CTI), Serial Wire Debug (SWD)
Security	TrustZone®, isolation, tamper detection, and cryptographic engine side-channel leakage protection
Peripherals (not all simultaneous)	SPI: up to 5 main node or sub-node instances with EasyDMA UART: up to 5 instances with RTS/CTS flow control and EasyDMA I2C (TWI): up to 5 main node or sub-node instances with EasyDMA I2S: 2 instances ADC with up to 8 programmable gain channels PWM: up to 3 instances, 4 channels each. NFC tag: 1 instance QDEC: 2 instances Comparator and low-power comparator with wake-up from System OFF mode Timer/counter: up to 7 instances, 32-bit GRTC, 25 bit
Radio	
Supported 2.4 GHz radio modes	Bluetooth LE tested and verified against Bluetooth Core 6.0 IEEE 802.15.4 proprietary modes
Bluetooth Low Energy specification	
Operating channels and frequencies	40 channels, channel numbers 0–39, 2402–2480 MHz
Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps (Coded PHY, S=2) 125 kbps (Coded PHY, S=8))
Typical conducted output power	+7.0 dBm
Radiated output power *	+10 dBm
Conducted RX sensitivity, 1 Mbps	-94 dBm
Conducted RX sensitivity, 2 Mbps	-91 dBm
Conducted RX sensitivity, long range 500 kbps (Coded PHY, S=2)	-97 dBm
Conducted RX sensitivity, long range 125 kbps (Coded PHY, S=8)	-102 dBm
IEEE 802.15.4	
Operating channels and frequencies	16 channels, channel numbers 11-26, 2405–2480 MHz
IEEE 802.15.4 data rate	250 kbps
Conducted RX sensitivity, 250 kbps	-100 dBm
Other	Proprietary 2.4 GHz – 4 Mbps, 2 Mbps, and 1 Mbps

*RF power including maximum antenna gain (3 dBi)

Table 2: NORA-B2 series common characteristics summary

1.6 Software

The Open CPU architecture of NORA-B2 series modules allows integrators to develop and run their own applications on the built-in Arm® Cortex®-M33 core. u-blox recommends the Nordic Semiconductor nRF Connect SDK [5] for development.

The nRF Connect SDK integrates the Zephyr Real-Time Operating System (RTOS), MCUboot secure bootloader, and Nordic Semiconductor's nrfxlib device drivers for the nRF54Lxx and peripherals.

2 Interfaces

NORA-B2 supports a wide range of connectivity options, including a 2.4 GHz radio with an antenna connection, digital and analog I/O, and debug capabilities. The module provides full access to all GPIOs and peripheral interfaces available on the embedded nRF54Lxx, ensuring seamless integration into customer applications. For more information regarding function and use, see also the nRF54Lxx datasheet [4].

2.1 Peripherals power domains

NORA-B2 features multiple Power Domains (PD) for low-power operation, including fast MCU and lower speed domains. Figure 2 shows the power domains supplying the integrated ARM Cortex processor, peripherals, and other functional units supported in NORA-B2, which feature:

- Different domains running at different speeds
- Each domain mapped to one low-power Advanced Peripheral Bus (APB) that can be powered independently to connect peripherals to the system
- EasyDMA traffic from each domain aggregated in a local AMBIX interconnect that can access RAMs in the fast MCU power domain.

Three of the power domains have their own GPIO ports. The GPIO pins can be used by peripherals in the same power domain. Several port2 pins, **P2.00-P2.10**, can be used for selecting serial interfaces in the peripheral domain, as described in Table 8. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

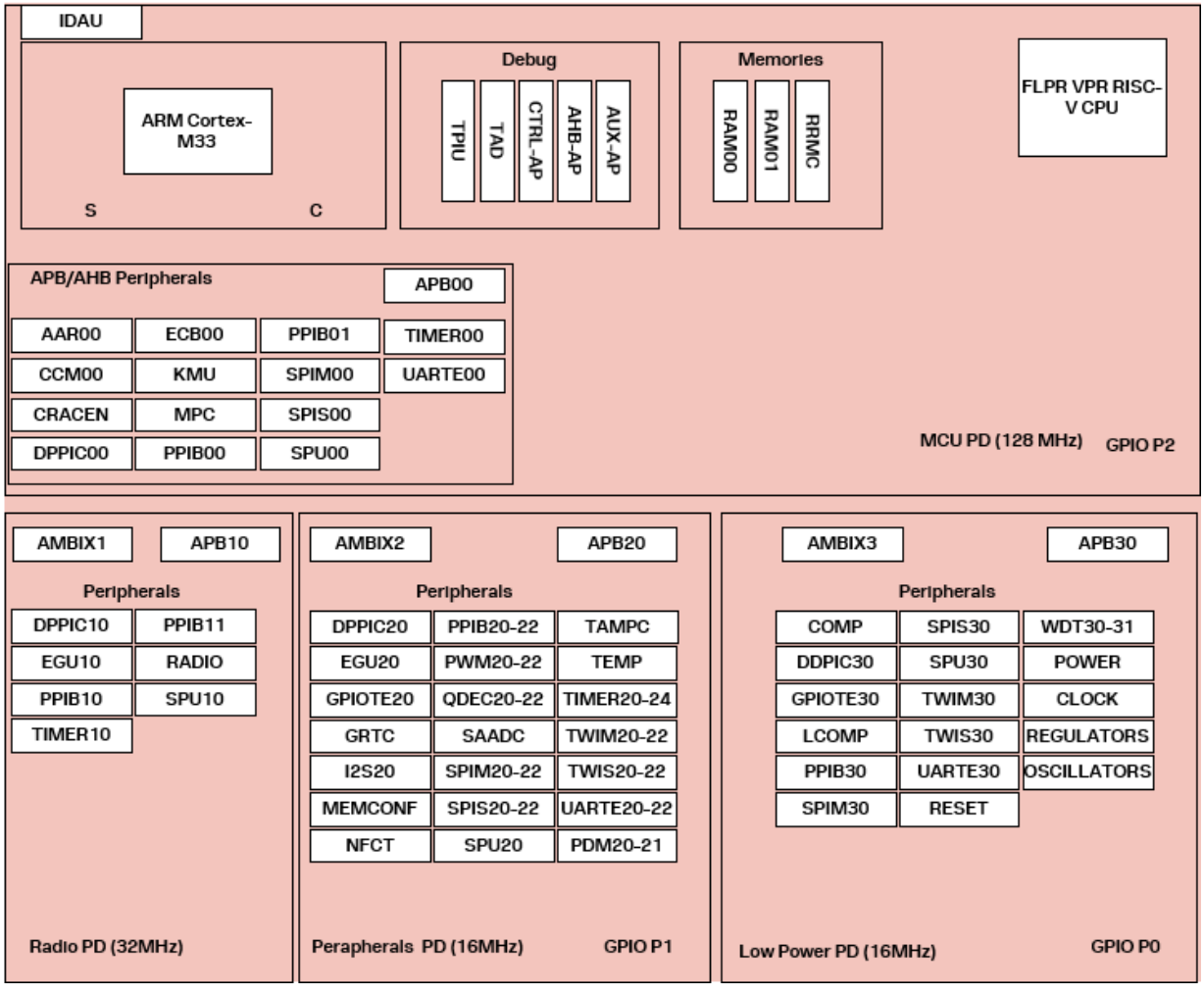


Figure 2: Power domains

2.1.1 Fast MCU domain

The fast MCU domain powers the Arm Cortex-M33 processor and its supporting debug system, which enables debugging and Embedded Trace Macrocell (ETM) tracing. The CPU executes program code from RRAM through an instruction cache. Data is stored in single-cycle RAMs, which are divided into multiple bus subordinates but form a continuous RAM space in the memory map. The fast domain also contains high-speed peripherals.

2.1.2 Lower speed domains

NORA-B2 are three lower speed power domains:

- Radio domain – contains the short-range radio as well as supporting peripherals used by the radio protocol stack. The domain runs at 32 MHz synchronously with the fast domain.
- Peripherals domain – contains most peripherals. The domain runs at 16 MHz synchronously with the Fast MCU domain.
- Low Power domain – contains peripherals for ultra-low-power modes. These can be used to wake the rest of the system even when the peripheral domain is powered off. The domain runs at 16 MHz asynchronously to the fast domain.

2.2 Power management

NORA-B2 series modules utilize integrated LDO and DC/DC regulators that maximize the power efficiency of the system. NORA-B2 has a main on-chip voltage regulator VREGMAIN, which converts the voltage supplied on VCC to internal voltage. VCC is also be the reference voltage for the I/O signals.

2.3 System clocks

The clock control system sources the system clocks from internal or external high and low frequency oscillators. The system distributes the clocks based on the module requirements.

2.3.1 High-frequency clock HFCLK

The high-frequency clock (HFCLK) is generated by either a 64 MHz or 128 MHz internal oscillator, or a 32 MHz crystal oscillator (HFXO) within the module. The clock is used to derive the internal clock frequencies required to operate the module. With due consideration for frequency tolerance, temperature drift, and aging, the HFXO has an accuracy of ±10 ppm.

The internal load capacitor must be configured before starting the high-frequency crystal oscillator, using the XOSTART task. To enable the internal capacitors, find the correct value for CINT in the `OSCILLATORS.XOSC32M.CONFIG.INTCAP` field. For further information, see also the nRF54Lxx datasheet [4].

The device uses the internal capacitor and the external crystal after configuration and HFXO starts.

☞ The recommended value of HFXO capacitance for NORA-B2 is 15.25 pF.

2.3.2 Low-frequency LFCLK

A 32.768 kHz low-frequency clock is used by NORA-B2 for various functions, including the timing of radio events, the global real-time counter (GRTC), and the watchdog timer (WDT). The choice of the LFCLK source depends on the accuracy required by the application. One of four sources is required for the low-frequency clock:

- RC oscillator (LFRC) – fully embedded in NORA-B2 and does not require external components
- Crystal oscillator (LFXO) – When greater than ± 500 ppm accuracy is required, an external 32.768 kHz crystal and optional loading capacitors must be added. Internal loading capacitors between 4 pF and 18 pF in 0.5 pF steps are also needed. The LFXO accuracy is dependent on the chosen crystal.

- External source – An externally generated 32.768 kHz clock source applied to **XL1**, and **XL2** pins. The accuracy of the clock is dependent on the external source.
- Synthesized clock (LFSYNT) – 32.768 kHz clock generated from the HFCLK, which assumes the accuracy is ±20 ppm. LFSYNT requires HFCLK to run, which results in higher-than-average power consumption.

2.4 RF antenna interfaces

2.4.1 2.4 GHz radio (ANT)

NORA-B2 model versions support two 2.4 GHz antenna solutions:

- NORA-B2x1 modules include an antenna pin (**ANT**). The pin has nominal characteristic impedance of 50 Ω and can be connected to an antenna or connector on the host board using a controlled impedance trace.
- NORA-B2x6 modules are equipped with an internal antenna that is integrated into the module PCB. This low-profile antenna solution uses antenna technology licensed from Abracon, which is particularly useful in space-constrained designs. The **ANT** pin is internally disconnected on this model.

For more information about the antennas that are approved for use with NORA-B2 series, see also the system integration manual [1].

2.4.2 Near Field Communication (NFC)

NORA-B2 series modules include an NFC interface, which is capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. This interface supports EasyDMA for reading and writing of data packets to and from RAM. As an NFC tag, data can be read from or written to the NORA-B2 modules using an NFC reader. However, NORA-B2 modules are not capable of reading other tags or initiating NFC communications. The NFC interface can be used to wake the module from System OFF mode, which means that the module can wake from the deepest power save mode and still react properly to an NFC field. Two GPIO pins are available for connecting to an external NFC antenna: NFC1 and NFC2 pins.

2.4.3 Channel sounding

NORA-B2 series supports channel sounding, which is a key feature of Bluetooth LE in the Bluetooth Core 6.0 specification. The feature enables accurate and secure distance measuring with built-in security features and seamless interoperability. Channel sounding utilizes various ranging techniques and security measures to enable secure and accurate distance measurement between two devices – without increasing product complexity or size. Channel Sounding accuracy meets the requirements for applications such as smart door locks, home appliances, personal item tracking tags, or the presence detection of high-value assets in industrial and professional settings.

For more information, see also *Channel Sounding at a glance* on the Nordic website [6].

2.5 System functions

2.5.1 Power modes

NORA-B2 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when they are not needed, and complex wake up events can be generated from different external and internal inputs.

The three main power modes are:

- *System ON*
- *System ON IDLE* sub-modes
- *System OFF* – lowest power consumption

Depending on the application, the module should spend most of its time in either System ON IDLE or System OFF mode to minimize current consumption.

2.5.1.1 System ON

System ON is the default operation after power-on reset. You can switch on or reboot the NORA-B2 modules in one of the following ways:

- Rising edge on the **VCC** pin to a valid supply voltage
- Issuing a reset of the module. See also Module reset.

An event to wake up from the *System OFF* mode to the active mode can be triggered by:

- Programmable digital or analog sensor event. For example, a rising voltage level on an analog comparator pin
- Detecting an NFC field
- Debug session
- A pin RESET.

When waking up from *System ON IDLE* mode to *System ON* mode, an event can also be triggered by:

- GRTC on-board Global Real Time Counter
- Radio interface
- Detection of an NFC field

2.5.1.2 System ON idle sub-modes

In *System ON* operation, when the CPU and all peripherals are idle, the system can reside in one of the following power sub-modes:

- Constant latency – wakeup and task response are constant and kept at a minimum. This is secured by a set of resources that are always enabled.
- Low-power – lowest System ON power consumption.

2.5.1.3 System OFF

System OFF is the lowest power consumption mode the system can enter. The core functionality of the system is powered down and all ongoing tasks are terminated.

There is no dedicated pin to power off NORA-B2 modules. Any available GPIO pin can be configured to trigger the application to enter *System OFF* mode which essentially powers down the module.

An under-voltage (brown-out) shutdown occurs on the NORA-B2 modules when the **VCC** supply drops below the operating range minimum limit. If this occurs, it is not possible to store the current parameter settings in the non-volatile area of the module memory.

2.5.2 Module reset

There are several reset sources:

- **Power-on reset**: The power-on reset generator initializes the system when **VCC** rises above the power-on threshold.
- **Pin reset**: A pin reset is generated when the physical reset pin on the device is asserted. Pin reset is available on the reset pin **J3** (**nRESET**).
- **Glitch detector**: The glitch detector (GLITCHDET) puts the system in a reset state if either the **VCC** supply voltage or the device's internal digital voltage drops below safe thresholds.

- **Brownout reset**: The system is placed in reset state if the **VCC** supply drops below the brownout threshold.
- **Wake from *System OFF* mode reset**: The system is reset when waking from *System OFF* mode.
- **Soft reset**: A soft reset is generated when the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR) in the Arm CPU is set. It can also be generated using CTRL-AP.
- **CTRL-AP reset**: CTRL-AP can generate the several resets, including Soft reset, Pin reset, and Hard reset – which is used during an erase-all operation and is less intrusive than Pin reset.
- **Watchdog timer (WDT) reset**: A watchdog timer (WDT) reset is generated when the watchdog timer times out.

2.5.3 CPU and memory

The integrated Nordic Semiconductor nRF54Lxx chip in NORA-B2 series modules includes powerful and fully programmable Arm Cortex-M33 processors, which feature a 32-bit instruction set (Thumb®-2 technology) with a superset of 16- and 32-bit instructions. For improved efficiency and power consumption, nRF54Lxx also features an integrated **RISC-V** coprocessor that is designed to offload tasks from the primary Cortex-M33 core.

The processor includes an FPU, TrustZone® technology, and a full set of peripherals. It has a flash, and low-leakage RAM. The operation can occur at 128 MHz or 64 MHz.

2.5.4 Direct Memory Access EasyDMA

Many of the peripherals described in this data sheet utilize Direct Memory Access (DMA), also known as EasyDMA, to provide a direct interface to the RAM – without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruptions. DMA should be used whenever possible to reduce overall power consumption.

2.5.5 Distributed Programmable Peripheral Interconnect (DPPI)

NORA-B2 series modules includes a distributed programmable peripheral interconnect (DPPI). Functioning as a switch matrix, the DPPI connects various control signals between the different interfaces and system functions.

With DPPI, most interfaces can bypass the CPU to trigger a system function. Consequently, an incoming data packet can trigger a counter, falling voltage level on an ADC, or toggle a GPIO – without having to interrupt the CPU. This facilitates the development of smart, power-efficient applications that wake up the CPU only when it is necessary.

2.5.6 Global Real-Time Counter (GRTC)

A key system feature available on the NORA-B2 is the Global Real-Time Counter which can operate in all power modes, including *System OFF* mode, and implement a shared system timer. This counter can generate multiple interrupts and events to the CPU and radio and internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to 142 years and allow periodic Bluetooth LE advertising events without involving the CPU for example.
GRTC uses the 16 MHz clock when the high-speed clock is active but automatically switches to the low frequency clock in other power modes.

2.6 Serial peripherals

NORA-B2 modules support the following serial communication interface:

- UART: Up to five instances with RTS/CTS flow control and EasyDMA/ One high-speed up to 4 Mbps
- SPI: Up to five main node or sub node instances with EasyDMA/ One high-speed SPIM up to 32 MHz
- QSPI: Emulated peripheral

- I2C (TWI): Up to five main node or sub node instances with EasyDMA/ up to 400 kHz
- I2S: Two channel Inter-IC sound interface

Most input/output pins on the module are shared between the digital interfaces, analog interfaces, and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

2.6.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control with baud rates up to 4 Mbps. Up to five instances can be defined. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

Other characteristics of the UART interface include:

- Pin configuration:
  - TXD: Transmit Data output pin
  - RXD: Receive Data input pin
  - RTS: Request To Send, flow control output pin (optional)
  - CTS: Clear To Send, flow control input pin (optional)
- Full-duplex operation
- EasyDMA direct transfer to/from RAM
- Individual selection of I/O pins
- Four slow instances with up to 1 Mbps baud rate/ one fast up to 4 Mbps
- Optional even/odd parity bit checking and generation
- One or two stop bits/ Configurable data frame size: 4-bit to 9-bit
- 9-bit support mode with address matching in RX
- Hardware flow control or no flow control is supported.
- Return to IDLE between transactions supported (when using HW flow control)

2.6.2 Serial Peripheral Interface (SPI)

NORA-B2 supports up to five Serial Peripheral Interfaces with serial clock frequencies of up to 32 MHz, with EasyDMA, and Individual selection of I/O pins. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

Other characteristics of the SPI interfaces include:

- Pin configuration in *Main* node mode:
  - **SCLK**, Serial clock output, up to 32 MHz for SPIM00, and 8 MHz for SPIM2x/30.
  - **MOSI**, *Main* node output to *Sub* node input data line
  - **MISO**, *Main* node Input from *Sub* node output data line
  - **CS**, Chip select output, active low, selects which peripheral on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
  - **DCX**, Data/Command signal. An optional signal used by SPI *Sub* nodes to distinguish between SPI commands and data
- Pin configuration in *Sub* mode:
  - **SCLK**, Serial clock input
  - **MOSI**, *Main* node *Output* to *Sub* node *Input* data line
  - **MISO**, *Main* node *Input* from *Sub* node *Output* data line
  - **CS**, Chip select input, active low, connects/disconnects the interface from the bus.
- Both *Main* node and *Sub* node modes are supported on all interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data can be captured on rising or falling clock edge (CPHA).

2.6.2.1 SPIM and SPIS shared resources

The SPI Main (SPIM), SPI Sub (SPIS) interfaces share registers and other resources with other peripherals that have the same ID as the SPIM or SPIS. Therefore, the user must disable all peripherals with the same ID as the SPIM and SPIS before the interfaces can be configured and used.

Disabling a peripheral that has the same ID as the SPIM or SPIS, does not reset any of the registers that are shared with these interfaces. It is therefore important to configure all relevant SPIM and SPIS registers explicitly to ensure that they operate correctly. For more information about the peripherals and their IDs, see the instantiation table included in the preliminary *nRF54L15/nRF54L10/nRF54L05 datasheet v0.8* [4].

2.6.3 Quad Serial Peripheral Interface (QSPI), (FLPR)

The Quad Serial Peripheral Interface (QSPI) external memory to be connected to NORA-B2 modules.

QSPI always operates in main node mode using the following pin configuration:

- **CLK**, serial clock output
- **CS**, chip select output, active low, selects which peripheral on the bus to talk to
- **D0**, serial output, *Main Out Sub In (MOSI)* data in single mode, data I/O signal in dual/quad mode
- **D1**, serial input, *Main In Sub Out (MISO)* data in single mode, data I/O signal in dual/quad mode
- **D2**, data I/O signal in quad mode (optional)
- **D3**, data I/O signal in quad mode (optional)

For information about each power domain and their associated GPIOs, see Figure 2 and Table 6.

2.6.4 Inter-Integrated Circuit interface (I2C)

The Inter-Integrated Circuit (I2C) interfaces can be used to transfer and/or receive data on a 2-wire bus network. NORA-B2 modules can operate as both *Controller* and *Target* nodes on the I2C bus, using 100 kbps (standard), 250 kbps, 400 kbps, and 1000 kbps transmission speeds with EasyDMA, and Individual selection of I/O pins. The interface supports clock stretching, which allows NORA-B2 modules to temporarily pause any I2C communication. Up to 127 individually addressable I2C devices can be connected to the same two signals. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

Pin configuration:

- **SCL**, clock output in *Controller* node, input in *Target* node
- **SDA**, data input/output pin

To work properly in the main node mode the I2C requires external pull-up resistors referenced to **VCC**. Pull-up resistors referenced to **VCC** are required in the *Target* node as well, but these should be placed at the *Controller* node end of the interface. The I2C specification allows a line capacitance of 400 pF at most. For information about the value of internal pullup resistor (Rpu) for use with NORA-B2, see Digital pins.

2.6.4.1 I2C shared resources

In *Controller* or *Target* nodes, the I2C shares registers and other resources with other peripherals that have the same ID as the I2C . Therefore, the user must disable all peripherals that have the same ID as the I2C before the I2C can be configured and used. Disabling a peripheral that has the same ID as the I2C will not reset any of the registers that are shared with the I2C. Therefore, it is important to configure all relevant I2C registers explicitly to ensure that they operate correctly.

For more information about peripherals and their IDs, see the instantiation table in the *nRF54L15_nRF54L10_nRF54L05 Preliminary Datasheet* [4].

2.6.5 Inter-IC Sound interface (I2S)

The Inter-IC Sound (I2S) interface transfers audio sample streams between NORA-B2 and external audio devices such as codecs, DACs, and microphones. It supports standard I2S, left- or right-aligned interface formats in both *Controller* and *Target* nodes, and features EasyDMA for efficient data transfer. The I2S pins can also be individually assigned to different GPIOs. I/O pins.

For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

Pin configuration:

- **MCK**, Main clock
- **LRCK**, Left Right/word/sample clock
- **SCK**, Serial Clock
- **SDIN**, Serial Data In
- **SDOUT**, Serial Data Out

The *Controller* side of an I2S interface always provides the **LRCK** and **SCK** clock signals, but some *Controller* node devices can't generate a **MCK** clock signal. For external systems that are unable to generate their own clock signal, NORA-B2 can supply a **MCK** clock signal in both the *Controller* and *Target*. The two data signals, **SDIN** and **SDOUT**, allow simultaneous bi-directional audio streaming. The interface supports 8, 16, 24 and 32-bit sample widths with up to 48 kHz sample rate.

2.7 Digital peripherals

2.7.1 Pulse Width Modulation (PWM)

NORA-B2 modules provide up to three PWM units – each with four PWM channels and with EasyDMA, that can be used to generate complex waveforms. These waveforms can be used for controlling motors, dimming LEDs, or functioning as audio signals when connected to speakers. Duty-cycle sequences can be stored in RAM and repeated or connected into loops. The duty-cycle values can be updated autonomously and glitch-free directly from memory through EasyDMA – without CPU intervention. Each channel uses a single GPIO pin as output. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

2.7.2 Quadrature Decoder (QDEC)

NORA-B2 modules provide up to two QDEC units that read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate the rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs, **PHASE_A** and **PHASE_B**, and an optional LED output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

2.8 Analog interfaces

8 out of the 31 digital GPIOs can be multiplexed to analog functions, including:

- 1x 8-channel ADC[1], 14-bit at 31.25 ksps, 12-bit at 250 ksps, and up to 10-bit at 2 Msps.
- 1x Analog comparator[1]
- 1x 8-channel Low-power analog comparator[1]

[1] Each analog pin may only be assigned to one function at any given time, ADC, COMP, or LPCOMP

2.8.1 Successive approximation Analog to Digital Converter (SAADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of the NORA-B2. Any of the 8 analog inputs can be used.

Characteristics of the ADC include:

- Three modes, 10-bit at 2 MS/s, 12-bit at 250 KS/s, or 14-bit at 31.25 MS/s
- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Full swing input range of 0 V to **VCC**
- Support for direct sample transfer to RAM using EasyDMA
- Single ended or continuous sampling
- Two operation modes: Single-ended or Differential
    - Single-ended mode, where a single input pin is used
    - Differential mode, where two inputs sample the voltage level difference between them

If the sampled signal level is much lower than the VCC, it is possible for the programmable gain factor of the ADC to better encompass the required signal. This produces a higher effective resolution. Continuous sampling can be configured for specific time intervals or at different internal or external events – without CPU involvement. For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

2.8.1.1 SAADC shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins. It is not advisable to select the same analog input pin for both SAADC modules.

2.8.2 Comparator (COMP)

The analog comparator compares the analog voltage on one of the analog-enabled pins in NORA-B2 with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross.

Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC.
- Two operation modes: *Single-ended* or *Differential*
    - *Single-ended* mode:
        - A single reference level or an upper and lower hysteresis
        - Selectable from a 64-level reference ladder with a range from 0 V to VREF, as described in Table 3.
    - *Differential* mode:
        - Two analog pin voltage levels are compared, optionally with configurable hysteresis.
        - Two selectable speed/power performance modes: Low power and High speed.

For information about each instance power domain and the related GPIOs, see Figure 2 and Table 6.

2.8.2.1 COMP shared resources

The COMP shares analog resources with other analog peripherals. It also shares registers and other resources with other peripherals with the same ID as the COMP. For further information about the peripherals and their IDs, see also the instantiation table on the *nRF54L15_nRF54L10_nRF54L05 Preliminary Datasheet* [4] The COMP peripheral must not be disabled (through write operations to the ENABLE register) before the peripheral has stopped. Failing to do so can result in unpredictable module behavior.

2.8.3 Low power comparator (LPCOMP)

In addition to the power save mode available for the comparator, there is also a separate low power comparator (LPCOMP) available on the NORA-B2 module. The LPCOMP allows for an even lower power operation – with slightly reduced performance and fewer configuration options.

Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**
- Two operation modes - *Single-ended* or *Differential*
- *Single-ended* mode:
  - The reference voltage **LP_VIN–** is selected from a 15-level reference ladder
- *Differential* mode:
  - Pin **P1.04/AIN0** or **P1.05/AIN1** is used as reference voltage **LP_VIN–**
  - Can be used to wake the system from *System OFF* or *Sleep* mode

Since the run current of the low power comparator is very low, it can be used as an analog trigger to wake up the CPU during the module sleep mode. See also Power modes. For information about power domain and related GPIOs, see Figure 2 and Table 6.

For a summary of the analog pin options, see also Table 3.

2.8.3.1 LCOMP shared resources

LPCOMP shares analog resources with SAADC. While it is possible to use the SAADC at the same time as the LPCOMP, selecting the same analog input pin for both modules is not supported.

Additionally, LPCOMP shares registers and other resources with other peripherals with the same ID as LPCOMP. For more information about the peripherals and their IDs, see the instantiation table in the *nRF54L15_nRF54L10_nRF54L05 Preliminary Datasheet* [4]. The LPCOMP peripheral should not be disabled (through write operation to the ENABLE register) before the peripheral has stopped. Failing to do so may result in unpredictable behavior.

2.8.4 Analog pin options

Table 3 shows the supported connections of the analog functions.

☞ An analog pin must not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	AIN0 to AIN7 pin or **VCC**
ADCN	ADC differential negative input	AIN0 to AIN7 pin or **VCC**
VIN+	Comparator input	AIN0 to AIN7 pin
VREF	Comparator single-ended mode reference ladder input	AIN0 to AIN7 pin, **VCC**, 1.2 V internal reference
VIN-	Comparator differential mode negative input	AIN0 to AIN7 pin in differential mode, VREF in single ended mode
LP_VIN+	Low-power comparator IN+	AIN0 to AIN7 pin
LP_VIN-	Low-power comparator IN-	**P1.04/AIN0** or **P1.05/AIN1**, 1/16 to 15/16 **VCC** in steps of 1/16 **VCC,** External selected reference.

Table 3: Possible uses of the analog pins

2.9 GPIO

NORA-B2 series modules have a versatile pin-out. In an un-configured state, NORA-B2 supports a total of 31 GPIO pins and no analog or digital interfaces. All interfaces or functions must then be allocated to a GPIO pin before use.

8 out of the 31 GPIO pins are analog enabled, which means that they can have an analog function allocated to them. Table 6 shows the number of digital and analog functions that can be assigned to a GPIO pin.

2.9.1 GPIO ports and capabilities

NORA-B2 power domains have their own GPIO ports with different capabilities.

Supported GPIO ports in the system, include:

- Port 0: In the low-power domain, this port can wake the system up from *System OFF* or *System ON* sleep and can be accessed by all peripherals in the low-power domain.
- Port 1: In the peripheral domain, this port can wake the system up from *System OFF* or *System ON* sleep and can be accessed by all peripherals in the peripheral domain.
- Port 2: In the MCU domain, this port has faster pins and can be used for high-speed signals, such as trace or fast serial peripheral communication. GPIO on Port 2 can't wake the system from sleep. Port 2 doesn't have a GPIO SENSE or DETECT mechanism and has no GPIO tasks and events (GPIOTE).

Table 4 describes the port's special functions and characteristics.

Port	Wakeup source	Extra drive strength (E0E1)	Pin sense/Detect	GPIOTE	Speed (MHz)
Port 0	Yes	No	Yes	Yes	8
Port 1	Yes	No	Yes	Yes	8
Port 2	No	Yes	No	No	64

Table 4: Port Capabilities

☞ **P1.00/XL1** and **P1.01/XL2** default to GPIO but can be configured to connect an external 32.768 kHz crystal circuit.

☞ **P1.02/NFC1** and **P1.03/NFC2** default to NFC but can also be configured to operate as GPIO.

☞ **P1.08** default to GPIO but can be configured to external reference for **SAADC**

2.9.2 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard drive strength, a pin configured as an output can only source or sink a certain amount of current.

If the timing requirements of a digital interface can't be met or if an LED requires more current, an extra drive strength mode is available on port 2 pins. This allows the digital output to draw more current. In addition to drive strength, GPIO pins configured for output can be set for push-pull or open-drain. GPIO pins configured for input can float or enable internal pull-up or pull-down resistors. For more information about the digital GPIO characteristics and extra drive strength values, see Table 18.

Table 5 shows GPIO custom functions configuration.

Function	Description	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation	Any
General purpose output	Digital output with configurable drive strength, push-pull or open drain output	Any
Pin disabled	Pin is disconnected from the input and output buffers	Any
Timer/ counter	High-precision time measurement between two pulses/ Pulse counting with interrupt/event generation	Any, in the same domain
Interrupt/ Event trigger	Interrupt/event trigger to the software application	Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement	Any
ADC input	8/10/12/14-bit analog to digital converter	Any analog
Analog comparator input	Compares two voltages. Capable of generating wake-up events and interrupts	Any analog
PWM output	Simple output or complex pulse-width modulation waveforms	Any, in the same domain

Table 5: GPIO custom functions configuration

2.10 Debug interface

2.10.1 Multi-drop Serial Wire Debug (SWD)

NORA-B2 series modules provide ARM Multi-drop SWD technology for flashing and debugging. Through two-pin serial SWD signals, **SWDIO** and **SWDCLK**. Additionally, NORA-B2 can be driven over the same SWD interface to other CPUs that support Multi-drop SWD.

2.10.2 Parallel trace

NORA-B2 series modules support parallel trace output. This facilitates output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) embedded in the Arm Cortex-M33 integrated in NORA-B2. The ETM trace data allows a user to record exactly how the application processes the CPU instructions in real time.

In addition to parallel trace, the NORA-B2 supports serial trace through the serial wire output SWO trace protocol. Parallel and serial trace can't be used at the same time. ETM trace is only supported in parallel trace mode. ITM trace is supported in both parallel and serial trace mode.

Trace pins are multiplexed with GPIOs. **SWO** and **TRACEDATA[0]** can use the same GPIO. **SWO** pin can also use a separate GPIO on Port 2.
The parallel trace interface uses one clock signal and four data signals respectively: **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2,** and **TRACE_D3**. For more information about the shared assignments of the GPIO pins, see the Pinout.

3 Pin definition

3.1 NORA-B2 pin assignment

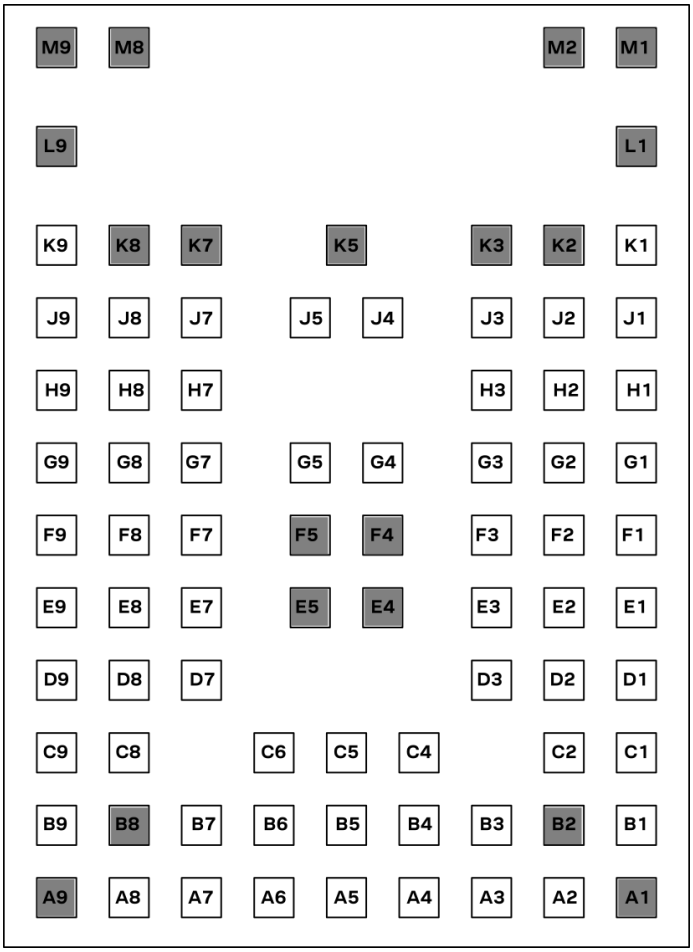


Figure 3: Pin assignment (top view)

NORA-B2 provides flexibility for GPIO pin routing and configuration. Several pins have limitations or recommendations about how each pin should be configured and what it should be used for. For information about the shared assignments of the GPIO pins, see Pinout.

Peripherals must use pins in their domain. Figure 2 shows which peripherals and ports belong to which domain. However, several pins on the P2 port, **P2.00**–**P2.10**, can be used for selected serial interfaces in the peripheral domain. These pins must be configured and used only for functions described in Table 8.

Do not apply an NFC field to the NFC pins when they are configured as GPIOs. Failure to observe this can cause permanent damage to the module. When driving different logic levels on these pins in the GPIO mode, a small current leakage occurs. Make sure these pins are set to the same logic level before entering any of the power saving modes. Refer to also RESET_N pin.

3.2 Pinout

Table 6 shows the module pin-out assignments of the NORA-B2 module in an unconfigured state.

No.	NORA function	I/O[2]	Description	nRF54Lxx function	Remarks
A1	VSS	Power	Ground pad	-	
A2	NC	-	-	-	
A3	I2C_SCL	I/O	General Purpose I/O	P1.11	AIN4
A4	NC	-	-	-	
A5	DEBUG_TX	I/O	General Purpose I/O	P0.00	
A6	DEBUG_RX	I/O	General Purpose I/O	P0.01	
A7	VCC	I	Module supply voltage input		1.7-3.5 V module supply
A8	VCC	I	Module supply voltage input		1.7-3.5 V module supply
B1	SPI_SCK	I/O	General Purpose I/O, SPIM_SCK, SPIS_SCK; TRACE_CLK	P2.06	Trace, Clock pin
B3	SPI_CS	I/O	General Purpose I/O, TRACEDATA [3], SPIM_CS, UARTE_RTS	P2.10	Trace
B4	I2C_SDA	I/O	General Purpose I/O	P1.12	AIN5, Clock pin
B5	NFC2	I/O	General Purpose I/O	P1.03	Clock Pin
B6	XTAL_32K	I/O	General Purpose I/O, 32.768 kHz crystal connection	P1.00	AIN
B7	VCC	I	Module supply voltage input		1.7-3.5 V module supply
B9	NC	-	-	-	
C1	SPI_MISO	I/O	General Purpose I/O, TRACEDATA [2], SPIM_MISO, SPIS_MOSI, UARTE_CTS	P2.09	Trace
C2	SPI_MOSI	I/O	General Purpose I/O, TRACEDATA [1], SPIM_MOSI, SPIS_MISO, UARTE_TXD	P2.08	Trace
C4	SPI_DCX	I/O	General Purpose I/O, TRACEDATA [0], Serial wire output (SWO), SPIM_DCX, UARTE_RXD	P2.07	Trace, SWO
C5	NFC1	I/O	General Purpose I/O	P1.02	NFC input
C6	XTAL_32K	I/O	General Purpose I/O, 32.768 kHz crystal connection	P1.01	AIN
C8	Switch 2	I/O	General Purpose I/O	P0.02	
C9	NC	-	-	-	
D1	QSPI_D2	I/O	General Purpose I/O, QSPI_D2	P2.03	FLPR
D2	QSPI_D0	I/O	General Purpose I/O, SPIM_MOSI, SPIS_MISO, UARTE_TXD, QSPI_D0, Serial wire output SWO	P2.02	FLPR, Trace
D3	NC	-	-	-	
D7	NC	-	-	-	
D8	Switch 1	I/O	General Purpose I/O	P1.09	
D9	NC	-	-	-	

[2] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AIN=Analog Input, NC=Not Connected

No.	NORA function	I/O[2]	Description	nRF54Lxx function	Remarks
E1	QSPI_CS	I/O	General Purpose I/O, SPIM_CS, UARTE_RTS, QSPI_CS	P2.05	FLPR, Clock pin
E2	QSPI_D1	I/O	General Purpose I/O, SPIM_MISO, SPIS_MOSI, UARTE_CTS, QSPI_D1	P2.04	FLPR(QSPI)
E3	NC	-	-	-	
E7	NC	-	-	-	
E8	WAKE-HOST	I/O	General Purpose I/O	P1.14	AIN7
E9	GPIO	I/O	General Purpose I/O	P1.08/EXTREF	AN, Clock pin (GRTC HF Clock output), External reference for SAADC
F1	QSPI_CLK	I/O	General Purpose I/O, SPIM_SCK, SPIS_ SCK, QSPI_SCK	P2.01	FLPR, Clock pin
F2	QSPI_D3	I/O	General Purpose I/O, SPIM_DCX, UARTE_RXD, QSPI_D3	P2.00	FLPR(QSPI)
F3	NC	-	-	-	
F7	NC	-	-	-	
F8	UART_RTS	I/O	General Purpose I/O	P1.06	AIN2
F9	UART_CTS	I/O	General Purpose I/O	P1.07	AIN3
G1	NC	-	-	-	
G2	NC	-	-	-	
G3	NC	-	-	-	
G4	NC	-	-	-	
G5	RF_CTRL1	I/O	General Purpose I/O	P1.13	P1.13 is also connected to J8
G7	RF_CTRL2	I/O	General Purpose I/O	P0.02	P0.02 is also connected to C8
G8	UART_TXD	I/O	General Purpose I/O	P1.04	Clock pin, AIN0
G9	UART_RXD	I/O	General Purpose I/O	P1.05	AIN1
H1	NC	-	-	-	
H2	SWDIO	Debug	Serial wire debug I/O	SWDIO	
H3	NC	-	-	-	
H7	NC	-	-	-	
H8	LED_GREEN	I/O	General Purpose I/O, GRTC LF clock output	P0.04	Clock pin, GRTC
H9	LED_BLUE	I/O	General Purpose I/O	P1.10	
J1	NC	-	-	-	
J2	SWDCLK	Debug	Serial wire debug clock	SWDCLK	
J3	RESET_N	I	RESET	RESET	
J4	NC	-	-	-	
J5	NC	-	-	-	
J7	NC	-	-	-	
J8	LED_RED	I/O	General Purpose I/O	P1.13	AIN6
J9	WAKE-UP	I/O	General Purpose I/O, GRTC PWM output	P0.03	Clock pin, GRTC
K1	NC	-	-	-	
K9	ANT	I/O	Antenna Tx/Rx interface		50 Ω nominal characteristic

No.	NORA function	I/O[2]	Description	nRF54Lxx function	Remarks
					impedance, only used with NORA-W251AWS modules. NC for NORA-W256AWS
	EGP	-	Exposed Ground pins		Exposed scattered gray pins on the module should be connected to GND
L1-M9	EAGP	-	Exposed Antenna ground pins		Exposed pins underneath the antenna area should be connected to GND

Table 6: NORA-B2 pinout

3.2.1 Clock pins

NORA-B2 has dedicated clock pins, which can also be used as regular I/O data pins, refer to the nRF54Lxx datasheet [4] for which peripheral signals must use clock pins.

No.	NORA function	I/O[3]	nRF54Lxx function
B5	NFC2	I/O	P1.03
G8	UART_TXD	I/O	P1.04
E9	GPIO	I/O	P1.08
B4	I2C_SDA	I/O	P1.11
A3	I2C_SCL	I/O	P1.12
F1	QSPI_CLK	I/O	P2.01
B1	SPI_SCK	I/O	P2.06
J9	WAKE-UP	I/O	P0.03
H8	LED_GREEN	I/O	P0.04

Table 7 Dedicated clock pins

3.3 Dedicated peripheral, and cross power-domain pins

The device has some pins dedicated for specific purposes. GPIO pin routing and configuration are flexible.

Some pins have limitations or recommendations for configuration and use. Selected pins of Port2 can be used for some interfaces in the peripheral's domain, SPIM, SPIS, and UARTE, as shown in Table 8.

No.	NORA function	I/O[4]	Dedicated function	nRF54Lxx function
B1	SPI_SCK	I/O	SPIM00/21, SPIS20/21, Trace	P2.06
B3	SPI_CS	I/O	SPIM00/21, UARTE00/21, Trace	P2.10
C1	SPI_MISO	I/O	SPIM00/21, SPIS00/21, UARTE00/21, Trace	P2.09
C2	SPI_MOSI	I/O	SPIM00/21, SPIS00/21, UARTE00/21, Trace	P2.08

[3] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AIN=Analog Input, NC=Not Connected

[4] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AIN=Analog Input, NC=Not Connected

No.	NORA function	I/O[4]	Dedicated function	nRF54Lxx function
C4	SPI_DCX	I/O	SPIM00/21, UARTE00/21	P2.07
D1	QSPI_D2	I/O	FLPR	P2.03
D2	QSPI_D0	I/O	SPIM00/20, SPIS00/20, UARTE00/20, FLPR, Trace	P2.02
E1	QSPI_CS	I/O	SPIM00/20, UARTE00/20, FLPR	P2.05
E2	QSPI_D1	I/O	SPIM00/20, SPIS00/20, UARTE00/20, FLPR	P2.04
F1	QSPI_CLK	I/O	SPIM00/20, SPIS00/S20, FLPR	P2.01
F2	QSPI_D3	I/O	SPIM00/20, UARTE00/20, FLPR	P2.00
B5	NFC2	I/O	NFC2	P1.03
C5	NFC1	I/O	NFC1	P1.02
D8	Switch 1	I/O	RADIO [0], DFEGPIO	P1.09
H9	LED_BLUE	I/O	RADIO [1], DFEGPIO	P1.10
A3	I2C_SCL	I/O	RADIO [2], DFEGPIO	P1.11
B4	I2C_SDA	I/O	RADIO [3], DFEGPIO	P1.12
G5	RF_CTRL1	I/O	RADIO [4], DFEGPIO	P1.13
E8	WAKE-HOST	I/O	RADIO [5], DFEGPIO	P1.14
G9	UART_RXD	I/O	RADIO [6], DFEGPIO	P1.05

Table 8: Dedicated peripheral, and cross-power domain pins

4 Electrical specifications

⚠ Stressing the device above one or more of the absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the recommended operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Signal	Description	Condition	Min	Max	Unit
VCC	NORA-B2 Module supply high voltage	Input DC voltage at VCC pin	-0.3	3.6	V
VSS				0	V
$V_{I/O}$	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC ≤ 3.5 V	-0.3	VCC + 0.3	V
P_ANT	Maximum power at the receiver	Input RF power at the antenna pin		0	dBm
$I_{NFC1/2}$	NFC Antenna pin current	Input current at NFC pin		130	mA

Table 9: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. Use appropriate protection devices to ensure that voltage spikes exceeding the power supply voltage specifications in Table 9 are kept within the specified limits.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except ANT pin			2	kV	Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
ESD sensitivity for all pins except ANT pin			500	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8*	kV	According to EN 301 489-1

*Tested on EVK-NORA-B20 evaluation board

Table 10: Maximum ESD ratings

⚠ NORA-B2 series modules are Electrostatic Sensitive Devices and require special precautions while handling. For ESD handling instructions, refer to also ESD precautions.

4.1.2 Flash memory endurance

Parameter	Value	Unit
Endurance	1000	Write/erase cycles
Retention	10	Years at [85] °C

Table 11: Flash memory endurance

4.2 Recommended operating conditions

Unless otherwise specified, all given specifications have been measured at an ambient temperature of 25 °C with a supply voltage of 3.3 V.

Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating and storage temperature range

Parameter	Min	Typ	Max	Unit
Storage temperature	–40		+105	°C
Operating temperature	–40	+25	+85	°C

Table 12: Temperature range

4.2.2 Supply/power pin

Symbol	Parameter	Min	Typ	Max	Unit
VCC	NORA-B2 module supply voltage	1.7	-	3.5	V

Table 13: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 14 shows the typical current consumption of a NORA-B2 module at 3.3 V supply, independent of the software used.

Condition	Min	Typ	Max	Units
Radio RX only @ 1 Mbps Bluetooth LE mode			3.3	mA
Radio RX only @ 2 Mbps Bluetooth LE mode			3.6	mA
Bluetooth LE TX 1 Mbps at 0 dBm			5.0	mA
Bluetooth LE TX 1 Mbps at +4 dBm			6.6	mA
Bluetooth LE TX 1 Mbps at +7 dBm			8.3	mA

Table 14: NORA-B2 VCC current consumption

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
	Bluetooth Low Energy mode				
Receiver input sensitivity*	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		–94		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		-91		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		-97		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		–102		dBm
Maximum output power**	Conducted at 25 °C		+7		dBm
	IEEE 802.15.4 mode				
Receiver input sensitivity*	Conducted at 25 °C, 250 kbit/s		-100		dBm
Maximum output power**	Conducted at 25 °C, 250 kbit/		+7		dBm
	Antenna				
NORA-B2x6 antenna gain	Integral to EVK-NORA-B2x6		+3		dBi

*Conducted test on EVK-NORA-B201 evaluation board with 3.0 V supply voltage at 25 °C.

** Depends on supply voltage

Table 15: NORA-B2 RF performance

4.2.5 Antenna radiation patterns

Figure 4 provides an overview of the measurement procedure and describes how the NORA-B2x6 module is aligned to the XYZ-coordinate system. A measurement is taken at every dotted position above the module image (shown left). Each measurement is represented as a grid point in the radiation pattern (shown right).

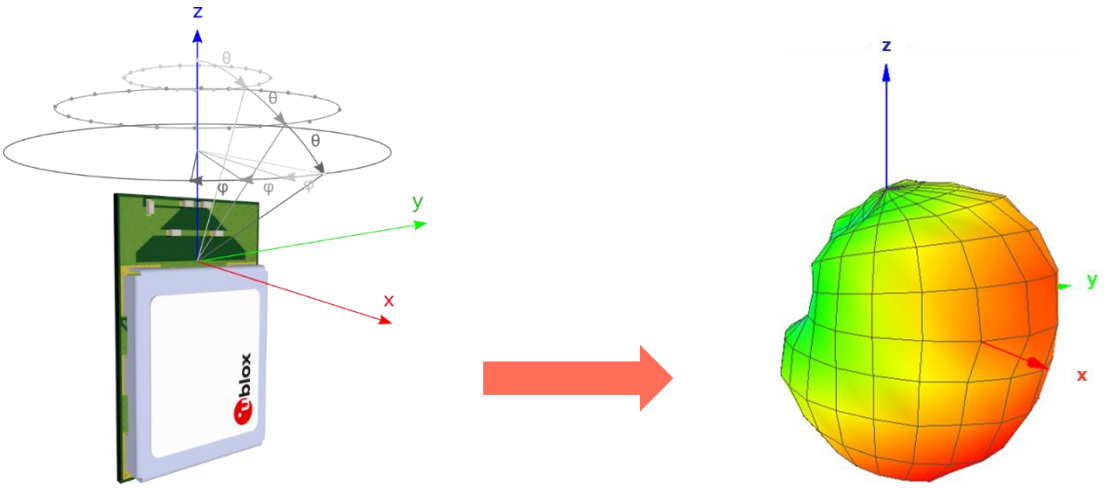
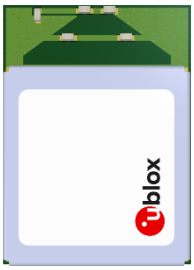
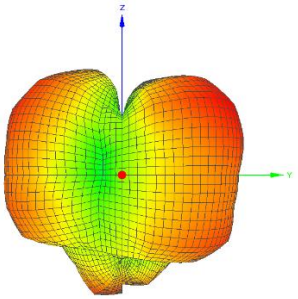
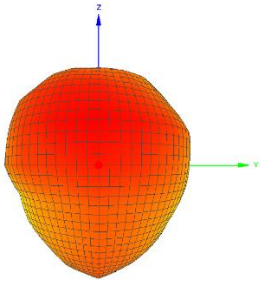
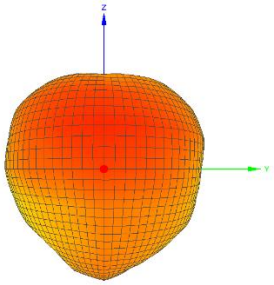
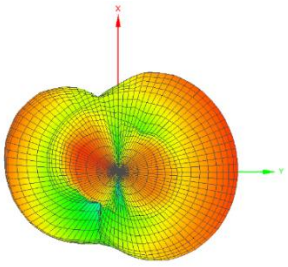
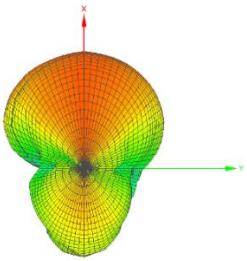
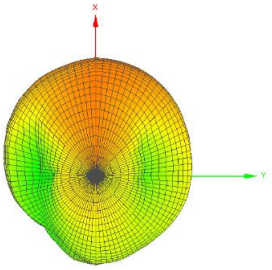


Figure 4: Spherical test points

Table 16 shows the displayed radiation patterns of the internal PCB trace antenna on NORA-B2x6.

View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 - -10 -2,5 5		
Top view, YZ plane positive X direction				
Side view, XY plane negative Z direction				

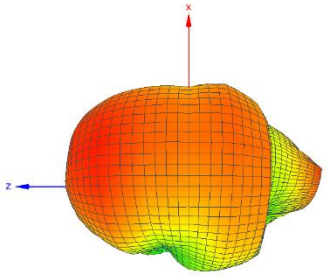
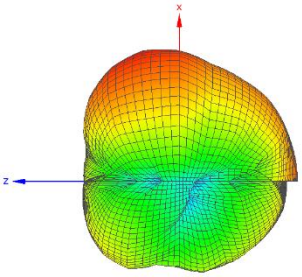
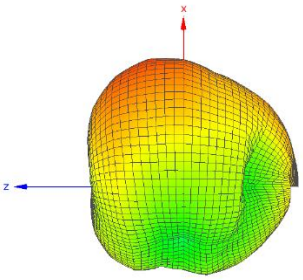
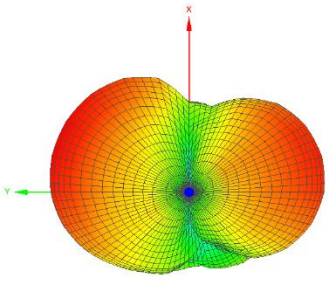
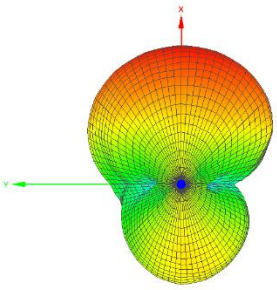
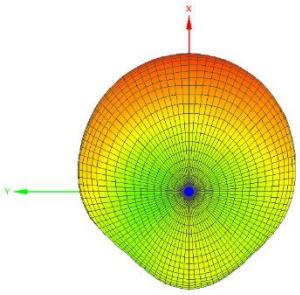
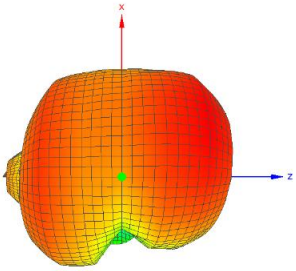
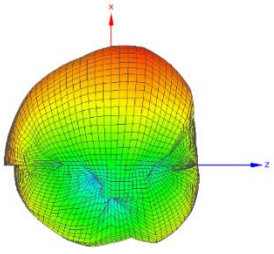
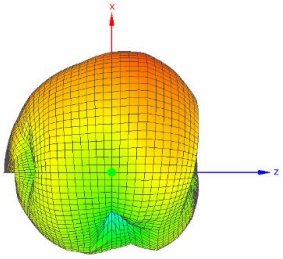
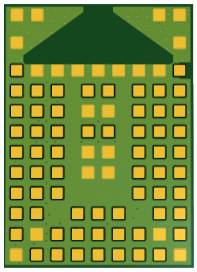
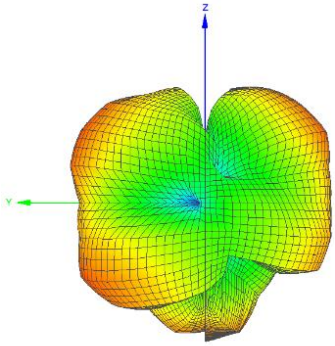
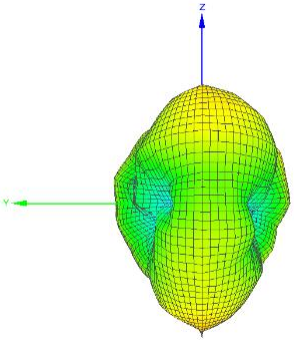
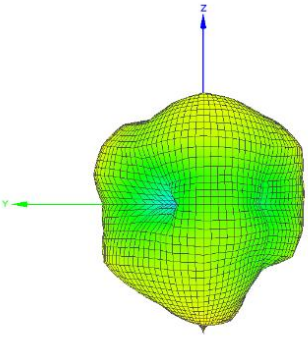
View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
Side view, XZ plane negative Y direction 			
Antenna Gain (dBi)  -25 - -10 -2,5 5			
Side view, XY plane positive Z direction 			
Side view, XZ plane positive Y direction 			
Bottom view, YZ plane negative X direction 			

Table 16: NORA-B2x6 antenna radiation patterns

4.2.6 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit
RESET_N	Time measured as time in power-on reset after supply reaches minimum operating voltage, with VCC rise time from 1 µs to 100ms		0.2	2	ms

Table 17: RESET_N pin characteristics

4.2.7 Digital pins

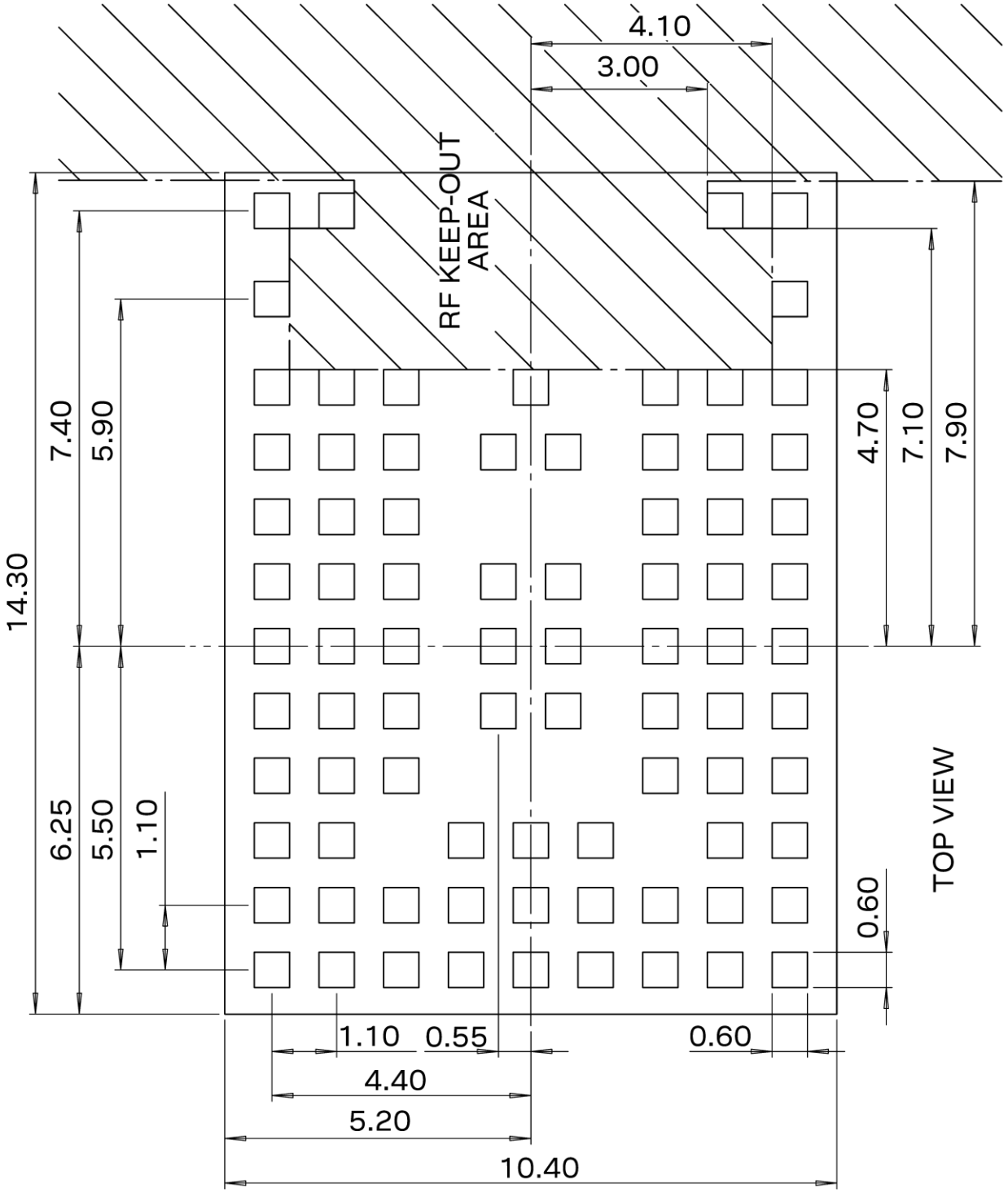
Condition	Min	Typ	Max	Units
Input high voltage	0.7 x VCC		VCC	V
Input low voltage	VSS		0.3 x VCC	V
Output high voltage, standard drive, 0.5 mA, VCC ≥1.7	VCC-0.4		VCC	V
Output high voltage, high drive, 5 mA, VCC >= 2.7 V	VCC-0.4		VCC	V
Output high voltage, high drive, 3 mA, VCC >= 1.7 V	VCC-0.4		VCC	V
Output low voltage, standard drive, 0.5 mA, VCC ≥1.7	VSS		VSS+0.4	V
Current at VSS+0.4 V, output set low, standard drive, VCC ≥1.7	1	3	4	mA
Current at VSS+0.4 V, output set low, high drive, VCC >= 1.7 V	3			mA
Current at VSS+0.4 V, output set low, extra drive, VCC >= 1.7 V	16			mA
Current at VCC-0.4 V, output set high, standard drive, VCC ≥1.7	1	3	4	mA
Current at VCC-0.4 V, output set high, high drive, VCC >= 1.7 V	4			mA
Current at VCC-0.4 V, output set high, extra drive, VCC >= 1.7 V	14			mA
Recommended maximum sustained current drawn by all GPIOs			15	mA
Rise/Fall time, high drive mode, 20-80%, 12 pF load		4		ns
Rise/Fall time, extra drive mode, 20-80%, 12 pF load		0.9		ns
Pull-up resistance	12	14	16	kΩ
Pull-down resistance	12	14	18	kΩ

Table 18: Digital pin characteristics

5 Mechanical specifications

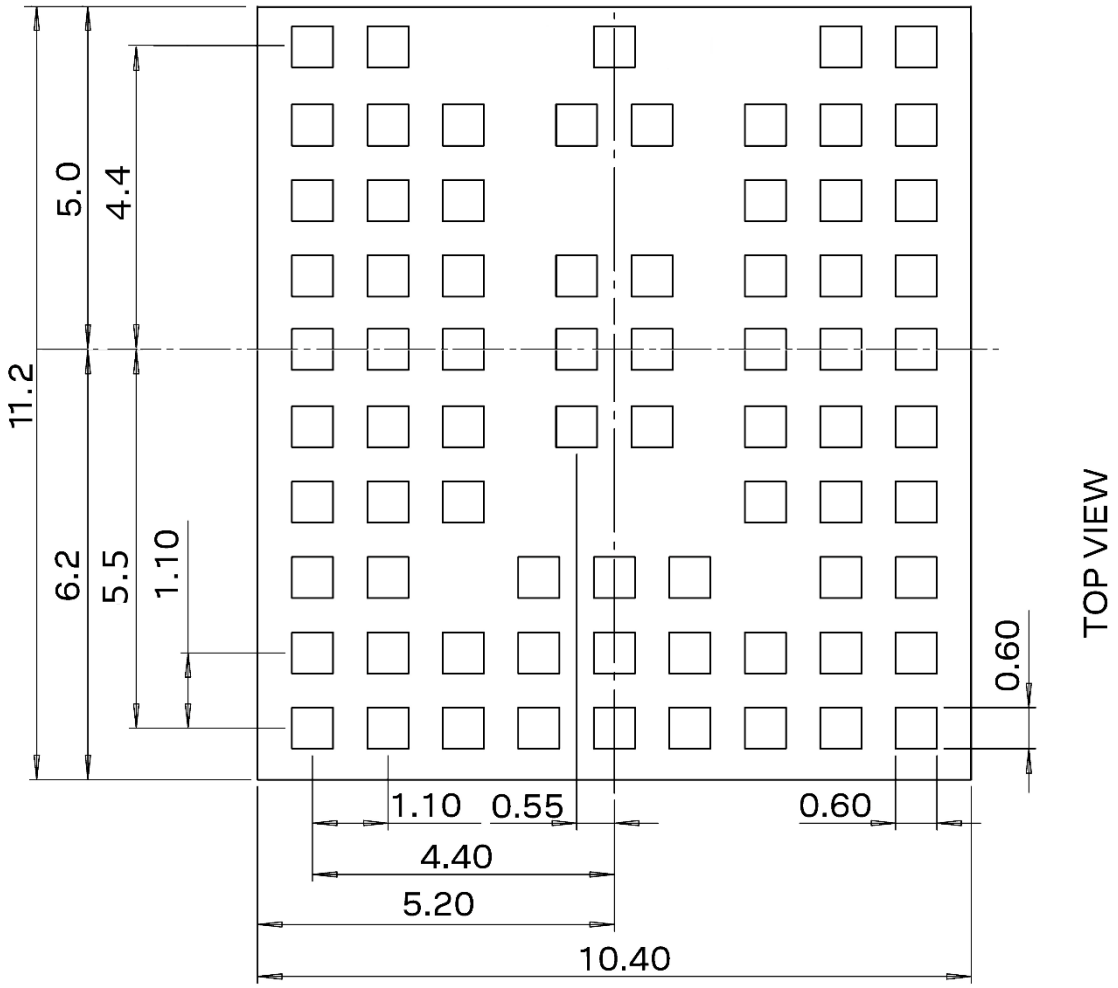
5.1 NORA-B2 footprint dimensions

Figure 5 shows the common footprint and dimensions of NORA-B2x6 modules, while Figure 6 shows the common footprint and dimensions of NORA-B2x1 modules. Nominal values are used.



All dimensions in mm.

Figure 5: NORA-B2x6 footprint dimensions

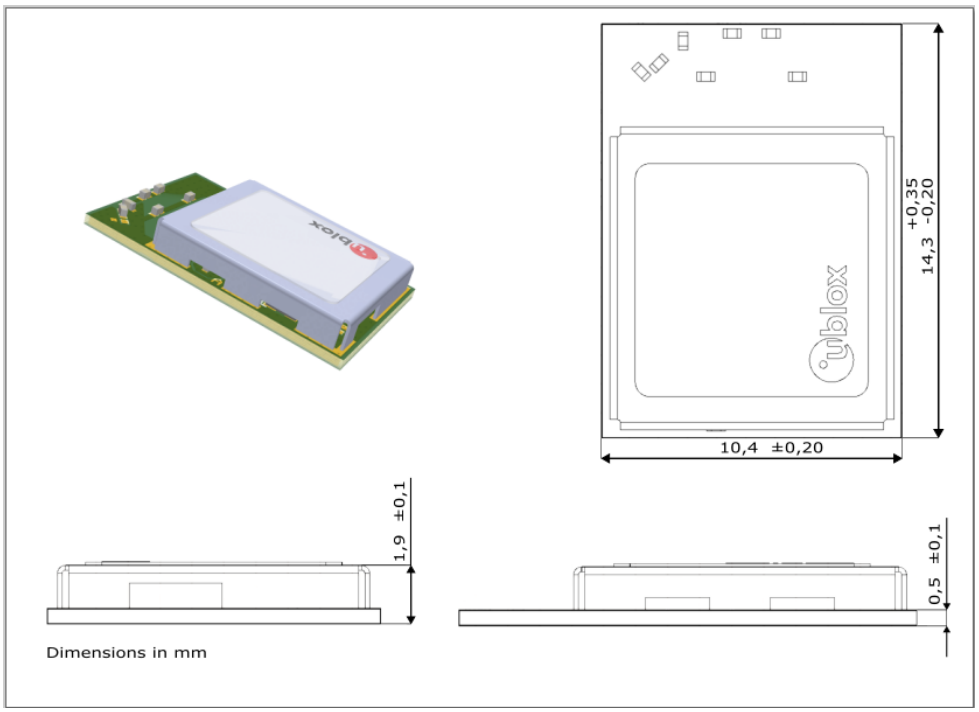


All dimensions in mm.

Figure 6: NORA-B2x1 footprint dimension

5.2 NORA-B2 mechanical specification

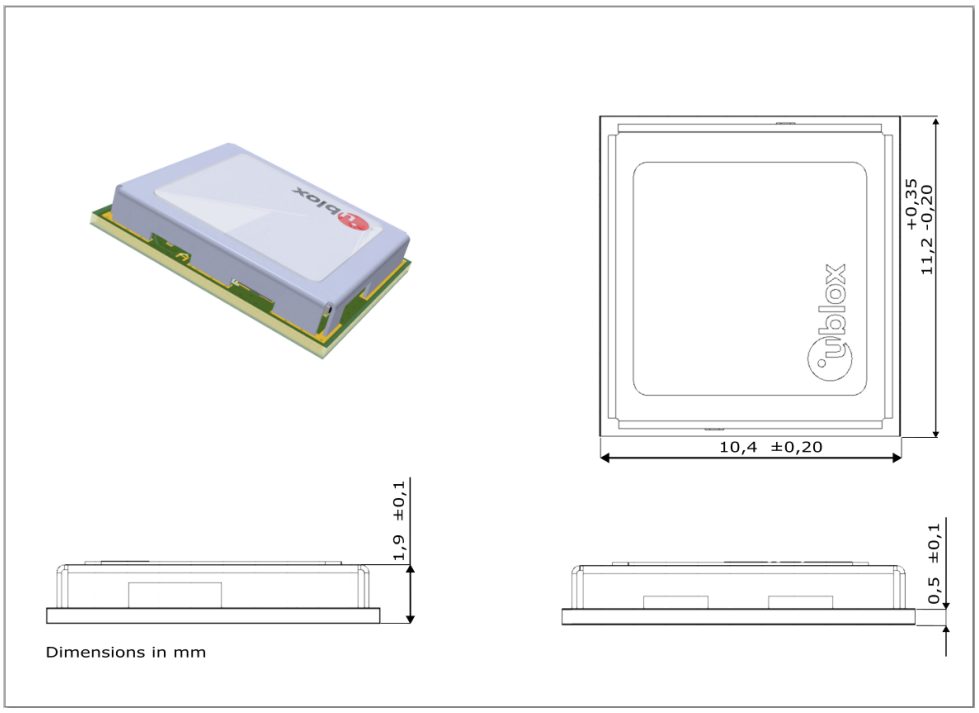
5.2.1 NORA-B2x6 mechanical specifications



Dimensions in mm

Figure 7: NORA-B2x6 mechanical specification

5.2.2 NORA-B2x1 mechanical specification



Dimensions in mm

Figure 8: NORA-B2x1 mechanical specification

6 Qualifications and approvals

⚠ All approvals are currently pending for all NORA-B2 module variants.

The development status of NORA-B2 series modules is described in the document information. Consequently, the information given in this chapter only becomes valid after each module variant has been fully tested and approved during the Initial Production stage.

6.1 Country approvals

NORA-B2 modules are certified for use in the following countries/regions:

Country/region	NORA-B2x1	NORA-B2x6
Europe	Pending	Pending
Great Britain (UKCA)	Pending	Pending
USA	Pending	Pending
Canada	Pending	Pending
Brazil	Pending	Pending
Japan	Pending	Pending
South Korea	Pending	Pending
Australia	Pending	Pending
New Zealand	Pending	Pending
Taiwan	Pending	Pending
South Africa	Pending	Pending

Table 19: Country approvals

☞ For detailed information about the regulatory requirements that must be met for all end-product applications based on NORA-B2 modules, refer to the system integration manual [1].

6.2 Bluetooth qualification

NORA-B2 series modules are qualified as Component (Tested) devices according to the Bluetooth 6.0 specification.

Product type	QDID	Listing date
NORA-B20 RF-PHY Component (tested)	Pending	08-Mar-2021

Table 20: NORA-B2 series Bluetooth qualified design ID

7 Product handling

7.1 Packaging

NORA-B2 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, refer to also the Packaging information reference guide [2].

7.1.1 Reels

NORA-B2 series modules are deliverable in quantities of 500 pieces on a reel. The reel types for the modules are shown in Table 21.

For more detailed information, see also the Packaging information reference guide [2].

Model	Reel type
NORA-B2x1	A3
NORA-B2x6	A3

Table 21: Reel types for different models of the NORA-B2 series

7.1.2 Tapes

Figure 9 and Figure 10 shows the position and orientation of the NORA-B2 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 11 and Figure 12

Figure 9: Orientation of NORA-B2 x6 module on tape

Figure 10: Orientation of NORA-B2 x1 module on tape

Figure 11 shows the tape and pocket dimensions for NORA-B2x6.

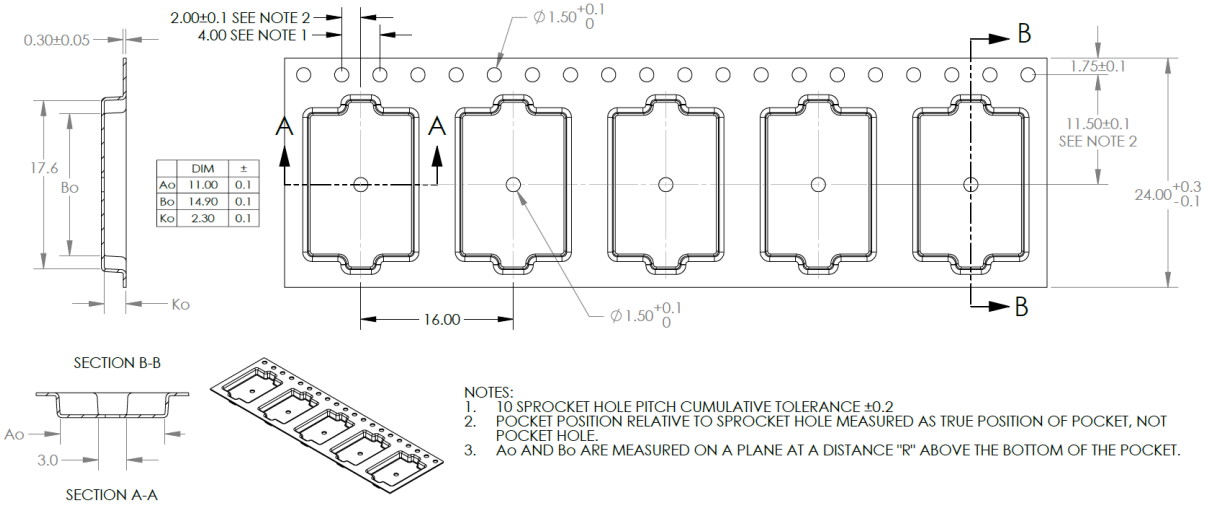


Figure 11: Tape and pocket dimensions for NORA-B2x6

Figure 12 shows the tape and pocket dimensions for NORA-B2x1

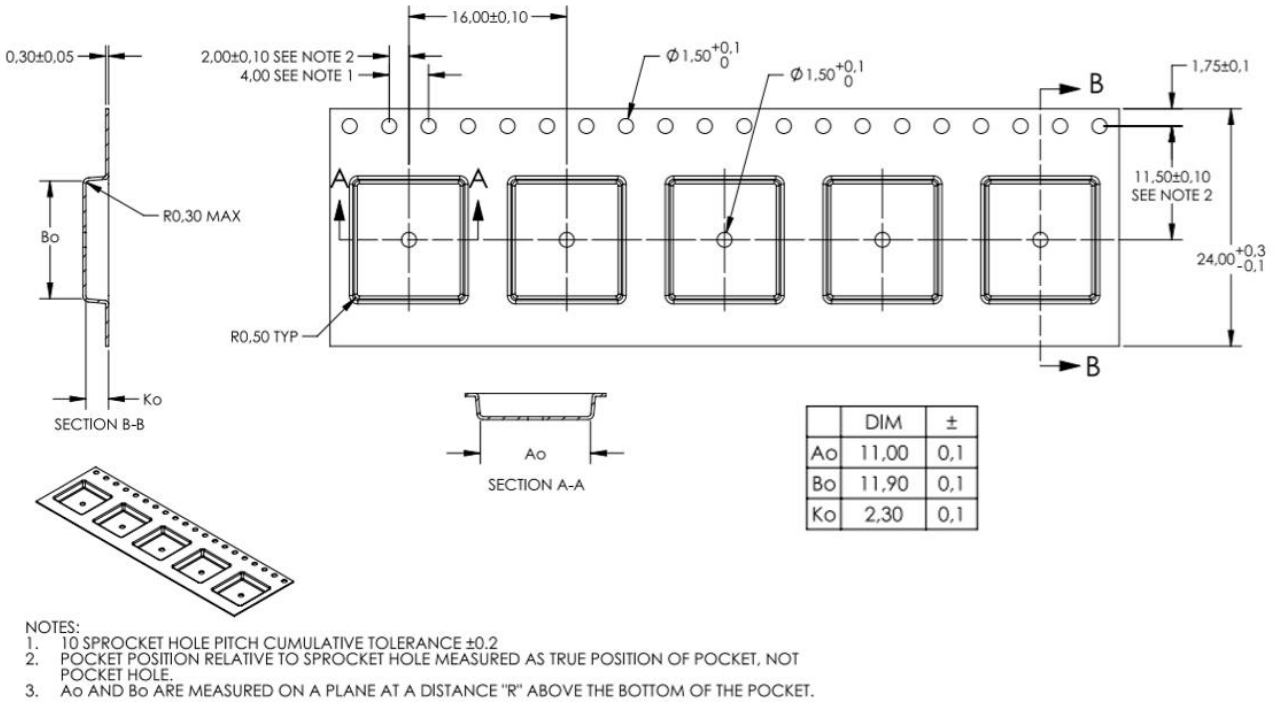


Figure 12: Tape and pocket dimensions for NORA-B2x1

7.2 Moisture sensitivity levels

NORA-B2 series modules are classified as Moisture Sensitive Devices (MSD) in accordance with the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions.

⚠ NORA-B2 series modules are rated at **MSL level 4** in accordance with the IPC/JEDEC J-STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 72 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding moisture sensitivity levels, labeling and storage, see the Packaging information reference guide [2].

☞ For MSL standards, see also IPC/JEDEC J-STD-020 and IPC/JEDED J-STD-033B. The standards can be downloaded from the JEDEC website [7].

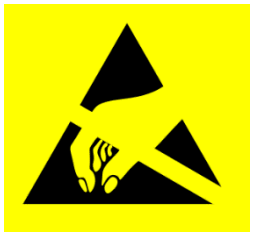
7.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. See the NORA-B2 series system integration manual [1] for more information.

⚠ Failure to follow these recommendations can result in severe damage to the device.

7.4 ESD precautions

⚠ NORA-B2 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the NORA-B2 series modules without proper ESD protection may destroy or damage them permanently.



NORA-B2 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to the ESD sensitive components. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the NORA-B2 series module. Failure to observe t hese recommendations can result in severe damage to the device.

8 Labeling and ordering information

The labels on NORA-B2 series modules include important product information.

8.1 Module marking

Figure 16 shows the label applied to NORA-B2 series modules. Each of the given label references are described in Table 22.

All units in mm unless specified otherwise specified.

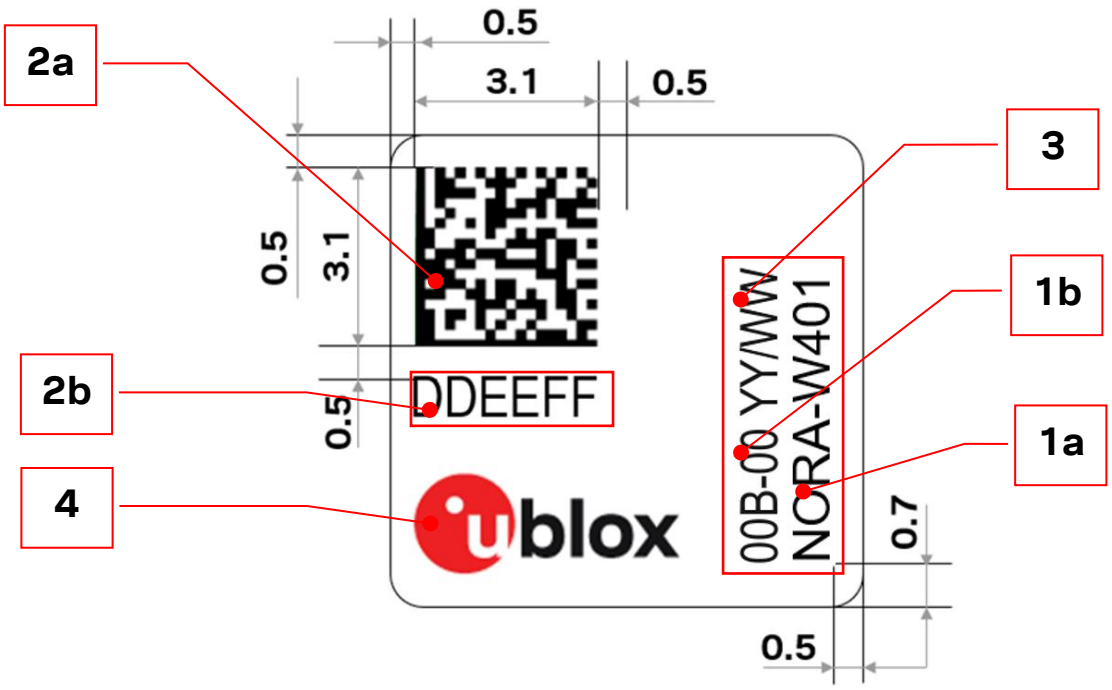


Figure 16: NORA-B2 series module marking

Reference	Description
1	Data Matrix with unique serial number comprising 19 alphanumeric symbols: - The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. - The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and The last 4 symbols represent the hardware and firmware version encoded HHFF.
2	Second half of the Bluetooth device address
3	Date of production encoded YY/WW (year / week)
4	Type number suffix
5	Product name (Model)

Table 22: NORA-B2 series module marking

8.2 Product identifiers

Table 23 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP-TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 23: Product code formats

8.3 Identification codes

Table 24 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	NORA
TG	Platform (Technology and Generation) T – Dominant technology, for example, W: Wi-Fi, B: Bluetooth G - Generation	B2: Bluetooth Generation 2 of NORA form factor
VV	Variant based on the same platform; range [00…99]	00: default configuration, with U.FL connector
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 24: Part identification code

8.4 Ordering information

Ordering Code	Product
NORA-B201-00B	NORA-B2 module with antenna pin, based on nRF54L15, open CPU for custom applications
NORA-B206-00B	NORA-B2 module with internal PCB antenna, based on nRF54L15, open CPU for custom applications
NORA-B211-00B	NORA-B2 module with antenna pin, based on nRF54L10, open CPU for custom applications
NORA-B216-00B	NORA-B2 module with internal PCB antenna, based on nRF54L10, open CPU for custom applications
NORA-B221-00B	NORA-B2 module with antenna pin, based on nRF54L05, open CPU for custom applications
NORA-B226-00B	NORA-B2 module with internal PCB antenna, based on nRF54L05, open CPU for custom applications

Table 25: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AoA	Angle of Arrival
AoD	Angle of Departure
BPF	Band Pass Filter
CBC-MAC	cipher block chaining - message authentication code
CCM	Counter with cipher block chaining - message authentication code
CMAC	Cipher-based Message Authentication Code
CPU	Central Processing Unit
CTI	Cross Trigger Interface
CTR	AES CCM combines counter
CTS	Clear To Send
DC	Direct Current
DMA	Direct Memory Access
DPPI	Distributed Programmable Peripheral Interconnect
DWT	Data Watchpoint and Trace
ECB	Electronic CodeBook
EDM	Extended Data Mode
ESD	ElectroStatic Discharge
ETM	Embedded Trace Macrocell
FCC	Federal Communications Commission (United States)
FEM	Front End Module
FLPR	Fast Lightweight Peripheral Processor
FPU	Floating Point Unit
GATT	Generic ATTribute profile
GCM	Galois/Counter Mode
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
ISED	Innovation, Science and Economic Development (Canada)
IEEE	Institute of Electrical and Electronics Engineers
IPC	Inter-Processor Communication
ITM	Instrumentation Trace Macrocell
LE	Low Energy
LNA	Low Noise Amplifier
MUTEX	Mutually Exclusive Peripheral
NFC	Near Field Communication
OEM	Original Equipment Manufacturer
OTP	One-Time Programmable
OUI	Organizationally Unique Identifier
PA	Power Amplifier
PDM	Pulse Density Modulation
PWM	Pulse Width Modulation

Abbreviation	Definition
QDEC	Quadrature DECoder
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RNG	Random Number Generator
GRTC	Global Real-Time Counter
RTLS	Real-Time Location Service
RTS	Request To Send
SDK	Software Development Kit
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TWI	Two-Wire Interface (See I2C)
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Control Registers
WDT	WatchDog Timer
XIP	eXecute In Place

Table 26: Explanation of the abbreviations and terms used

Related documents

[1] NORA-B2 system integration manual, UBXDOC-465451970-334
[2] Packaging information reference guide, UBX-14001652
[3] u-blox GitHub repository
[4] Nordic Semiconductor nRF54L15_nRF54L10_nRF54L05 Preliminary Datasheet v0.8
[5] Nordic Semiconductor nRF Connect SDK
[6] Channel Sounding at a glance
[7] JEDEC website

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	14-Jun-2024	habd	Initial release
R02	19-Feb-2025	habd	Updated according to the nRF54L15_nRF54L10_nRF54L05 Preliminary Datasheet v0.8 and nRF54L series revision **B** chipsets, Added support of all nRF54L series, added new 4 variants of the module in Document information. Updated the supply voltage to a single supply for the supply and the GPIO voltage 1.7V – 3.6V. Updated verification references from Bluetooth Core 5.4 to Bluetooth Core 6.0, Updated the Block diagram to reflect all module variants. Updated power domain diagram in Peripheral power domains. Updated Power management to describe that voltage modes are no longer relevant. Added the recommended value for the LFXO internal capacitance value in High-frequency clock HFCLK, added Channel sounding Channel sounding. Renamed **VCCIO** pins to **VCC**, revised assignments for pads G5, and G7 from NC to RF control pins in Pinout. Added Clock pins, Dedicated peripheral, and cross power-domain pins. Revised recommended operating voltage updated to 3.5V in Table 27. Updated Table 25: Product ordering codes. Minor updates and documentation improvements throughout the document.

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Mouser Electronics

Authorized Distributor

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