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NINA-B50 series

Stand-alone Bluetooth 5.3 low energy modules

Data sheet

Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for NINA-B50 series Bluetooth® 5.3 Low Energy modules. NINA-B50 provides an open CPU architecture with a powerful MCU for developing customer applications.

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Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Ordering code	Type number	Hardware version	IN/PCN reference	Product status
NINA-B501	NINA-B501-10B	NINA-B501-10B-00	01	N/A	In development
NINA-B506	NINA-B506-10B	NINA-B506-10B-00	01	N/A	In development
NINA-B501	NINA-B501-00B	NINA-B501-00B-00	06	N/A	Initial Production
NINA-B506	NINA-B506-00B	NINA-B506-00B-00	07	N/A	Initial Production

Contents

1 Functional description

1.1 Overview

Built on the NXP MCX W71 [5] or K32W1480 chip [3], NINA-B50 series modules feature Bluetooth 5.3 LE connectivity and a robust multicore MCU with an Arm® Cortex®-M33 supporting a Floating Point Unit (FPU) as the application core.

NINA-B50 module series offer cutting-edge power performance and incorporates state-of-the-art security features through the Arm TrustZone-M® secure storage and EdgeLock® Secure Enclave – including hardware cryptographic accelerators, random number generators, secure key generation, storage and management, secure boot and secure debug.

In addition to Bluetooth low energy, NINA-B50 also supports IEEE 802.15.4 including Thread®, Matter™, and Zigbee™, and a FlexCAN communication interface supporting CAN and CAN FD.

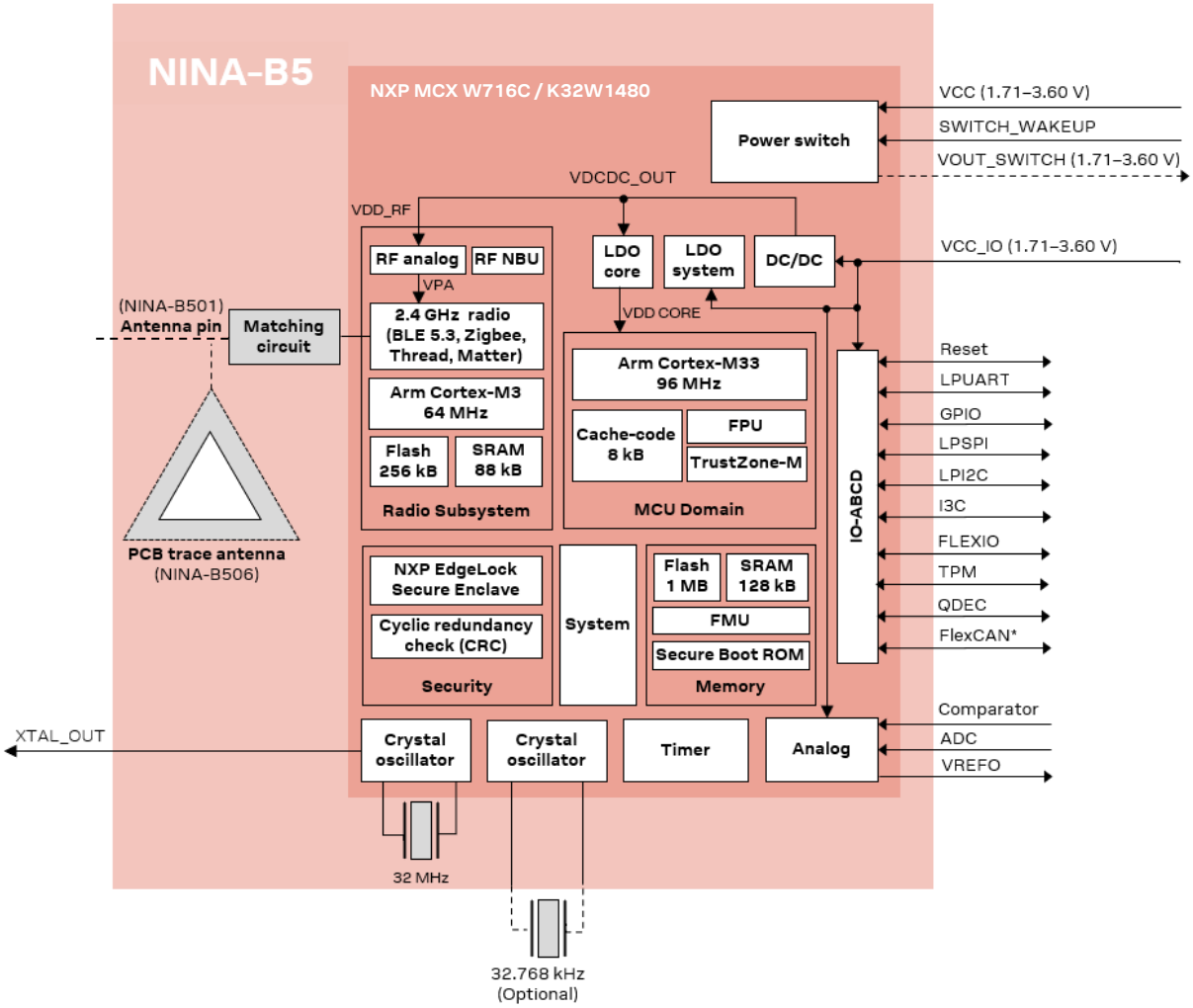
As the module design of NINA-B50 is common with other modules following the NINA form factor, NINA-B50 offers flexibility for similar product variants when designing the host platform.

1.2 Applications

1.2.1 Application examples

- Industrial automation
- Smart home, buildings and cities
- Low power sensors
- Wireless-connected and configurable equipment
- Point-of-sales
- Healthcare
- Tachograph

1.3 Block diagram



* FlexCAN is only supported by NINA-B50x-10B modules.

Figure 1: Block diagram of NINA-B50 series

1.4 Product variants

The NINA-B50 series modules consist of modules with two different antenna options. NINA-B501 supports an antenna pin for use with external antennas, while NINA-B506 includes an integrated PCB antenna.

1.4.1 NINA-B501

NINA-B501 has a pin for connecting to an external antenna. The RF signal for routing to an external antenna or antenna connector signal is exposed through a dedicated module pin (ANT). The module size of the NINA-B501 is smaller than that of the NINA-B506 (10.0 x 11.6 x 2.38 mm).

1.4.2 NINA-B506

NINA-B506 is equipped with an internal PCB trace antenna, using antenna technology licensed from Abracon. The RF signal is connected to the internal PCB trace antenna directly and is not connected to any pin on the module. The module size is 10.0 x 15.0 x 2.38 mm.

1.4.3 Modules with/without CAN

The latest revisions of NINA-B50 (NINA-B501-10B and NINA-B506-10B) are built on the NXP MCX W716C chip and support CAN and CAN FD. The predecessor modules NINA-B501-00B and NINA-B506-00B are built on the NXP K32W1480 and do not support CAN or CAN FD. The modules are hardware and software compatible, but a re-compile of the software is required. The predecessor modules are not recommended for new designs.

1.5 Product description

Item	NINA-B501	NINA-B506
Radio chipset, module with CAN Radio chipset, module without CAN	NXP MCXW716C [5] NXP K32W1480 [3]	NXP MCXW716C [5] NXP K32W1480 [3]
Supported 2.4 GHz radio protocols	Bluetooth 5.3 Low Energy IEEE 802.15.4 -2015 (Thread, Matter, Zigbee)	Bluetooth 5.3 Low Energy IEEE 802.15.4 -2015 (Thread, Matter, Zigbee)
	Bluetooth Low Energy specification	
Operating channels and frequencies	40 channels Channel numbers 0–39 2402–2480 MHz	40 channels Channel numbers 0-39 2402–2480 MHz
Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps (Coded PHY, S=2) 125 kbps (Coded PHY, S=8)	1 Mbps 2 Mbps 500 kbps (Coded PHY, S=2) 125 kbps (Coded PHY, S=8)
Typical conducted output power*	+7 dBm / +10 dBm	+7 dBm / +10 dBm
Radiated output power (EIRP)*	+10 dBm / +13 dBm with external 3 dBi antenna gain	+10 dBm / +13 dBm
Conducted RX sensitivity, 1 Mbps	-97.0 dBm	-97.0 dBm
Conducted RX sensitivity, 2 Mbps	-94.0 dBm	-94.0 dBm
Conducted RX sensitivity, long range 500 kbps (Coded PHY, S=2)	-101 dBm	-101 dBm
Conducted RX sensitivity, long range 125 kbps (Coded PHY, S=8)	-105 dBm	-105 dBm
	IEEE 802.15.4 specification	
Operating channels and frequencies	16 channels Channel numbers 11-26 2405–2480 MHz	16 channels Channel numbers 11-26 2405–2480 MHz
IEEE 802.15.4 data rate	250 kbps	250 kbps
Typical conducted output power*	+7 dBm / +10 dBm	+7 dBm / +10 dBm
Radiated output power (EIRP)*	+10 dBm / +13 dBm with external 3 dBi antenna gain	+10 dBm / +13 dBm
Conducted RX sensitivity, 250 kbps	-103 dBm	-103 dBm
	Module dimensions	
Module size	10.0 x 11.6 x 2.38 mm	10.0 x 15.0 x 2.38 mm

Table 1: NINA-B50 characteristics summary

* Depends on regulatory requirements and supply voltage level. For more details, see Table 11: RF performance.

1.6 Software

The open CPU architecture of the NINA-B50 series modules allows integrators to create their own applications by utilizing the comprehensive MCUXpresso SDK software from NXP. For more details, see the NINA-B50 system integration manual [6] [2].

1.7 Bluetooth device address

Each NINA-B50 module is pre-programmed with a unique 48-bit Bluetooth device address. If the memory of a NINA-B50 module is erased or otherwise lost, the address can be recovered from the data matrix barcode printed on the module label, as described in Product labeling.

2 Interfaces

For optimal design flexibility, NINA-B50 supports a wide range of interfaces, including a 2.4 GHz radio and antenna interface, digital interface, analog interface, and debug interface. See also the NXP MCX W71 data sheet [5], NXP MCX W71 reference manual [6], NXP K32W1480 data sheet [3] and NXP K32W1480 reference manual [4].

2.1 Power management

2.1.1 Power switch

NINA-B50 modules include an on-module power switch that can be used to switch off all or part of MCU power supply. When activated, the power switch reduces the module power consumption to a level that is less than that achievable in the Deep Power Down mode. You can also use the switch to supply power to an external device through **VOUT_SWITCH**.

The **VCC** input supply must be permanently applied to support both the standby RAM LDO and the RAM power switch. The power switch output signal, **VOUT_SWITCH,** can be enabled or disabled.

The power switch can be turned on in several ways:

- Power-On-Reset (POR). This condition is triggered when the module is initially powered on or when the power level falls below the POR threshold. POR resets all power domains, including the supply input to the switch, VCC of power switch input supply **VCC.**
- Drive **SWITCH_WAKEUP** low externally. The pin is internally pulled up to the switch input through a resistor and can be pulled down to wake up the smart power switch. To generate a valid internal wake-up signal successfully, a maximum pulldown voltage of 0.7 V on **SWITCH_WAKEUP** is required. The duration time should be greater than 1 µs.
- Through the System Power Controller (SPC). The SPC contains internal wake-up logic that controls the operation of the power system. The switch activates when **VSYS** is powered on.

2.1.2 DC-DC, digital I/O, analog, and system input supply (VCC_IO)

NINA-B50 modules require an additional voltage supply input **VCC_IO**. This voltage supply, **VCC_IO**, supply power for the following on-module function parts:

- DC-DC buck converter: Regulates the system core and radio power to provide the best power efficiency.
- LDO-System: A low-dropout regulator that generates the system voltage for the module.
- Analog domain, including an Analog-to-digital converter (ADC), comparators (CMP) and Voltage Reference (Vref) parts.
- Digital I/O interfaces

VCC_IO must be supplied through either **VCC** or **VOUT_SWITCH.** See also Power supply configuration.

☞ The voltage level of **VCC_IO** must be the same as the **VCC**.

2.1.3 Power supply configuration

NINA-B50 modules support two power supply configurations:

- Power efficient configuration
  - Supply external power to **VCC**
  - **VCC_IO** supplied from **VCC**
  - **VDD_LDO_CORE** and **VDD_RF** supplied from the DCDC output
  - VPA supplied from **VDD_RF**
- Power switch configuration
  - Supply external power to **VCC**
  - Supply the power switch output **VOUT_SWITCH** to **VCC_IO**
  - **VDD_LDO_CORE** and **VDD_RF** are supplied from DCDC output
  - VPA is supplied from **VDD_RF**

☞ A voltage level less than 3 V on **VCC** and **VCC_IO** has negative impact on the Tx output power.

☞ The on-module power switch can be disabled when it is not used. This means that the **VOUT_SWITCH** pin can be floating.

☞ See also the System integration manual [2] for power management and power supply configuration.

2.2 2.4 GHz radio

NINA-B50 includes a 2.4 GHz radio transceiver ,an integrated balun and filter/matching circuitry. NINA-B50 modules also have an integrated 32 MHz crystal as source of radio clock of the modules. See also Block diagram.

☞ For information about 32 MHz crystal trim value configuration, antenna reference designs, integration instructions and approved external antennas, see also the system integration manual [2].

2.3 RF antenna interfaces

NINA-B501 and NINA-B506 modules support different 2.4 GHz antenna solutions.

2.3.1 Internal antenna

NINA-B506 modules are equipped with an internal PCB antenna. This low-profile antenna solution is useful in space constrained designs and in designs that don't require an external antenna. The antenna pin (**ANT**) is internally disconnected on these modules. This solution uses antenna technology licensed from Abracon. See also antenna solutions in the System integration manual [2].

2.3.2 External antenna

NINA-B501 modules are equipped with an antenna pin (**ANT**) for connecting either an antenna connector or an external antenna. **ANT** is matched to 50 Ω and connected to the single-ended Tx/Rx antenna pin on the integrated 2.4 GHz radio transceiver in the main chip. The pin can be connected to an antenna connector or external antenna using a controlled impedance trace. See also antenna solutions in the System integration manual [2].

2.4 System functions

2.4.1 Power modes

NINA-B50 modules are power efficient devices that can operate in different power modes that control both power consumption levels and wake-up times. Specific parts of the module can be powered off when they are not needed. Complex wake-up events can also be generated from different external and internal inputs.

NINA-B50 supports several power modes:

- Active
- Sleep
- Deep Sleep
- Power Down
- Deep Power Down

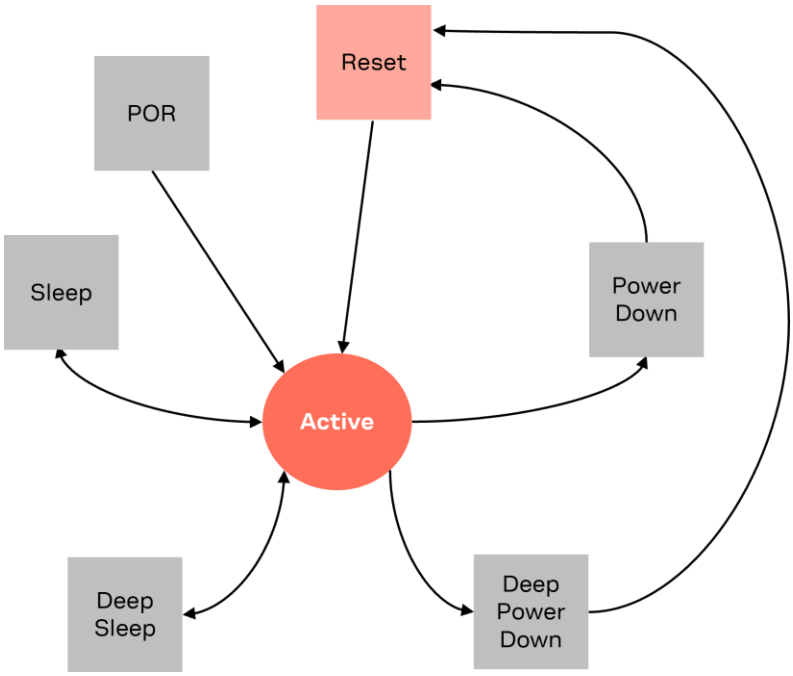


Figure 2: NINA-B50 modules power modes

2.4.1.1 Active

When powered on or reset, NINA-B50 enters Active mode and is initialized according to the configuration defined in the application software flashed in the modules.

In Active mode, CPU execution is possible. To achieve the performance requirements of a given system application while minimizing power consumption. Active mode provides different power-saving options.

Any reset brings the module back to the Active mode.

2.4.1.2 Power Down

NINA-B50 modules do not have a dedicated pin for powering off. The Power Down mode puts the module in a power-off state. The module wakes up from Power Down mode through the reset routine.

2.4.1.3 Deep Power Down mode

In Deep Power Down mode, NINA-B50 modules operate at the lowest possible power level. In this mode, the entire **VDD_CORE** domain (including all subdomains) is power gated and the on-module regulator for **VDD_CORE** is powered off. The **VDD_SYS** on-module regulator is powered, and the **VDD_SYS** power domain is enabled.

To avoid extra leakage, the external power supply to any disabled on-module regulators should be turned off. Memory data held in static RAM (SRAM) cannot be retained in Deep Power Down mode.

The module wakes from Deep Power Down mode through the reset routine. External reset or the **VDD_SYS** domain peripherals can wake the module.

2.4.1.4 Sleep

Sleep mode minimizes power consumption while maintaining the performance requirements of the system application.

In Sleep mode, CPU execution is halted. The core clock is gated off. The system clock as well as the bus clocks, if enabled, continue to operate.

Wake from Sleep mode is triggered by an interrupt or a wakeup event. Sleep mode also supports a partial wake-up where a bus controller other than the CPU, e.g., DMA is recovered by a wakeup event. The module automatically re-enters sleep mode after the bus controller finishes its task.

2.4.1.5 Deep Sleep

Deep Sleep mode sets NINA-B50 into a static state. It is the lowest power mode that retains all register data. The software can individually configure SRAM for deep sleep or shut down.

The module wakes from Deep Sleep mode through the interrupt routine or a wake-up event. Peripherals connected to the **VDD_CORE_WAKE** subdomain can wake the module. External signals can also wake the module through GPIO or **VDD_SYS** domain peripherals.

2.4.2 Module reset

NINA-B50 can be reset in one of the following ways:

- Pin reset: A low level on the **RESET_N** input pin.
- Power-on reset (POR): When supply voltage is below the POR threshold, the POR circuit triggers the power-on reset condition.
- Low Voltage Detect (HVD) reset: The HVD circuit is disabled by default. When the LVD is enabled and the supply voltage is above the HVD threshold, the circuit triggers an HVD reset.
- High Voltage Detect (LVD) reset: The LVD circuit is enabled by default. When the LVD is enabled and supply voltage is below the LVD falling threshold, the circuit triggers an LVD reset.

- Wakeup (WAKEUP) reset: When module wakes from Power Down or Deep Power Down modes, the power management logic triggers a wakeup reset in power domains that were previously powered off.
- Debug Access Port (DAP) reset: Any debug access port that can initiate a reset request from a connected debugger can trigger the DAP reset.
- Reset Timeout (RSTACK): The reset state machine includes a timeout counter that is triggered when the stack is inactive for more than 8192 cycles of the RTC 32.768 kHz clock. This condition triggers the RSTACK reset.
- Low Power Timeout (LPACK) reset: The low power entry state machine includes a timeout counter that is triggered if a module does not acknowledge entry into a low power mode after 8192 cycles of the RTC 32.768 kHz clock. This condition triggers the LPACK reset.
- System Clock Generation (SCG) reset: The system clock generator includes loss-of-clock and/or loss-of-lock monitors that can be configured to generate a reset. Either condition triggers the SCG reset.
- Software (SW) reset: When the software configures a system reset request in the MCU core.
- Watchdog 0 (WDOG0) reset: A watchdog timer monitors the software and expects periodic refreshing of the watchdog counter. A WDOG0 reset condition is triggered if the counter is not refreshed periodically.
- Watchdog 1 (WDOG1) reset: A watchdog timer monitors the software and expects periodic refreshing of the watchdog counter. A WDOG1 reset condition is triggered if the counter is not refreshed periodically.
- Lockup (LOCKUP) reset: Triggered when the Cortex-M33 core enters the lockup state as a result of certain illegal operations.
- JTAG (JTAG) reset: Occurs when a JTAG instruction places the module in reset.
- Security Violation (SECVIO) reset: Triggered when the module detects a security violation.

2.4.3 CPU and memory

NINA-B50 modules includes an Arm Cortex-M33 MCU with FPU, supporting clock speeds of up to 96 MHz with 1 MB flash, 128 kB SRAM, 8 kB code cache for data storage and code, and 96 kB Secure Boot ROM that stores the boot code and time-critical software library routines.

NINA-B50 series modules include a multicore microcontroller unit (MCU) handling security, radio, and application tasks, where each core manages its own dedicated memory resources. Users can develop applications using the application core, which integrates an Arm Cortex-M33 MCU with an FPU, 1 MB flash memory, and 128 kB SRAM. NINA-B50 also provides an external memory connection to the Low-power serial peripheral interface (LPSPI).

2.4.4 ROM bootloader

The ROM bootloader is the boot code that resides in the internal read-only memory (ROM) of the module. The bootloader is executed when the host processor is released from reset. The code supports automated booting from the internal flash and downloads an image over the serial interface, LPUART, LPI2C, or LPSPI.

2.4.5 Enhanced Direct Memory Access (eDMA)

The enhanced Direct Memory Access (eDMA) can perform complex data transfers with minimal intervention from a host processor. The eDMA is a highly programmable data-transfer engine that is optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data transfer is of a static size and not defined within the data itself.

2.4.6 Real Time Clock (RTC)

The Real Time Clock (RTC) is a key system feature of the module.

By default, the time counter in the RTC is driven from a 32.768 kHz clock, which can also supply other peripherals. The clock can be sourced from an external 32 kHz Crystal Oscillator (OSC) or an embedded 32 kHz Free Running Oscillator (FRO) on the module.

The RTC block includes an internal clock validation mechanism that ensures the clock from OSC is stable. It also incorporates a switch that allows the module to switch the clock source from the 32 kHz FRO to the OSC when it is stable. The module can switch back to the 32 kHz FRO clock if the software disables the 32 kHz OSC.

The 32 kHz FRO is enabled after Power-On-Reset (POR) and serves as the clock source to the device. The 32 kHz FRO can be disabled by the software when necessary.

The external 32 kHz OSC is disabled after POR but can be enabled by software when needed.

The RTC is an “always-powered” block that remains functional in all low power modes. It can generate an interrupt to exit any low-power mode.

The RTC operates in one of the two available modes of operation:

- Power-on mode. The RTC remains powered During module power-up. In this mode, all RTC registers are accessible by software and all functions are operational. If enabled, the 32.768 kHz clock can be supplied to the rest of the module.
- Power-down mode. During module power-down, the RTC remains powered and is electrically isolated from the rest of the chip. If enabled, the RTC continues to increment the time counter and retains the state of the RTC registers. The RTC registers are not accessible. The time counter can generate multiple interrupts and events for the CPU, radio, as well as the internal and external hardware blocks. By default, the frequency of the interrupt is 1 Hz, but it can also be configured to trigger every 2, 4, 8, 16, 32, 64, or 128 Hz.

The RTC signals and pinout for NINA-B50 is shown in Table 2.

Signal	I/O	Pinout	Description
PTD5/EXTAL32K	I	2	32.768 kHz oscillator input, connection to an optional external 32.768kHz crystal Can be configured as a GPIO pin
PTD4/XTAL32K	O	3	32.768 kHz oscillator output, connection to an optional external 32.768kHz crystal Can be configured as a GPIO pin
RTC_CLKOUT	O	NA	Prescaler square-wave output or RTC 32.768 kHz clock Can be configured to get the signal via TAMPER1
RTC_WAKEUP_b	O	NA	Active low wakeup for external device Can be configured to get the signal via TAMPER0
RTC_TAMPER0	I	17	Tamper pin input

Signal	I/O	Pinout	Description
RTC_TAMPER1	I	18	Tamper pin input
RTC_TAMPER2	I	NA	Tamper pin input Connects to an external 32.768kHz crystal

Table 2: RTC signals and pinout on NINA-B50

2.5 Serial interfaces

NINA-B50 supports the following serial communication interfaces:

- Two Low Power UART (LPUART) interfaces: 4-wire universal asynchronous receiver/transmitter interface.
- Two Low Power SPI (LPSPI) interfaces: Up to three serial peripheral interfaces can be used simultaneously.
- Two Low Power I2C (LPI2C) interfaces: Inter-Integrated Circuit (I2C) interface for communication with digital sensors.
- Single I3C interface: Based on an enhanced serial communication specification, this interface improves the features, performance, and power efficiency available in I2C. For mid-speed applications, it provides an alternative to the Standard Peripheral Interface (SPI).
- Single programmable FLEXIO: This highly configurable interface is suitable for a wide range of functionalities, including but not limited to UART, I2C, SPI, I2S, Camera IF, Motorola 68K/Intel 8080 bus, PWM/Waveform generation, and input capture for interval measurements using the Single-Edge Nibble Transmission (SENT) protocol, for example.
- Single highly configurable, synthesizable Controller Area Network (FlexCAN) interface to be used as a serial data bus (not supported by NINA-B501-00B or NINA-B506-00B).

☞ The module shares most digital interface pins between digital and analog interfaces, and GPIOs. By multiplexing the signals, several digital functions can be made available on a single pin.

☞ Two of the SPI interfaces share common hardware with the I2C interfaces, which means that they can't be used simultaneously. If both I2C interfaces are in use, then only one SPI interface is available.

2.5.1 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

NINA-B50 supports two Low Power Universal Asynchronous Receiver/Transmitter (LPUART) interfaces, LPUART0 and LPUART1.

LPUART interfaces provide asynchronous, serial communication capability with external devices. LPUART supports a non-return-to-zero (NRZ) encoding format and IrDA compatible, low-speed, serial infrared (SIR) format. The LPUART interfaces can continue operating while the processor is in low-power mode – if an appropriate peripheral clock is available. The LPUART can generate an interrupt or DMA request to wake up the module from low power modes.

The LPUART interfaces support hardware flow control and baud rates up to 1 Mbps.

Pin configuration:
- TXD, data output pin
- RXD, data input pin

- RTS, Request To Send, flow control output pin (optional)
- CTS, Clear To Send, flow control input pin (optional)

2.5.2 Low-power serial peripheral interface (LPSPI)

NINA-B50 supports two Low-power Serial Peripheral Interface (LPSPI) interfaces, LPSPI0, and LPSPI1.

- LPSPI0 doesn't support a PCS1/HREQ pin and the related fields in the CFGR0 register are reserved.
- LPSPI is a low-power SPI that provides an efficient interface to a SPI bus – either as a Main and/or Sub node. The SPI bus is a synchronous serial communication interface commonly used in embedded systems for communications between microcontrollers and peripheral devices over short distances. Low-power serial peripheral interfaces are typically used in Secure Digital cards and LCD displays.

Features of the LPSPI include:

- Pin configuration in main node configuration:
  - SCK, Serial clock output, up to 12 MHz for LPSPI0 and 24 MHz for LPSPI1
  - SOUT, Serial Output data line
  - SIN, Serial Input data line
  - PCS[0-3], Active-low, Chip select outputs that define which Sub node to communicate with on the bus.
- Pin configuration in sub node configuration:
  - SCK, Serial clock input up to 12 MHz
  - SOUT, Serial Output data line
  - SIN, Serial Input data line
  - PCS[0-3], Chip select, active-low, inputs that connect/disconnect the Sub-node interface from the bus.
- Supports Main and Sub node on both interfaces. Main node operation supports up to four peripheral Chip selects.
- Continues operating in Sleep modes – if configured to do so and an appropriate clock is available
- Minor CPU overhead with DMA offloading of FIFO register accesses.
- Supports DMA accesses and generates a DMA request
- Configurable clock polarity and clock phase
- Enables external memory to connect to the module for use as external storage, including SD cards, LCD displays, and graphic data. If external flash is used, LPSPI1 is configured as the Main mode, using the pin assignments shown in Figure 3.

Signal name	NINA-B50 pin	Description
LPSPI1_SCK	PTB2	Serial clock output, up to 24 MHz
LPSPI1_SIN	PTB1	Serial input data/ Data 1 I/O signal
LPSPI1_SOUT	PTB3	Serial output data/ Data 0 I/O signal
LPSPI1_PCS2	PTC0	Data 2 I/O signal
LPSPI1_PCS3	PTC1	Data 3 I/O signal
LPSPI1_PCS0	PTB0	Active-low Chip/Sub node select output, Selects which Sub node on the bus is to communicate with.

Figure 3: Main node configuration for external flash

☞ By default, SIN is input signal and SOUT is output signal but SIN and SOUT can be configured differently.

☞ SIN and SOUT instead of commonly used MOSI and MISO are used for SPI data signal names throughout this datasheet to keep the names aligned with the names in the NXP K32W1480 data sheet [3], NXP K32W1480 reference manual [4], NXP MCX W71 data sheet [5] and NXP MCX W71 reference manual [6].

2.5.3 Low Power Inter-Integrated Circuit (LPI2C)

NINA-B50 supports two Low Power Inter-Integrated Circuit (LPI2C) interfaces, LPI2C0, and LPI2C1. The interfaces provide a synchronous packet-switched, single-ended serial bus that can be used for Main and Sub nodes. It can transfer and/or receive data on a 2-wire bus network and is often used to attach microcontrollers to lower-speed peripheral ICs.

The interfaces comply with the System Management Bus (SMBus) specification (version 3) and can operate as both Main and Sub nodes. The I2C bus supports standard-mode (100 kbps), fast-mode (400 kbps), fast-mode plus (1 Mbps) and ultra-fast (3.2/3.33 Mbps) operation. The interfaces also support multiple Main nodes including synchronization and arbitration. Any number of Main nodes can be present on the LPI2C interface. Additionally, Main and Sub node roles may change between messages (after a STOP is sent).

DMA offloading of FIFO register accesses mean that use of the interfaces operate with only a minor CPU overhead. The interfaces continue to operate in sleep modes if an appropriate clock is available.

- The I2C 2-wire pin configuration:
  - SCL, clock output in Main mode, input in Sub mode
  - SDA, data input/output pin
- The I2C 4-wire pin configuration:
  - SCL, clock input pin
  - SDA, data input pin
  - SCLS, secondary clock line. SCLS output pin in Main mode. If LPI2C Main/Sub nodes are configured to use separate pins, then this is the SCL pin for the Main node.
  - SDAS, secondary data line. SDAS output pin in Main mode. If LPI2C Main/Sub nodes are configured to use separate pins, then this is the SDA pin for the Sub node.

2.5.4 Improved Inter-Integrated Circuit (I3C)

NINA-B50 supports a single Improved Inter-Integrated Circuit (I3C) interface, I3C0. Based on an enhanced serial communication specification developed by the Mobile Industry Processor Interface Alliance (MIPI Alliance), this interface improves the features, performance, and power efficiency available in I2C. For mid-speed applications, it provides an alternative to the Standard Peripheral Interface (SPI). The I3C bus is intended to connect microcontrollers (MCU) and application processors (AP) to sensors, actuators, and other MCUs as Sub nodes.

The major use cases for this interface include:

- Connecting an MCU to other MCUs, and
- Connecting an Access Point (AP) to an MCU

To operate in I3C mode, the PV, PE, and PS values in the corresponding PORT_PCR registers must be correctly configured with a pull-up resistor.

Features of the I3C interface include:

- 2-wire multi-drop bus capable of 12 MHz clock speeds for up to 11 devices.
- In-band interrupts (IBI) are allowed, which allow Sub nodes to notify Main nodes.
- Built-in commands are issued in a separate “space,” so that these commands do not collide with normal messaging between the Main and Sub nodes.
- Organized forms of multiple main nodes modes. Secondary Main nodes can use clean handoffs between other Main nodes.
- Devices can hot-join the bus later than when the bus starts.
- Capable of using both I2C and I3C busses with bridging support for to I2C, SPI, UART, and other busses.
- Higher data rate modes (about 20 Mbps) are optionally available.
- Sub nodes can be as small as 2K gates (or less), which allows the I3C interface to be controlled by a processor and fully state-machine driven.
- Supports the full I3C feature set – except for ternary data rates (HDR-TSP, HDR-TSL).

2.5.5 Flexible input/output (FlexIO)

NINA-B50 supports a single FlexIO interface, FLEXIO0. This highly configurable interface is suitable for a wide range of functionalities, including but not limited to:

- UART
- I2C
- SPI
- I2S
- Camera IF
- Motorola 68K/Intel 8080 bus
- PWM/Waveform generation
  Input capture for interval measurements using the Single-Edge Nibble Transmission (SENT) protocol, for example.

Features of the FlexIO include:

- Emulation of a variety of serial/parallel communication protocols
- 32-bit, shift register array with support for transmit, receive, data match, logic mode, and state modes
- Double-buffered, shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start/stop bit generation
- 1, 2, 4, 8, 16, or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA or polled transmit/receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions
- Programmable logic mode for integrating external digital logic operations, including on-chip or combining pin/shifter/timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU, with support for up to eight states, eight outputs, and three selectable inputs per state
- Integrated, general-purpose, input/output registers and pin rising/falling edge interrupts to simplify software support

- Flexible 16-bit timers with support for a variety of trigger, reset, enable and disable conditions
- Programmable logic blocks allowing the implementation of digital logic functions on-chip and configurable interaction of internal and external modules
- Programmable state machine for offloading basic system control functions from CPU

2.5.6 FlexCAN

The FlexCAN interface is a full implementation of the CAN protocol specification, the CAN with Flexible Data Rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads.

The CAN interfaces include the following features:

- Compliant with the ISO 11898-1:2015 standard
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured legacy Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Full-featured enhanced Rx FIFO with storage capacity for up to 12 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Total 32 Flexible message buffers (MBs) configurable as Rx or Tx with 8 bytes data length of each
- RAM not used by reception or transmission structures can be used as general-purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority fist
- Time stamp based on 16-bit free running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wakeup on bus activity or matching with received frames (Pretended Networking)
- Transceiver delay compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the module is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process

- Powerful legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 16 extended or 32 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask.
- 100% backward compatibility with previous FlexCAN version
- Supports Pretended Networking functionality in low power: Doze mode, Stop mode

☞ A CAN transceiver needs to be connected to the CAN interface of the NINA-B50 module to support the CAN feature.

☞ CAN interface is supported on NINA-B501-10B and NINA-B506-10B, but not supported on the NINA-B501-00B or NINA-B506-00B modules.

2.6 Other digital interfaces

2.6.1 Timer/ PWM (TPM)

NINA-B50 modules support three Pulse Width Modulation timers, TPM0, TPM1 and TPM2. TPM0 is a 2-channel 32-bit timer and TPM1 and TPM2 are 6-channel 32-bit timers.

The Pulse Width Modulation timer (TPM) supports input capture, output compare, and the generation of Pulse Width Modulation (PWM) signals to control electric motor and power management applications. The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

Features of TPM include:

- Selectable clock mode. In this mode the timer can be incremented on every edge of the asynchronous clock or on the rising edge of an external clock input synchronized to the asynchronous counter clock
- Pre-scaler allows the timer to divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- 32-bit counter that operates as a free-running or modulo counter. The counting can be both up or up-down
- Six configurable channels for input capture, output compare, edge-aligned or center-aligned PWM modes
- Interrupts and/or DMA requests per channel and on counter overflow conditions
- Selectable trigger input to optionally reset, start, increment, or stop the counter in overflow conditions
- Generation of hardware triggers per channel when the counter overflows

2.6.2 Quadrature Decoder (QDEC)

The quadrature decoder (QDEC) is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction.

The QDEC uses two inputs, **channel 0** (**PHASE_A)** and **channel 1 (PHASE_B)**, to control incremental and decremental counting in the TPM counter. The QDEC supports two encoding modes: count and direction encoding mode and phase encoding mode. See also Timer/ PWM (TPM).

2.7 Analog interface

14 out of the 29 digital GPIOs can be multiplexed to analog functions. The following analog functions are available:

- 1x 16-bit Analog to Digital Converter (ADC)
- 2x Low-power Comparator (LPCMP)
- 1x Voltage Reference (VREF)

2.7.1 Analog to Digital Converter (ADC)

A 16-bit dual successive approximation Analog to Digital Converter (ADC) is used to sample an analog voltage on any of the analog-capable pins on the module.

Features of the ADC include:

- Full swing input range of 0 V to **VCC_IO**
- Supports three sampling modes:
  - Single-ended mode: Only one side channel from A-side or B-side is converted.
  - Differential mode: A single input pin is used.
  - Dual single-ended mode: Both A-side and B-side channels are converted independently and simultaneously. In this case, fixed pairs of input pins are used. For example, **ADC0_A5** and **ADC0_B5** or **ADC0_A6** and **ADC0_B6**.
- Resolution:
  - Differential mode: 16-bit high resolution or 13-bit standard resolution
  - Single-ended mode: 16-bit high resolution or 12-bit standard resolution
- Sample rates up to 2 MS/s
- Configurable analog input sample time
- Configurable speed options to accommodate operation in low-power modes
- Trigger detection with up to four trigger sources with priority level configuration
- Multiple command buffers provide flexibility for channel scanning and independent channel selections for different trigger sources.
- Automatic comparison of conversion results
- Two independent FIFO result registers, each containing 16 entries
- Interrupt, DMA, or polled operation
- Linearity and Gain adjustment calibration logic

2.7.2 Low Power Comparator (LPCMP)

NINA-B50 supports two Low Power Comparators, (LPCMP), LPCMP0, and LPCMP1.

The comparators provide circuits for comparing two analog input voltages on the analog-enabled pins on the module. The comparators are comprised of a comparator (CMP), DAC, and analog mux (ANMUX).

Features of the comparator include:

- Operation over the full input range of 0 V to **VCC_IO**
- Multiple operation modes with advanced features to produce a wide range of outputs, such as sampled, windowed, and digitally filtered.
- Selectable performance levels: nano power mode, low power/speed mode, and high power/speed mode
- Supports interrupt and DMA, programmable hysteresis control, and selectable inversion on comparator output
- Two 8-to-1 channel ANMUX that can operate over the full range of the supply voltage to select input signal from eight channels
- 8-bit resolution DAC with a 256-tap resistor, ladder network that provides selectable supply reference source, selectable reference voltage, and configurable low power/speed mode or high power/speed mode

2.7.3 Voltage Reference (VREF)

NINA-B50 series modules have one Voltage Reference (VREF) buffer system that employs unity gain amplifiers.

For use with external devices, VREF provides reference voltage that can be set from 1.0 V to 2.1 V. The buffered reference is also available internally for use with on-module analog peripherals, such as the ADC, DAC, or CMP. VREF has a dedicated output pin, **VREFO**. When VREF is enabled, the reference voltage is placed on the **VREFO** pin.

The voltage reference has three operating modes yield different levels of supply rejection and power consumption. The operating modes are OFF mode, low-power buffer mode, and high-power buffer mode.

- In the OFF mode, the VREF bandgap and the output buffers are disabled, which means that the voltage output is not buffered.
- In low power buffer mode, the module activates the buffer to generate a buffered voltage for **VREF_OUT.** This voltage can be adjusted within the range of 1.0 V to 2.1 V.
- In high-power buffer mode, the module activates the high-power buffer to generate a programmable buffered voltage for **VREF_OUT**. The voltage can be adjusted in 0.1 V increments ranging from 1.0 V to 2.1 V. The reference voltage output can be fine-tuned with 0.5 mV increments. For course tuning adjust the output with 100 mV resolution using the trim registers.

The VREF system includes an internal voltage regulator that you can enable to enhance supply noise rejection, as well as an internal oscillator that provides the chop clock. For optimal VREF performance, it is advisable to enable the regulator and oscillator whenever possible. If you are using the chop function, you must also enable the internal voltage regulator. When enabling the internal regulator, a specific sequence should be followed.

VREF can operate when the chip is in a low-power mode. However, enabling the VREF regulator results in increased current consumption. In low power mode, it may be appropriate to disable the VREF regulator to minimize current consumption. Disabling the VREF regulator can lead to a reduction in the accuracy of the output voltage, by as much as several millivolts (mV).

2.7.4 Analog pin options

☞ An analog pin may not be simultaneously used for multiple functions.

Table 3 shows the supported connections of the analog functions.

Symbol	Analog function	Can be connected to
VCC_IO	**Analog** domain **power supply**	**VCC or VOUT_SWITCH**
ADCP	ADC single-ended or differential positive input	Any analog input on A-side (ADC0_An) or on B-side (ADC0_Bn)
ADCN	ADC differential negative input	Any analog pin of ADC0_An and ADC0_Bn pin pairs
VREFH	Reference voltage for the CMP-DAC	Can be configured to be VCC_IO or VREFO
LP_INP	Low-power comparator IN+	Any analog pin CMPn_INx
LP_INM	Low-power comparator IN-	Any analog pin CMPn_INx
LPCMPO	Low-power comparator output	CMP0_OUT or CMP1_OUT

Table 3: Possible uses of the analog pins

2.8 GPIO

NINA-B50 supports four General-Purpose Input and Output (GPIO) interfaces: GPIOA, GPIOB, GPIOC, and GPIOD. Two interrupt channels have been assigned to each GPIO interface.

For optimal pin performance, the GPIO interfaces communicate with the processor core through a zero-wait state interface.

The module has 29 GPIO pins. 14 of these are analog-capable pins that can be assigned to analog functions. The signal multiplexing of each pin is shown in Table 5.

2.8.1 Drive strength

All GPIO pins are configured for low current consumption by default. Using this standard drive strength, a pin configured as output can source or sink a specific amount of current.

If the timing requirements of a digital interface can't be met, or if an LED requires more current, a high drive strength mode is also available. This mode allows the digital output to draw more current. See also Digital pins.

2.9 Debug interfaces

2.9.1 SWD

NINA-B50 supports a single external Serial Wire Debug (SWD) interface for debugging and testing. The SWD interface consists of two pins: the clock pin, **SWDCLK**, and the single bi-directional data pin, **SWDIO**.

2.9.2 DAP

NINA-B50 supports a Debug Access Port (DAP) to debug and trace the core system of the module. DAP is a standard Arm CoreSight component. The DAP allows real-time access to the module registers from an external debugger without halting the processor cores. The DAP provides multiple, Main node, driving ports. All ports are accessible and controlled through a single external interface port to provide system-wide debug. On NINA-B50, the SWD interface is used as the external connection interface of DAP.

2.9.3 SWO

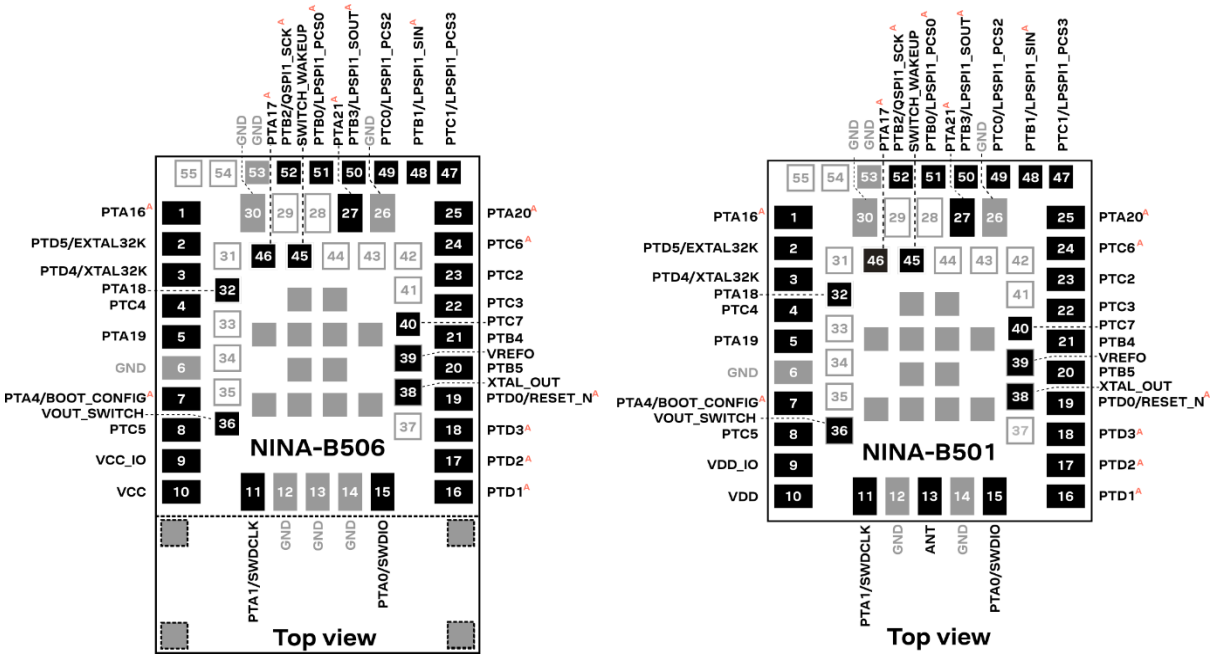
NINA-B50 supports a 1-bit Serial Wire Output (SWO) trace port for efficiently accessing core trace information from outside of the module. The SWO pin is used to stream-out trace information from various parts of the module, including the Data Watchpoint and Trace (DWT) part, Instrumentation Trace Macrocell (ITM) part, and Breakpoint Unit (BPU) part.

3 Pin definition

3.1 NINA-B50 series pin assignment

Figure 4 shows a typical pin-out assignment for NINA-B50 in an unconfigured state, where:

- The gray pins shown in the center of module are GND pins
- The four gray pins in the antenna area are GND pins
- The antenna area in NINA-B506 is shown as a dotted line at the bottom of the module
- NINA-B501 has the same pinout as NINA-B506 – except in the antenna area.
- NINA-B501 has smaller physical size than NINA-B506
- Many digital or analog signals shown here and described in this data sheet may be multiplexed onto a single pin. To view the signal multiplexing pins and gain a clearer understanding of which signals can be used on each pin, see Table 5.



A = Analog function capable pin

Figure 4: NINA-B50 pin assignments – top view showing NINA-B506 (left) and NINA-B501 (right)

The pinout for NINA-B50 is shown in Table 4.

No.	Name	I/O	Description	MCX W71 / K32W1480 pin	Remarks
1	PTA16	I/O	General purpose I/O	PTA16	
2	PTD5/EXTAL32K	I/O	Connection for optional 32.768 kHz crystal May be used as general purpose I/O	PTD5	
3	PTD4/XTAL32K	I/O	Connection for optional 32.768 kHz crystal May be used as general purpose I/O	PTD4	
4	PTC4	I/O	General purpose I/O	PTC4	
5	PTA19	I/O	General purpose I/O	PTA19	
6	GND	-	Ground		
7	PTA4/BOOT_CONFIG	I/O	General purpose I/O	PTA4	Can be used as BOOT_CONFIG signal
8	PTC5	I/O	General purpose I/O	PTC5	
9	VCC_IO	I	Module DCDC, I/O and system input supply	VDD_IO_D/VDD_DCDC VDD_IO_ABC VDD_ANA	Must be connected to either VCC or VOUT_SWITCH on NINA-B50
10	VCC	I	Module power switch input supply	VDD_SWITCH	1.71-3.6 V range
11	PTA1/SWDCLK	I	Serial Wire Debug port clock signal	PTA1	
12	GND	-	Ground	VSS	
13	ANT/GND	I/O	Tx/Rx antenna interface for NINA-B501 GND for NINA-B506	ANT_2P4 GHZ	50 Ω nominal characteristic impedance, only used with NINA-B501 modules
14	GND	-	Ground	VSS	
15	PTA0/SWDIO	I/O	Serial Wire Debug port data signal	PTA0	
16	PTD1	I/O	General purpose I/O	PTD1	Pin is analog capable
17	PTD2	I/O	General purpose I/O	PTD2	Pin is analog capable
18	PTD3	I/O	General purpose I/O	PTD3	Pin is analog capable
19	PTD0/RESET_N	I/O	System reset input	PTD0/ RESET_b	Active low
20	PTB5	I/O	General purpose I/O	PTB5	
21	PTB4	I/O	General purpose I/O	PTB4	
22	PTC3	I/O	General purpose I/O	PTC3	
23	PTC2	I/O	General purpose I/O	PTC2	
24	PTC6	I/O	General purpose I/O	PTC6	Pin is analog capable
25	PTA20	I/O	General purpose I/O	PTA20	Pin is analog capable
26	GND	-	Ground	VSS	

No.	Name	I/O	Description	MCX W71 / K32W1480 pin	Remarks
27	PTA21	I/O	General purpose I/O	PTA21	Pin is analog capable
28	RSVD	-	RESERVED pin		Leave unconnected
29	RSVD	-	RESERVED pin		Leave unconnected
30	GND	-	Ground	VSS	
31	RSVD	-	RESERVED pin		Leave unconnected
32	PTA18	I/O	General purpose I/O	PTA18	
33	RSVD	-	RESERVED pin		Leave unconnected
34	RSVD	-	RESERVED pin		Leave unconnected
35	RSVD	-	RESERVED pin		Leave unconnected
36	VOUT_SWITCH	O	Power switch output	VOUT_SWITCH	Power switch output 1.71-3.6 V range
37	RSVD	-	RESERVED pin		Leave unconnected
38	XTAL_OUT	O	XO analog oscillator clock output	XTAL_OUT	XO analog oscillator clock output
39	VREFO	O	Voltage reference output	VREFO	Voltage reference output 1.0-2.1 V range, in 0.1 V step
40	PTC7	I/O	General purpose I/O	PTC7	
41	RSVD	-	RESERVED pin		Leave unconnected
42	RSVD	-	RESERVED pin		Leave unconnected
43	RSVD	-	RESERVED pin		Leave unconnected
44	RSVD	-	RESERVED pin		Leave unconnected
45	SWITCH_WAKEUP	I	Power switch wake up pin	SWITCH_WAKEUP_B	Active low
46	PTA17	-	General purpose I/O	PTA17	
47	PTC1/LPSPI1_PCS3	I/O	General purpose I/O	PTC1	Recommended pin for QSPI_D3
48	PTB1/LPSPI1_SIN	I/O	General purpose I/O	PTB1	Recommended pin for QSPI_D1
49	PTC0/LPSPI1_PCS2	I/O	General purpose I/O	PTC0	Recommended pin for QSPI_D2
50	PTB3/LPSPI1_SOUT	I/O	General purpose I/O	PTB3	Recommended pin for QSPI_D0
51	PTB0/LPSPI1_PCS0	I/O	General purpose I/O	PTB0	Recommended pin for QSPI_CS

No.	Name	I/O	Description	MCX W71 / K32W1480 pin	Remarks
52	PTB2/QSPI1_SCK	I/O	General purpose I/O	PTB2	Recommended pin for QSPI_CLK
53	GND	-	Ground	VSS	
54	RSVD	-	RESERVED pin		Leave unconnected
55	RSVD	-	RESERVED pin		Leave unconnected
	EGP	-	Exposed Ground Pins	VSS	The exposed pins in the center of the module should be connected to GND
	EAGP	-	Exposed Antenna Ground Pins	VSS	Only on NINA-B506. The exposed pins underneath the antenna area should be connected to GND

Table 4: NINA-B50 series pinout

The signal multiplexing pins on NINA-50 are shown in Table 5.

Pin	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	WAKE UP
PTA0		PTA0	CMP0_OUT	LPUART0_CTS_B	RF_GPO_11	TPM0_CH4	FLEXIO0_D0	SWDIO					WUU0_P0
PTA1		PTA1	CMP1_OUT	LPUART0_RTS_b	RF_GPO_10	TPM0_CH5	FLEXIO0_D1	SWD_CLK					
PTA4	ADC0_A10/ CMP0_IN0	PTA4		RF_GPO_9	TPM0_CLKIN	TRACE DATA_SWO	FLEXIO0_D4	BOOT_CONFIG					WUU0_P2/ RF_XTAL_OUT_ ENABLE
PTA16	ADC0_A12	PTA16	LPSPI0_PCS0	EWM0_OUT_b	LPI2C0_SCLS	TPM0_CH4	LPUART0_ RX	RF_GPO_8		FLEXIO0_D5			RF_NOT_ALLOWED
PTA17	ADC0_A13	PTA17	LPSPI0_SIN	EWM0_IN	LPI2C0_SDAS	TPM0_CH5	LPUART0_ TX	RF_GPO_7	RF_GPO_8	FLEXIO0_D6		EXT_XTAL_REQUEST/RF_GPO_7	WUU0_P3/RF_ NOT_ALLOWED
PTA18	CMP1_IN1	PTA18	LPSPI0_SOUT	LPUART0_CTS_b	LPI2C0_SDA	TPM0_CH3	RF_GPO_0				LPUART0_RX	SPC0_LPREQ	
PTA19	CMP1_IN0	PTA19	LPSPI0_SCK	LPUART0_RTS_b	LPI2C0_SCL	TPM0_CH2	RF_GPO_1						WUU0_P4
PTA20	ADC0_A14/ CMP0_IN3	PTA20	LPSPI0_PCS2	LPUART0_TX	EWM0_IN	TPM0_CH1	RF_GPO_2		FLEXIO0_D7				
PTA21	ADC0_A15/ CMP0_IN2	PTA21	LPSPI0_PCS3	LPUART0_RX	EWM0_OUT_b	TPM0_CH0	RF_GPO_3	RF_GPO_7	FLEXIO0_D8	RF_GPO_10			WUU0_P5
PTB0	ADC0_B10	PTB0	LPSPI1_PCS0			TPM1_CH0				FLEXIO0_D26			WUU0_P13
PTB1	ADC0_B11	PTB1	LPSPI1_SIN			TPM1_CH1				FLEXIO0_D27			
PTB2	ADC0_B12	PTB2	LPSPI1_SCK	LPUART1_TX		TPM1_CH2				FLEXIO0_D28			
PTB3	ADC0_B13	PTB3	LPSPI1_SOUT	LPUART1_RX		TPM1_CH3				FLEXIO0_D29			WUU0_P14
PTB4		PTB4	LPSPI1_PCS3	LPUART1_CTS_b	LPI2C1_SDA	I3C0_SDA	TRGMUX0_ IN0			FLEXIO0_D30			WUU0_P15

Pin	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	WAKE UP
PTB5		PTB5	LPSPI1_PCS2	LPUART1_RTS_b	LPI2C1_SCL	I3C0_SCL	TRGMUX0_OUT0			FLEXIO0_D31			
PTC0		PTC0	LPSPI1_PCS2	CAN0_TX[1]	I3C0_SDA	TPM1_CH0		LPI2C1_SCL		FLEXIO0_D16			WUU0_P7
PTC1		PTC1	LPSPI1_PCS3	CAN0_RX[1]	I3C0_SCL	TPM1_CH1		LPI2C1_SDA		FLEXIO0_D17			WUU0_P8
PTC2		PTC2	LPSPI1_SOUT	LPUART1_RX	LPI2C1_SCLS	TPM1_CH2		I3C0_RUR		FLEXIO0_D18			WUU0_P9
PTC3		PTC3	LPSPI1_SCK	LPUART1_TX	LPI2C1_SDAS	TPM1_CH3				FLEXIO0_D19			
PTC4		PTC4	LPSPI1_SIN	CAN0_TX[1]	LPI2C1_SCL		TPM2_CH0			FLEXIO0_D20			WUU0_P10
PTC5		PTC5	LPSPI1_PCS0	CAN0_RX[1]	LPI2C1_SDA	TPM1_CH4	TPM2_CH1			FLEXIO0_D21			
PTC6	ADC0_A8	PTC6	LPSPI1_PCS1			TPM1_CH5				FLEXIO0_D22			WUU0_P11[2]
PTC7	DISABLED	PTC7	TRGMUX0_IN3	TRGMUX0_OUT3	SFA0_CLK	TPM1_CLKIN	TPM2_CLKIN	CLKOUT		FLEXIO0_D23			WUU0_P12/NMI_b/RF_NOT_ALLOWED
PTD0	ADC0_A5	PTD0		RESET_b									
PTD1	ADC0_B5	PTD1	SPC0_LPREQ	NMI_b	RF_GPO_4								
PTD2	ADC0_A6	PTD2	LPTMR0_ALT3	TAMPER0	RF_GPO_5								
PTD3	ADC0_B6	PTD3	LPTMR1_ALT3	TAMPER1	RF_GPO_6		TRGMUX0_IN2						
PTD4	XTAL32K	PTD4	LPTMR0_ALT2	TAMPER2									
PTD5	EXTAL32K	PTD5	LPTMR1_ALT2										

Table 5: Signal multiplexing pins on NINA-50 series modules

[1] This signal is only available on the NINA-B501-10B or NINA-B506-10B modules.
[2] PTC6_WUU0_P11 pin signal available only as a wake-up source for FlexCAN module on signal CAN0_RX from pin PTC5. In this case, other configuration on PTC6 shall not be used.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute maximum ratings can cause permanent damage. These are stress ratings only.

Operating the module in conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is advisory and not part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.3	3.63	V
VCC_IO	Digital pin voltage	Input DC voltage at any digital I/O pin, VCC_IO ≤ 3.6 V	–0.3	VCC + 0.3	V
		Input DC voltage at any digital I/O pin, VCC > 3.6 V	–0.3	3.63	V
RFinMax	Maximum power at receiver	Input RF power at antenna pin		+10	dBm

Table 6: Absolute maximum ratings

⚠ The module is not protected against overvoltage or reversed voltages. Always use suitable protection devices to prevent voltage spikes that can potentially exceed the power boundary values shown in Table 6.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except ANT pin			2	kV	Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
ESD sensitivity for all pins except ANT pin			500	V	Charged device model according to JESD22-C101
ESD indirect contact discharge			±8*	kV	According to EN 301 489-1

*Tested on EVK-NINA-B5 evaluation board

Table 7: Maximum ESD ratings

⚠ NINA-B50 series modules are Electrostatic Sensitive Device that require special precautions while handling. See also ESD precautions for ESD handling instructions.

4.2 Operating conditions

☞ Unless otherwise specified, all given operating condition specifications are based on an ambient temperature of 25 °C with a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended. Any extended exposure outside these specific limits can affect the device reliability.

4.2.1 Operating temperature range

Parameter	Min	Max	Unit
Storage temperature	-40	+85	°C
Operating temperature	-40	+85	°C

Table 8: Temperature range

4.2.2 Supply/Power pins

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input supply voltage	1.71	-	3.60	V
t_RVCC	Supply voltage rise time			12	ms
VCC_IO	I/O reference voltage	1.71	-	3.60	V

Table 9: Input characteristics of voltage supply pins

☞ Less than 3 V voltage level of **VCC** and **VCC_IO** has negative impact on Tx output power.

4.3 Current consumption

Table 10 shows the typical current consumption of NINA-B50 modules with 3.3 V external voltage supply at 25 °C.

Mode	Condition	Typical	Unit
Deep power down	Power switch output VOUT_SWITCH connects to VCC_IO. All regulators off, 8KB RAM retained, no radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO16K enabled.	0.4	µA
Deep power down	External 3.3 V connects to VCC and VCC_IO. LDO_CORE and DCDC off, LDO_SYS in low power, no RAM retained, no radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO32K enabled	1.2	µA
Power down	External 3.3 V connects to VCC and VCC_IO. All regulators in low power, 16KB of RAM retained, all radio RAM retained, all peripherals, NBU, and EdgeLock disabled, FRO32K enabled	3.4	µA
Deep sleep	External 3.3 V connects to VCC and VCC_IO. All regulators in low power, 16 KB of RAM retained, all radio RAM retained, all peripherals, NBU, and Edge Lock disabled, external 32.768 kHz crystal is enabled.	2.5	µA
Deep sleep	External 3.3 V connects to VCC and VCC_IO. All regulators in low power, all RAM retained, all peripherals, NBU, and Edge Lock disabled, external 32.768 kHz crystal is enabled.	2.8	µA

Mode	Condition	Typical	Unit
CoreMark	External 3.3 V connects to VCC and VCC_IO. DCDC in low strength, Core voltage = 1.0V, all peripherals disabled, executing CoreMark® code from FLASH in CM33 at 48MHz, NBU in sleep mode.	4.6	mA
CoreMark	External 3.3 V connects to VCC and VCC_IO. DCDC in normal strength, Core voltage = 1.1V, all peripherals disabled, executing CoreMark® code from FLASH in CM33 at 96MHz, NBU in sleep mode.	6.2	mA
Active	Radio RX ON for BLE VDD_RF = VDD_LDO_CORE = 1.25 V	4.68	mA
Active	Radio RX On for IEEE 802.15.4 VDD_RF = VDD_LDO_CORE = 1.25 V	3.69	mA
Active	Radio TX ON with 0 dBm output power for BLE VDD_RF = VDD_LDO_CORE = 1.25 V NBU running at @16 MHz.	4.60	mA
Active	Radio TX ON with +7 dBm output power for BLE VDD_RF = VDD_LDO_CORE = 1.8 V NBU running at @16 MHz.	10.79	mA
Active	Radio TX ON with +10 dBm output power for BLE VDD_RF = VDD_LDO_CORE = 2.4 V NBU running at @16 MHz.	18.71	mA
Active	Radio TX ON with 0 dBm output power for IEEE 802.15.4 VDD_RF = VDD_LDO_CORE = 1.25 V NBU running at @16 MHz.	3.75	mA
Active	Radio TX ON with +10 dBm output power for IEEE 802.15.4 VDD_RF = VDD_LDO_CORE = 2.4 V NBU running at @16 MHz.	17.10	mA

Table 10: Module VCC current consumption with 3.3 V external voltage supply at 25 °C

4.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
	Bluetooth Low Energy mode				
Receiver sensitivity*	1 Mbit/s data rate		-97		dBm
	2 Mbit/s data rate		-94		dBm
	500 kbit/s data rate		-101		dBm
	125 kbit/s data rate		-105		dBm
Maximum output power** (2.9 ≤ VCC = VCC_IO ≤ 3.6)	1 Mbit/s, 2 Mbit/s, 500 kbit/s, 125 kbit/s		+10		dBm
Maximum output power** (1.71 ≤ VCC = VCC_IO ≤ 1.8 V)	1 Mbit/s, 2 Mbit/s, 500 kbit/s, 125 kbit/s		+7		dBm
	IEEE 802.15.4 mode				
Receiver sensitivity*	250 kbit/s data rate		-103		dBm
Maximum output power** (2.9 ≤ VCC = VCC_IO ≤ 3.6)	250 kbit/s data rate		+10		dBm
Maximum output power** (1.71 ≤ VCC = VCC_IO ≤ 1.8 V)	250 kbit/s data rate		+7		dBm

Parameter	Test condition	Min	Typ	Max	Unit
		Antenna			
Peak gain	PCB antenna integrated on NINA-B506 modules		+3		dBi
Peak gain	External antenna		+3		dBi

*Conducted test on EVK-NINA-B501 evaluation board with 3.3 V supply voltage at 25 °C.
** Depends on supply voltage

Table 11: RF performance

4.5 Antenna radiation patterns

Figure 5 provides an overview of the measurement procedure and describes how the NINA-B506 module is aligned to the XYZ-coordinate system.

Measurements are taken at every dotted position above the module image (shown left). Each measurement is represented as a grid point in the radiation pattern (shown right).

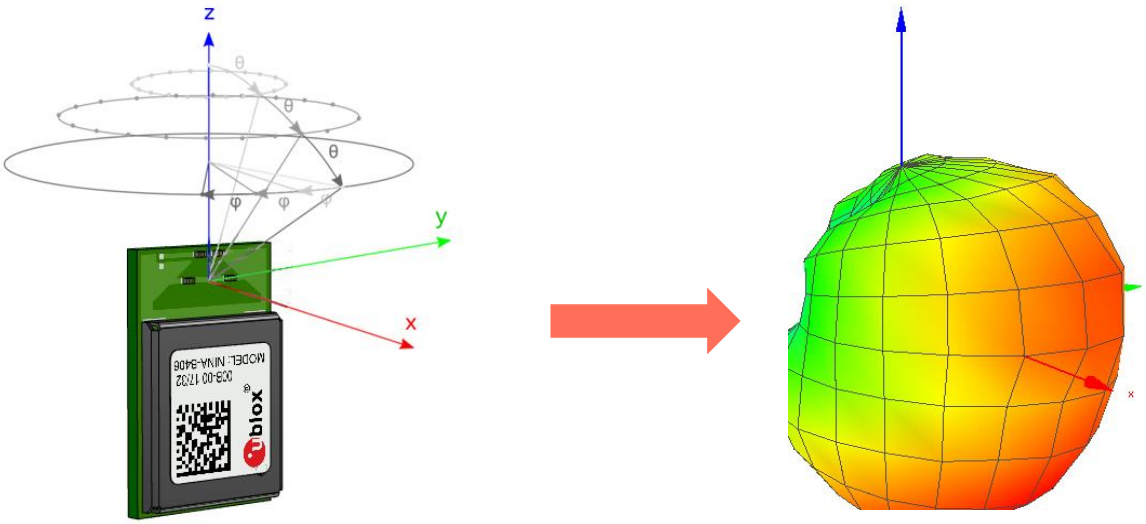
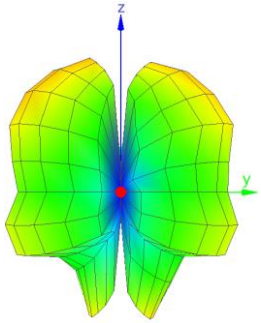
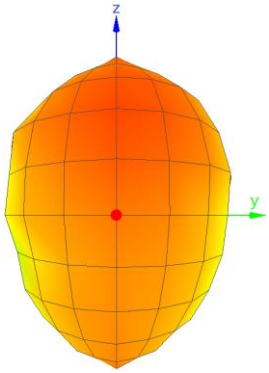
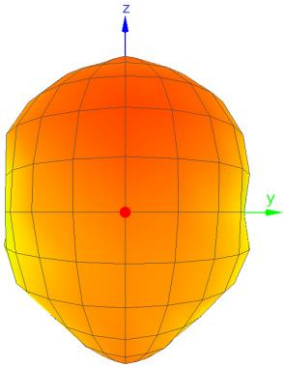
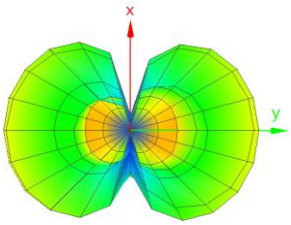
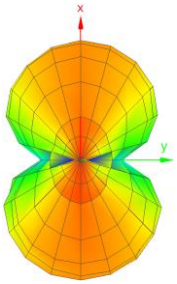
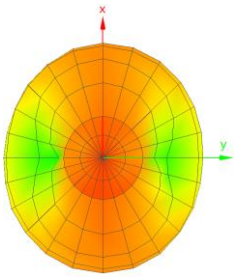
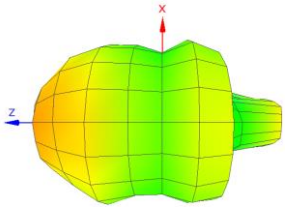
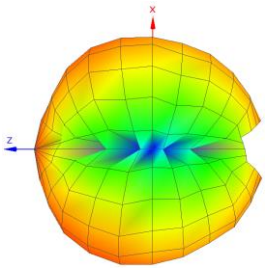
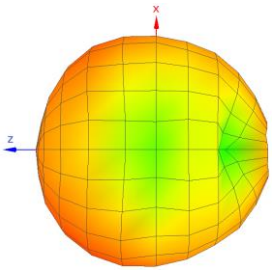
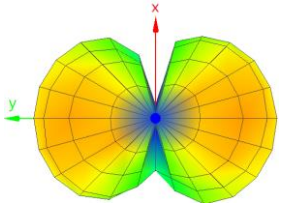
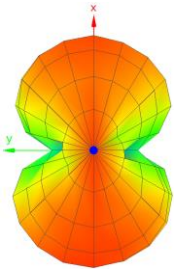
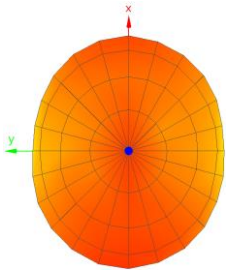


Figure 5: Measurement procedure for determining radiation patterns

Table 12 shows the radiation patterns of the NINA-B506 module with internal antenna.

View	Vertical polarization	Horizontal polarization	otal (Vertical + Horizontal)
	Antenna Gain (dBi) -25 -20 -15 -10 -5 0 5		
Top view, YZ plane positive X direction 			
Side view, XY plane negative Z direction 			
Side view, XZ plane negative Y direction 			
Side view, XY plane positive Z direction 			

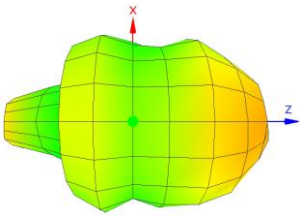
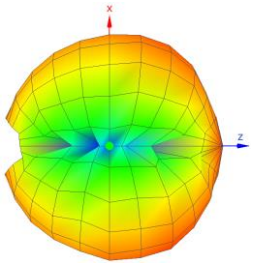
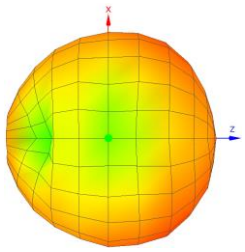
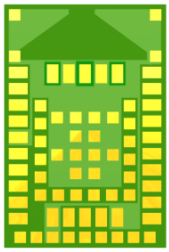
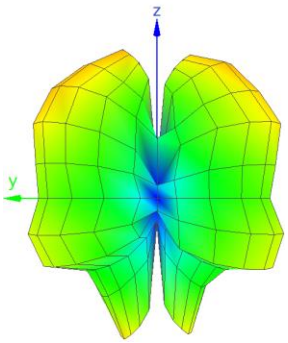
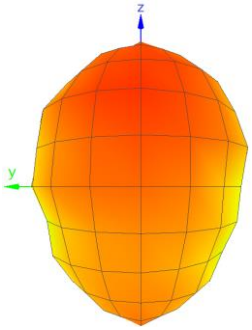
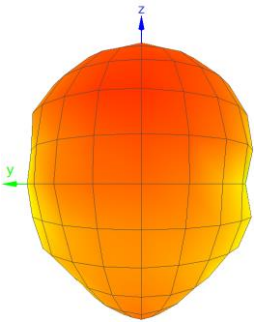
View	Vertical polarization	Horizontal polarization	otal (Vertical + Horizontal)
Side view, XZ plane positive Y direction 			
Bottom view, YZ plane negative X direction 			

Table 12: NINA-B506 antenna radiation patterns

4.6 32 kHz FRO

Table 13 summarizes the specifications of the 32 kHz free running oscillator (FRO).

Symbol	Description	Min	Typ	Max	Unit
f_32KFRO	32 kHz FRO frequency	-	32.768	-	kHz
Δ f_32KFRO	Frequency deviation (open loop)	-	-	±2	%
TRIMstep	Trimming step	-	0.03	-	%
t_startup	Start-up time	-	-	120	µs
f_os	Frequency overshoot during startup (trimmed)	-	10	-	%
I_32KFRO	Current consumption	-	350	-	nA

Table 13: 32 kHz FRO specifications

4.7 External 32 kHz crystal oscillator

Table 14 shows the reference specifications of the external optional 32 kHz crystal oscillator.

Symbol	Description	Min	Typ	Max	Unit
FNOM_LFXO	Crystal frequency	-	32.768	-	kHz
FTOL_LFXO	Frequency tolerance	-	±100	-	ppm
CL_LFXO	EXTAL32K, XTAL32K Load Capacitance[3]	0	-	30	pF

[3] NINA-B5 modules support internal load capacitance for 32 kHz crystal oscillators via an internal capacitance bank. The load capacitance value can be selected and configured via software configuration in 2 pF step. See also the System integration manual [2] for configuring the load capacitance for 32 kHz crystal oscillators.

Symbol	Description	Min	Typ	Max	Unit
C0_LFXO	Shunt Capacitance	-	-		pF
ESR	Equivalent series resistance	-	-	80	kΩ
Cpara	Parasitic capacitance of EXTAL32K and XTAL32K	-	-	2	pF
Fextal32K	Externally provided input clock frequency[4]	-	32.768	-	kHz
Vextal32K	Externally provided input clock voltage	VSS	-	VCC_IO	mV

Table 14: External 32 kHz crystal oscillator specifications

4.8 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit	Remarks
RESET_N	Low-level input	0		0.3* VCC_IO	V	
	High-level input	0.7*VCC_IO		VCC_IO	V	
	Internal pull-up resistance	0.67	1.5		kΩ	
	RESET duration	330			ns	Time taken to release a pin reset.

Table 15: RESET_N pin characteristics

[4] This specification is for an externally supplied clock driven to EXTAL32K and does not apply to any other clock input. The oscillator remains enabled and XTAL32K must be left unconnected.

4.9 Digital pins

Table 16 shows characteristics of all digital pins.

Parameter	Min	Typ	Max	Unit	Remarks
Input characteristic: Low-level input	0		0.3*VCC_IO	V	
Input characteristic: high-level input	0.7*VCC_IO		VCC_IO	V	
Output characteristic: Low-level output	0		0.5	V	Standard drive strength
	0		0.5	V	High drive strength
Output characteristic: High-level output	VCC_IO-0.5		VCC_IO	V	Standard drive strength
	VCC_IO-0.5		VCC_IO	V	High drive strength
Sink/Source current		2.5		mA	Standard drive strength, VCC_IO < 2.7 V
		4		mA	Standard drive strength, VCC_IO ≥ 2.7 V
		3.75		mA	High drive strength, VCC_IO < 2.7 V
		6		mA	High drive strength, VCC_IO ≥ 2.7 V
Rise/Fall time (Normal I/O pins)	2.9	–	15	ns	Standard drive strength with 25 pF load, depending on VCC_IO level
	2.4	–	20	ns	High drive strength with 25 pF load, depending on VCC_IO level
Rise/Fall time (I2C/I3C pins)	2.8	–	20	ns	Standard drive strength with 25 pF load, depending on VCC_IO level
	2.3	–	20	ns	High drive strength with 25 pF load, depending on VCC_IO level
Internal pull-up resistance	33	50	75	kΩ	Can be added to any GPIO pin configured as input
Internal pull-up resistance (I3C pins)	1.1	2	2.833	kΩ	Can be added to I3C pins only
High-resistance pull-up resistance	0.67	-	1.5	kΩ	Can be added to Port D pins only
Internal pull-down resistance	33	50	75	kΩ	Can be added to any GPIO pin configured as input
High-resistance pull-down resistance	0.67	-	1.5	kΩ	Can be added to Port D pins only
Input leakage current per pin at 25 °C	-	-	0.025*	µA	Measured at VCC_IO = 3.6 V
Input leakage current per pin for full temperature range	-	-	1*	µA	Measured at VCC_IO = 3.6 V

Table 16: Digital pin characteristics

4.10 Analog comparator

Symbol	Parameter	Min	Typ	Max	Unit
I_high-speed	Current consumption when the comparator is in 'high-speed' mode		200		µA
I_normal-speed	Current consumption when the comparator is in 'normal' mode		10		µA
I_nano-speed	Current consumption when the comparator is in 'Nano speed' mode		400		nA
t_high-speed, 100 mV overdrive	Propagation delay*, 100 mV overdrive, power > 1.71 V in high-speed mode		25		ns
t_high-speed, 30 mV overdrive	Propagation delay, 30 mV overdrive, power > 1.71 V in high-speed mode		50		ns
t_normal-speed	Propagation delay, 30 mV overdrive, power > 1.71 V in normal-speed mode		600		ns
t_nano-speed	Propagation delay, 30 mV overdrive, power > 1.71 V in nano-speed mode		5		µs
t_initialization	Time between software writes to change control inputs and the comparator output settling to a stable level		40		µs

* Propagation delays are measured from the 50 % rise time point to the 50 % fall time point.

Table 17: Electrical specification of the analog comparator

5 Mechanical specifications

5.1 NINA-B501 mechanical specification

Figure 6 shows the mechanical outline of NINA-B501 modules.

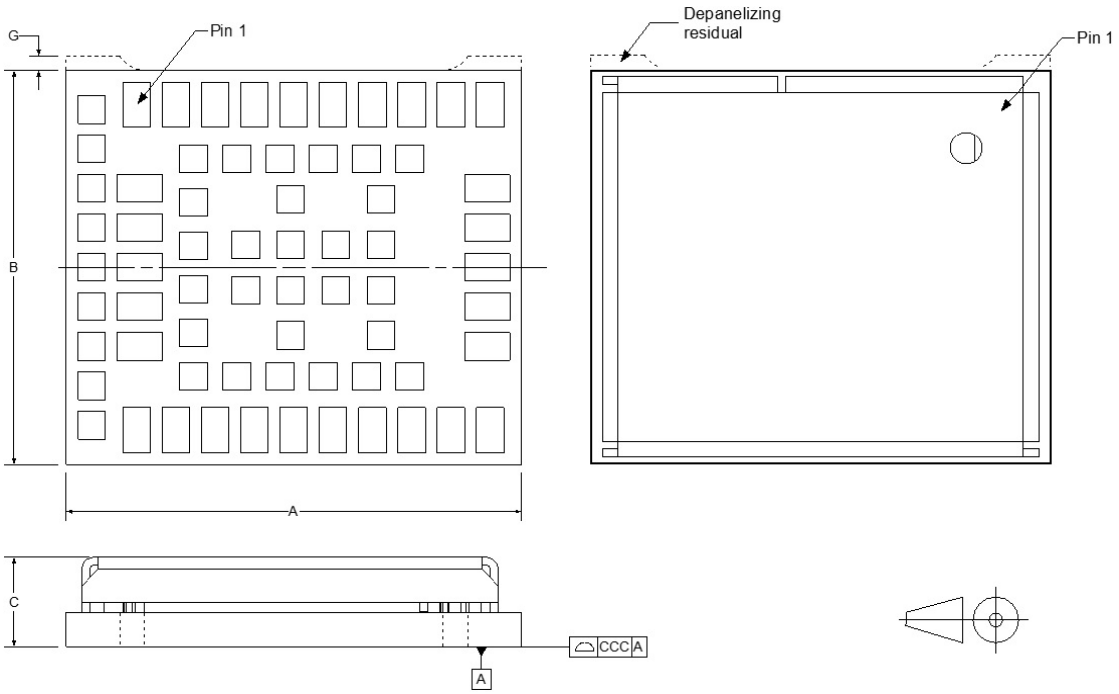


Figure 6: NINA-B501 mechanical outline

Figure 7 shows the detailed dimensions of NINA-B501 modules.

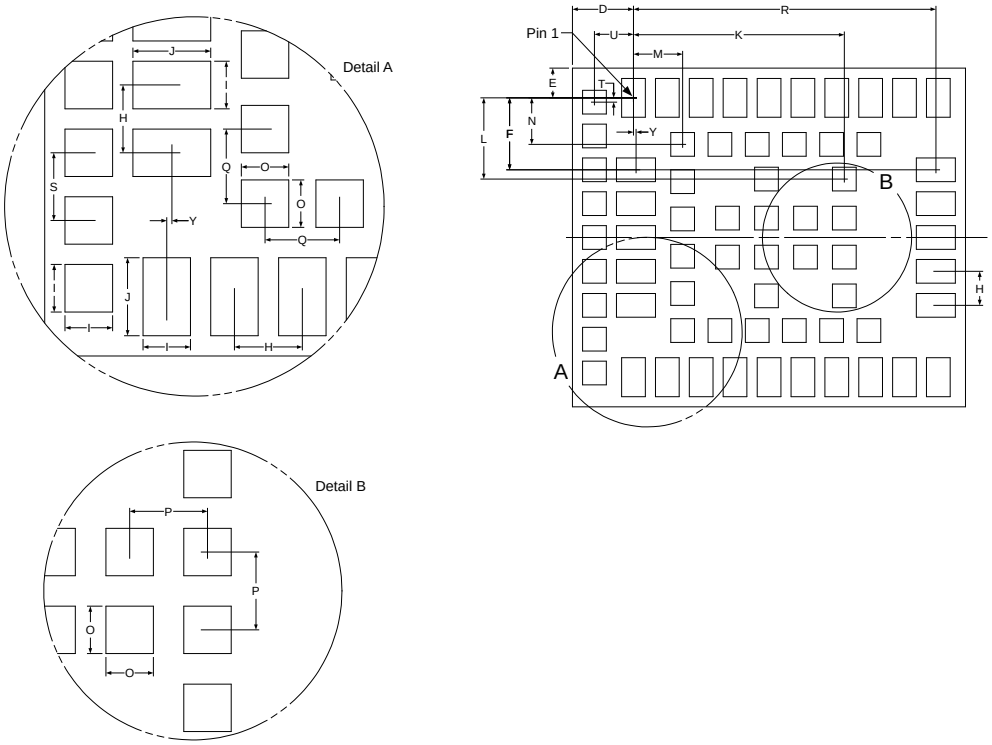


Figure 7: NINA-B50 detailed dimensions

Table 18 describes the mechanical outline data of NINA-B501 modules.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	11.6	456.7	+0.20/-0.10	+7.9/-3.9
B	Module PCB width	10.0	393.7	+0.20/-0.10	+7.9/-3.9
C	Module thickness	2.38	93.7	+0.40/-0.20	+15.8/-7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/-0.10	+0.8/-3.9
D	Horizontal edge to pin no. 1 center	1.80	70.9	+/-0.10	+/-3.9
E	Vertical edge to pin no. 1 center	0.875	34.4	+/-0.10	+/-3.9
F	Vertical pin no. 1 center to lateral pin center	2.125	83.7	+/-0.05	+/-2.0
G	Depanelizing residual	0.10	3.9	+0.25/-0.1	+9.8/-3.9
H	Lateral and antenna row pin to pin pitch	1.00	39.4	+/-0.05	+/-2.0
I	Lateral, antenna row and outer pin width	0.70	27.6	+/-0.05	+/-2.0
J	Lateral and antenna row pin length	1.15	45.3	+/-0.05	+/-2.0
K	Horizontal pin no. 1 center to central pin center	6.225	245.1	+/-0.05	+/-2.0
L	Vertical pin no. 1 center to central pin center	2.40	94.5	+/-0.05	+/-2.0
M	Horizontal pin no. 1 center to inner row pin center	1.45	57.1	+/-0.05	+/-2.0
N	Vertical pin no. 1 center to inner row pin center	1.375	54.1	+/-0.05	+/-2.0
O	Central, inner and outer row pin width and length	0.70	27.6	+/-0.05	+/-2.0
P	Central pin to central pin pitch	1.15	45.3	+/-0.05	+/-2.0
Q	Inner row pin to pin pitch	1.10	43.3	+/-0.05	+/-2.0
R	Horizontal pin no. 1 center to antenna row pin center	8.925	351.4	+/-0.05	+/-2.0
S	Outer row pin to pin pitch	1.00	39.4	+/-0.05	+/-2.0
T	Vertical pin no. 1 center to outer row pin center	0.125	4.9	+/-0.05	+/-2.0
U	Horizontal pin no. 1 center to outer row pin center	1.15	45.3	+/-0.05	+/-2.0
Y	Horizontal pin no. 1 center to lateral pin center	0.075	3.0	+/-0.05	+/-2.0
	Module weight [g]	<1.0			

Table 18: NINA-B501 mechanical outline data

5.2 NINA-B506 mechanical specification

Figure 8 shows the mechanical outline of NINA-B506 modules.

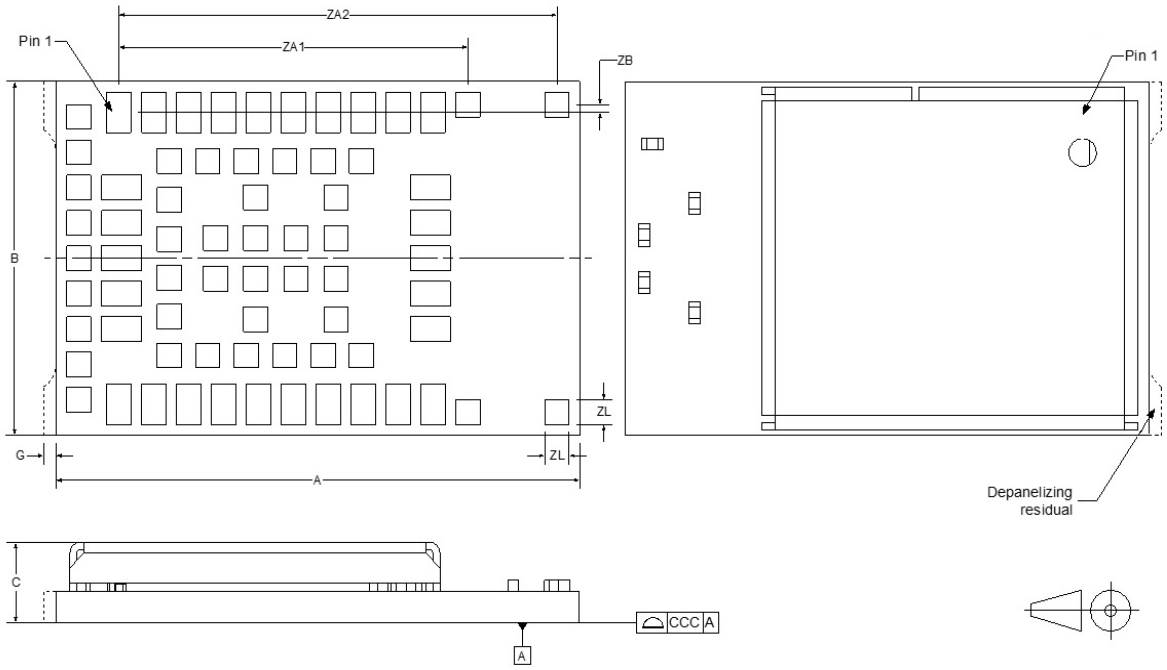


Figure 8 : NINA-B506 mechanical outline

Figure 9 shows the detailed dimensions of NINA-B506 modules.

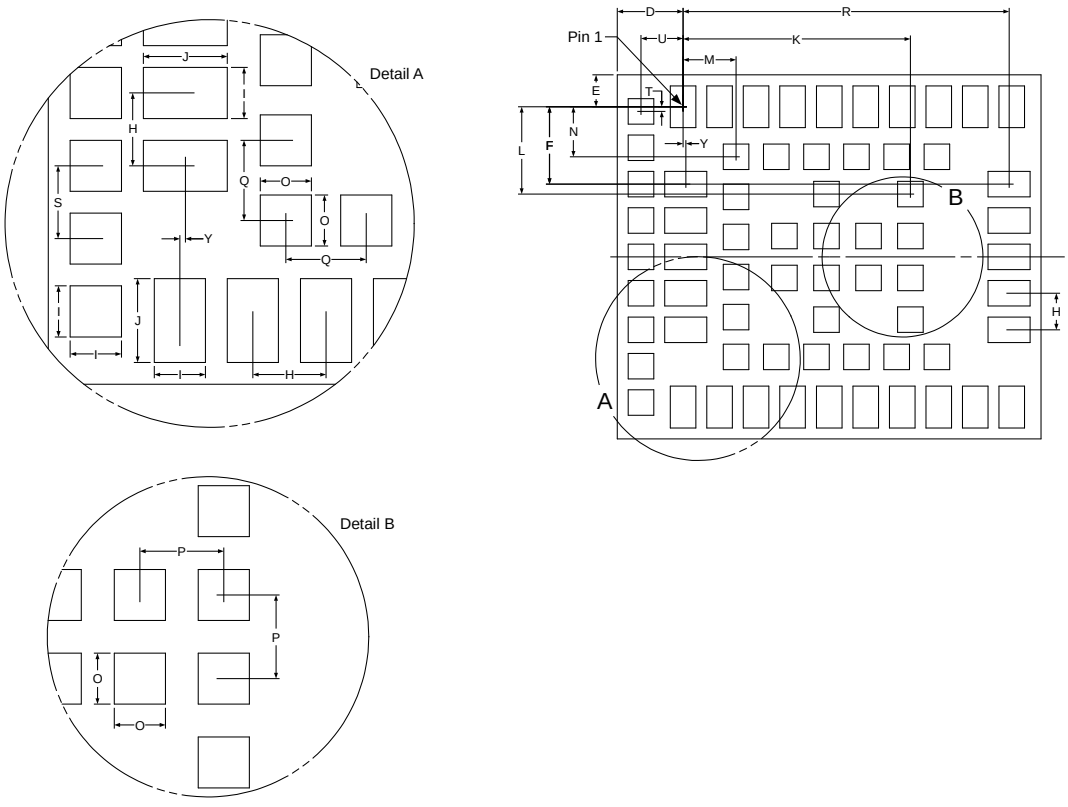


Figure 9: NINA-B506 detailed dimensions

Table 19 describes the mechanical outline data of NINA-B506 modules.

Parameter	Description	Typical [mm]	[mil]	Tolerance [mm]	[mil]
A	Module PCB length	15.0	590.6	+0.20/-0.10	+7.9/-3.9
B	Module PCB width	10.0	393.7	+0.20/-0.10	+7.9/-3.9
C	Module thickness	2.38	93.7	+0.40/-0.20	+15.8/-7.9
ccc	Seating plane coplanarity	0.10	3.9	+0.02/-0.10	+0.8/-3.9
D	Horizontal edge to pin no. 1 center	1.80	70.9	+/-0.10	+/-3.9
E	Vertical edge to pin no. 1 center	0.875	34.4	+/-0.10	+/-3.9
F	Vertical pin no. 1 center to lateral pin center	2.125	83.7	+/-0.05	+/-2.0
G	Depanelizing residual	0.10	3.9	+0.25/-0.1	+9.8/-3.9
H	Lateral and antenna row pin to pin pitch	1.00	39.4	+/-0.05	+/-2.0
I	Lateral, antenna row and outer pin width	0.70	27.6	+/-0.05	+/-2.0
J	Lateral and antenna row pin length	1.15	45.3	+/-0.05	+/-2.0
K	Horizontal pin no. 1 center to central pin center	6.225	245.1	+/-0.05	+/-2.0
L	Vertical pin no. 1 center to central pin center	2.40	94.5	+/-0.05	+/-2.0
M	Horizontal pin no. 1 center to inner row pin center	1.45	57.1	+/-0.05	+/-2.0
N	Vertical pin no. 1 center to inner row pin center	1.375	54.1	+/-0.05	+/-2.0
O	Central, inner and outer row pin width and length	0.70	27.6	+/-0.05	+/-2.0
P	Central pin to central pin pitch	1.15	45.3	+/-0.05	+/-2.0
Q	Inner row pin to pin pitch	1.10	43.3	+/-0.05	+/-2.0
R	Horizontal pin no. 1 center to antenna row pin	8.925	351.4	+/-0.05	+/-2.0
S	Outer row pin to pin pitch	1.00	39.4	+/-0.05	+/-2.0
T	Vertical pin no. 1 center to outer row pin center	0.125	4.9	+/-0.05	+/-2.0
U	Horizontal pin no. 1 center to outer row pin center	1.15	45.3	+/-0.05	+/-2.0
Y	Horizontal pin no. 1 center to lateral pin center	0.075	3.0	+/-0.05	+/-2.0
ZA1	Horizontal pin no. 1 center to first set of antenna GND pins pin center	10.0	393.7	+/-0.05	+/-2.0
ZA2	Horizontal pin no. 1 center to second set of antenna GND pins pin center	12.55	494.1	+/-0.05	+/-2.0
ZB	Vertical pin no.1 center to antenna GND pin center	0.225	8.9	+/-0.05	+/-2.0
ZL	Antenna GND pin width and length	0.70	27.6	+/-0.05	+/-2.0
	Module weight [g]	<1.0			

Table 19: NINA-B506 mechanical outline data

6 Qualifications and approvals

6.1 Compliance with the RoHS directive

NINA-B50 modules comply with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

6.2 Country approvals

NINA-B50 series modules are certified for use in the following countries/regions:

Country/region	NINA-B501	NINA-B506
Europe	Approved	Approved
USA	Approved	Approved
Canada	Approved	Approved
Great Britain	Approved	Approved
Japan	Pending	Pending
Taiwan	Approved	Approved
South Korea	Approved	Approved
Australia	Approved	Approved
New Zealand	Approved	Approved

See the NINA-B50 series system integration manual [2] for detailed information about the regulatory requirements that must be met when using NINA-B50 modules in an end product.

6.3 Bluetooth qualification

The NINA-B50 module series is a Bluetooth qualified design, listed in accordance with the Bluetooth 5.3 specification.

All products that use Bluetooth technology must be qualified with the Bluetooth Special Interest Group (SIG) to obtain its own declaration ID. This is applicable also for products that are using an already Bluetooth qualified module.

The Bluetooth Qualification Process is initiated at the Bluetooth SIG Launch Studio website. When submitting the qualification, use the “Qualification without required testing” path, and combine the QDID for the Host Subsystem (the Bluetooth stack) with the QDID of the Controller Subsystem, as shown in Table 20.

Product type	QDID
Controller Subsystem	184881
Host Subsystem	186187

Table 20: NINA-B50 series Bluetooth qualified design ID

7 Product handling

7.1 Packaging

NINA-B50 modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see also the Packaging reference guide [1].

7.1.1 Reels

NINA-B50 series modules are deliverable in quantities of 500 pieces on a reel. The reel types for each module variant are described in Table 21. For more information about the reel types, see also the Packaging reference guide [1].

Model	Reel type
NINA-B501	B1
NINA-B506	A3

Table 21: Reel types

7.1.2 Tapes

Figure 10 shows the position and orientation of NINA-B50 modules as they are delivered on tape.

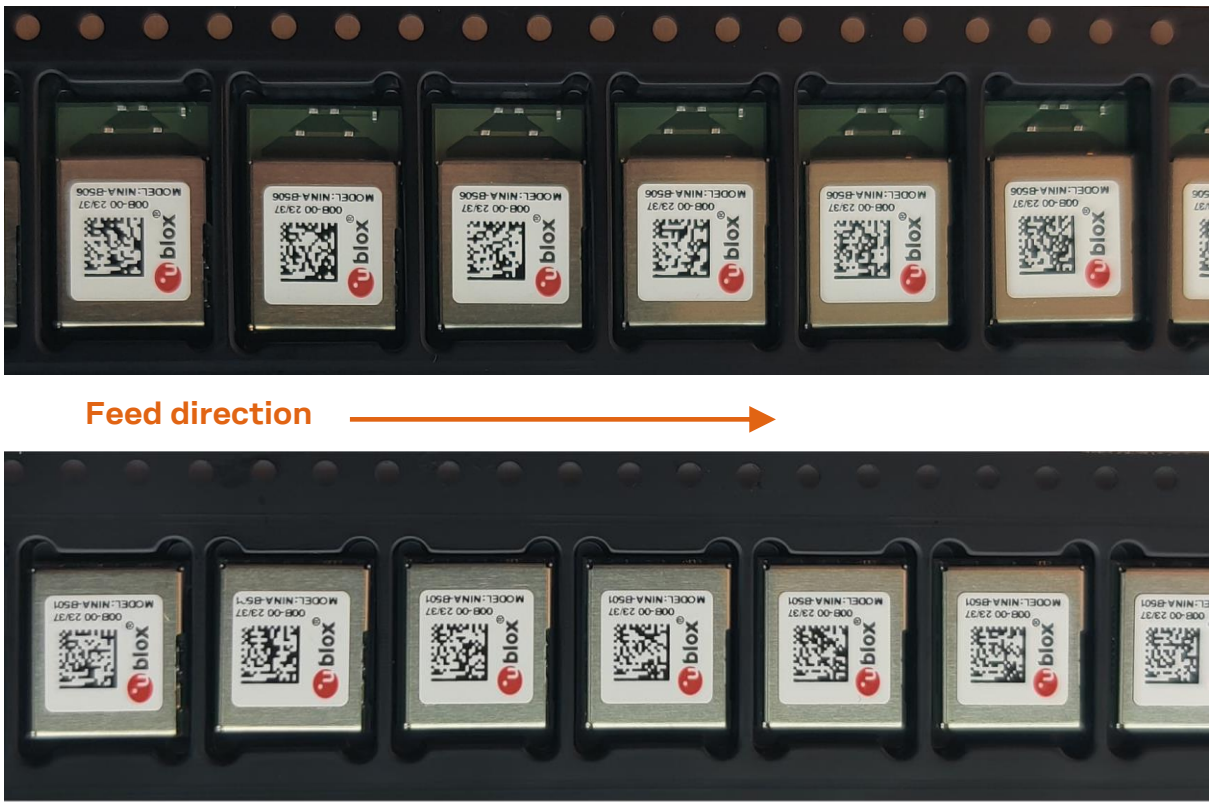
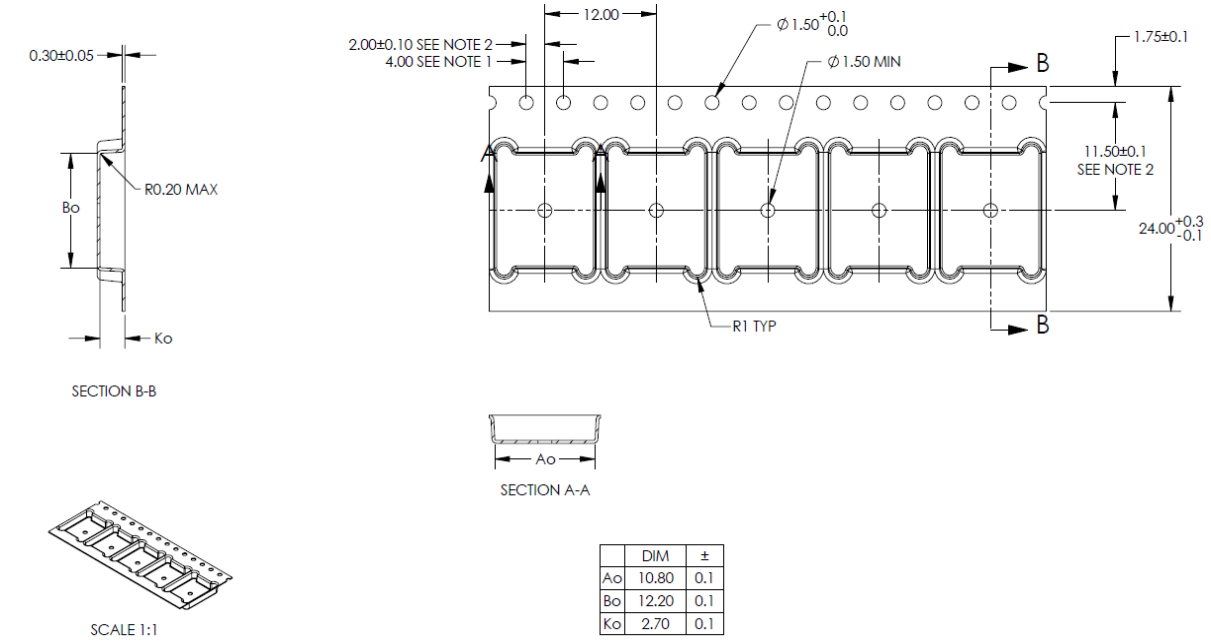


Figure 10: Orientation of NINA-B50 modules on tape

The tape dimensions for NINA-B501 modules are shown in Figure 11.

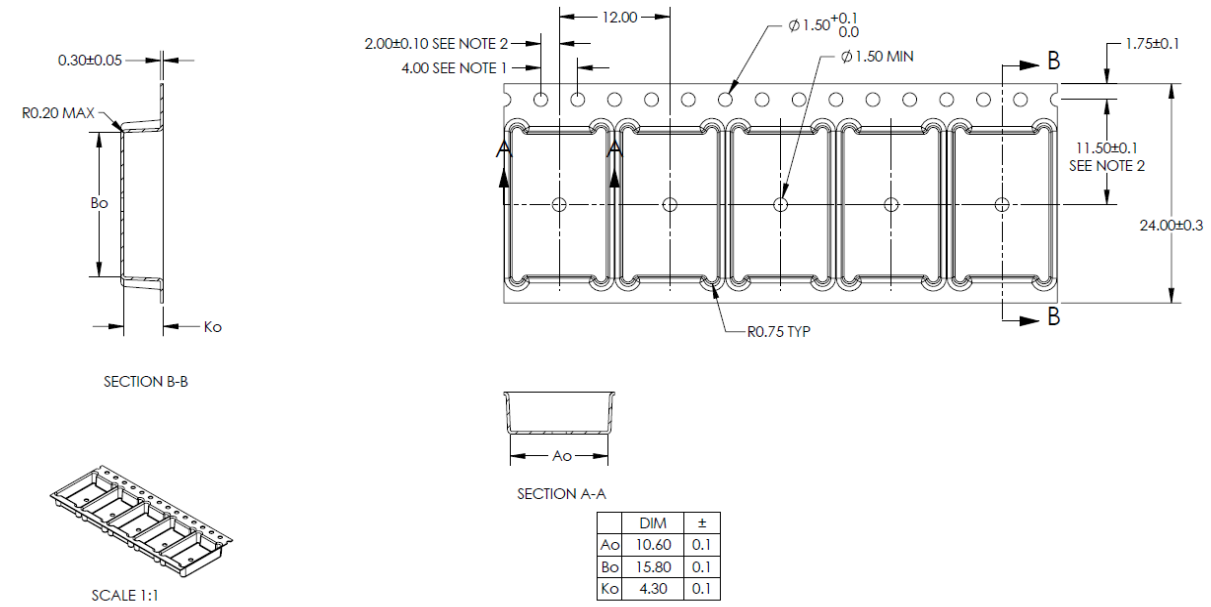


	DIM	±
Ao	10.80	0.1
Bo	12.20	0.1
Ko	2.70	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 11: NINA-B501 tape dimensions

The tape dimensions for NINA-B506 are shown in Figure 12.



	DIM	±
Ao	10.60	0.1
Bo	15.80	0.1
Ko	4.30	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 12: NINA-B506 tape dimensions

7.2 Moisture sensitivity levels

⚠ NINA-B50 series modules are rated as MSL Level 4 devices in accordance with the IPC/JEDEC J-STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 72 hours in factory conditions of maximum 30 °C/60% RH or must be stored at less than 10% RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding MSL (Moisture Sensitivity Level), labeling, and storage, see also the Packaging reference guide [1].

7.3 Reflow soldering

NINA-B50 modules are approved for one-time reflow processes only.

⚠ Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

7.4 ESD precautions

NINA-B50 modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the NINA-B50 module. ESD precautions are particularly relevant when handling the application board on which the module is mounted.

See also, “Handling and Soldering” in the NINA-B50 system integration manual [2].

8 Labeling and ordering information

8.1 Product labeling

The (7.5 x 7.5 mm) labels on the NINA-B50 series modules include important product information.

Figure 13 shows the label applied to NINA-B50 series modules. Each of the given label references are described in Table 22.

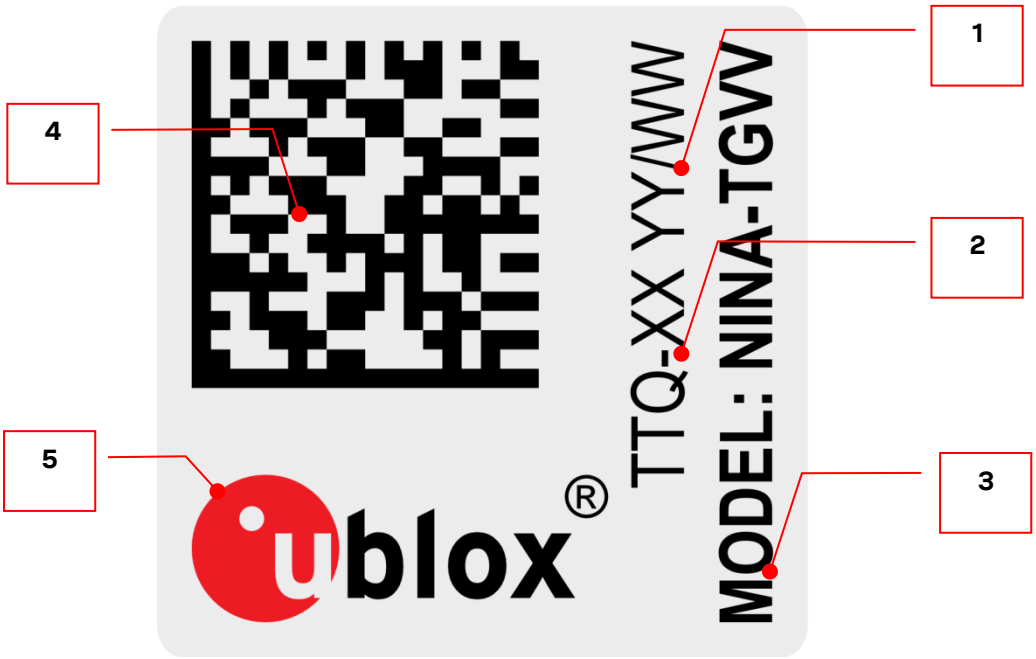


Figure 13: Layout of the NINA-B50 module label

Reference	Description
1	Date of unit production encoded YY/WW (year, week)
2	Major and minor product version information
3	Product model name (NINA-B501, NINA-B506)
4	Data Matrix with unique serial number comprising 19 alphanumeric symbols: The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF. The last 4 symbols represent the hardware and firmware version encoded HHFF. See also MAC addresses.
5	u-blox logo. The red dot also indicates pin 1.

Table 22: NINA-B50 series label description

8.1.1 Product identifiers

Table 23 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade	PPPP-TGVV-TTQ
Type number	Comprises the ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 23: Product code formats

8.1.2 Identification codes

Table 24 describes the individual identification codes represented in each product identifier.

Code	Meaning	Example
PPPP	Form factor	NINA
TG	Platform (Technology and Generation) T – Dominant technology, For example: W: Wi-Fi, B: Bluetooth G - Generation	B5: Bluetooth Generation 5
VV	Variant based on the same platform; range [00…99]	01: open CPU product with antenna pin
TT	Major product version	00: first revision
Q	Quality grade A: Automotive B: Professional C: Standard	B: professional grade
XX	Minor product version	Default value is 00

Table 24: Part identification code

8.2 Ordering information

Ordering code	Product
NINA-B501-10B	NINA-B50 professional grade module based on NXP MCX W716C with CAN controller, with antenna pin for external antenna and open CPU for custom applications
NINA-B506-10B	NINA-B50 professional grade module based on NXP MCX W716C CAN controller, with internal PCB trace antenna and open CPU for custom applications
NINA-B501-00B	NINA-B50 professional grade module based on NXP K32W1480 with antenna pin for external antenna and open CPU for custom applications
NINA-B506-00B	NINA-B50 professional grade module based on NXP K32W1480 with internal PCB trace antenna and open CPU for custom applications

Table 25: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
BLE	Bluetooth Low Energy
CTS	Clear To Send
eDMA	enhanced Direct Memory Access
ESD	Electro Static Discharge
FPU	Floating Point Unit
GATT	Generic ATTribute profile
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
MCU	Micro Controller Unit
MSD	Moisture Sensitive Device
RTS	Request To Send
SPI	Serial Peripheral Interface
TBD	To be Defined
TPM	Timer/PWM Module
UART	Universal Asynchronous Receiver/Transmitter
VPA	Supply voltage for 2.4 GHz radio power amplifier
VREF	Voltage Reference

Table 26: Explanation of the abbreviations and terms used

Related documentation

[1] Packaging reference guide, UBX-14001652
[2] NINA-B50 series system integration manual, UBX-22021116
[3] NXP K32W1480 Data Sheet
[4] NXP K32W1480 Reference Manual
[5] NXP MCX W71 Data Sheet
[6] NXP MCX W71 Reference Manual
[7] u-blox product grades

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	18-Nov-2022	yach	Initial release
R02	19-Jun-2023	yach	Updated NINA-B501-00B and NINA-B506-00B to hardware version 02 and product status to “Prototype”. Updated Bluetooth 5.2 to Bluetooth 5.3. Updated Block diagram. Updated pin assignment in Figure 4. Updated module height to 2.38 mm. Updated section about Low Frequency crystal to sections 4.5 and 4.7 External 32 kHz crystal oscillator. Updated section 4.3 Current consumption. Updated contact information. Minor updates and documentation improvements throughout the document.
R03	27-Oct-2023	yach	Updated NINA-B501-00B and NINA-B506-00B hardware version and product status to “Engineering sample”. Updated conducted RX sensitivity level of Bluetooth LE in Table 1: NINA-B50 characteristics summary and Table 11: RF performance. Added a note in Table 9: Input characteristics of voltage supply pins. Added information for 32 MHz crystal trim value configuration in section 2.4 GHz radio. Updated Antenna radiation patterns. Updated notes describing “EXTAL32K, XTAL32K Load Capacitance” parameters and “Externally provided input clock frequency” in section External 32 kHz crystal oscillator. Updated Figure 10: Orientation of NINA-B50 modules on tape to show correct feed direction. Minor updates and documentation improvements throughout the document.
R04	08-Mar-2024	yach, fkru	Updated NINA-B50 professional grade modules product status to “Initial Production”. Changed status of the regulatory country approvals of NINA-NINA-B50 professional grade modules from “pending” to “approved” for USA, Canada, Europe, and Great Britain in Country approvals. Updated maximum output power from target values to final values in Table 11: RF performance. Improved the Bluetooth qualification information in section 6.3 Bluetooth qualification . Added information for the NINA-B50 automotive grade modules throughout the document.
R05	11-Nov-2024	lalb, fkru	Removed the automotive grade NINA-B50 module variant and related information. Added information for the new NINA-B50 professional grade module variants with CAN, based on the NXP MCX W71 SoC. Changed status of the regulatory country approvals of NINA-NINA-B50 professional grade modules from “pending” to “approved” for Australia, New Zealand, South Korea and Taiwan in Country approvals. Confirmed final values for ESD sensitivity in Maximum ESD ratings

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NINA-B501-00B NINA-B506-00B