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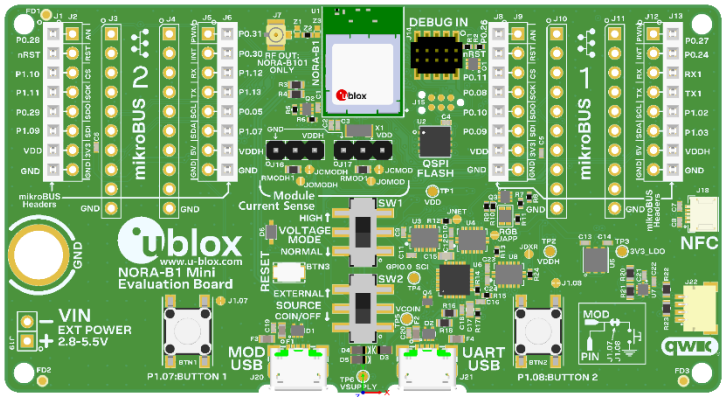
MINI-NORA-B1 EVK, rev B

Evaluation kit revision B for NORA-B1 series modules

User guide



Abstract

This document describes how to set up the MINI-NORA-B1 evaluation kits to evaluate the NORA-B10 series modules. It is applicable only to Rev B of the MINI-NORA-B1 EVK. It also describes the different options for debugging and the development capabilities included in the evaluation board.

Document information

Title	**MINI-NORA-B1 EVK, rev B**
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Product status	Corresponding content status	
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Document status
MINI-NORA-B106, Rev B only	Early production information

For information about the hardware, software, and status of the available product types, see also the NORA-B1 data sheet [1].

Contents

1 Product description

The MINI-NORA-B1 evaluation kit provides stand-alone use of the NORA-B1 series module featuring the Nordic Semiconductor nRF5340 dual-core RF System on Chip (SoC).

The evaluation kit provides a great starting point for almost any Bluetooth® 5.2 Low Energy (LE), Thread, or Zigbee project. All features of the NORA-B1 series modules are easily accessed from the evaluation board. A simple USB connection provides power and two virtual COM ports. Two user buttons are available, as well as a USB peripheral connector, an RGB LED, and a reset button. QSPI flash provides an additional 64 Mbit (8 MB) memory, including execute-in-place (XIP). All 48 GPIO signals of the NORA-B1 are available on headers. Two mikroBUS™ sockets allow the NORA-B1 to host mikroBUS add-on boards. One Qwiic® connecter allows the use of external QWIIC® boards. A low, 1A, drop-out regulator (LDO) provides power to the MINI-NORA-B1. Current sense resistors and connectors allow for measuring load current used by the module.

This guide provides setup instructions for starting development and describes the hardware functionality of the MINI-NORA-B1 board Rev B only[1]. For Rev C and newer, see reference [20].

☞ An external debug probe is required to program and debug applications on the NORA-B1 module on MINI-NORA-B1. See Table 1.

1.1 Key features

- Evaluation platform of the NORA-B106 module
- Two virtual COM ports over USB
- Full GPIO of the NORA-B1 series
- Buttons and LEDs user interaction
- NFC antenna connector
- 32.768 kHz Crystal
- 64 Mbit (8 MB) QSPI flash
- CR2032 battery holder
- USB peripheral connector
- Power input connectors
- 1A LDO regulator
- Two mikroBUS headers
- One Qwiic connector

[1] Rev A was not release to the public.

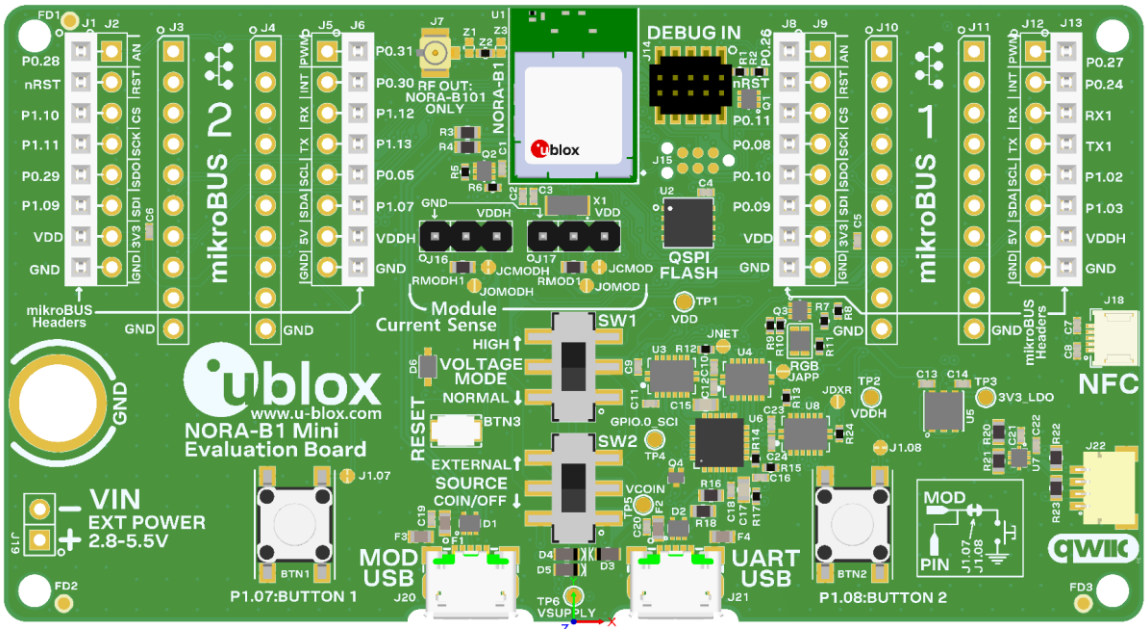

Figure 1: MINI-NORA-B1 Rev B evaluation board (top view)

1.2 MINI-NORA-B106 kit contents

- MINI-NORA-B1 Rev B evaluation board with NORA-B106 module
- NFC antenna
- 2.4 GHz antenna integrated onto NORA-B106 module (no external antenna)
- 2.54 mm center headers for mikroBUS and GPIO connections (for jumper locations J1 – J6, J8 – J13, J16, and J17)

1.3 Revision identification

The revision of the EVK is shown in silkscreen on the bottom side of the PCB. See the highlighted area in Figure 2.

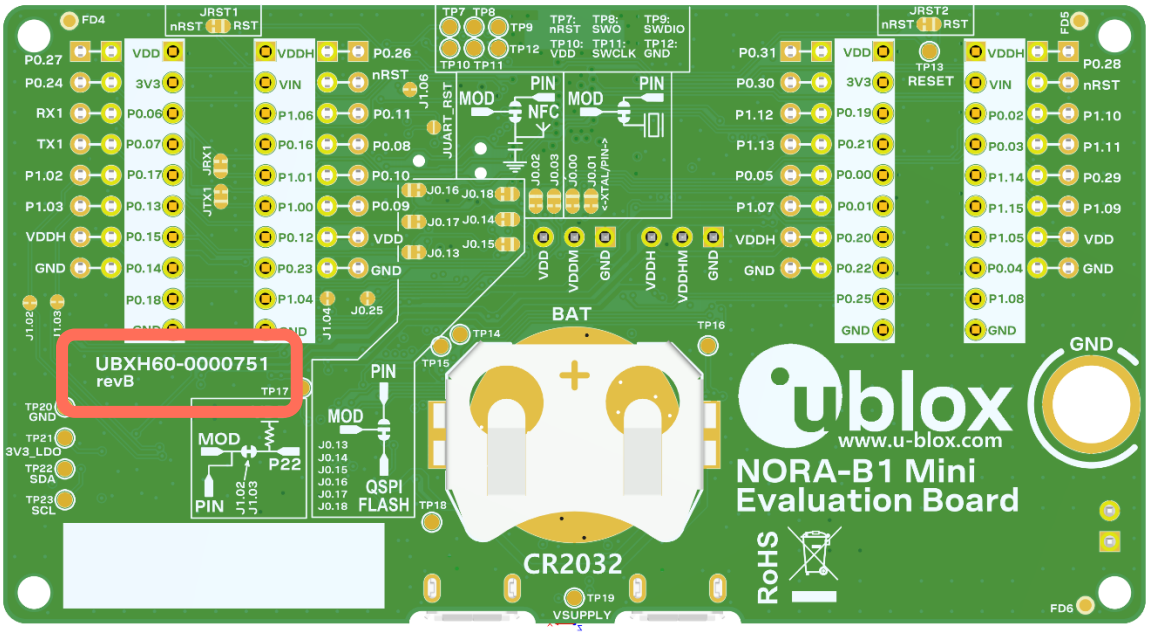

Figure 2: MINI-NORA-B1 Rev B evaluation board (bottom view)

1.4 Required development tools

The tools shown in Table 1 are required for NORA-B1 series Bluetooth LE and IEEE 802.15.4 module applications.

Tool	Description
SEGGER J-Link debug probe	An external SEGGER J-Link debug probe is required to program the NORA-B1 module over the SWD port. A SEGGER J-Link or J-Trace probe [9] or the EVK-NORA-B1 with its J-LINK-OB interface [3] may be used.
Nordic Semiconductor nRF Connect SDK (NCS)	nRF Connect SDK contains several components, including the Zephyr RTOS, MCUboot, and nrfxlib peripheral libraries for the nRF5340 CPU within the NORA-B1 series modules. Installation of NCS is managed through nRF Connect for Desktop. Available for 32- and 64-bit Windows, macOS, and 64-bit Linux platforms. See also reference [6]. Nordic Command Line Tools are installed with NCS, including nrfjprog. ☞ nrfjprog is not supported on ARM Linux.
Nordic Semiconductor nRF Connect for Desktop	nRF Connect for Desktop is the primary development tool used with the NORA-B1 series modules. This tool includes an installation and maintenance utility for the nRF Connect SDK, Toolchain Manager. See also reference [13]. nRF Connect for Desktop is a cross-platform tool that also enables testing and development with Bluetooth LE. It allows easy setup of connections with other devices and uses these connections to read and write the external nodes. Available for Windows, macOS, and Linux.

Table 1: Required development tools

1.5 Optional development tools

The tools shown in Table 2 are additional, optional development tools to aid in NORA-B1 application development.

Tool	Description
Nordic Semiconductor nRF Connect for Mobile	nRF Connect for Mobile is a powerful generic tool that allows you to scan and explore your Bluetooth LE devices and communicate with them. nRF Connect for Mobile supports several Bluetooth SIG adopted profiles, as well as the Device Firmware Update profile (DFU) from Nordic Semiconductor or Eddystone from Google. Available for iOS and Android. Installation is nRF Connect for Mobile is optional. See also reference [14].
SEGGER J-Link Software and Documentation Pack	J-Link Commander (`JLink.exe`) is a command line-based utility that can be used for verifying proper functionality of J-Link as well as for simple analysis of the target system. It supports some simple commands, such as memory dump, halt, step, go, etc., to verify the target connection. Available for Windows, macOS, and Linux. J-Link software may also be used in scripts for end-product programming at the factory. See also reference [10].
Nordic Semiconductor Mobile Apps	Additional, optional mobile utilities for application development. Available for iOS and Android. See also reference [15].
Nordic Semiconductor Power Profiler Kit II (PPK2)	The Power Profiler Kit II is a standalone unit, which can measure and optionally supply currents all the way from sub-µA and as high as 1A on the MINI-NORA-B1 and other hardware. See also reference [16].

Table 2: Optional development tools

2 Hardware description

Design files for the MINI-NORA-B1 PCB may be requested from the u-blox support team.

2.1 Power

The MINI-NORA-B1 has four possible power sources, as described in Table 3.

Source	Voltage	Current (max.)	Remarks
USB from Virtual COM PORT (VCP), J21	+5 VDC nominal	500 mA	Enumerates as USB 2.0, full-speed, USB high-power
USB from NORA-B1, J20	+5 VDC nominal	100 mA	Without application code enabling USB peripheral
		500 mA	With application code enumerating as USB 2.0 peripheral in USB high-power mode
2.54 mm center pins, J19	+2.8 VDC to +5.5 VDC	1000 mA	High voltage mode. See Table 4 and Table 5
	+2.0 VDC to +5.5 VDC	1000 mA	Low voltage mode See Table 4 and Table 5
CR2032 coin cell battery	+3 VDC nominal	-	See the coin cell data sheet for current capacity

Table 3: Power sources

Power settings are determined by SW1 and SW2.

SW1 position	Power mode	Supply voltage	Remarks
HIGH (up)	Enable internal high voltage LDO	2.8 VDC to 5.5 VDC	GPIO voltage reference is set by VREGHVOUT register of the application core Default value is 1.8 VDC
		3.6 VDC to 5.5 VDC for mikroBUS compatibility	Must set VREGHVOUT of the application core to 3.3 VDC for compatibility with mikroBUS standard
NORMAL (down)	Bypass internal high voltage LDO	2.25 VDC to 3.6 VDC	Module supply and GPIO voltage reference is derived See pointer note below.
		3.6 VDC to 5.5 VDC for mikroBUS compatibility	Module supply and GPIO voltage reference = 3.3 VDC, derived from the on-board 3.3 VDC / 1 A discrete LDO

Table 4: Power mode switch SW1

SW2 position	Source	Supply voltage	Remarks
EXTERNAL (up)	J19 or either USB	3.6 VDC to 5.5 VDC 2.8 VDC to 5.5 VDC	When SW1 is in the NORMAL position When SW1 is in the HIGH position
COIN/OFF (down)	CR2032 coin cell	3 VDC nominal	Board off position when no battery is present

Table 5: Power source switch SW2

☞ A voltage as low as 2.25 VDC may be supplied. Between 2.25 VDC and 3.85 VDC, VDD is equal to the supply voltage minus a Schottky diode drop (~300 mVDC) and the LDO dropout voltage (<= 250 VDC): $VDD = V_{IN} - V_{LDO} - V_{DIODE}$

At 3.85 VDC and above, VDD is regulated to 3.3 VDC.

⚠ Only non-rechargeable coin cells, such as the CR2032, are supported.

The two USB connectors and J19 are protected from reverse polarity with Schottky diodes. This allows them to be used simultaneously with the highest voltage supply chosen.

The coin cell is reverse polarity protected and isolated from the other sources to avoid the voltage drop across a protection diode.

2.2 Reset

The EVK primary reset circuit and button (RESET) connects to the following locations:

- NORA-B1 module **nRESET**: active low
- Both SWD debug connectors **nRESET**: active low
- mikroBUS sockets **nRESET:** active low by default. Active high may be selected by changing **JRST1** and **JRST2** jumpers.

The Virtual COM Port (VCP) interface can also be connected to **nRESET** when the solder bridge **JUART_RST** is shorted.

2.3 Buttons

The EVK provides two active-low user buttons that connect to ground when pressed. Table 6 associates the button number and corresponding components.

Button	Switch	GPIO	Jumper
1	BUTTON1	P1.07	J1.07
2	BUTTON2	P1.08	J1.08

Table 6: User button components

Break the associated jumper to remove the button from the circuit.

2.4 Tri-color LED

The EVK provides a tricolor LED – red, green, and blue (RGB). The LED is powered by **VDDH,** and each LED color can be removed from the circuit by breaking the associated jumper. The GPIO control signals are active high.

Color	GPIO	Jumper
Red	P1.04	J1.04
Green	P0.25	J0.25
Blue	P1.06	J1.06

Table 7: LED signals

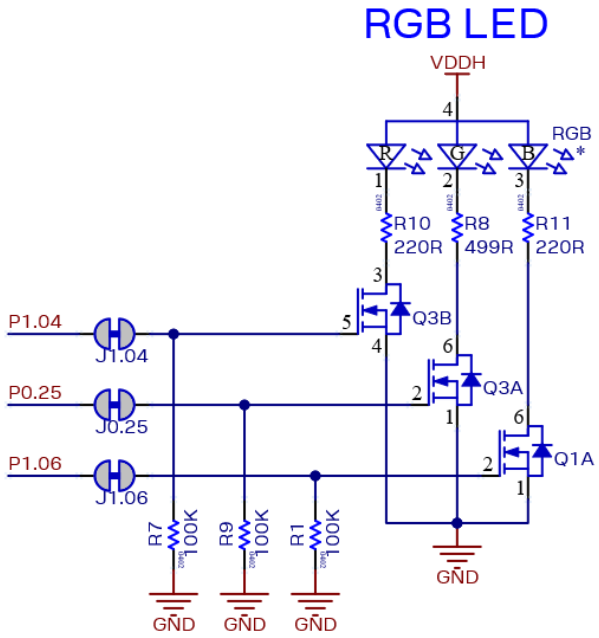

Figure 3: RGB LED schematic

☞ The NCS board support package (BSP) for MINI-NORA-B1 configures both Zephyr and Nordic's LED and button service (LBS) for active-high. No modification to example source code is required.

2.5 Serial communication

The EVK provides two USB-to-serial channels – one for each processor core of the NORA-B1 module. The USB-UART interface comprises a Silicon Labs CP2105 dual UART bridge that includes an Enhanced Communications Interface (ECI) and Standard Communications Interface (SCI). Table 8 describes the function for each UART signal.

NORA-B1 pin name	NORA-B1 function	USB serial IC function
P0.20	Application core TXD	CP2105 ECI RXD
P0.22	Application core RXD	CP2105 ECI TXD
P0.19	Application core RTS	CP2105 ECI CTS
P0.21	Application core CTS	CP2105 ECI RTS
P0.04	Standard GPIO or GPIO output to USB host	CP2105 GPIO 1 ECI
P1.05	Standard GPIO or GPIO input to USB host	CP2105 GPIO 0 ECI
P1.01	Network core TXD	CP2105 SCI RXD
P1.00	Network core RXD	CP2105 SCI TXD
P0.23	Network core RTS	CP2105 SCI CTS
P0.12	Network core CTS	CP2105 SCI RTS
P1.15	Standard GPIO or GPIO output to USB host	CP2105 GPIO 2 SCI
P1.14	Standard GPIO or GPIO input to USB host	CP2105 GPIO 1 SCI

Table 8: USB to serial/GPIO signal assignments

☞ The UART pin assignments for the NORA-B1 network core **RTS** and **CTS** signals are different than those of the EVK-NORA-B1.

Each CP2105 UART interface includes one GPIO input and one output connected to NORA-B1. Use of these signals is optional. To use these signals, an application on the host PC must use the Silicon Labs device driver and DLL. For more information on how to configure the port pins of the CP2105, see also reference [18].

Each CP2105 UART can be isolated from NORA-B1 by shorting the associated solder jumper. Doing so frees up the associated pins in Table 8 for other assignments.

- **JAPP**: short to isolate the application core UART
- **JNET**: short to isolate network core UART
- **JDXR**: short to isolate GPIO from NORA-B1

2.6 32.768 kHz low frequency clock

The low frequency (LF) clock of the NORA-B1 module is supplied from one of four possible sources:

- Internal calibrated RC oscillator (LFRC) – for applications with no strict real-time requirements
- External crystal oscillator (LFXO) – offers the most accurate and lowest power LF clock
- External source (LFXO and **OSCILLATORS.XOSC32KI.BYPASS** settings [11]) – allows the use of a common clock source for other components in a system
- Synthesized LF clock (LFSYNT) derived from the system clock (HFCLK).

The EVK has a 32.768 kHz crystal connected to the NORA-B1 module to allow use of the external crystal oscillator option (LFXO), providing tighter frequency tolerances (±20 ppm). Loading capacitors for the oscillator circuit are provided in the nRF53 integrated within the module.

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. The load capacitance that best matches the crystal specification, 6 pF, 7 pF, or 9 pF, must then be defined in the **XOSC32KI.INTCAP** register.

The formula for calculating the required value of internal capacitor (C_{CAP}) is 2 * C_L – C_{PAD} where:

- Load capacitance (C_L) = 7 pF (crystal data sheet)
- Pad capacitance (C_{PAD}) = 4 pF (nRF53 product specification)

C_{CAP} = 2 * 7 pF – 4 pF = 10 pF. Select the closest available value for the **XOSC32KI.INTCAP** register. For the EVK, this is 9 pF.

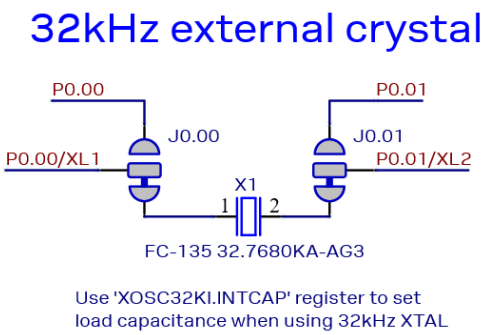

Figure 4: Schematic – 32 kHz crystal

If an internal RC oscillator or external input LF clock source is used, the crystal can be removed from the circuit by opening jumpers **J0.00** and **J0.01**. Soldering across the normally open position connects **P0.00/XL1** and **P0.01/XL2** to the EVK headers.

When using an external clock source, connect it to **P00/XL1** and set **LFCLKSRC.SRC** to LFXO. For a low-swing source, ground P0.01 and set **OSCILLATORS.XOSC32KI.BYPASS** to disabled. For a rail-to-rail source, leave P0.01 open and set **OSCILLATORS.XOSC32KI.BYPASS** to enabled. See also reference [5].

2.7 NFC connector

Connection to an external NFC antenna is provided through a Molex flat-flex connector, part number 051281-0594. Capacitors C7 and C8 provide tuning of the NFC antenna for resonance at 13.56 MHz.

☞ The values of C7 and C8 are tuned for use with the supplied NFC antenna. These values may need to be changed if a different antenna is used. See also reference [3].

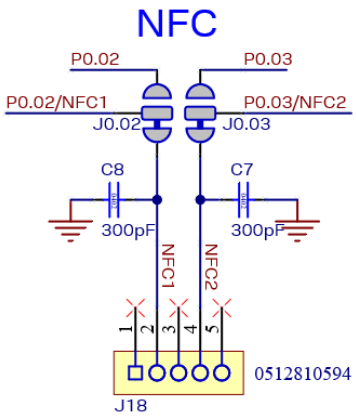

Figure 5: NFC connector

By default, the NORA-B1 module pins P0.02 and P0.03 are configured for NFC use. These pins can also be used for digital GPIO functions by modifying the position of jumpers J0.02 and J0.03 and the value of the NFCPINS UICR register of the application core.

Mode	Short position:	J0.02	J0.03	J0.02	J0.03	NFCPINS UICR register
NFC (default)				Bottom	Bottom	0xFFFFFFFF (enable protection, use as NFC)
GPIO[2,3]		Top	Top			0xFFFFFFFE (disable protection, use as GPIO)

Table 9: P0.02 and P0.03 pin configuration

2.8 Quad SPI (QSPI) flash memory

A 64 Mbit (8 MB) Quad SPI (MX25R6435F) flash is available on the MINI-NORA-B1. This memory can be used for execute-in- place (XIP) directly from the flash as well as general data storage.

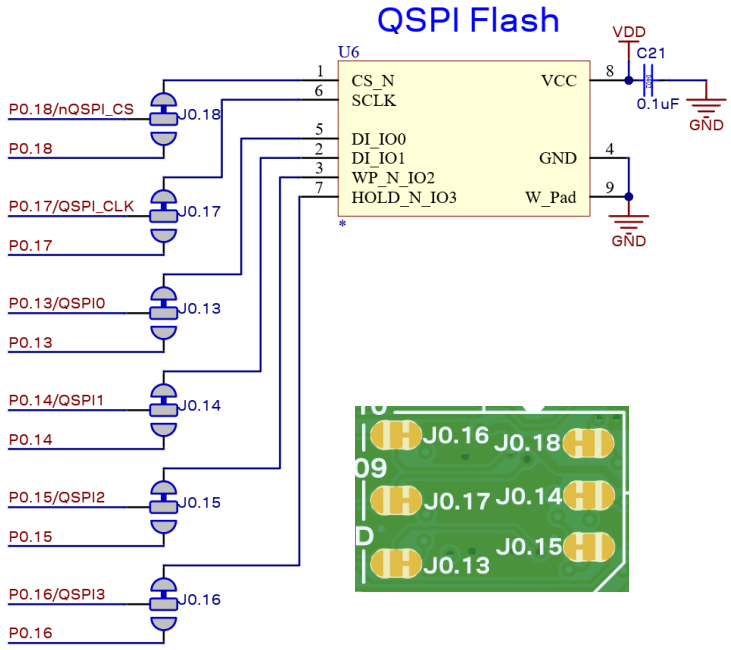

Figure 6: QSPI flash

By default, the NORA-B1 module pins P0.13 and P0.18 are configured for QSPI use. These pins can also be used for digital GPIO functions by modifying the position of jumpers J0.13 through J0.18.

2.9 USB

Two micro-USB connectors are provided on the MINI-NORA-B1. Either connection may be used to power the EVK.

J2 is a micro-USB socket that connects to the USB peripheral of the NORA-B1 module. Application firmware must enable the USB peripheral.

J3 is a micro-USB socket that connects to a dual USB-UART interface. UART port 1 is connected to the application core of the NORA-B1 module. UART port 2 is connected to the network core of the NORA-B1 module. Two output and two input GPIO between the USB host and NORA-B1 are also provided.

[2] P0.02 and P0.03 have a pad capacitance of approximately 2.5 pF higher than other GPIO pins.
[3] When used as GPIO, P0.02 and P0.03 will exhibit approximately 1 µA leakage when driven to different states.

2.10 SWD

Applications are loaded to both the application core and network core of the NORA-B1 module through either J14 or J15. J14 is a 2x5 header on 1.27 mm centers. J15 is a set of PCB test points in the Tag-Connect TC2030-CTX-NL form factor. **SWDIO**, **SWDCLK**, **SWO**, **nRESET**, **VDD**, and **GND** are run in parallel to both connectors.

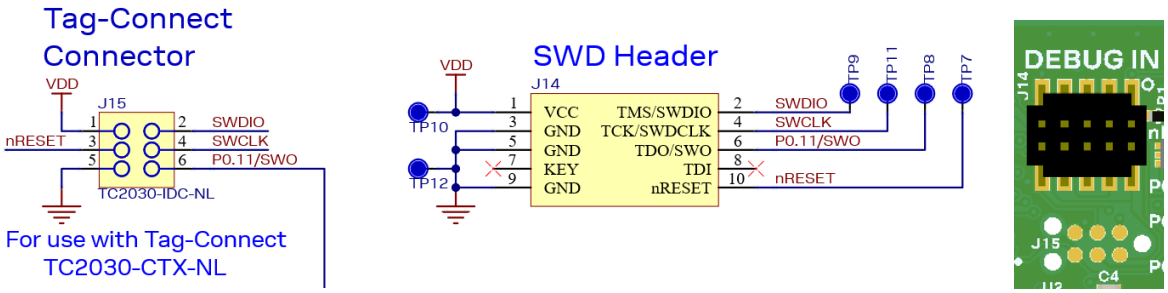

Figure 7: SWD connectors

2.11 Current sensing headers

The EVK provides two current sensing headers:

- J17 allows for power consumption measurement of the NORA-B1 module **VDD**.
- J16 allows for power consumption measurement of the NORA-B1 module **VDDH**.

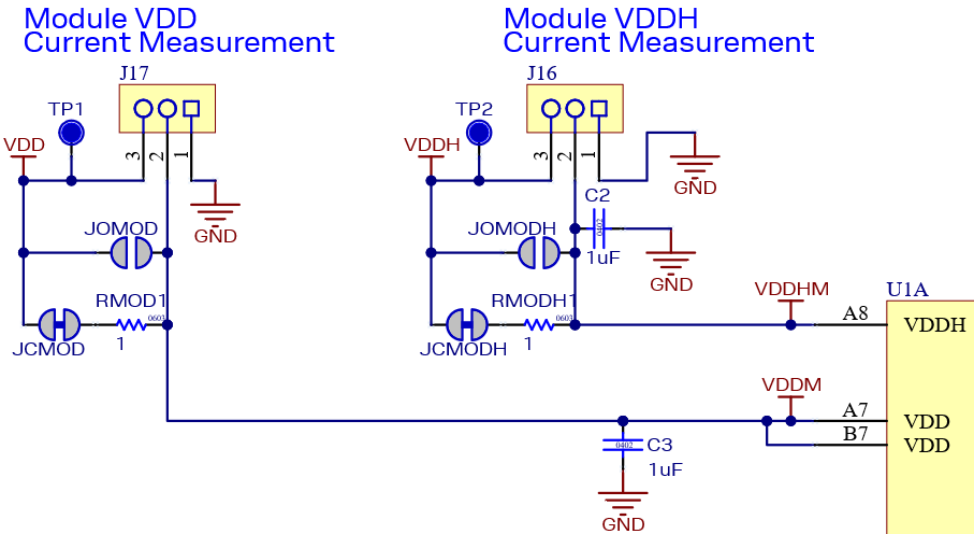

Figure 8: Current measurement

Each 3-pin 2.54 mm pitch header has two pins connected across a 1 Ω current-sense resistor powering the module or the shield, and a third pin connected to ground. To measure current consumption, use a multimeter or other precision voltage measurement device to measure voltage drop across pins 2 and 3. Current can also be measured directly by opening **JCMOD** or **JCMODH** to remove the current-sense resistor from the circuit. Use an ammeter in series with pins 2 and 3 of the desired header.

⚠ Pin 1 of J16 and J17 are connected to **GND**.

The current sense resistors can be bypassed by soldering the respective jumper: **JOMOD** or **JOMODH**.

The default hardware configuration does not require any modification of the current sense headers for the MINI-NORA-B1 to perform properly.

☞ Only current flowing through VMOD into the module is measured; current sunk through GPIO pins is not measured.

2.12 GPIO pin assignments

Header locations on 2.54 mm centers are provided on the EVK to connect the GPIO signals. The socket headers are provided in the kit, though not soldered to the PCB to allow flexibility in connecting external devices.

2.12.1 mikroBUS interfaces

Two mikroBUS sockets are available to incorporate mikroBUS application boards into a project. The pins are duplicated to allow connection flexibility. To connect a mikroBUS application board, solder the supplied socket headers to the outer rows of pins as shown in Figure 9.

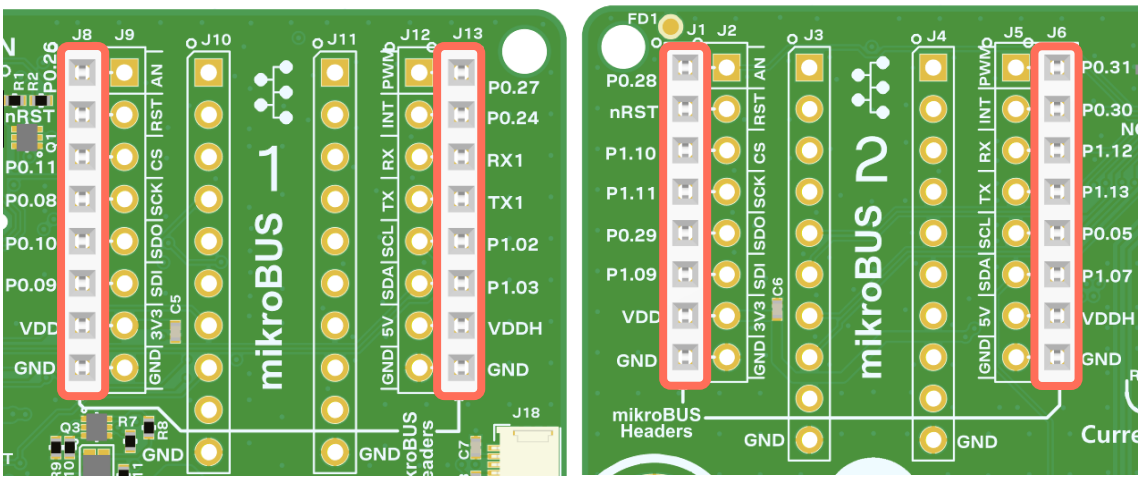

Figure 9: mikroBUS header location

2.12.1.1 mikroBUS interface 1

J8 / J9 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	AN	P0.26	GPIO	Analog input capable GPIO
2	nRESET (active low)	nRESET (active low)	Reset	Active high RESET is available by changing JRST1
3	CS	P0.11/SWO	GPIO	High-speed SPI chip select
4	SCK	P0.08	GPIO	High-speed SPI clock
5	MISO	P0.10	GPIO	High-speed SPI input
6	MOSI	P0.09	GPIO	High-speed SPI output
7	mBUS3V3	–	Power	VDD
8	GND	Ground	Ground	

Table 10: mikroBUS interface 1 connector 1

J12 / J13 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	PWM	P0.27	GPIO	
2	INT	P0.24	GPIO	
3	RX	P0.06 or P1.01/NET_NORA_TX	GPIO	P0.06 default, change JRX1 to select P1.01/NET_NORA_TX
4	TX	P0.07 or P1.00/NET_NORA_RX	GPIO	P0.07 default, change JTX1 to select P0.00/NET_NORA_RX
5	SCL	P1.02	GPIO	High-speed I2C clock
6	SDA	P1.03	GPIO	High-speed I2C data

J12 / J13 Pin	mikroBUS pin	EVK signal	Function	Remarks
7	+5V	VDDH	Power	
8	GND	GND	Ground	

Table 11: mikroBUS interface 1 connector 2

2.12.1.2 mikroBUS interface 2

J1 / J2 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	AN	P0.28	GPIO	Analog input capable GPIO
2	nRESET (active low)	nRESET (active low)	Reset	Active high RESET is available by changing JRST2
3	CS	P1.10	GPIO	SPI chip select
4	SCK	P1.11	GPIO	SPI clock
5	MISO	P0.29	GPIO	SPI input
6	MOSI	P1.09	GPIO	SPI output
7	mBUS3V3	–	Power	VDD default, change J14 to select 3V3_LDO
8	GND	GND	Ground	

Table 12: mikroBUS interface 2 connector 1

J5 / J6 Pin	mikroBUS pin	EVK signal	Function	Remarks
1	PWM	P0.31	GPIO	
2	INT	P0.30	GPIO	
3	RX	P1.12	GPIO	UART input
4	TX	P1.13	GPIO	UART output
5	SCL	P0.05	GPIO	I2C clock
6	SDA	P1.07	GPIO	Shared with BUTTON1, cut J1.07 to isolate for GPIO or mikroBUS use as I2C data
7	+5V	VDDH	Power	
8	GND	GND	Ground	

Table 13: mikroBUS interface 2 connector 2

2.12.2 Other GPIO signals

The remainder of the NORA-B1 GPIO pins are located on 10-pin headers.

J3 Pin	EVK pin name	Remarks
1	VDDH	
2	VIN	
3	P0.02	Shared with NFC, change J0.02 to isolate for GPIO use
4	P0.03	Shared with NFC, change J0.03 to isolate for GPIO use
5	P1.14/GPIO_1_SCI	Shared with USB-UART bridge, short JDXR to isolate for GPIO use
6	P1.15/GPIO2_SCI	Shared with USB-UART bridge, short JDXR to isolate for GPIO use
7	P1.05/GPIO_0_ECI	Shared with USB-UART bridge, short JDXR to isolate for GPIO use
8	P0.04/GPIO_1_ECI	Shared with USB-UART bridge, short JDXR to isolate for GPIO use
9	P1.08	Shared with BUTTON2, cut J1.08 to isolate for GPIO use
10	GND	

Table 14: Header J3

J4 Pin	EVK pin name	Remarks
1	VDD	
2	3V3_LDO	3.3V output of LDO
3	P0.19/APP_NORA_RTS	Shared with USB-UART bridge, short JAPP to isolate for GPIO use
4	P0.21/APP_NORA_CTS	Shared with USB-UART bridge, short JAPP to isolate for GPIO use
5	P0.00	Shared with 32.768 kHz crystal, change J0.00 to isolate for GPIO use
6	P0.01	Shared with 32.768 kHz crystal, change J0.01 to isolate for GPIO use
7	P0.20/APP_NORA_TX	Shared with USB-UART bridge, short JAPP to isolate for GPIO use
8	P0.22/APP_NORA_RX	Shared with USB-UART bridge, short JAPP to isolate for GPIO use
9	P0.25	Shared with REG LED (green), open J0.30 to isolate for GPIO use
10	GND	

Table 15: Header J4

J10 Pin	EVK pin name	Remarks
1	VDDH	
2	VIN	
3	P1.06	Shared with RGB LED (blue), open J1.06 to isolate for GPIO use
4	P0.16	Shared with QSPI flash, change J0.16 to isolate for GPIO use
5	P1.01/NET_NORA_TX	Shared with USB-UART bridge, short JNET to isolate for GPIO use
6	P1.00/NET_NORA_RX	Shared with USB-UART bridge, short JNET to isolate for GPIO use
7	P0.12/NET_NORA_CTS	Shared with USB-UART bridge, short JNET to isolate for GPIO use
8	P0.23/NET_NORA_RTS	Shared with USB-UART bridge, short JNET to isolate for GPIO use
9	P1.04	Shared with RGB LED (red), open J1.06 to isolate for GPIO use
10	GND	

Table 16: Header J10

J11 Pin	EVK pin name	Remarks
1	VDD	
2	3V3_LDO	
3	P0.06	Shared with REG LED (blue), open J1.06 to isolate for GPIO use
4	P0.07	
5	P0.17	Shared with QSPI flash, change J0.17 to isolate for GPIO use
6	P0.13	Shared with QSPI flash, change J0.13 to isolate for GPIO use
7	P0.15	Shared with QSPI flash, change J0.15 to isolate for GPIO use
8	P0.14	Shared with QSPI flash, change J0.14 to isolate for GPIO use
9	P0.18	Shared with QSPI flash, change J0.18 to isolate for GPIO use
10	GND	

Table 17: Header J11

2.13 Antenna

The NORA-B106 module on the MINI-NORA-B106 incorporates a PCB antenna. For best performance, ensure the module antenna is not placed near metallic objects.

3 Software

3.1 Development environment

Software for the MINI-NORA-B1 is developed in the same method as for the EVK-NORA-B1 and the module itself. Nordic Semiconductor nRF Connect SDK provides Zephyr RTOS, MCUboot, and nrfxlib. nRF Connect for Desktop and the Toolchain Manager provide the development environment and updates. See also references [2], [3], [6], [7], and [13].

An external debug interface is required to load and debug application firmware. Suitable debug interfaces include:

- EVK-NORA-B1: a J-Link-OB interface is provided on the full EVK. The debug-out connector may be used to connect the MINI-NORA-B1 with the 10-pin cable provided with the EVK-NORA-B1. See also reference [3].
- Full J-Link debug interface: Any of the available models are suitable. See also reference [9].

3.2 Board support package

MINI-NORA-B1 requires a unique board support package (BSP) to account for the GPIO assignments within the design. An official BSP shall be submitted for inclusion in mainline Zephyr RTOS. Until the submission is merged into the main branch, see the u-blox GitHub repository [4]. Copy the entire `ubx_mininorab1_nrf5340` folder into the NCS `.\ncs\vX.Y.Z\zephyr\boards\arm` directory, where "`X.Y.Z`" is the NCS version in use.

Appendix

A Glossary

Abbreviation	Definition
ARM	Arm (Advanced RISC Machines) Holdings
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC-DC	DC to DC converter
DFU	Device Firmware Update
EVK	Evaluation Kit
FICR	Factory Information Configuration Register
GPIO	General Purpose Input / Output
LDO	Low Drop-Out voltage regulator
LE	Low Energy
LED	Light Emitting Diode
LF	Low Frequency
LiPo	Lithium-Polymer battery
MB	1048576 bytes (binary)
NCS	nRF Connect SDK
NFC	Near-Field Communications
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor network
RTS	Request To Send
RXD	Receive data signal
SES	SEGGER Embedded Studio
SIG	Special Interest Group
SoC	System on Chip
SPI	Serial Peripheral Interface
TXD	Transmit data signal
UICR	User Information Configuration Register
USB	Universal Serial Bus

Table 18: Explanation of the abbreviations and terms used

Related documentation

[1] NORA-B1 data sheet, UBX-20027119
[2] NORA-B1 system integration manual, UBX-20027617
[3] EVK-NORA-B1 user guide, UBX-20030319
[4] MINI-NORA-B1 Zephyr RTOS BSP on u-blox GitHub
[5] Nordic Semiconductor nRF5340 product specification
[6] Nordic Semiconductor nRF Connect SDK documentation
[7] Nordic Semiconductor Toolchain Manager
[8] Nordic Semiconductor Getting Started Assistant
[9] SEGGER J-Link debug probes
[10] SEGGER J-Link Software and Documentation Pack
[11] Nordic Semiconductor nRF53 LFCLK registers
[12] Nordic Semiconductor nRF Command Line Tools
[13] Nordic Semiconductor nRF Connect for Desktop
[14] Nordic Semiconductor nRF Connect for Mobile
[15] Nordic Semiconductor mobile apps
[16] Nordic Semiconductor Power Profiler Kit II
[17] Nordic Semiconductor GitHub site
[18] Silicon Labs application note AN223: Runtime GPIO Control for CP210x
[19] Zephyr project West
[20] MINI-NORA-B1 user guide (Rev C and newer), UBX-23000300

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Revision history

Revision	Date	Name	Comments
R01	03-Sep-2021	brec	Initial release
R02	09-May-2023	brec	Updated to reference only Rev B of MINI-NORA-B1. For newer versions of the EVK, see also [20]. Removed configuration of nRF Connect SDK, see also [6]. Corrected MiB to MB.

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