

ADP-uSD-M2

MicroSD to M.2 adapter

Data sheet



Abstract

This technical data sheet describes the ADP-uSD-M2 microSD to M.2 adapter that converts the M.2 2230 Key E format modules to microSD. It provides an overview and full functional description of the adapter, including a detailed pin definition, block diagram, schematic, assembly drawing, and ordering information. Aimed towards developers and other technical staff, the document provides the critical information for using the adapter to connect any device that is compliant with M.2 2230 Key E interface to 4-bit uSD (SDIO).

Document information

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Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Firmware version	PCN reference	Product status
ADP-uSD-M2	ADP-uSD-M2-00C-00	-	-	Engineering sample

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1 Functional description

1.1 Overview

The microSD to M.2 adapter module, ADP-uSD-M2, is a small and flexible device that gives the user the ability to connect any device with an M.2 2230 Key E interface to a 4-bit SDIO through microSD connector. The module incorporates a 4-wire, UART interface with a break-out connector to expose the M.2 Key E UART signals.

1.2 Product features

ADP-uSD-M2 interfaces	Description
microSD (uSD) for WLAN-SDIO	4 –bit SDIO interface, 208 MHz max. clock rate
M.2(NGFF)	67 pin M.2 2230 Key E format
UART	4-wire UART interface break-out connector with support for hardware flow control and baud rates up to 4Mbps
Package	
Dimensions	60.7 x 30.7 x 9.4 mm
Environmental data, quality, and reliability	
RoHS and REACH compliance	Yes
Electrical data	
microSD power supply	3.0–3.6 VDC
Certifications and approvals	

Table 1: ADP-uSD-M2 product features

1.3 Block diagram

Figure 1 shows the functional block diagram of the ADP-uSD-M2. The M.2 card is connected to an M.2 key E socket whose SDIO signal lines are broken out to a MicroSD-card-shaped, edge connector that can be inserted into the MicroSD slot of a host platform. UART signals can additionally be accessed through a pin header. A jumper, when inserted, is used to disable the Bluetooth radio on the M.2 card.

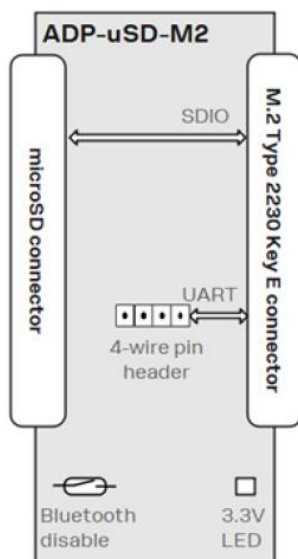


Figure 1: Block diagram of ADP-uSD-M2

1.4 Kit contents

ADP-uSD-M2 kit includes:

- 1x MicroSD-to-M.2 adapter
- 1x M2.5x5 screw

1.5 Product high-level description

Figure 2 shows the various components of the ADP-uSD-M2 adapter:

- **LED1:** Power LED indicator (green) that illuminates when power is applied to the adapter
- **J1:** 4-bit SDIO: MicroSD connector that supplies power and WLAN-SDIO interface
- **J2:** 67 pin, M.2 2230 Key E format
- **J3:** Short this jumper to drive LOW pin 54 (**W_DISABLE2#**) and, depending on the card that is connected to the adapter, invoke the Bluetooth independent reset functionality.
- **J4:** 4-wire UART pin header for Bluetooth communication
- **M1:** Threaded mount for M.2 card retention screw: 30 mm distance from M.2 connector, M2.5 screw is supported

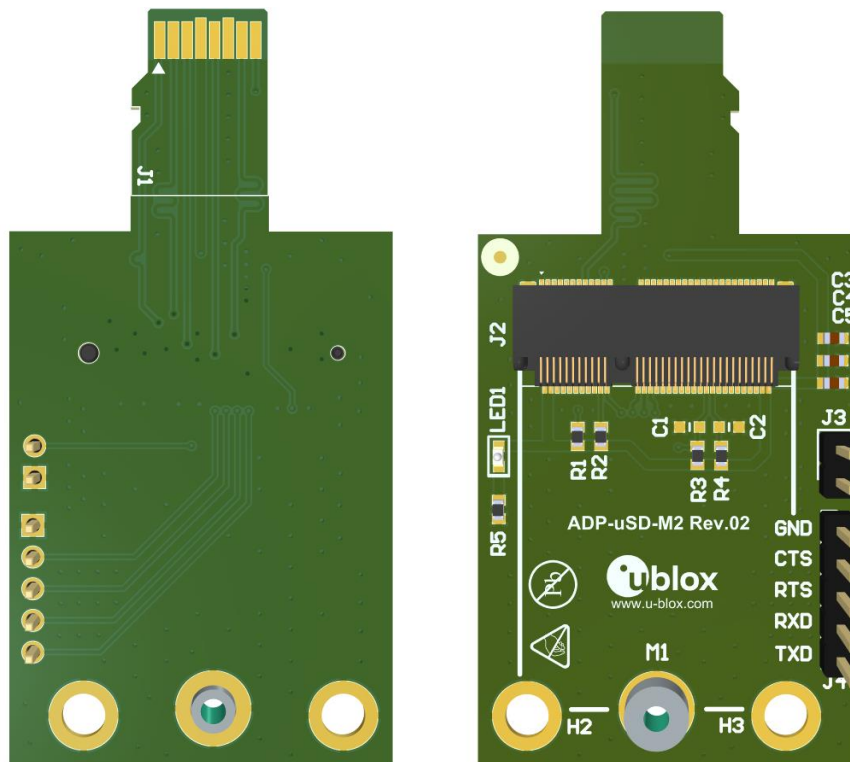


Figure 2: ADP-uSD-M2 top view (left) and bottom view (right)

1.6 ADP-uSD-M2 pinout definition

Table 2 describes the J2 connector pins located on the bottom side of the M.2 card.

Pin no.	Pin name	Pin type	Voltage	Description
1	GND1	GND		Ground
3	USB_D+	NC		USB data + serial data interface. Not connected
5	USB_D-	NC		USB data – serial data interface. Not connected
7	GND2	GND		Ground
9	SDIO_CLK	I	1.8 V	SDIO Clock
11	SDIO_CMD	I/O	1.8 V	SDIO Command
13	SDIO_D0	I/O	1.8 V	SDIO Data 1
15	SDIO_D1	I/O	1.8 V	SDIO Data 2
17	SDIO_D2	I/O	1.8 V	SDIO Data 3
19	SDIO_D3	I/O	1.8 V	SDIO Data 4
21	SDIO_WAKE#	O	VIO	NXP usage: WLAN_WAKE_HOST . Sideband signal used by the Wi-Fi radio to wake up the platform. Active Low by default. Pulled up to 3.3 V.
23	SDIO_RESET#	NC	VIO	NXP usage: WLAN_INDEPENDENT_RESET . Sideband signal to independently reset the Wi-Fi radio. Not connected.
M.2 Key E connector notch				
33	GND4	GND		Ground
35	PERP0	NC		PCIe RX. Not connected
37	PERN0	NC		PCIe RX. Not connected
39	GND5	GND		Ground
41	PETP0	NC		PCIe TX. Not connected
43	PETN0	NC		PCIe TX. Not connected
45	GND6	GND		Ground
47	REFCLKP0	NC		PCIe Reference Clock. Not connected
49	REFCLKN0	NC		PCIe Reference Clock. Not connected
51	GND7	GND		Ground
53	CLKREQ0#	NC		PCIe Clock Request. Not connected
55	PEWAKE0#	NC		PCIe PME Wake. Not connected
57	GND8	GND		Ground
59	PERP1	NC		PCIe RX. Not connected
61	PERN1	NC		PCIe RX. Not connected
63	GND9	GND		Ground
65	PETP1	NC		PCIe TX. Not connected
67	PETN1	NC		PCIe TX. Not connected
69	GND10	GND		Ground
71	REFCLKP1	NC		PCIe Reference Clock. Not connected
73	REFCLKN1	NC		PCIe Reference Clock. Not connected
75	GND11	GND		Ground

Table 2: ADP-uSD-M2 connector J2 pinout (top side)

Table 3 describes the J2 connector pins located on the top and bottom side of the M.2 card.

Pin no.	Pin name	Pin type	Voltage	Description
2	3.3V	P	3.3 V	Supply voltage pin
4	3.3V	P	3.3 V	Supply voltage pin
6	LED_1#	NC		Not connected
8	PCM_CLK/I2S_SCK	NC		PCM data clock. Not connected
10	PCM_SYNC/I2S_WS	NC		PCM frame sync. Not connected
12	PCM_OUT/I2S_SD_OUT	NC		PCM data output. Not connected
14	PCM_IN/I2S_SD_IN	NC		PCM data input. Not connected
16	LED2#	NC		Not connected
18	GND3	GND		Ground
20	UART_WAKE#	O	3.3 V	NXP usage: BT_WAKE_HOST . Sideband signal used by the Bluetooth radio to wake up the platform. Active Low by default. Pulled up to 3.3 V.
22	UART_TXD	O	VIO	UART transmit. Connected to UART header J4.
M.2 Key E connector notch				
32	UART_RXD	I	VIO	UART receive. Connected to UART header J4.
34	UART_RTS	O	VIO	UART Request-To-Send. Connected to UART header J4.
36	UART_CTS	I	VIO	UART Clear-To-Send. Connected to UART header J4.
38	VENDOR_DEF1	NC	VIO	Not connected
40	VENDOR_DEF2	I	VIO	NXP usage: DEV_WLAN_WAKE . Sideband signal used by the platform to wake up the Wi-Fi radio. Active Low. Connect to Host GPIO
42	VENDOR_DEF3	I	VIO	NXP usage: DEV_BT_WAKE . Sideband signal used by the platform to wake up the Bluetooth radio. Active Low. Connect to Host GPIO
44	COEX3	NC	VIO	Not connected
46	COEX2	NC	VIO	Not connected
48	COEX1	NC	VIO	Not connected
50	SUSCLK(32KHZ)	NC		Not connected
52	PERST0#	NC		PCIe host indication to reset the device. Not connected
54	W_DISABLE2#	I	3.3 V	NXP usage: BT_INDEPENDENT_RESET . Sideband signal to independently reset the Bluetooth radio. Active Low by default. Connected to jumper J3 on the adapter and pulled up to 3.3 V.
56	W_DISABLE1#	I	3.3 V	NXP usage. PDn . Full Power-down for the Wi-Fi/BT radio: High = normal mode, Low = full power-down mode. Pulled up to 3.3 V.
58	I2C_DATA	NC		I2C data. Not connected
60	I2C_CLK	NC		I2C clock. Not connected
62	ALERT#	NC		Not connected
64	RESERVED	NC		Not connected
66	UIM_SWP/PERST1#	NC		Not connected
68	UIM_PWR_SNK/CLKREQ1#	NC		Not connected
70	UIM_PWR_SRC/GPIO1/PEWAKE1#	NC		Not connected
72	3V3_3	P	3.3 V	Supply voltage pin
74	3V3_4	P	3.3 V	Supply voltage pin

Table 3: ADP-uSD-M2 connector J2 pinout (bottom side)

Table 4 describes the J4 connector pins, where the UART signals are broken out.

Pin no.	Pin name	Pin type	Description
1	GND	GND	Ground
2	BT_UART_CTS	I	Bluetooth UART Clear-To-Send
3	BT_UART_RTS	O	Bluetooth UART Request-To-Send
4	BT_UART_RXD	I	Bluetooth UART Receive
5	BT_UART_TXD	O	Bluetooth UART Transmit

Table 4: ADP-uSD-M2 connector J4 pinout

Table 5 describes the J3 connector jumper pins.

Pin no.	Pin name	Pin type	Description
1	GND	GND	Ground
2	BT_REG_ON	I	Enable/Disable Bluetooth core. Active High

Table 5: ADP-uSD-M2 connector J3 pinout

Table 6 describes the microSD-card-shaped, J1 connector pins.

Pin no.	Pin name	Pin type	Description
1	USD_DATA2	I/O	microSD SDIO DATA2
2	USD_DATA3	I/O	microSD SDIO DATA3
3	USD_CMD	I/O	microSD SDIO Command
4	VCC	P	Power supply from microSD (3V3)
5	USD_CLK	O	microSD SDIO Clock
6	GND	GND	microSD Ground
7	USD_DATA0	I/O	microSD SDIO DATA0
8	USD_DATA1	I/O	microSD SDIO DATA1

Table 6: ADP-uSD-M2 connector J1 pinout

2.3 PCB assembly drawings

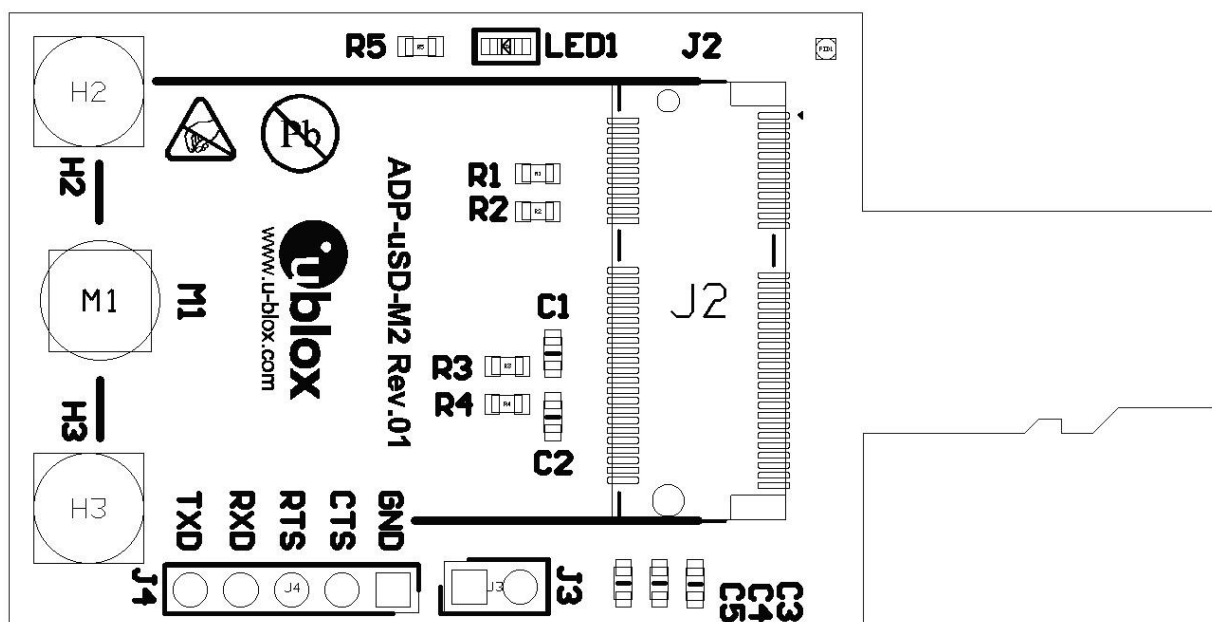


Figure 4: ADP-uSD-M2 top assembly

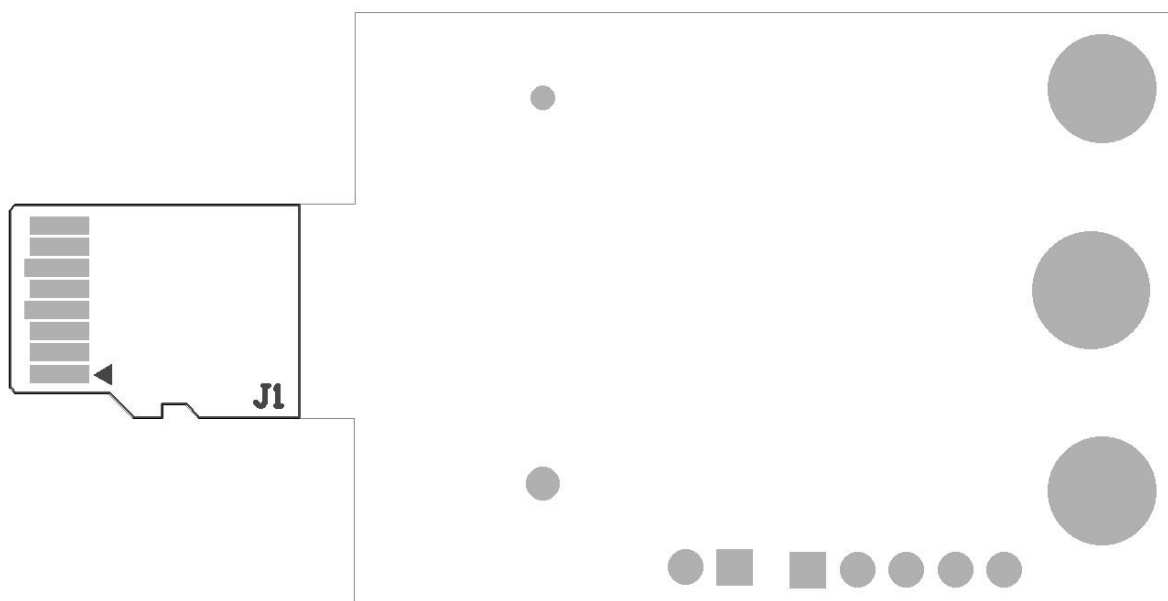


Figure 5: ADP-uSD-M2 bottom assembly

3 Product handling

3.1 Shipment, storage, and handling

 For information regarding shipment, storage, and handling, see the Product packaging reference guide [\[2\]](#).

3.1.1 ESD handling precautions

 ADP-uSD-M2 modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Handling the modules without proper ESD protection can destroy or damage them permanently.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates ADP-uSD-M2. These procedures are particularly important when handling the application board on which the module is mounted.

4 Labeling and ordering information

4.1 Product labeling

The labels applied to ADP-uSD-M2 modules include important product information. [Figure 6](#) shows the given label information, where each given reference is described in [Table 8](#).

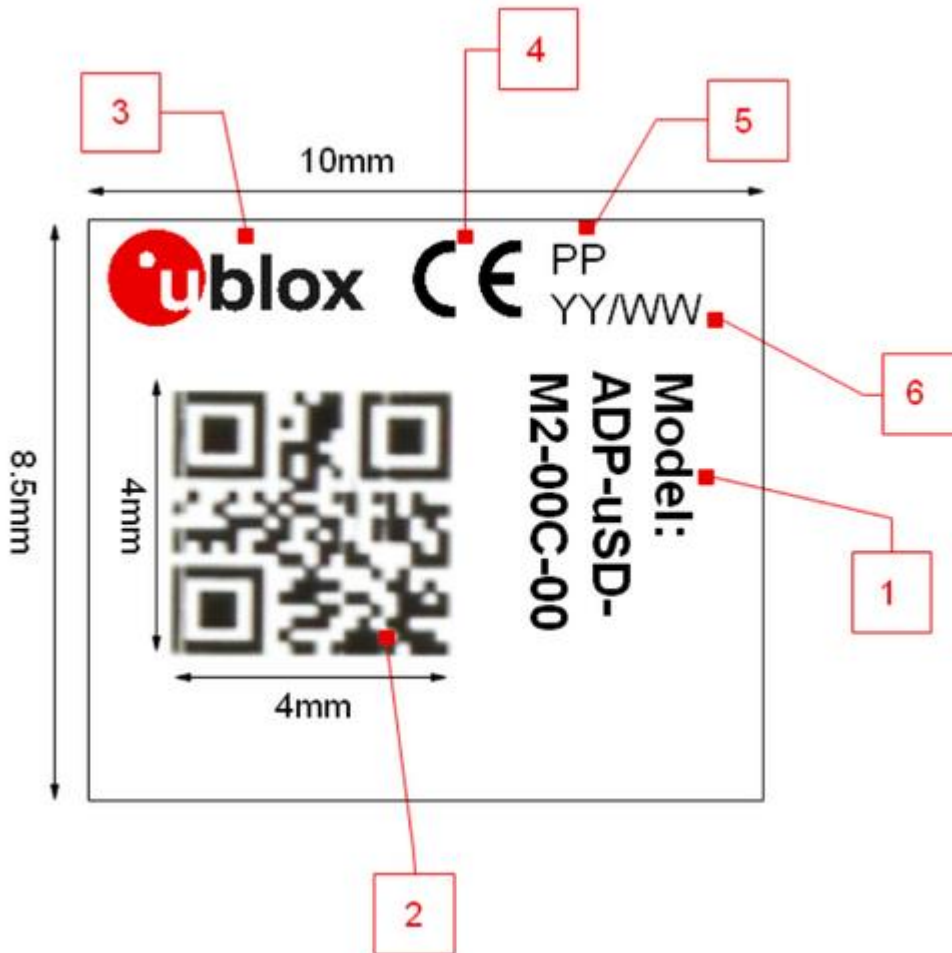


Figure 6: Label information shown on the ADP-uSD-M2

Reference	Description
1	Text box containing product name and version
2	Data Matrix with unique serial number
3	u-blox logo
4	CE certification
5	Panel position number (used for production tracking)
6	Date of production in the format YY/WW (year/week)

Table 8: ADP-uSD-M2 label references

4.2 Ordering information

Ordering Code	Product
ADP-uSD-M2-00C	MicroSD to M.2 adapter

Table 9: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
CTS	Clear to send
DC	Direct current
DSR	Data set ready
DTR	Data terminal ready
GND	Ground
H	High (logic state)
I	Input (means that this is an input port of the module)
MSD	Moisture sensitive device
L	Low (logic state)
N/A	Not applicable
NC	Not connected
O	Output (means that this is an output port of the module)
P	Power (means that a power supply voltage is applied to this port)
PCN/IN	Product change notification / Information note
RTS	Request to send
RXD	Receive data
SDIO	Secure digital input output
TXD	Transmit data
UART	Universal asynchronous Receiver/Transmitter
M.2	Formerly known as the Next Generation Form Factor (NGFF), is a specification for internally mounted computer expansion cards and associated connectors. The M.2 specification is defined by PCI-SIG (www.pcisig.com).

Table 10: Explanation of the abbreviations and terms used

Related documents

- [1] ADP-uSD-M2 product summary, [UBX-21040110](#)
- [2] Product packaging reference guide, [UBX-14001652](#)

 For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	27-Sep-2021	iban	Initial draft.

Contact

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