

TFT MODULE SPECIFICATION



RVT35HHBNWCA0

EVE4 IPS 3.5" LCD TFT DATASHEET

Rev.1.3
2022-11-30

| ITEM | CONTENTS | UNIT |
|--------------------------------|---|-------------------|
| LCD Type | TFT/Transmissive/Normally Black/IPS | / |
| Size | 3.5 | Inch |
| Viewing Direction | Free | / |
| Outside Dimensions (W x H x D) | 76.90 x 63.90 x 12.25 | mm |
| Active Area (W x H) | 70.08 x 52.56 | mm |
| Pixel Pitch (W x H) | 0.219 x 0.219 | mm |
| Resolution | 320 (RGB) x 240 | / |
| Brightness | 800 | cd/m ² |
| Color Depth | 16.7 M | / |
| Pixel Arrangement | RGB Vertical Stripe | / |
| Driver IC of Board | BT817Q | / |
| Interface | SPI/QSPI | / |
| QSPI Flash Memory size | 256 | Mb |
| Host Connector | RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact | / |
| With/Without Touch | With Projected Capacitive Touch Panel | / |
| CTP Driver | ILI2132A | / |
| Supply Voltage for Module | 3.3 | V |
| Supply Voltage for Backlight | 5.0 (TYP.) | V |
| Audio amplifier | Build in class-D 1.5W audio amplifier | / |
| Weight | 69 | g |

Note 1. RoHS3 compliant

Note 2. LCM weight tolerance: ± 5%.



1. REVISION RECORD

| REV NO. | REV DATE | CONTENTS | REMARKS |
|---------|------------|---|---------|
| 1.0 | 2021-07-27 | Initial Release | |
| 1.1 | 2021-12-06 | Add the accessory link of Riverdi louder speaker: RVA-SPK1.5W-C150, which is matched with Riverdi all EVE4 series displays. | |
| 1.2 | 2022-04-13 | Correction on figure of simplified audio circuit design from R4, 1K resistor to R4, 100K resistor. R4 100K is the actual resistor value on PCB. | |
| 1.3 | 2022-11-30 | <ul style="list-style-type: none">• Update the backlight electrical parameters• Add more detailed info like QSPI flash memory size, Audio amplifier etc.• Drawing update with adding grounding tape and dimensions overhaul | |



2. CONTENTS

| | |
|---|----|
| 1. REVISION RECORD..... | 2 |
| 2. CONTENTS..... | 3 |
| 3. MODULE CLASSIFICATION INFORMATION..... | 4 |
| 4. MODULE DRAWING..... | 5 |
| 5. ABSOLUTE MAXIMUM RATINGS..... | 6 |
| 6. ELECTRICAL CHARACTERISTICS | 6 |
| 7. BACKLIGHT ELECTRICAL CHARACTERISTICS..... | 6 |
| 8. ELECTRO-OPTICAL CHARACTERISTICS..... | 7 |
| 9. INTERFACES DESCRIPTION..... | 9 |
| 9.1 P1 connector - RiBUS description | 9 |
| 9.2 P2 connector - Audio interface description | 10 |
| 10. BT817Q CONTROLLER SPECIFICATION..... | 11 |
| 10.1 Serial host interface | 11 |
| 10.2 Block diagram..... | 11 |
| 10.3 Host interface SPI mode 0..... | 12 |
| 10.4 Backlight driver block diagram..... | 12 |
| 11. 256Mb NOR FLASH MEMORY..... | 13 |
| 12. TIMING CHARACTERISTICS | 13 |
| 12.1 Input setup timing setting..... | 13 |
| 12.1.1 Parallel 24-bit RGB timing table..... | 13 |
| 12.2 System bus timing for RGB interface..... | 14 |
| 13. CAPACITIVE TOUCH SCREEN PANEL SPECIFICATIONS..... | 14 |
| 13.1 Mechanical characteristics..... | 14 |
| 13.2 Electrical characteristics..... | 15 |
| 14. MODULE INITIALIZATION..... | 15 |
| 15. INSPECTION | 16 |
| 15.1 Inspection condition | 16 |
| 15.2 Inspection standard..... | 17 |
| 16. RELIABILITY TEST..... | 18 |
| 17. LEGAL INFORMATION | 19 |

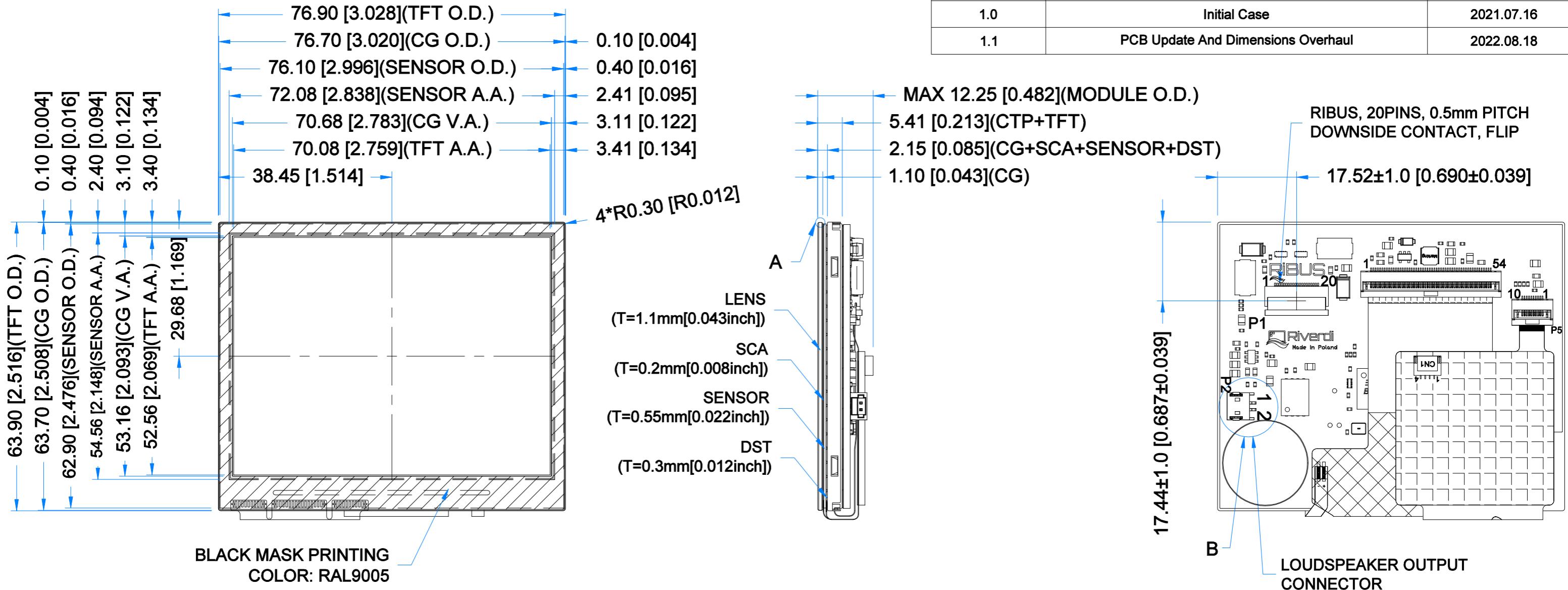


3. MODULE CLASSIFICATION INFORMATION

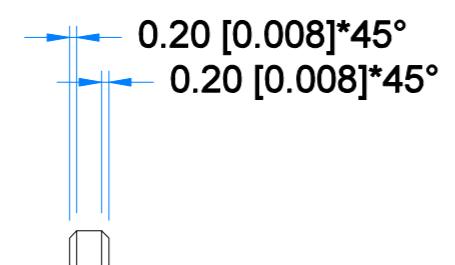
| RV | T | 35 | H | H | B | N | W | C | A0 |
|----|----|----|----|----|----|----|----|----|-----|
| 1. | 2. | 3. | 4. | 5. | 6. | 7. | 8. | 9. | 10. |

| NO. | PARAMETER | SYMBOL |
|-----|------------------|----------------------------------|
| 1. | BRAND | RV – Riverdi |
| 2. | PRODUCT TYPE | T – TFT Standard |
| 3. | DISPLAY SIZE | 35 – 3.5" |
| 4. | MODEL SERIAL NO. | H – High Brightness, IPS |
| 5. | RESOLUTION | H – 320 x 240 px |
| 6. | INTERFACE | B – SPI/QSPI |
| 7. | FRAME | N – Without Mounting Metal Frame |
| 8. | BACKLIGHT TYPE | W – LED White |
| 9. | TOUCH PANEL | C – With Capacitive Touch Panel |
| 10. | VERSION | A0 – aTouch |

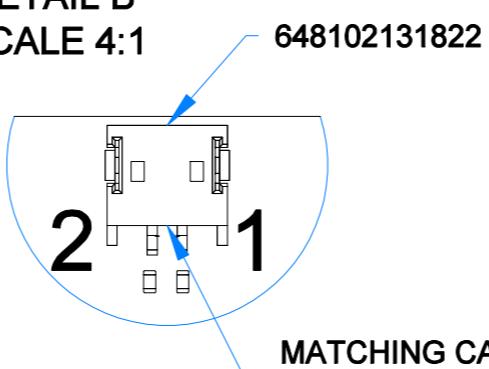
| Revision: | Changes: | Date: |
|-----------|------------------------------------|------------|
| 1.0 | Initial Case | 2021.07.16 |
| 1.1 | PCB Update And Dimensions Overhaul | 2022.08.18 |



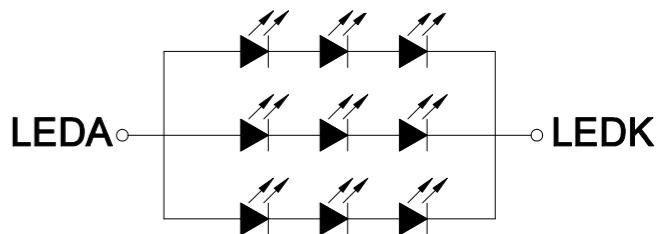
DETAIL A
SCALE 4:1



DETAIL B
SCALE 4:1



MATCHING CABLE CONNECTOR:
648002113322



LED Diagram Circuit

TFT NOTES:
1. LCD TYPE: TRANSMISSIVE, NORMALLY BLACK, IPS
2. RESOLUTION: 320x240
3. VIEWING ANGLE: FREE
4. SURFACE LUMINANCE: 800 cd/m²
5. DRIVING IC ON THE BOARD: BT817Q
6. INTERFACE: SPI/QSPI
7. SUPPLY VOLTAGE FOR MODULE: 3.3V
8. SUPPLY VOLTAGE FOR BACKLIGHT: 5.0V(TYP.), BUILT-IN LED INVERTER

TP NOTES:
1. TP STRUCTURE: G+G
2. CG THICKNESS: 1.10mm [0.043inch]
3. SURFACE HARDNESS: 7H
4. DRIVER IC: ILI2132A
5. INTERFACE: SPI/QSPI VIA RIBUS AND BT817Q

GENERAL NOTES:
1. AIR BONDING BETWEEN TFT AND CTP
2. OPERATING TEMPERATURE: -20°C ~ 70°C
3. STORAGE TEMPERATURE: -30°C ~ 80°C
4. WITHOUT INDIVIDUAL TOLERANCE:
±0.3mm [0.012inch]
5. RoHS3 COMPLIANT

PN: RVT35HHBNWCA0

SN:

DRAWN: M.Natywa

 Riverdi

2022.08.18

1:0.85



CHECKED: Carol Gao

2022.08.22

[mm]



APPR:

ISO A3 P. 1 of 1



5. ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN | MAX | UNIT | NOTE |
|---|-----------------|------|-----|------|----------|
| Supply Voltage for Module | VDD | 0 | 3.6 | V | NOTE 1 |
| Digital I/O signals (SPI/QSPI/GPIO) Voltage | VIN | -0.5 | 3.3 | V | NOTE 1,2 |
| Supply voltage for Backlight | BLVDD | -0.3 | 7.0 | V | NOTE 1 |
| Operating Temperature | T _{OP} | -20 | 70 | °C | |
| Storage Temperature | T _{ST} | -30 | 80 | °C | |
| Storage Humidity (@ 25 ± 5°C) | H _{ST} | 10 | - | % RH | |
| Operating Ambient Humidity (@ 25 ± 5°C) | H _{OP} | 10 | - | % RH | |

Note 1. Exceeding maximum values may cause improper operation or permanent damage to the unit.

Note 2. Digital I/O signals are to be connected to pins 3 ÷ 9, 11 and 12 pins at RiBUS connector (P1).

6. ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | NOTE |
|---------------------------|-----------------|-----|-----|-----|------|------|
| Supply Voltage for Module | VDD | 3.0 | 3.3 | 3.6 | V | |
| Input Voltage "H" Level | V _{IH} | 2.0 | - | 3.3 | V | |
| Input Voltage "L" Level | V _{IL} | 0 | - | 0.8 | V | |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | NOTE |
|-----------------------------|------------------|-----|-----|-----|------|--------|
| Current drawn from VDD@3.3V | I _{VDD} | - | 104 | 398 | mA | Note 1 |

Note 1. Animated pictures are displayed on the screen and there is no QSPI communication during the measurement of TYP and MAX values.

TYP value is measured when the audio is off.

MAX value is measured when the audio is on, and volume is set to maximum.

Riverdi loudspeaker RVA-SPK1.5W-C150 is applied during the measurement.

7. BACKLIGHT ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | NOTE |
|------------------------------|--------|-----|--------|-----|-------|--------|
| Supply Voltage for Backlight | BLVDD | 4.5 | 5.0 | 5.5 | V | Note 1 |
| Lifetime | - | - | 50,000 | - | hours | Note 2 |

Note 1. The Min voltage of BL driver is 2.7V, the modules will work, but full brightness can't be achieved.

Note 2. Operating life means the period in which the LED brightness goes down to 50% of the initial brightness. Typical operating lifetime is the estimated parameter.



| PARAMETER | SYMBOL | MIN BL | 50% BL | 100% BL | UNIT | NOTE |
|--------------------------------|--------------------|--------|--------|---------|------|--------|
| Current drawn from BLVDD @4.5V | I _{BLVDD} | TBD | TBD | TBD | mA | Note 3 |
| Current drawn from BLVDD @5.0V | | 4.29 | 56 | 135 | | |
| Current drawn from BLVDD @5.5V | | 4.16 | 51 | 119 | | |

Note 3. To control the backlight dimming, please refer to subchapter 10.4.

MIN BL is when REG_PWM_DUTY = 1

50% BL is when REG_PWM_DUTY = 64

100% BL is when REG_PWM_DUTY = 128

8. ELECTRO-OPTICAL CHARACTERISTICS

| ITEM | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT | RMK | NOTE |
|----------------------------|----------------|--------------------------|-------|-------|-------|-------------------|--------|------|
| Response Time | Tr+Tf | θ=0° φ=0° Ta=25 °C | - | 50 | - | ms | FIG 1. | 4 |
| Contrast Ratio | Cr | | - | 700 | - | --- | FIG 2. | 1 |
| Luminance Uniformity | δ WHITE | | - | 75 | - | % | FIG 2. | 3 |
| Surface Luminance | L _v | | - | 800 | - | cd/m ² | FIG 2. | 2 |
| Viewing Angle | θ | φ = 90° | - | 80 | - | deg | FIG 3. | 6 |
| | | φ = 270° | - | 80 | - | deg | FIG 3. | |
| | | φ = 0° | - | 80 | - | deg | FIG 3. | |
| | | φ = 180° | - | 80 | - | deg | FIG 3. | |
| CIE (x, y) Chromaticity | R _x | θ=0° φ=0° Ta=25 °C | 0.573 | 0.613 | 0.653 | - | FIG 2. | 5 |
| | R _y | | 0.317 | 0.357 | 0.397 | - | | |
| | G _x | | 0.324 | 0.364 | 0.404 | - | | |
| | G _y | | 0.263 | 0.603 | 0.643 | - | | |
| | B _x | | 0.110 | 0.150 | 0.190 | - | | |
| | B _y | | 0.069 | 0.109 | 0.149 | - | | |
| | W _x | | 0.277 | 0.317 | 0.357 | - | | |
| | W _y | | 0.299 | 0.339 | 0.379 | - | | |

Note 1. Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

L_v = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of



5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 1. The test equipment is BM-7A.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then calculating the average value.

Note 6. For TFT module, viewing angle is the angle at which the contrast ratio is greater 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

Note 7. Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A.

Figure 1. The definition of response time

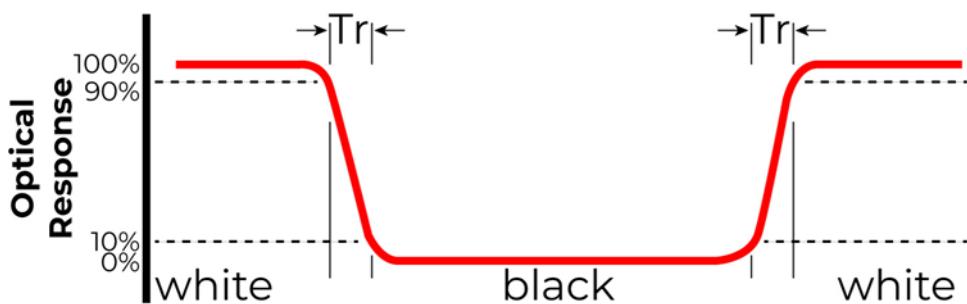
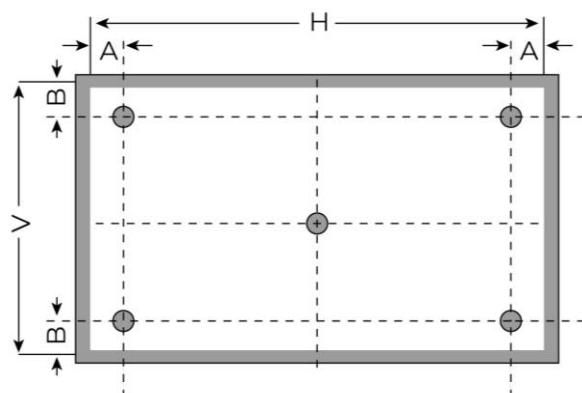


Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity



A: 5mm

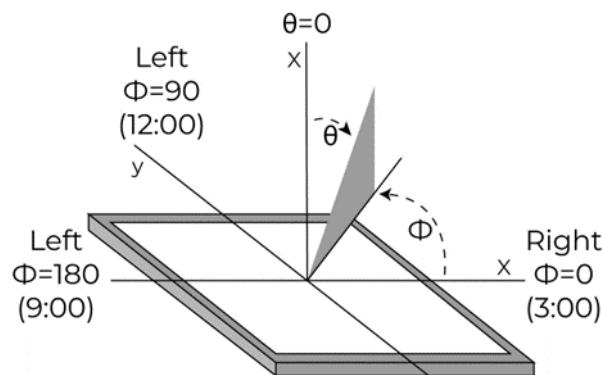
B: 5mm

H, V: Active Area

Light spot size $\phi=5\text{mm}$, 500mm distance from the LCD surface to detector lens.

Measurement instrument is SR-3A

Figure 3. The definition of viewing angle



9. INTERFACES DESCRIPTION

9.1 P1 connector - RiBUS description

| PIN NO. | CONNECTOR | DESCRIPTION | NOTE |
|---------|-------------|--|------|
| 1 | VDD | Supply voltage for module; TYP 3.3 V | |
| 2 | GND | Ground | |
| 3 | SPI_SCLK | SPI SCK signal | |
| 4 | MISO/ IO.1 | SPI MISO signal / SPI Quad mode: SPI data line 1 | |
| 5 | MOSI/ IO.0 | SPI MOSI signal / SPI Quad mode: SPI data line 0 | |
| 6 | CS | SPI chip select signal | |
| 7 | INT | Interrupt signal from device to the system, Active Low, internally 47k Pull UP | |
| 8 | RST/PD | Reset / Power down signal, Active Low, Internally Pulled UP 47k | |
| 9 | GPIO.0 | GPIO.0 | |
| 10 | DISP_AUDIO | Display audio in/out | |
| 11 | GPIO.1/IO.2 | SPI Single/Dual mode: General purpose IO0. QSPI mode: SPI data line 2 | |
| 12 | GPIO.2/IO.3 | SPI Single/Dual mode: General purpose IO1. QSPI mode: SPI data line 3 | |
| 13 | NC | Not connected | |
| 14 | NC | Not connected | |
| 15 | NC | Not connected | |
| 16 | NC | Not connected | |
| 17 | BLVDD | Supply voltage for backlight | |
| 18 | BLVDD | Supply voltage for backlight | |
| 19 | BLGND | Backlight Ground, internally connected to GND | |
| 20 | BLGND | Backlight Ground, internally connected to GND | |

Note. Matched 20 pins, 0.5 mm pitch, FFC accessory: FFC0520150



9.2 P2 connector - Audio interface description

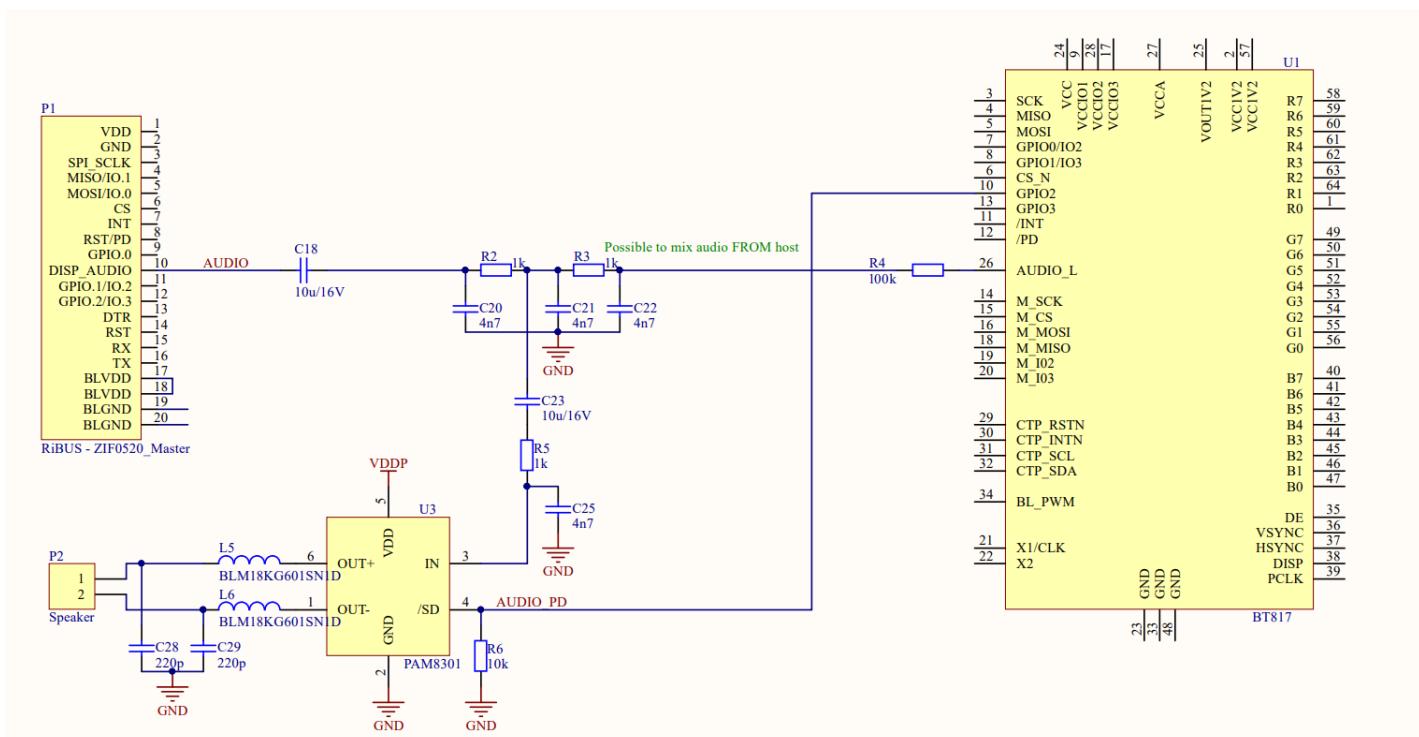
| PIN NO. | SYMBOL | DESCRIPTION | NOTE |
|---------|-----------|---------------------------|--------|
| 1 | SPEAKER + | Speaker coil "+" terminal | |
| 2 | SPEAKER - | Speaker coil "-" terminal | Note 1 |

The audio circuit allows for the following 3 modes:

1. To play sounds from BT817Q on internal amplifier U3.
2. To play sounds from host on internal amplifier U3.
3. To play sounds from BT817Q on external amplifier.

Note 1. Matched Riverdi louder speaker for all EVE4 series displays: RVA-SPK1.5W-C150

Figure 4. The simplified audio circuit design





10. BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

10.1 Serial host interface

Figure 5. SPI single/dual interface connection

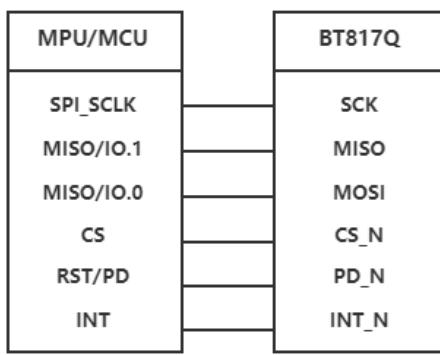
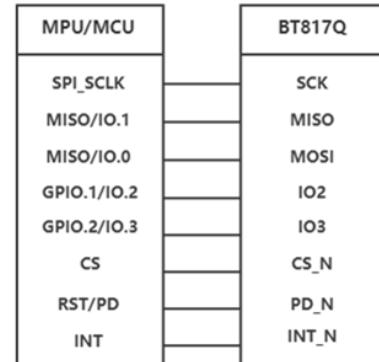


Figure 6. QSPI interface connection



SPI Interface – the SPI slave interface operates up to 30MHz

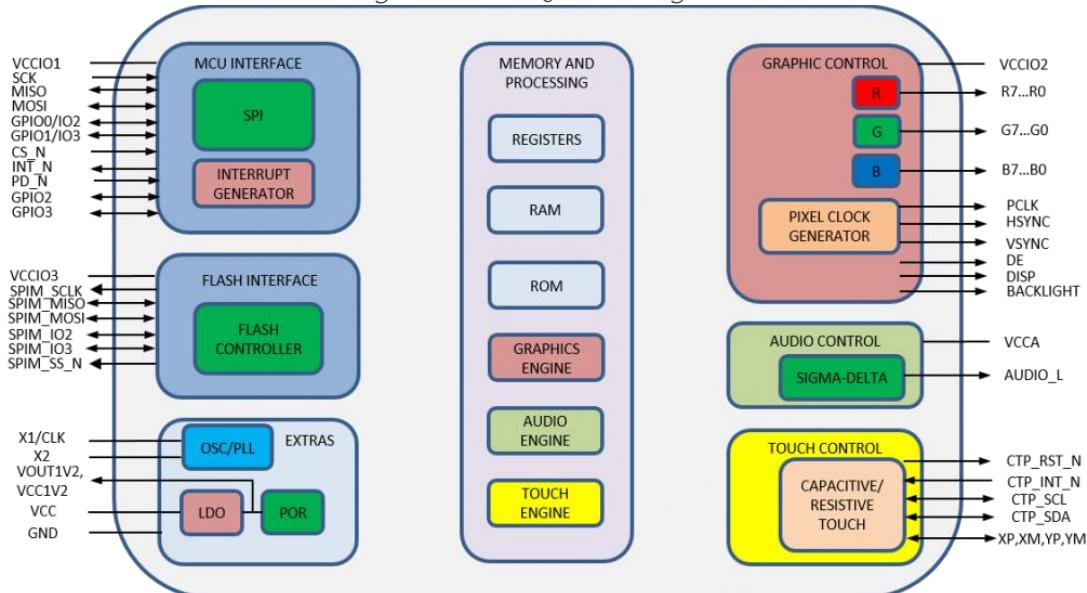
Only SPI mode 0 is supported. The SPI interface is selected by default.

QSPI Interface – the QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH.

10.2 Block diagram

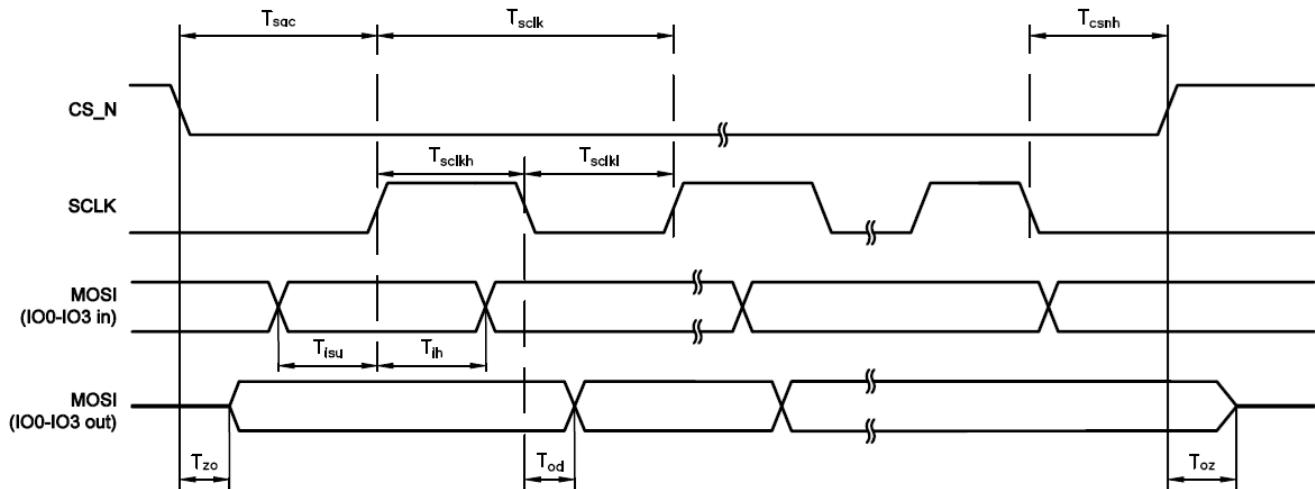
Figure 7. BT817Q Block diagram





10.3 Host interface SPI mode 0

Figure 8. SPI timing diagram



The meanings of the timings in the Figure 8 are defined in the table below.

| PARAMETER | DESCRIPTION | VCCIO=1.8V | | VCCIO=2.5V | | VCCIO=3.3V | | UNIT |
|-----------|-------------------------|------------|-----|------------|-----|------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| T_sclk | SPI clock period | 33.3 | - | 33.3 | - | 33.3 | - | ns |
| T_sclkl | SPI clock low duration | 13 | - | 13 | - | 13 | - | |
| T_sclkh | SPI clock high duration | 13 | - | 13 | - | 13 | - | |
| T_sac | SPI access time | 4 | - | 3.5 | - | 3 | - | |
| T_isu | Input Setup | 4 | - | 3.5 | - | 3 | - | |
| T_ih | Input Hold | 0 | - | 0 | - | 0 | - | |
| T_zo | Output enable delay | - | 16 | - | 13 | 11 | - | |
| T_oz | Output disable delay | - | 13 | - | 11 | 10 | - | |
| T_od | Output data delay | - | 15 | - | 12 | 11 | - | |
| T_csnh | CSN hold time | 0 | - | 0 | - | 0 | - | |

For more information about BT817Q controller please go to official BT81x website.

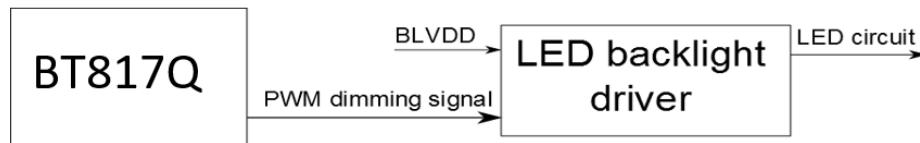
<https://brtchip.com/product/bt817/>

10.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. REG_PWM_HZ specifies the PWM output frequency. REG_PWM_DUTY specifies the duty cycle.

Refer to BT817Q datasheet for more information.

Figure 9. Backlight driver block diagram





The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED lifetime, as LED current peaks are reduced significantly.

11. 256Mb NOR FLASH MEMORY

The Riverdi EVE4 3.5" series modules are built with a 256Mb NOR flash memory chip. Graphics assets such as fonts, audio, and images can be stored in the flash memory. Up to 410 full resolution (320 * 240 pixels, JPG) images can be stored. If you need to change the memory size, please contact: contact@riverdi.com

There is an additional port P3 for programming the flash memory directly from an external source. This port is designed to be used during production if the customer wants to order pre-programmed EVE4 boards with graphic content of their own choice.

Cable TC2050-IDC-NL is compatible with P3 programming port.

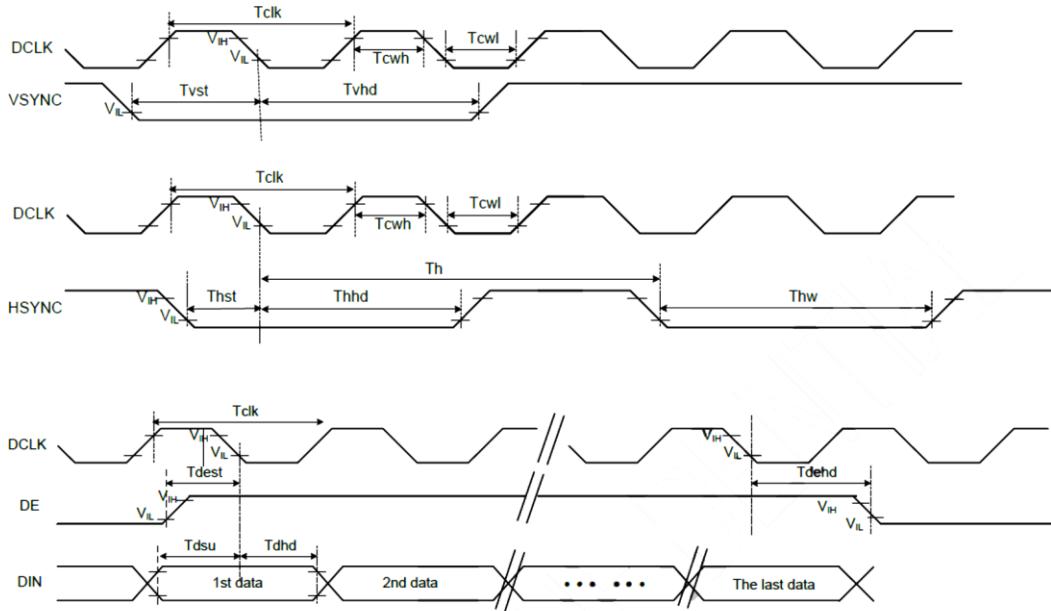
12. TIMING CHARACTERISTICS

12.1 Input setup timing setting

12.1.1 Parallel 24-bit RGB timing table

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | NOTE |
|----------------|----------------|-------------|-----|-----|------|---|
| DCLK Frequency | F_{clk} | 5 | 6 | 8 | MHz | |
| DCLK Period | T_{clk} | 125 | 167 | 200 | ns | |
| Hsync | Period Time | T_h | 325 | 371 | 438 | DCLK |
| | Display Period | T_{hdisp} | 320 | | | DCLK |
| | Back Porch | T_{hbp} | 3 | 43 | 43 | DCLK SYNC mode back porch control by H_BLANKING [7:0] setting, Thbp= H_BLANKING [7:0] |
| | Front Porch | T_{hfp} | 2 | 8 | 75 | DCLK |
| | Pulse Width | T_{hw} | 2 | 4 | 43 | DCLK |
| Vsync | Period Time | T_v | 244 | 260 | 289 | Hsync |
| | Display Period | T_{vdisp} | 240 | | | Hsync |
| | Back Porch | T_{vbp} | 2 | 12 | 12 | Hsync SYNC mode back porch control by V_BLANKING [7:0] setting, Tvbp= V_BLANKING [7:0] |
| | Front Porch | T_{vfp} | 2 | 8 | 37 | Hsync |
| | Pulse Width | T_{vw} | 2 | 4 | 12 | Hsync |

12.2 System bus timing for RGB interface



| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|------------------|------------|-----|-----|-----|------|
| CLK Pulse Duty | T_{clk} | 40 | 50 | 60 | % |
| HSYNC Width | T_{hw} | 2 | - | - | |
| HSYNC Period | T_h | 55 | 60 | 65 | |
| VSYNC Setup Time | T_{vst} | 12 | - | - | |
| VSYNC Hold Time | T_{vhhd} | 12 | - | - | |
| HSYNC Setup Time | T_{hst} | 12 | - | - | |
| HSYNC Hold Time | T_{hhhd} | 12 | - | - | |
| Data Setup Time | T_{dsu} | 12 | - | - | |
| Data Hold Time | T_{dhd} | 12 | - | - | |
| DE Setup Time | T_{dest} | 12 | - | - | |
| DE Hold Time | T_{dehd} | 12 | - | - | |

13. CAPACITIVE TOUCH SCREEN PANEL SPECIFICATIONS

13.1 Mechanical characteristics

| DESCRIPTION | SPECIFICATION | REMARK |
|--------------------------|---------------------|--------|
| Touch Panel Size | 3.5 inch | aTouch |
| Outline Dimension of CTP | 76.70 mm x 63.70 mm | |
| Product Thickness | 2.15 mm | |
| Glass Thickness | 1.1 mm | |
| CTP View Area | 70.68 mm x 53.16 mm | |
| Sensor Active Area | 72.08 mm x 54.56 mm | |
| Structure type | Glass + Glass | |
| Surface Hardness | 7H | |



13.2 Electrical characteristics

| DESCRIPTION | SPECIFICATION | NOTE |
|-------------------------|---------------|------|
| Power Consumption (IDD) | 60 mA | |
| Linearity | +/-1.5mm | |
| Controller | ILI2132A | |
| Resolution | 320 x 240 | |

14. MODULE INITIALIZATION

1. There is no need to set touch calibration matrix (REG_TOUCH_TRANSFORM_A-F registers in BT817Q) as touch panel resolution and orientation are the same as display, so default values in BT817Q are correct.
2. Initialization data, timings and example codes are available on the Riverdi GitHub, at address: <https://github.com/riverdi/riverdi-eve>
3. REGISTER VALUES:

| REGISTER NAME | REGISTER VALUE (DEC.) |
|---------------|-----------------------|
| REG_HSIZE | 320 |
| REG_VSIZE | 240 |
| REG_HCYCLE | 371 |
| REG_HOFFSET | 43 |
| REG_HSYNC0 | 0 |
| REG_HSYNC1 | 4 |
| REG_VCYCLE | 260 |
| REG_VOFFSET | 12 |
| REG_VSYNC0 | 0 |
| REG_VSYNC1 | 4 |
| REG_PCLK | 1 |
| REG_SWIZZLE | 0 |
| REG_PCLK_POL | 1 |
| REG_CSPREAD | 0 |
| REG_DITHER | 0 |
| REG_PCLK_FREQ | 34 (0x22) |
| REG_PCLK_2X | 0 |

15. INSPECTION

Standard acceptance/rejection criteria for TFT module

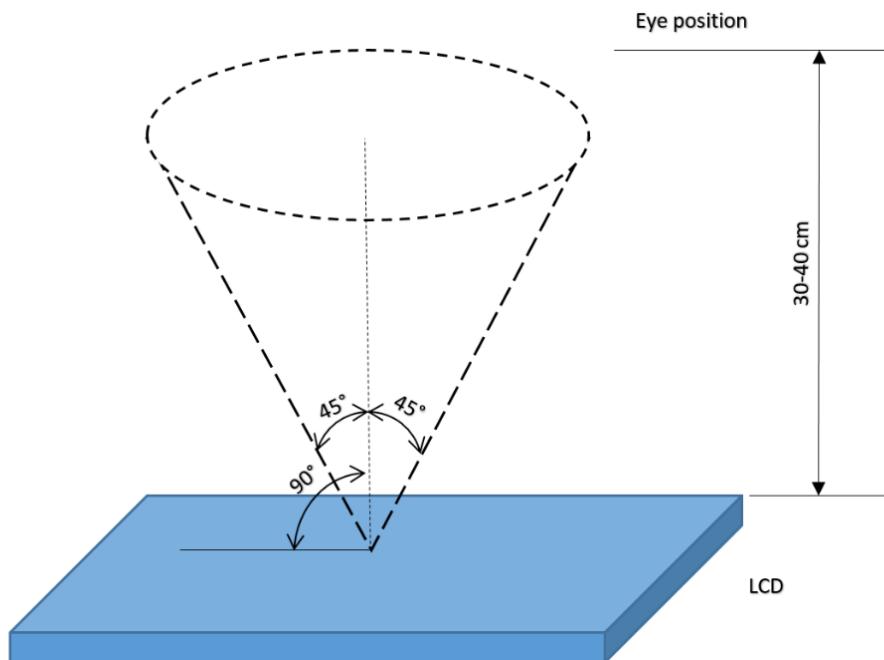
15.1 Inspection condition

Ambient conditions:

- Temperature: $25 \pm 2^\circ\text{C}$
- Humidity: $(60 \pm 10) \% \text{RH}$
- Illumination: Single fluorescent lamp non-directive (300 to 700 lux)

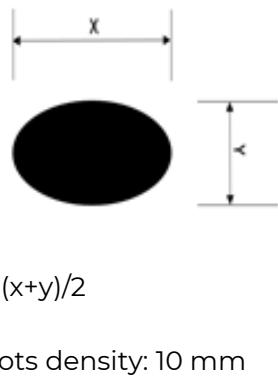
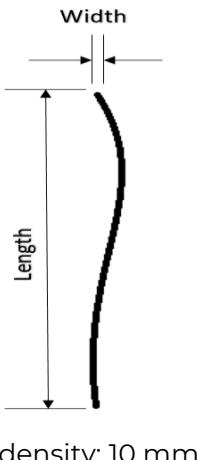
Viewing distance: $35 \pm 5\text{cm}$ between inspector bare eye and LCD.

Viewing Angle: U/D: $45^\circ/45^\circ$, L/R: $45^\circ/45^\circ$





15.2 Inspection standard

| ITEM | CRITERION | | | |
|--|--|---|----------------------|---------------|
| Black spots, white spots, light leakage, Foreign Particle (round Type) |  $D = \frac{x+y}{2}$ Spots density: 10 mm | $3.5'' \leq \text{Size} \leq 5''$ | | |
| | | Average Diameter | | Qualified Qty |
| | | $D \leq 0.15 \text{ mm}$ | | Ignored |
| | | $0.15 \text{ mm} < D \leq 0.3 \text{ mm}$ | | $N \leq 3$ |
| | | $0.3 \text{ mm} < D$ | | Not allowed |
| LCD black spots, white spots, light leakage (line Type) |  Spots density: 10 mm | $3.5'' \leq \text{Size} \leq 5''$ | | |
| | | Length | Width | Qualified Qty |
| | | - | $W \leq 0.03$ | Ignored |
| | | $L \leq 3.0$ | $0.03 < W \leq 0.05$ | 2 |
| | | $L \leq 3.0$ | $0.05 < W \leq 0.1$ | 1 |
| | | $3.0 < L$ | $0.1 < W$ | Not allowed |
| Bright/Dark Dots | $3.5'' \leq \text{Size} \leq 5''$ | | | |
| | Item | Qualified Qty | | |
| | Bright dots | $N \leq 1$ | | |
| | Dark dots | $N \leq 2$ | | |
| | Total Bright and Dark Dots | $N \leq 3$ | | |
| Clear spots | $\text{Size} < 5.0''$ | | | |
| | Average Diameter | Qualified Qty | | |
| | $D < 0.2 \text{ mm}$ | Ignored | | |
| | $0.2 \text{ mm} < D < 0.3 \text{ mm}$ | 3 | | |
| | $0.3 \text{ mm} < D < 0.5 \text{ mm}$ | 2 | | |
| | $0.5 \text{ mm} < D$ | 0 | | |
| | Spots density: 10 mm | | | |
| Polarizer bubbles | $3.5'' \leq \text{Size} \leq 5''$ | | | |
| | Average Diameter | Qualified Qty | | |
| | $D \leq 0.2 \text{ mm}$ | Ignored | | |
| | $0.2 \text{ mm} < D \leq 0.3 \text{ mm}$ | 2 | | |
| | $0.3 \text{ mm} < D \leq 0.5 \text{ mm}$ | 1 | | |
| | $0.5 \text{ mm} < D$ | 0 | | |
| | Total Q'ty | 3 | | |
| Touch panel spots | $\text{Size} < 5.0''$ | | | |
| | Average Diameter | Qualified Qty | | |



| | | |
|--------------------------------|---------------------|-----------------|
| | D < 0.2 mm | Ignored |
| | 0.2 mm < D < 0.4 mm | 5 |
| | 0.4 mm < D < 0.5 mm | 2 |
| | 0.5 mm < D | 0 |
| Touch panel white line scratch | | Size < 5.0" |
| | Length | Width |
| | - | W < 0.02 |
| | L < 3.0 | 0.02 < W < 0.05 |
| | L < 2.5 | 0.05 < W < 0.08 |
| | - | 0.08 < W |
| | | 0 |
| | | |
| | | |

16. RELIABILITY TEST

| NO. | TEST ITEM | TEST CONDITION | NOTE |
|-----|-------------------------------------|--|--------|
| 1 | High Temperature Storage | 80°C/120 hours | Note 1 |
| 2 | Low Temperature Storage | -30°C/120 hours | |
| 3 | High Temperature Operating | 70 °C /120 hours | |
| 4 | Low Temperature Operating | -20°C/120 hours | |
| 5 | High Temperature and High Humidity | Humidity 40°C, 90%RH, 120Hrs | |
| 6 | Thermal Cycling Test (No operation) | -20°C for 30min, 70°C for 30 min. 100 cycles. Then test at room temperature after 1 hour | Note 2 |
| 7 | Vibration Test | Frequency: 10 ÷ 55 Hz. Stroke: 1.5 mm. Sweep: 10Hz ÷ 55Hz ÷ 10 Hz. 2 hours for each direction of X, Y, Z (Total 6 hours) | |
| 8 | Package Drop Test | Height: 60 cm 1 corner, 3 edges, 6 surfaces | |

Note 1. Sample quantity for each test item is 5 ÷ 10 pcs.

Note 2. Before running cosmetic and function tests, the product must have enough recovery time, at least 2 hours at room temperature.



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