Features

- Supports Cypress’s Ultra37000™ and Ultra37000V™ families of products
- STAPL (Chain Dependent and Chain Independent) programming language support
- SVF programming language support
- Standard JTAG programming interface
- Multi-device programming
- Eliminates programming insertion to improve manufacturing efficiency
- For programming in the lab, on manufacturing floor, or at remote sites
- ATE support via STAPL on industry leading ATE platforms

CYUSBIRPC Kit Contents

- USBISR Programming Cable for use with Ultra37000 and Ultra37000V™ families of products
- CY ISR4.0.1 Software Installation CD

Functional Description

The CYUSBISRPC Programming Cable enables users to program Ultra37000 and Ultra37000V CPLDs on board with our ISR Programming Software, and a personal computer. The USBISR Programming Cable connects to a USB 1.1/USB 2.0 port of a PC into a standard 10-pin male connector mounted on the user’s board. The ISR software provides an easy-to-use Graphical User Interface that accepts JEDEC or hex files as input. The JEDEC/.hex files are used to compose platform independent STAPL/SVF files. STAPL/SVF files contain all the information needed to program the device. The ISR software is used to define how many devices are in the daisy chain and what operation is to be done on each Cypress device. The same chain can be used with other JTAG-compliant devices.

The ISR User’s Guide describes the operation of the ISR software. The application notes included in the software installation CD describe all system design considerations for programming with this Programming Cable.

10-pin Programming Connector

The view looking into the end of the 10-pin ISR cable is shown below.

In-System Reprogrammable™ (ISR™) Programming with CYUSBISRPC cable
Table 1 describes the function of each of these pins on the USBISR Programming Cable. An OUTPUT is provided by the PC and an INPUT is provided by the target system.

### Male Connector Specifications

<table>
<thead>
<tr>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTAGen</td>
<td>OUTPUT</td>
<td>In System Reprogramming JTAG Enable (active HIGH).</td>
</tr>
<tr>
<td>ISR*</td>
<td>OUTPUT</td>
<td>In System Reprogramming Enable Indicator (active LOW).</td>
</tr>
<tr>
<td>VCC</td>
<td>INPUT</td>
<td>+5V and +3.3V Supply Voltage provided from the target system to the cable.</td>
</tr>
<tr>
<td>TDO</td>
<td>INPUT</td>
<td>Test Data Output Receiver. The TDO output pin of the last device in the ISR chain is connected to this input pin.</td>
</tr>
<tr>
<td>TMS</td>
<td>OUTPUT</td>
<td>Test Mode Control. This is the mode select control input for the TAP controller state machine contained in the ISR interface.</td>
</tr>
<tr>
<td>TCK</td>
<td>OUTPUT</td>
<td>Test Clock. ISR interface clock.</td>
</tr>
<tr>
<td>TDI</td>
<td>OUTPUT</td>
<td>Test Data Input Driver. This output pin is connected to the TDI input of the first device in the ISR chain.</td>
</tr>
<tr>
<td>NC</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>Zero volt common ground for PC and target system.</td>
</tr>
</tbody>
</table>

**Table 1. USBISR Cable Pin Descriptions**

PC System Requirements

- IBM PC or compatible running Windows 98, Windows 98 Second Edition, Windows ME, Windows NT 4.0 Service Pack 5 or later or Windows 2000 Service Pack 1 or later and Windows XP.
- One free parallel, USB 1.1 or 2.0 (recommended) port
- A minimum of 32 MB of RAM.
- Approximately 30 MB of free hard disk space.

Ordering Information

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYUSBIRPC</td>
<td>CYUSBISRPC Programming Cable</td>
</tr>
</tbody>
</table>

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