S6BP203A

ASSP, 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC

S6BP203A is a 1ch Buck-boost DC/DC converter IC with four built-in switching FETs. This IC is able to supply up to 2.4A of load current within the very wide range from 2.5V to 42V in the input voltage. This IC has an operation mode that is automatically changed to PFM operation during low load, which can achieve super-high efficiency with a very low quiescent current 50 µA. It is possible to provide stable output voltage from an automotive cold cranking and load dump, up to 42V, conditions within 1 ms transition time. As a result, this IC is suitable for power supply solutions of automotive and Industrial applications. This IC has the SYNC function, which is capable of selecting the SYNC_IN that is able to inputs an external clock signal. When an external clock signal in the range from 200 kHz to 400 kHz is inputted, the FETs perform the switching operation with synchronizing signal from an external clock. When an external clock signal is not inputted, the FETs perform the switching operation from an internal clock. The internal clock signal in the range from 200 kHz to 2.1 MHz can be set by an external resistor. Since external voltage setting resistors and phase compensation capacitors are not required with this IC, it can reduce the number of parts and a part mounting area. This IC has five protection functions, input under voltage lockout (input UVLO), output under voltage protection (output UVP), output over voltage protection (output OVP), output over current protection (output OCP), and thermal shutdown (TSD). Moreover, this IC has the power good (PG) function that indicates the state of the output voltage (VOUT pin). When the output voltage reaches the PG voltage, the PG signal is outputted.

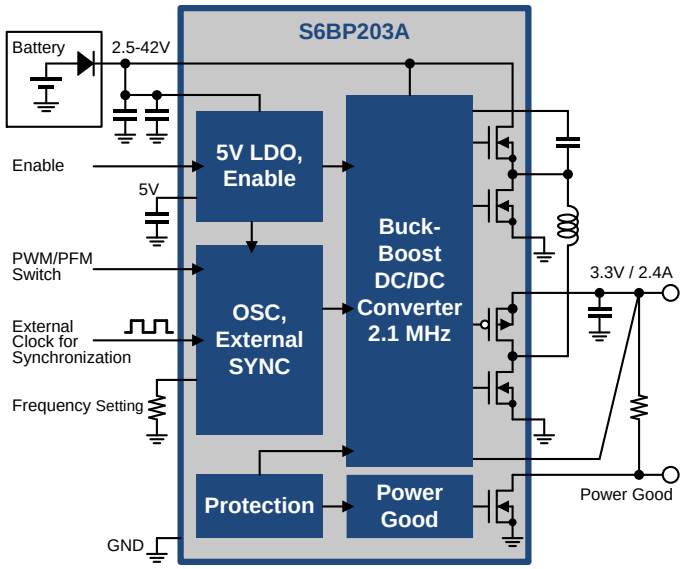
Features

- Wide input voltage range: 2.5V to 42V
- Output voltage: 3.3V
- Wide operating frequency range: 200 kHz to 2.1 MHz
- External synchronized clock range: 200 kHz to 400 kHz
- SYNC function
  - SYNC_IN: External clock input
    (Unless inputting clock, this IC operates by internal clock)
- Super-high efficiency by PFM operation
  (When setting MODE pin to a low level)
- Automatic PWM/PFM switching operation and fixed PWM operation are selectable by MODE pin
- Built-in switching FET
- Synchronous current mode architecture
- Shutdown current: Lower than 1 µA
- Quiescent current: 50 µA
- Power Good Monitor
  - Output voltage monitoring by window comparator
  - Power-on reset time: 14 ms
- Soft start time without load dependence: 0.9 ms
  (When switching frequency = 2.1 MHz)
- Enhanced protection functions
  - Input under voltage lockout
  - Output under voltage protection: 92.0%
  - Output over voltage protection: 108.0%
  - Output over current protection
  - Thermal shutdown
- Small TSSOP16 package (exposed PAD): 5 mm × 6.4 mm
- AEC-Q100 compliant (Grade-1)

Applications

- Advanced driver assistance systems (ADAS)
- Instrument cluster
- Automotive applications
- Industrial applications

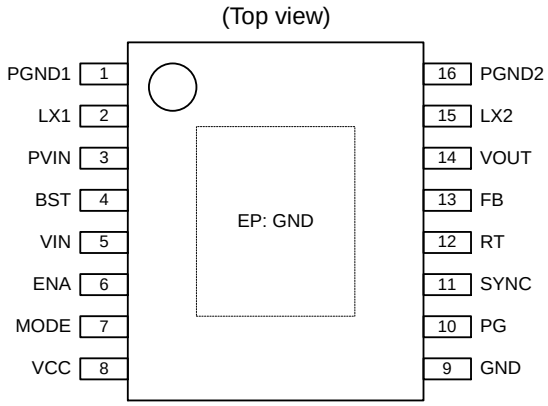
Block Diagram



Contents

1. Pin Assignment

Figure 1-1 Pin Assignment

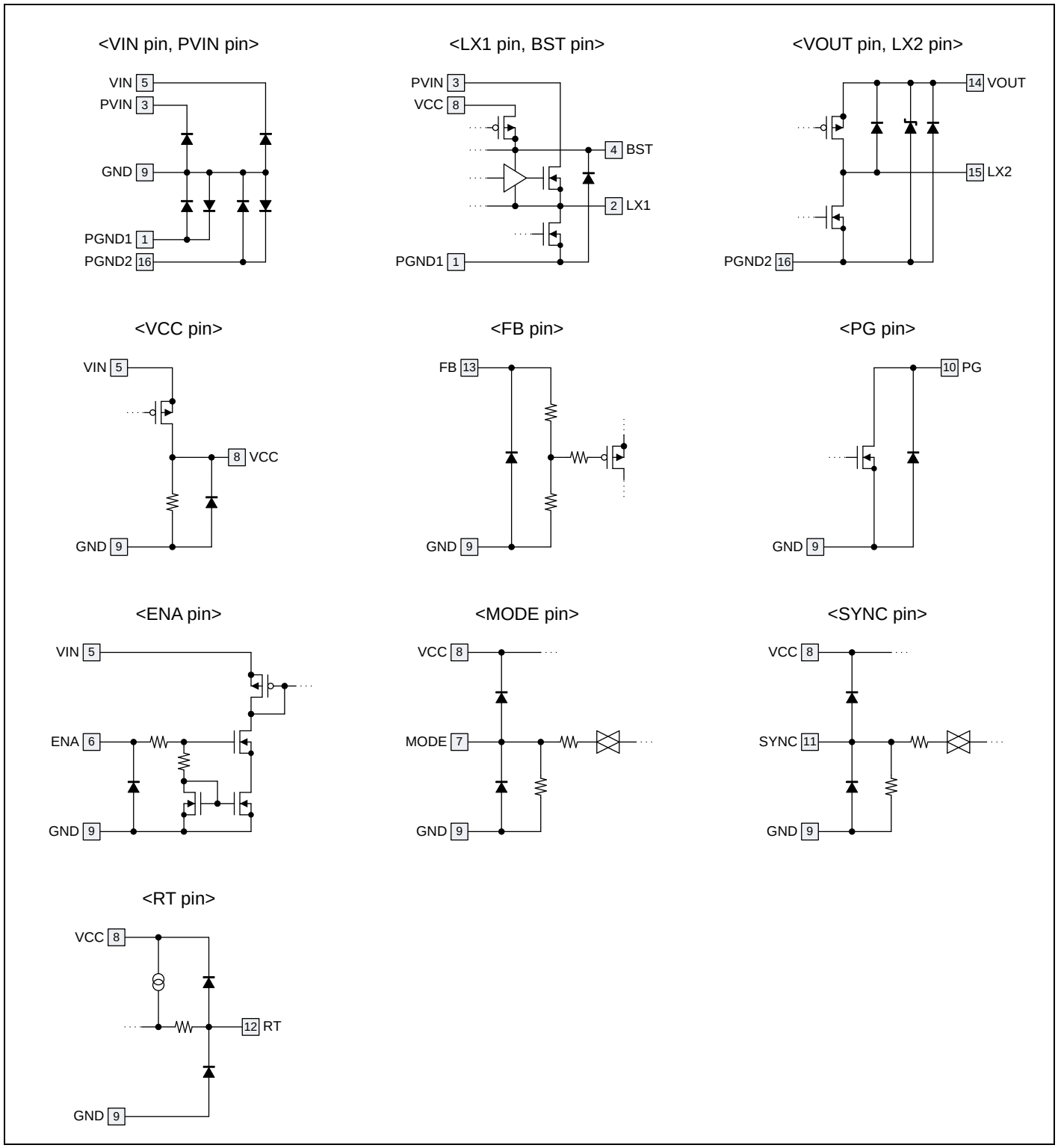


2. Pin Descriptions

Table 2-1 Pin Descriptions

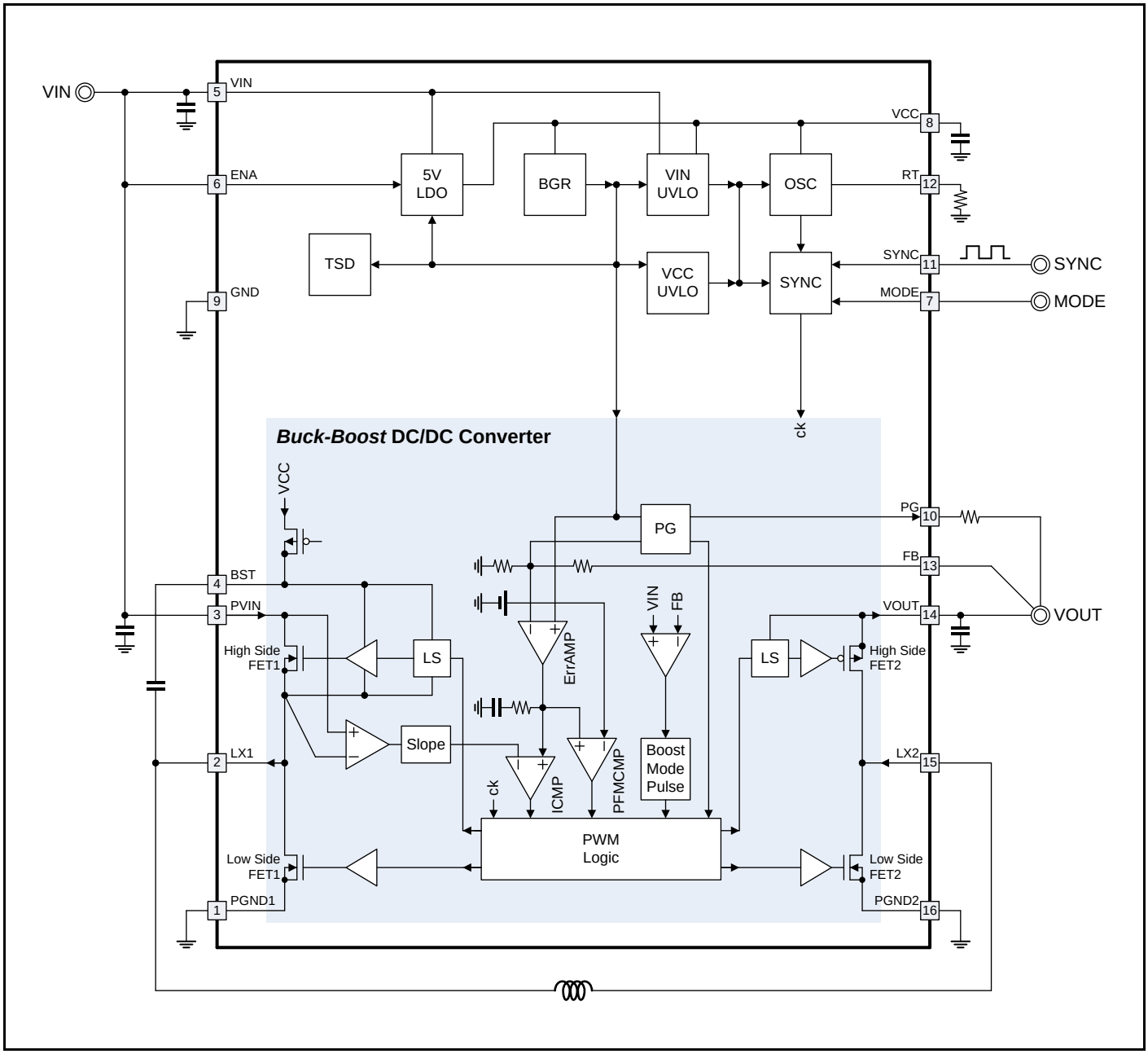
Pin No.	Pin Name	I/O	Description
1	PGND1	−	GND pin for built-in switching FET
2	LX1	O	Inductor connection pin
3	PVIN	I	Power supply pin for PWM controller and switching FETs
4	BST	I	BST(Boost) capacitor connection pin
5	VIN	I	Power supply pin
6	ENA	I	DC/DC converter enable pin
7	MODE	I	PWM/PFM operation control pin For the MODE pin setting, refer to "9.1 Setting the Operation Conditions"
8	VCC	O	VCC capacitor connection pin LDO output pin of Internal reference voltage
9	GND	−	GND pin
10	PG	O	Open drain output pin for power good When being used, connect PG pin to VOUT pin. When not being used, leave PG pin open.
11	SYNC	I	External clock input pin. For the SYNC pin setting, refer to "9.1 Setting the Operation Conditions"
12	RT	O	Timing resistor connection pin for internal clock (switching frequency) For the resistance, refer to "9.1 Setting the Operation Conditions"
13	FB	I	Output voltage feedback pin
14	VOUT	O	DC/DC converter output pin
15	LX2	O	Inductor connection output pin.
16	PGND2	−	GND pin for built-in switching FET
EP	GND	−	GND pin

Figure 2-1 I/O Pin Equivalent Circuit Diagram



3. Architecture Block Diagram

Figure 3-1 Architecture Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V_{VIN}	VIN pin	−0.3	+48.0	V
	V_{PVIN}	PVIN pin	−0.3	+48.0	V
	V_{VCC}	VCC pin	−0.3	+6.9	V
Terminal voltage(*1)	V_{BST}	BST pin	−0.3	+48.0	V
	V_{LX1}	LX1 pin	−2.0	+48.0	V
	V_{LX2}	LX2 pin	−2.0	+6.9	V
	V_{FB}	FB pin	−0.3	V_{VCC}	V
	V_{RT}	RT pin	−0.3	V_{VCC}	V
	V_{MODE}	MODE pin	−0.3	V_{VCC}	V
	V_{SYNC}	SYNC pin	−0.3	V_{VCC}	V
	V_{ENA}	ENA pin	−0.3	+48.0	V
	V_{PG}	PG pin	−0.3	+6.9	V
Difference voltage(*1)	V_{BST-LX}	Between BST–LX1 pins	−0.3	+6.9	V
	V_{GND}	Between GND–PGND1 pins, Between GND–PGND2 pins	−0.3	+0.3	V
PG output current	I_{PG}	PG pin	−3	0	mA
Power dissipation (*1)	P_D	Ta ≤ ±25°C	0	3324 (*2)	mW
Storage temperature	T_{STG}	−	−55	+150	°C

*1: When PGND1 = PGND2 = GND = 0V

*2: When the product is mounted on 76.2 mm × 114.3 mm, four-layer FR-4 board

Warning:

1. *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

5. Recommended Operating Conditions

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Power supply voltage (*1)	V_{VIN}	VIN pin	At start-up	5.0	12.0	42.0	V
			After start-up	2.5	12.0	42.0	V
Terminal voltage (*1)	V_{BST}	BST pin		0.0	−	47.5	V
	V_{LX1}	LX1 pin		−1.0	+12.0	+42.0	V
	V_{LX2}	LX2 pin		−1.0	−	+5.5	V
	V_{FB}	FB pin		0.0	−	5.5	V
	V_{MODE}	MODE pin		0.0	−	5.5	V
	V_{SYNC}	SYNC pin		0.0	−	5.5	V
	V_{ENA}	ENA pin		0.0	12.0	42.0	V
	V_{PG}	PG pin		0.0	−	5.5	V
Difference voltage(*1)	$V_{BST-LX1}$	Between BST−LX1 pins		0.0	−	5.5	V
	V_{GND}	Between GND−PGND1 pins, Between GND−PGND2 pins		−0.05	0.00	+0.05	V
PG output current	I_{PG}	PG pin (sink current)		0	−	1	mA
BST capacitance	C_{BST}	Between BST−LX1 pins		0.068	0.100	0.470	µF
VCC capacitance	C_{VCC}	Between VCC−GND pins		2.2	4.7	10.0	µF
Timing resistance	R_{RT}	Between RT−GND pins. When using internal clock		22	−	270	kΩ
Operating ambient Temperature	Ta	−		−40	+25	+125	°C

*1: When PGND1 = PGND2 = GND = 0V

Warning:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

6. Electrical Characteristics

VIN=PVIN=12V, ENA=5V

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Buck-boost DC/DC converter Block	VOUT output voltage	V_{VOUT}	I_{VOUT} = 0A	3.251	3.300	3.349	V
	FB input resistance	R_{FB}	EN = 0V, Ta = +25°C	2.53	3.17	3.80	MΩ
	Switching FET on-resistance	$R_{HSIDEFET1}$	LX1 = −30 mA (Between PVIN−LX1)	−	150	−	mΩ
		$R_{LSIDEFET1}$	LX1 = 30 mA (Between LX1−PGND1)	−	150	−	mΩ
		$R_{HSIDEFET2}$	LX2 =−30 mA (Between VOUT−LX2)	−	150	−	mΩ
		$R_{LSIDEFET2}$	LX2 = 30 mA (Between LX2−PGND2)	−	150	−	mΩ
	Switching FET leakage current	I_{LEAK}	−	−	−	5	µA
	Soft-start time	T_{SS}	R_{RT} = 22 kΩ	0.855	0.9	0.945	ms
	Maximum output current	I_{VOUT}	PVIN ≥ 7.5V, Ta = 25°C	2.4 (*1)	−	−	A
			PVIN = 4.5V, Ta = 25°C	1.0 (*1)	−	−	A
	Current limit	I_{LIMT}	PVIN = 12V, L = 2.2µH	2.4 (*1)	−	−	A
5V LDO block	VCC output voltage	V_{VCC}	VIN = 12V	4.9	5.0	5.1	V
VIN UVLO block	VIN UVLO falling threshold	$V_{UVLOVINHL}$	VIN input voltage when falling	2.30	2.40	2.50	V
	VIN UVLO rising threshold	$V_{UVLOVINLH}$	VIN input voltage when rising	4.55	4.75	4.95	V
VCC UVLO block	VCC UVLO falling threshold	$V_{UVLOVCCHL}$	VCC input voltage when falling	2.30	2.40	2.50	V
	VCC UVLO rising threshold	$V_{UVLOVCCLH}$	VCC input voltage when rising	4.55	4.75	4.95	V
ENA pin	Enable condition	V_{ENA}	Enable voltage range	1.10	−	V_{VIN}	V
		V_{DSB}	Disable voltage range	0.0	−	0.2	V
	ENA input current	I_{ENA}	V_{ENA} = 12V	−	1	3	µA
MODE pin	MODE input voltage	V_{MODE_L}	Automatic PWM/PFM switching operation	0.0	−	0.4	V
		V_{MODE_H}	Fixed PWM mode	2.0	−	V_{VOUT}	V
	MODE Input current	I_{MODE}	MODE = 5.0V	−	5	10	µA
OSC block	Switching frequency	F_{OSC}	R_{RT} = 22 kΩ	2.0	2.1	2.2	MHz
			R_{RT} = 270 kΩ	180	200	220	kHz
SYNC block (SYNC_IN)	SYNC input threshold	V_{SYNC_L}	−	0.0	−	0.4	V
		V_{SYNC_H}	−	2.0	−	V_{VOUT}	V
	SYNC input frequency	V_{SYNC_L}	−	200	−	400	kHz
	SYNC input duty ratio	V_{SYNC_H}	−	+20	+50	+80	%
	SYNC leakage current	I_{LKSYNC}	V_{SYNC} = 5.0V	−	5	10	µA
PG block (UVP, OVP)	VOUT UVP falling threshold	P_{GUVPHL}	Falling threshold for output voltage	90.5	92.0	93.5	%
	VOUT UVP rising threshold	P_{GUVPLH}	Rising threshold for output voltage	91.5	93.0	94.5	%
	VOUT OVP rising threshold	P_{GOVPLH}	Rising threshold for output voltage	106.5	108.0	109.5	%
	VOUT OVP falling threshold	P_{GOVPHL}	Falling threshold for output voltage	105.5	107.0	108.5	%
	Leak current	I_{LKPG}	V_{PWRGD} = 5.0V, V_{ENA} = 0V	0	−	1	µA
	Low level output voltage	V_{OLPG}	I_{PGSINK} = 1 mA	0.025	0.05	0.15	V
	Delay time at abnormal detection	T_{PPG}	At power shutdown	−	7 (*1)	12 (*1)	µs
	Power-on reset time	T_{RPG}	At power good	9.1	14.0	18.9	ms
Thermal shutdown block (TSD)	Shutdown temperature	T_{TSDH}	−	−	165 (*1)	−	°C
		T_{TSDL}	Hysteresis	−	10 (*1)	−	°C
Supply current	Shutdown current	I_{VINSDN}	VIN input current, V_{ENA} = 0V	−	1	5	µA
	Quiescent current	I_{VINQ}	VIN input current, V_{ENA} = 12V, I_{VOUT} = 0A, MODE/SYNC/PG Pins = OPEN	−	50	70	µA

*1: The electrical characteristic is ensured by statistical characterization and indirect tests.

7. Functional Description

7.1 Block Description

Input Under Voltage Lockout (Input UVLO)

The input UVLO is the function that prevents a malfunction of this IC from the following status, and protects poststage devices.

- Transitional state at start-up
- Momentary drop of power supply voltage

To prevent such a malfunction, this protection monitors the VIN input voltage and VCC voltage. When either VIN or VCC voltage falls to the UVLO falling threshold, 2.4V (Typ), or lower, the IC stops the VOUT voltage output and becomes UVLO status. When both VIN and VCC voltages reach the UVLO rising threshold, 4.75V (Typ), or higher, the IC is released from the UVLO state and returns to the normal operation.

Output Under Voltage Protection (Output UVP)

The output UVP is the function that monitors the voltage drop of the VOUT pin and notifies by the PG pin.

When the output voltage falls to the UVP falling threshold (P_{GUVPHL}) for the output voltage setting or lower, the PG voltage is fixed to the low level. The IC becomes the UVP status, but the switching operation is maintained under the UVP status.

When the output voltage once again reaches the UVP rising threshold (P_{GUVPLH}) for the output voltage setting or higher, the IC is released from the UVP state and the PG voltage is fixed to the high level.

Output Over Voltage Protection (Output OVP)

The output OVP is the function that monitors the voltage rise of the VOUT pin and stops the switching operations, which protects poststate devices from overvoltage. Also, the VOUT state is notified by the PG pin.

When the output voltage rises to the OVP falling threshold (P_{GOVPLH}) for the output voltage setting or higher, the PG voltage is fixed to the low level. The IC becomes the OVP status, and the switching operations of the High-Side FETs are stopped. When the output voltage once again falls to the OVP falling threshold (P_{GOVPHL}) for the output voltage setting or lower, the IC is released from the OVP state and resumes the switching operations. The PG voltage is fixed to the high level again.

Output Over Current Protection (Output OCP)

The output OCP is the function that limits the excessive current load and protects poststage devices.

Thermal Shutdown (TSD)

The TSD is the function that protects the IC from heat-destruction. When the junction temperature reaches +165°C (Typ), the high-side and low-side switching FET are turned off and the IC becomes the TSD status. When the junction temperature once again falls to +155°C (Typ) or lower, the IC is released from the TSD state and restarts the power supply.

7.2 Protection Function Table

The following table shows the state of each pin when each protection function operates.

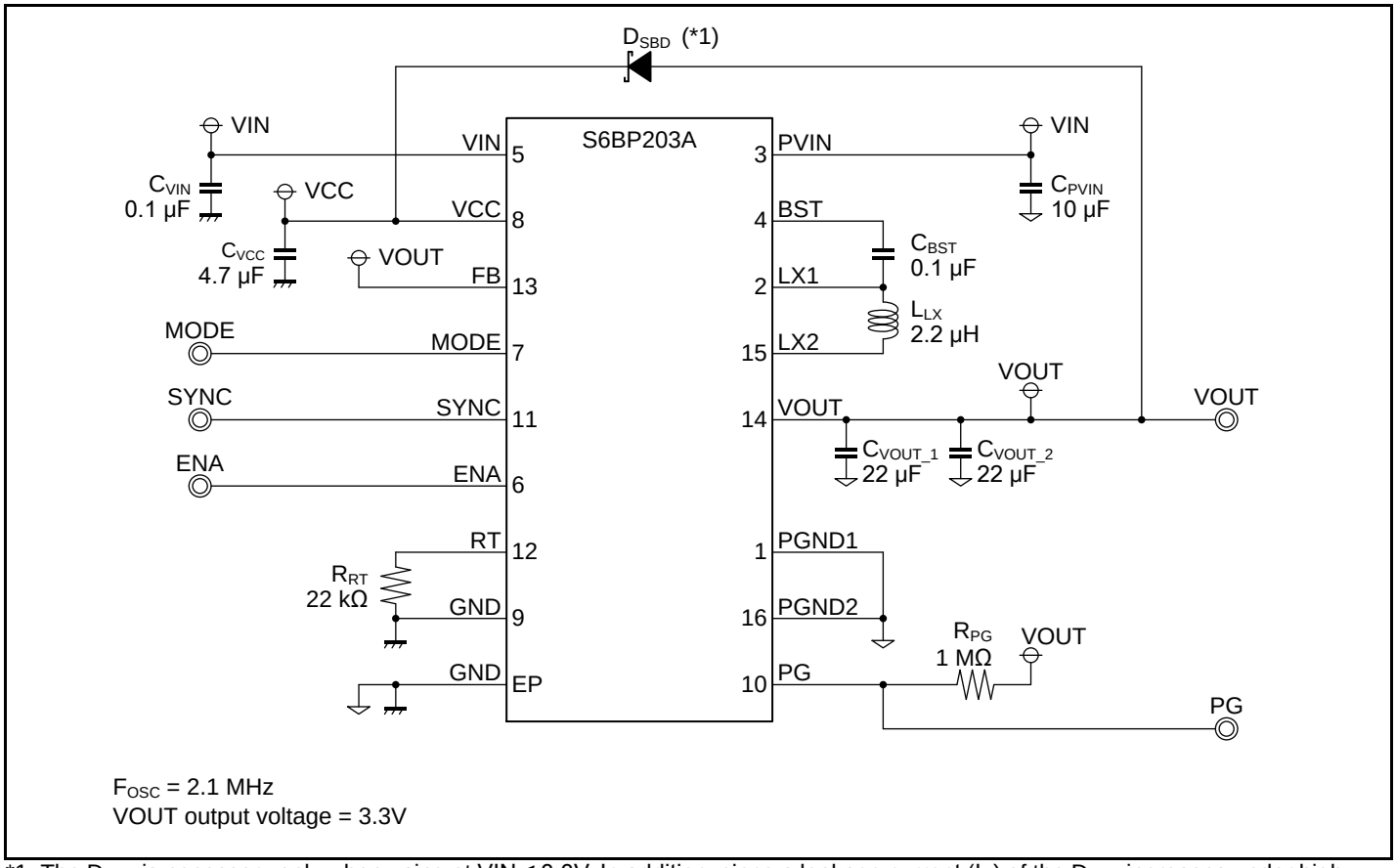
Table 7-1 Protection Function Table

Function	ENA Pin Setting	PG Pin Output	DC/DC Converter Operation	Remarks
Shutdown operation	L	Hi-Z (*1)	Shutdown	It is recommended to connect PG pin to VOUT pin via a pull-up resistor. When setting ENA pin to a low level, VOUT pin voltage drops to 0V. Therefore, PG pin outputs 0V.
Nominal operation	H	Hi-Z (*1)	Switching	–
Input under voltage protection (Input UVLO)	H	L	Shutdown	After releasing UVLO state, this IC is automatically reset with soft start.
Output under voltage protection (Output UVP)	H	L	Switching	–
Output over voltage protection (Output OVP)	H	L	Shutdown	–
Output over current protection (Output OCP)	H	L	Switching	OCP operates to drop the output voltage.
Thermal shutdown (TSD)	H	L	Shutdown	After releasing TSD state, this IC is automatically reset with soft start.

*1: PG pin is formed as an open drain structure. The internal MOSFET is in the OFF state.

8. Application Circuit Example and Parts list

Figure 8-1 Application Circuit Example



*1: The D_{SBD} is necessary only when using at VIN ≤ 3.3V. In addition, since a leakage current (I_R) of the D_{SBD} increases under high temperature, it is necessary to connect a load according to the leakage current of the D_{SBD} to VOUT pin under the automatic PWM/PFM switching operation (MODE = L, SYNC = L).

Table 8-1 Parts List

Symbol	Item	Value	Part Number	Vendor	Package Size (W×L×H[mm])	Remarks
C_{VIN}, C_{BST}	Ceramic capacitor	0.1 µF	CGA2B3X7R1H104K050BB	TDK	1.0×0.5×0.5	X7R, Rated Voltage: 50 Vdc
C_{PVIN}	Ceramic capacitor	10 µF	CGA9N3X7R1H106K230KB	TDK	5.7×5.0×2.3	X7R, Rated Voltage: 50 Vdc
C_{VCC}	Ceramic capacitor	4.7 µF	CGA4J3X7R1C475K125AB	TDK	2.0×1.25×1.25	X7R, Rated Voltage: 16 Vdc
C_{VOUT_1}, C_{VOUT_2}	Ceramic capacitor	22 µF	CGA6P1X7R1C226M250AC	TDK	3.2×2.5×2.5	X7R, Rated Voltage: 16 Vdc
L_{LX}	Inductor	2.2 µH	CLF7045T-2R2N-D	TDK	7.2×6.9×4.5	DCR: 14.6 mΩ, I_{DC_MAX}: 5.5A
R_{RT}	Resistor	22 kΩ	RK73H1JTTD2202F	KOA	0.8×1.6×0.45	–
R_{PG}	Resistor	1 MΩ	RK73H1JTTD1004F	KOA	0.8×1.6×0.45	–
D_{SBD}	Schottky barrier diode	–	MBR140SF	ON	1.65×2.7×0.95	–

TDK: TDK Corporation
KOA: KOA Corporation
ON: ON Semiconductor Corporation

9. Application Note

9.1 Setting the Operation Conditions

Operation State of DC/DC Convertor

The operation stage of DC/CD converter is set by both MODE pin and SYNC pin.

Table 9-1 Operation State of DC/DC Convertor

MODE Pin	SYNC Pin (Signal Input)	Operation State of DC/DC Convertor
L (*3)	L (*3)	Automatic PWM/PFM switching operation from an internal clock
	External clock input (*5)	Fixed PWM operation with synchronizing signal from an external clock (*2)
	H (*4)	Prohibition of use (*1)
H (*4)	L (*3)	Fixed PWM operation from an internal clock
	External clock input (*5)	Fixed PWM operation with synchronizing signal from an external clock (*2)
	H (*4)	Prohibition of use (*1)

*1: When setting SYNC pin to a high level, the quiescent current (I_{VINQ}) is increased.
*2: Set the timing resistance (R_{RT}) to 330 kΩ.
*3: Apply the GND1 or GND2 voltage.
*4: Apply the VOUT voltage.
*5: Apply the VOUT voltage at a high level. Apply the GND1 or GND2 voltage at a low level

Setting of Switching Frequency (Internal Clock)

The switching frequency (internal clock) can be set by RT resistor, which value is the timing resistance (R_{RT}), connected to RT pin. Set the timing resistance in a range within the Figure 9-1. The switching frequency is also limited by VIN input voltage. Set the switching frequency in a range within the Figure 9-2.

Figure 9-1 F_{OSC} vs R_{RT} Measured Characteristic

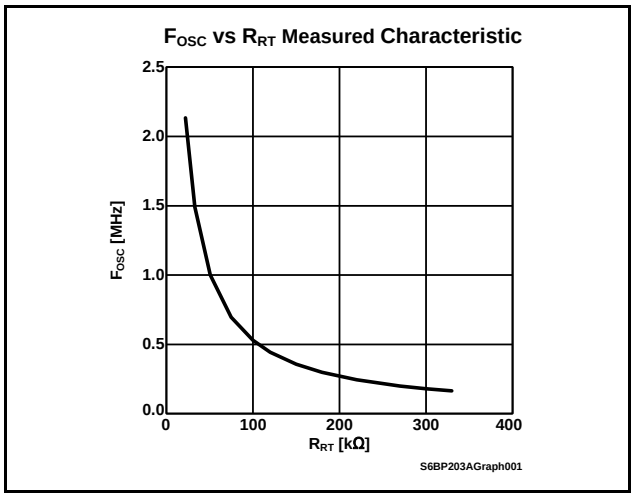
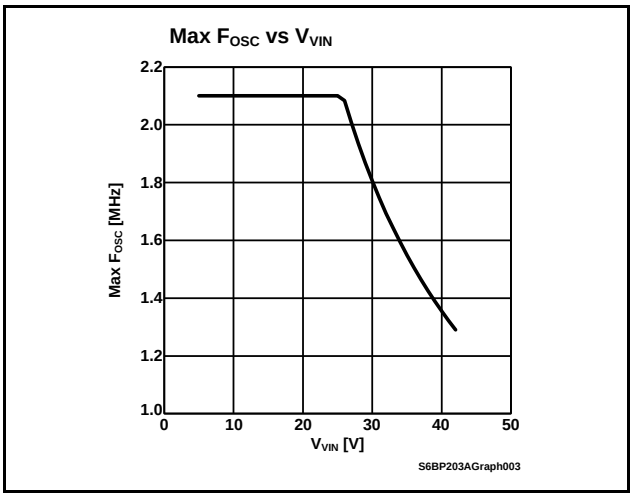


Figure 9-2 Max F_{OSC} vs V_{VIN}



The reference value can be calculated by the following formula.

$$F_{OSC}\,[Hz] \approx \frac{1}{R_{RT} \times 21.7 \times 10^{-12}}$$

F_{OSC} : Switching frequency [Hz]
R_{RT} : Timing resistance [Ω]

Setting of Soft-start Time

The Soft-start time is determined by the timing resistance (R_{RT}), the value of the resistor connected to RT pin.

$$T_{SS}\,[s] = \frac{1}{F_{OSC}} \times 2 \times 1024$$

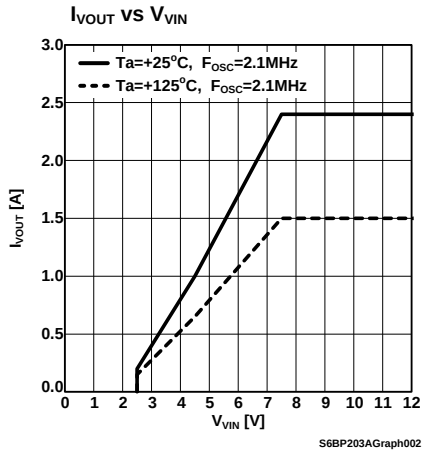
T_{SS} : Soft-start time [s]

F_{OSC} : Switching frequency [Hz]

Consideration of VOUT Maximum Output Current

Make sure the VOUT maximum output current in a range within the following graph.

Figure 9-3 I_{VOUT} vs V_{VIN}



10. Development Support

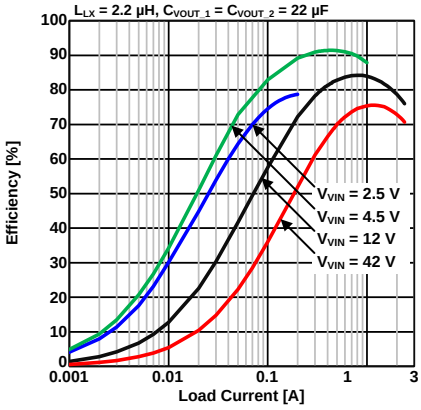
The IC has a set of documentation, such as application notes, development tools, and online resources to assist you during your development process. Visit www.cypress.com/automotive-pmic to find out more.

11. Reference Data

The followings are the reference data measured under the conditions shown in ”8. Application Circuit Example and Parts list”.

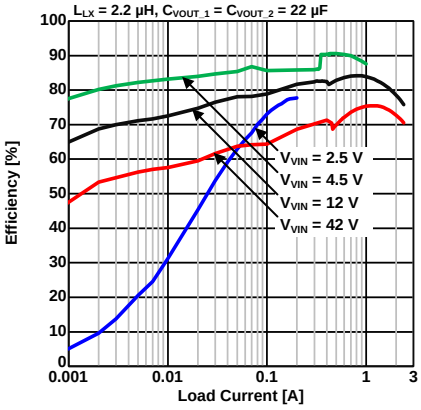
Efficiency (Fixed PWM)

V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set, T_A = +25°C,
L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



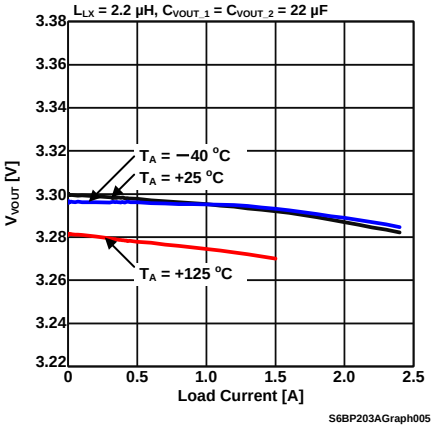
Efficiency (Automatic PWM/PFM)

V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set, T_A = +25°C,
L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



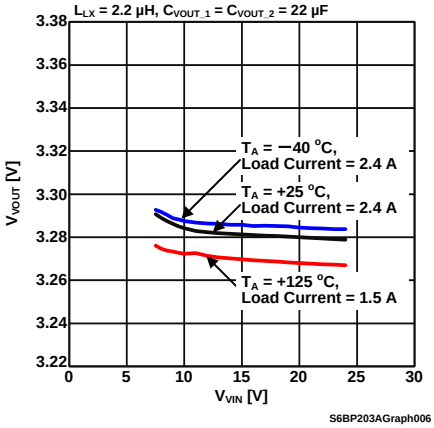
Load Regulation (Fixed PWM)

V_{VIN} = 12V, V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set,
L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



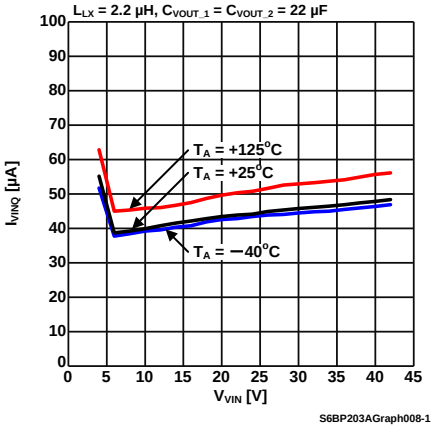
Line Regulation (Fixed PWM)

V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set,
L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



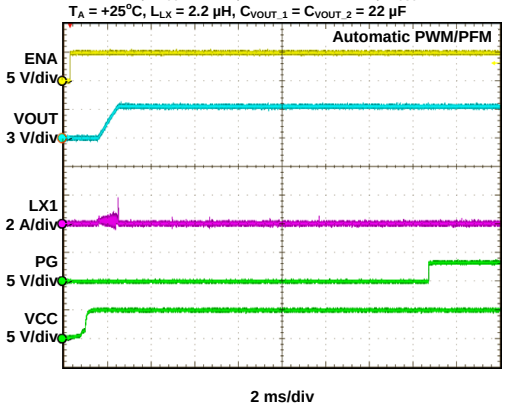
I_{VINQ} vs V_{VIN} (Automatic PWM/PFM)

V_{VOUT} = 3.3 V, Load Current = 0 A, F_{OSC} = 2.1 MHz set,
L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



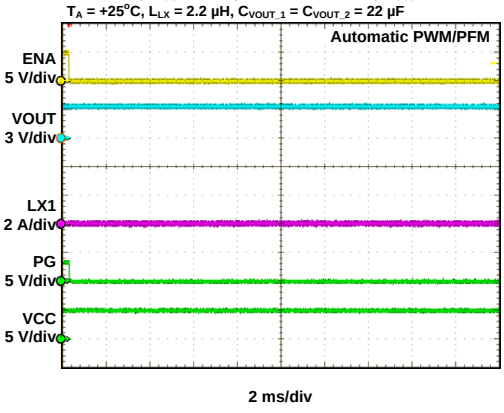
Turn On Response

V_{VIN} = 12 V, V_{VOUT} = 3.3 V, Load Current = 0 A, F_{OSC} = 2.1 MHz set,
T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



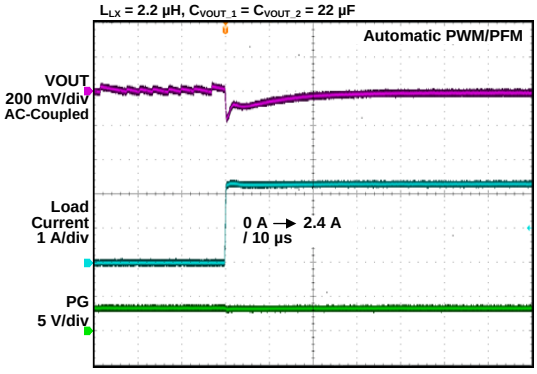
Turn Off Response

V_{VIN} = 12 V, V_{VOUT} = 3.3 V, Load Current = 0 A, F_{OSC} = 2.1 MHz set,
T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



Load Transient Response

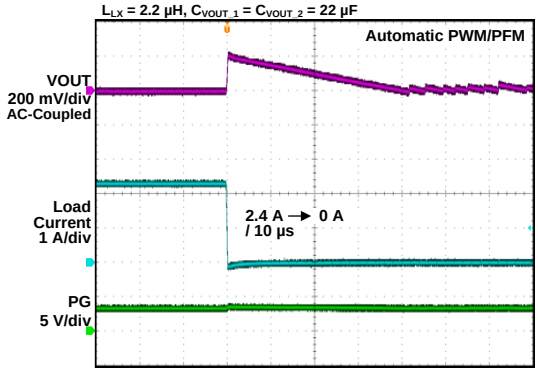
V_{VIN} = 12 V, V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set, T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph010-1

Load Transient Response

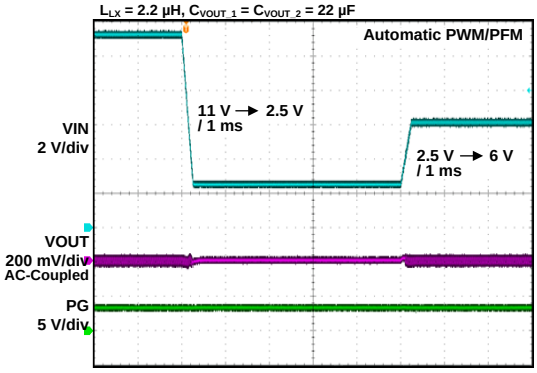
V_{VIN} = 12 V, V_{VOUT} = 3.3 V, F_{OSC} = 2.1 MHz set, T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph010-2

Cold Crank Line Transient Response

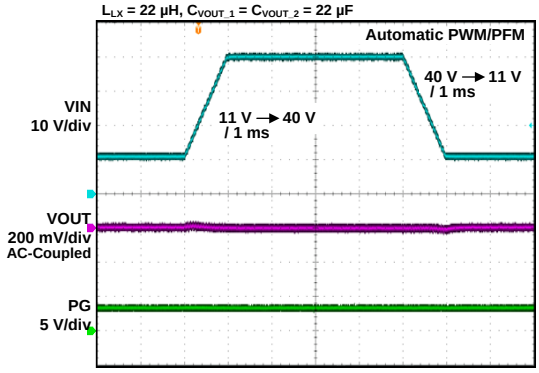
V_{VOUT} = 3.3 V, Load Current = 0.2 A, F_{OSC} = 2.1 MHz set, T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph011-1

Load Dump Line Transient Response

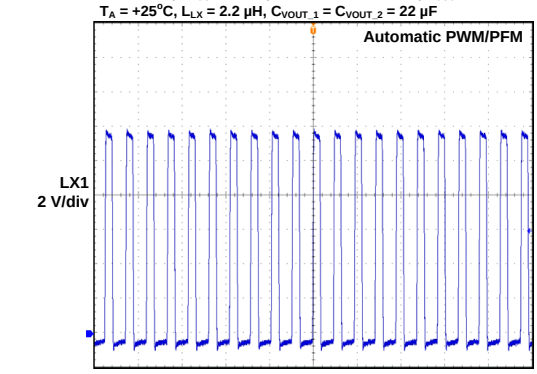
V_{VOUT} = 3.3 V, Load Current = 2.4 A, F_{OSC} = 200 kHz set, T_A = +25°C, L_{LX} = 22 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph011-2

Switching Waveform

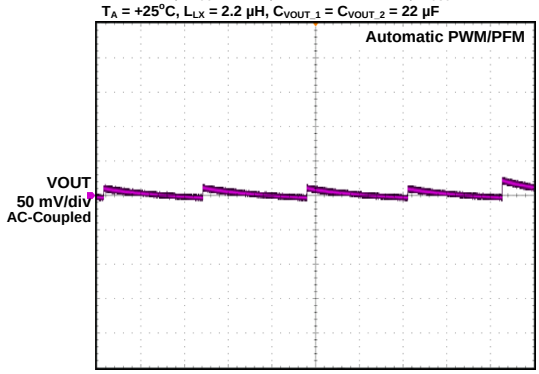
V_{VIN} = 12 V, V_{VOUT} = 3.3 V, Load Current = 2.4 A, F_{OSC} = 2.1 MHz set, T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph012-1

Ripple Waveform

V_{VIN} = 12 V, V_{VOUT} = 3.3 V, Load Current = 0 A, F_{OSC} = 2.1 MHz set, T_A = +25°C, L_{LX} = 2.2 µH, C_{VOUT_1} = C_{VOUT_2} = 22 µF



S6BP203AGraph012-2

12. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

13. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

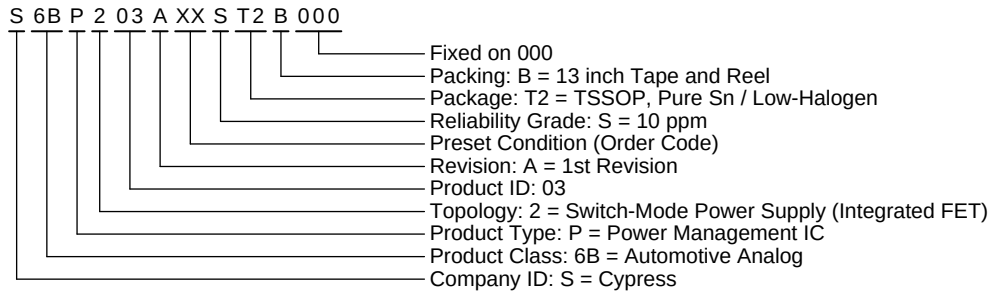
14. Ordering Information

Table 14-1 Ordering Information

Order Code	Part Number (MPN)	Package
8F	S6BP203A8FST2B000	Plastic TSSOP16 (0.65 mm pitch), 16-pin (SEC016)

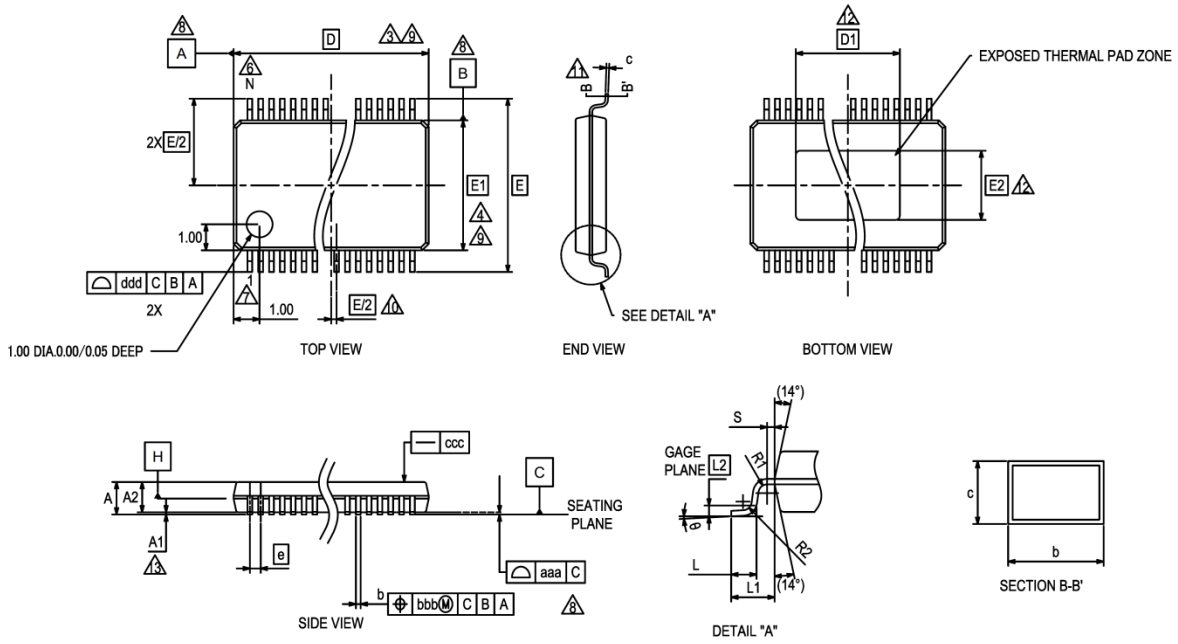
MPN: Marketing Part Number

Figure 14-1 Ordering Part Number Definitions



15. Package Dimensions

SEC016 16PIN Thin Shrink Small Outline Package



PACKAGE	SEC016		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.10
A_1	0.05	—	0.15
A_2	0.85	0.90	0.95
D	4.90	5.00	5.10
E_1	4.30	4.40	4.50
E	6.40 BSC		
D_1	2.90	3.00	3.10
E_2	2.90	3.00	3.10
S	0.20	—	—
R_1	0.09	—	—
R_2	0.09	—	—
θ	0°	—	8°
c	0.09	—	0.20
b	0.19	—	0.30
L	0.50	0.60	0.70
L_1	1.00 REF		
L_2	0.25 BSC		
e	0.65 BSC		
aaa	0.076		
bbb	0.10		
ccc	0.05		
ddd	0.20		
N	016		

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES) .
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DEMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBER PROTRUSION.ALLOWABLE DAMBER PROTRUSIONS SHALL BE 0.07mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHOULD BE 0.08mm FOR 0.65mm PITCH,0.08mm FOR 0.50mm PITCH AND 0.07mm FOR 0.40mm PITCH PACKAGES.
6. 'N' IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
8. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
9. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.
10. THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE, DATUM A.
11. CROSS SECTION B-B' TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.
12. DIMENSIONS "D1" AND "E2" ARE THERMALLY ENHANCED VARIATIONS. END USER SHOULD VERIFY AVAILABLE SIZE OF EXPOSED PER FOR SPECIFIC DEVICE APPLICATION "D1" AND "E2" DIMENSIONS DO NOT INCLUDE MOLD FLASH.
13. A1 IS DEFINED AS THE VERTICAL CLEARANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

Rev. 0A

16. Major Changes

Spansion Publication Number: S6BP203A_DS405-00031

Page	Section	Change Results
Preliminary 0.1		
–	–	Initial release
Preliminary 0.2		
11	9. Electrical Characteristics	"(TSD)" was added in the table of "9. Electrical Characteristics".

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: S6BP203A, ASSP, 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC
Document Number: 002-08534

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	HIXT	09/04/2015	New Spec.
*A	5056149	HIXT	12/18/2015	Added Block Diagram Added Figure 14-1 Updated 15. Package Dimensions
*B	5164343	HIXT	03/08/2016	Added "AEC-Q100 compliant (Grade-1)" in Features Added Figure 2-1 I/O Pin Equivalent Circuit Diagram The followings in 6. Electrical Characteristics were updated. The parameter name of I_{VOUT} was changed from "VOUT output voltage" to "Maximum output current" The max values of I_{VOUT} were moved to the min column. Added 10. Development Support Added 11. Reference Data Deleted the ES part number from Table 14-1
*C	5843027	MASG	08/03/2017	Adapted Cypress new logo.

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