

16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Temperature range
 - Automotive-E: -40°C to 125°C
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
 - $I_{CC} = 90\text{-mA}$ typical at 100 MHz
 - $I_{SB2} = 20\text{-mA}$ typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY7C1061G^[1] is a high-performance CMOS fast static RAM automotive part with embedded ECC. ECC logic can detect and correct single-bit error in read data word during read cycles.

This device has single chip enable input and is accessed by asserting the chip enable input (CE) LOW.

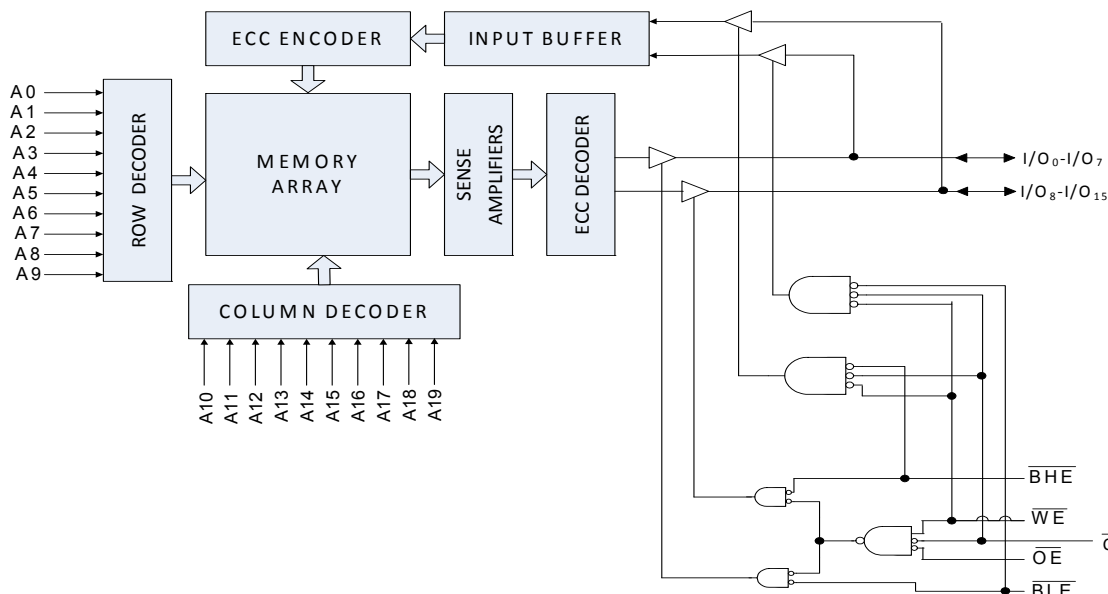
To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$), inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7 .

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/O s (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$). Refer to the below logic block diagram.

The CY7C1061G automotive device is available in 48-ball VFBGA and 48-pin TSOP I packages.

Logic Block Diagram – CY7C1061G



Note

1. The device does not support automatic write-back on error detection.

Contents

Pin Configurations	3	Ordering Information	13
Product Portfolio	3	Ordering Code Definitions	13
Maximum Ratings	4	Package Diagrams	14
Operating Range	4	Acronyms	15
DC Electrical Characteristics	4	Document Conventions	15
Capacitance	5	Units of Measure	15
Thermal Resistance	5	Document History Page	16
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	18
Data Retention Characteristics	6	Worldwide Sales and Design Support	18
Data Retention Waveform	6	Products	18
AC Switching Characteristics	7	PSoC® Solutions	18
Switching Waveforms	8	Cypress Developer Community	18
Truth Table	12	Technical Support	18

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout^[2]

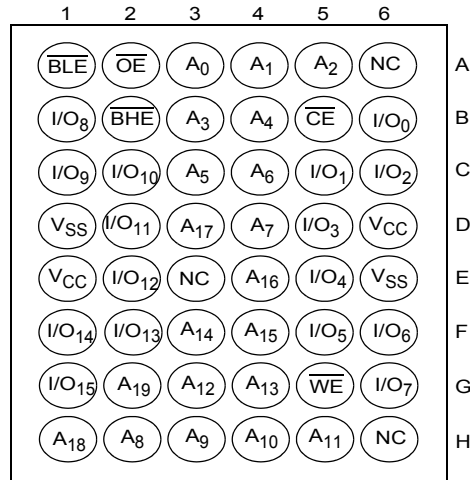
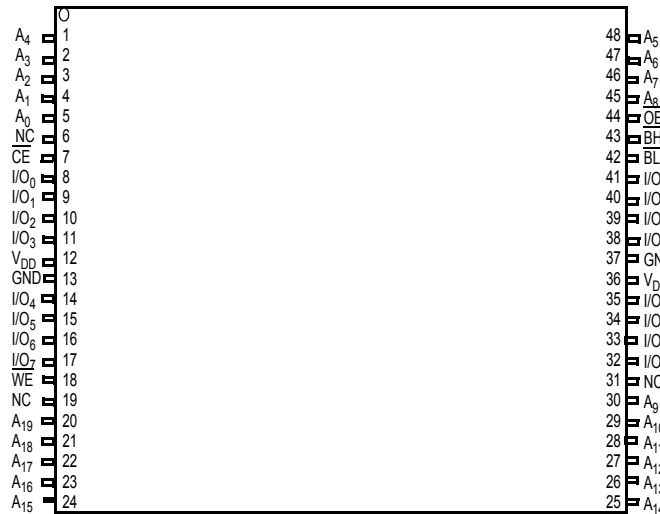


Figure 2. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout^[2]



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Current Consumption			
				Operating I _{CC} (mA)		Standby, I _{SB2} (mA)	
				Typ ^[3]	Max	Typ ^[3]	Max
CY7C1061G30	Automotive	2.2 V–3.6 V	10	90	160	20	50

Notes

- NC pins are not connected internally to the die.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND -0.5 V to +6.0 V

DC voltage applied to outputs
in High-Z State^[4] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[4] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-E	-40 °C to +125 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the operating range of -40 °C to 125 °C

Parameter	Description	Test Conditions	10 ns			Unit
			Min	Typ ^[5]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.0	—	—	V
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	—	—	
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	—	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	—	—	—	V
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	
$V_{IH}^{[4]}$	Input HIGH voltage	2.2 V to 2.7 V —	2.0	—	$V_{CC} + 0.3$	V
		2.7 V to 3.6 V —	2.0	—	$V_{CC} + 0.3$	
$V_{IL}^{[4]}$	Input LOW voltage	2.2 V to 2.7 V —	-0.3	—	0.6	V
		2.7 V to 3.6 V —	-0.3	—	0.8	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-5.0	—	+5.0	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-5.0	—	+5.0	μA
I_{CC}	Operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}$, CMOS levels $f = f_{MAX} = 1/t_{RC}$	—	90.0	160.0	mA
I_{SB1}	Automatic CE power down current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	—	—	60.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$	—	20.0	50.0	mA

Notes

4. $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

5. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3 \text{ V}$, $T_A = 25 \text{ °C}$.

Capacitance

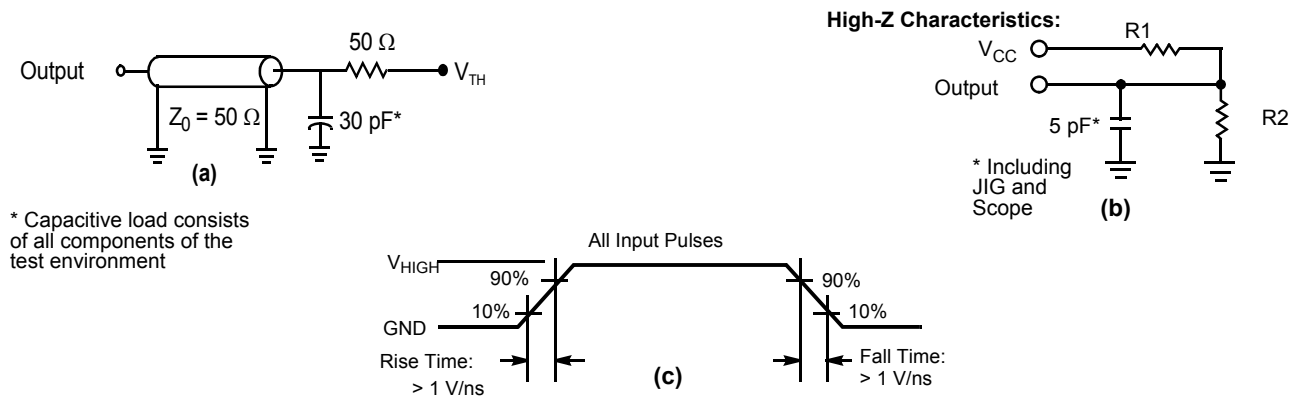
Parameter ^[6]	Description	Test Conditions	All Packages	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter ^[6]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four layer printed circuit board	31.50	57.99	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms^[7]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a $100\text{-}\mu\text{s}$ ramp time from 0 to $V_{CC(\text{min})}$ and $100\text{-}\mu\text{s}$ wait time after V_{CC} stabilizes to its operational value.

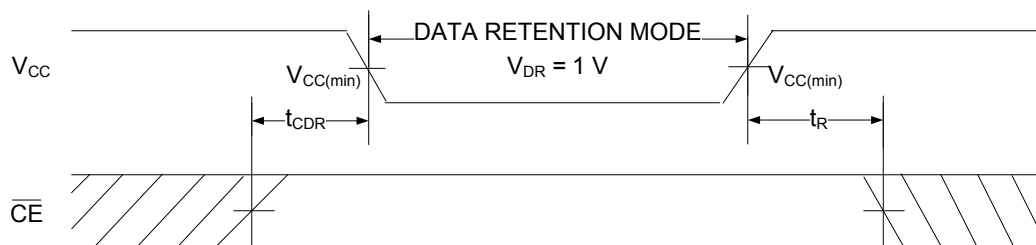
Data Retention Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	—	1.0	—	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	—	50.0	mA
$t_{CDR}^{[8]}$	Chip deselect to data retention time	—	0	—	ns
$t_R^{[8]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10.0	—	ns

Data Retention Waveform

Figure 4. Data Retention Waveform^[9]



Notes

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

AC Switching Characteristics

Over the operating range of -40°C to 125°C

Parameter ^[10]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t _{POWER}	V _{CC} (stable) to the first access ^[11]	100.0	–	μs
t _{RC}	Read cycle time	10.0	–	ns
t _{AA}	Address to data	–	10.0	ns
t _{OHA}	Data hold from address change	3.0	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data	–	10.0	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data	–	5.0	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to low-Z ^[12, 13]	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to high-Z ^[12, 13]	–	5.0	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to low-Z ^[12, 13]	3.0	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to high-Z ^[12, 13]	–	5.0	ns
t _{PU}	$\overline{\text{CE}}$ LOW to power-up ^[14]	0	–	ns
t _{PD}	$\overline{\text{CE}}$ HIGH to power-down ^[14]	–	10.0	ns
t _{DBE}	Byte enable to data valid	–	5.0	ns
t _{LZBE}	Byte enable to low-Z ^[12, 13]	0	–	ns
t _{HZBE}	Byte disable to high-Z ^[12, 13]	–	6.0	ns
Write Cycle ^[15, 16]				
t _{WC}	Write cycle time	10.0	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	7.0	–	ns
t _{AW}	Address setup to write end	7.0	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	7.0	–	ns
t _{SD}	Data setup to write end	5.0	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to low-Z ^[12, 13]	3.0	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to high-Z ^[12, 13]	–	5.0	ns
t _{BW}	Byte Enable to write end	7.0	–	ns

Notes

10. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{\text{CC}} \geq 3\text{ V}$) and $V_{\text{CC}}/2$ (for $V_{\text{CC}} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{\text{CC}} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{\text{CC}} < 3\text{ V}$). Test conditions for the read cycle use the output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
12. t_{HZOE} , t_{HZCE} , t_{HZWE} , and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 5. Hi-Z, Lo-Z transition is measured $\pm 200\text{ mV}$ from steady state voltage.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
14. These parameters are guaranteed by design and are not tested.
15. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$, or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled)^[17, 18]

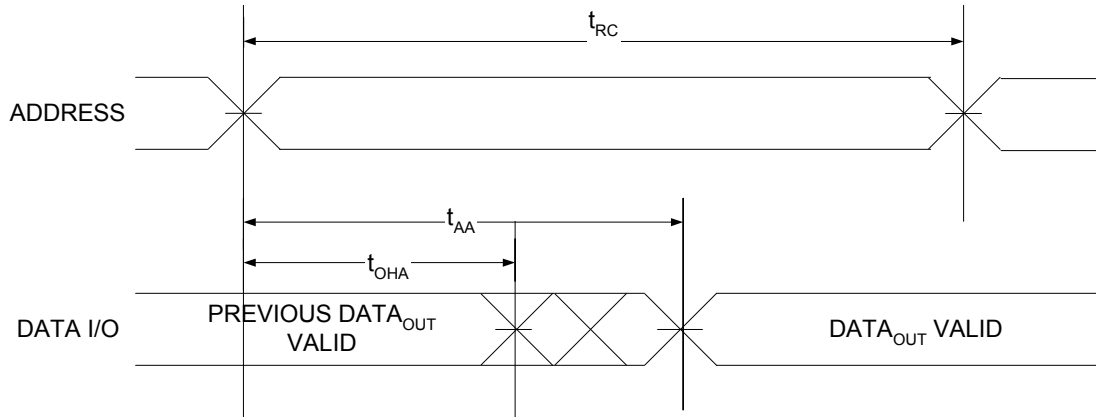
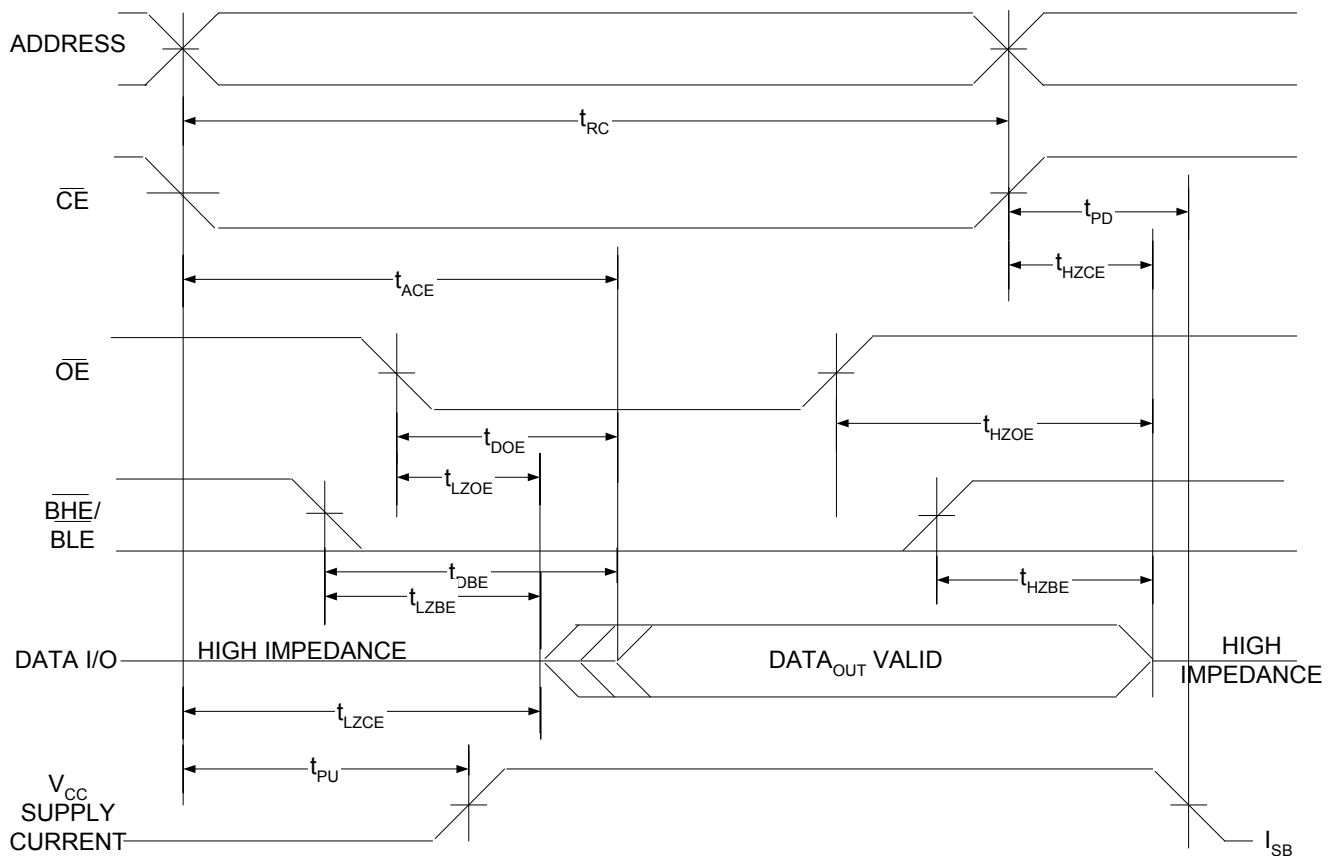


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)^[18, 19]



Notes

17. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL} .
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[20, 21]

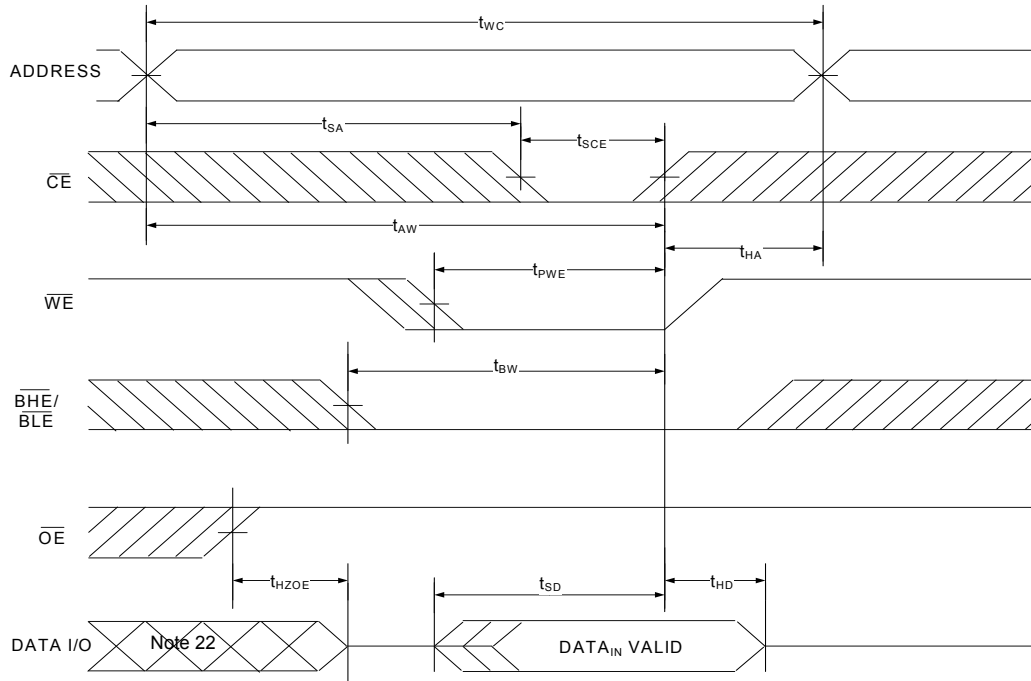
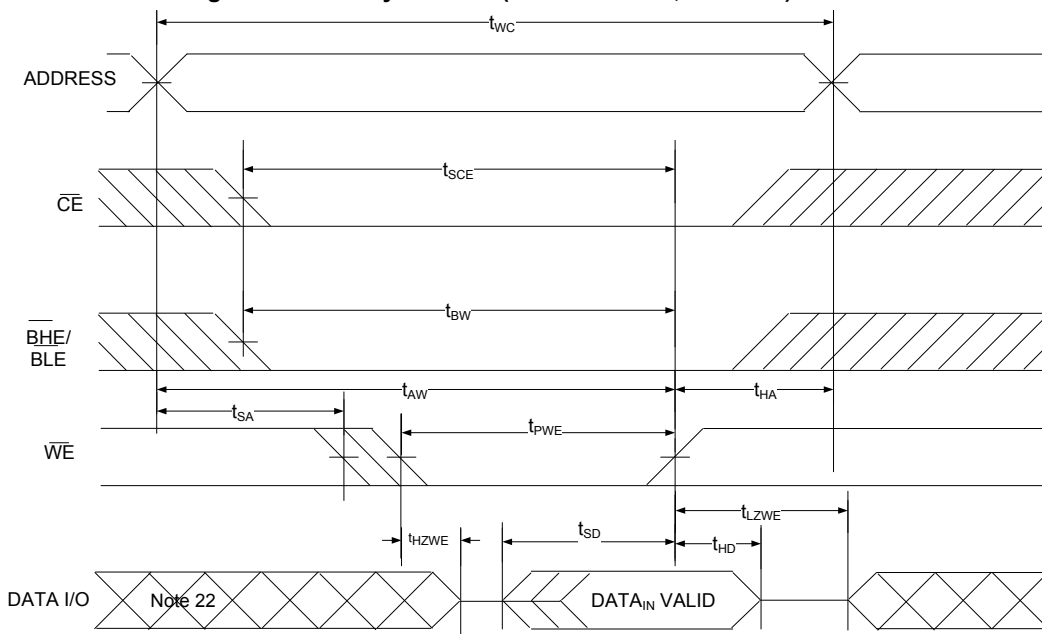


Figure 8. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[20, 21, 23]

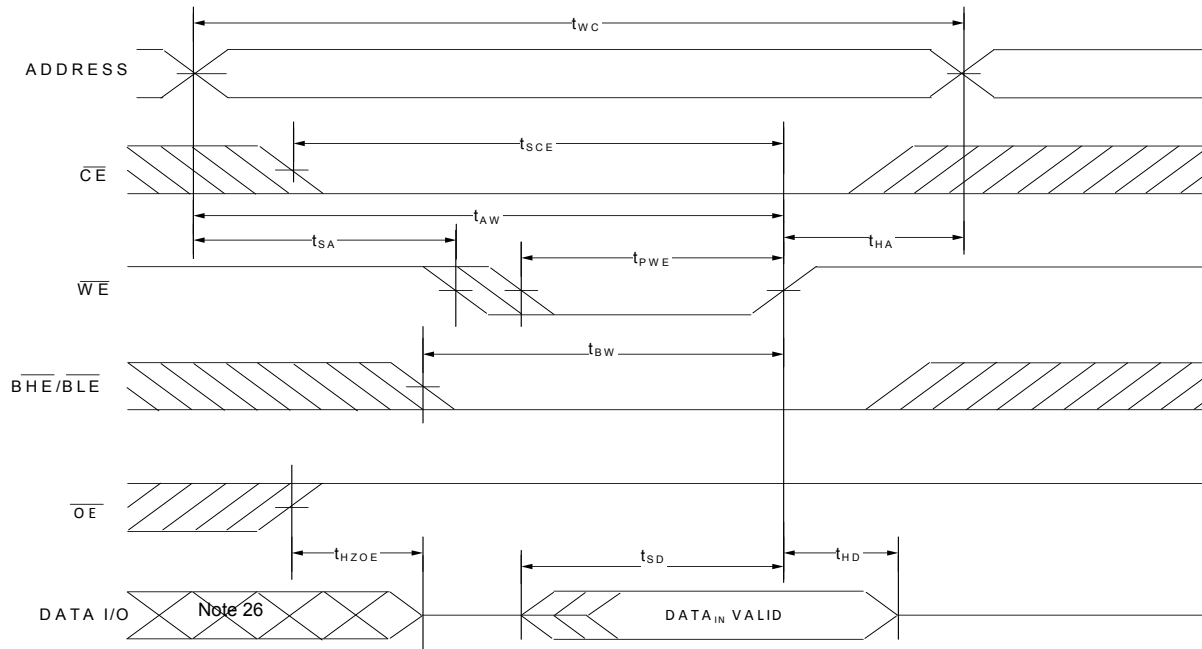


Notes

20. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is in high-impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
22. During this period, the I/Os are in output state. Do not apply input signals.
23. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled)^[24, 25]



Notes

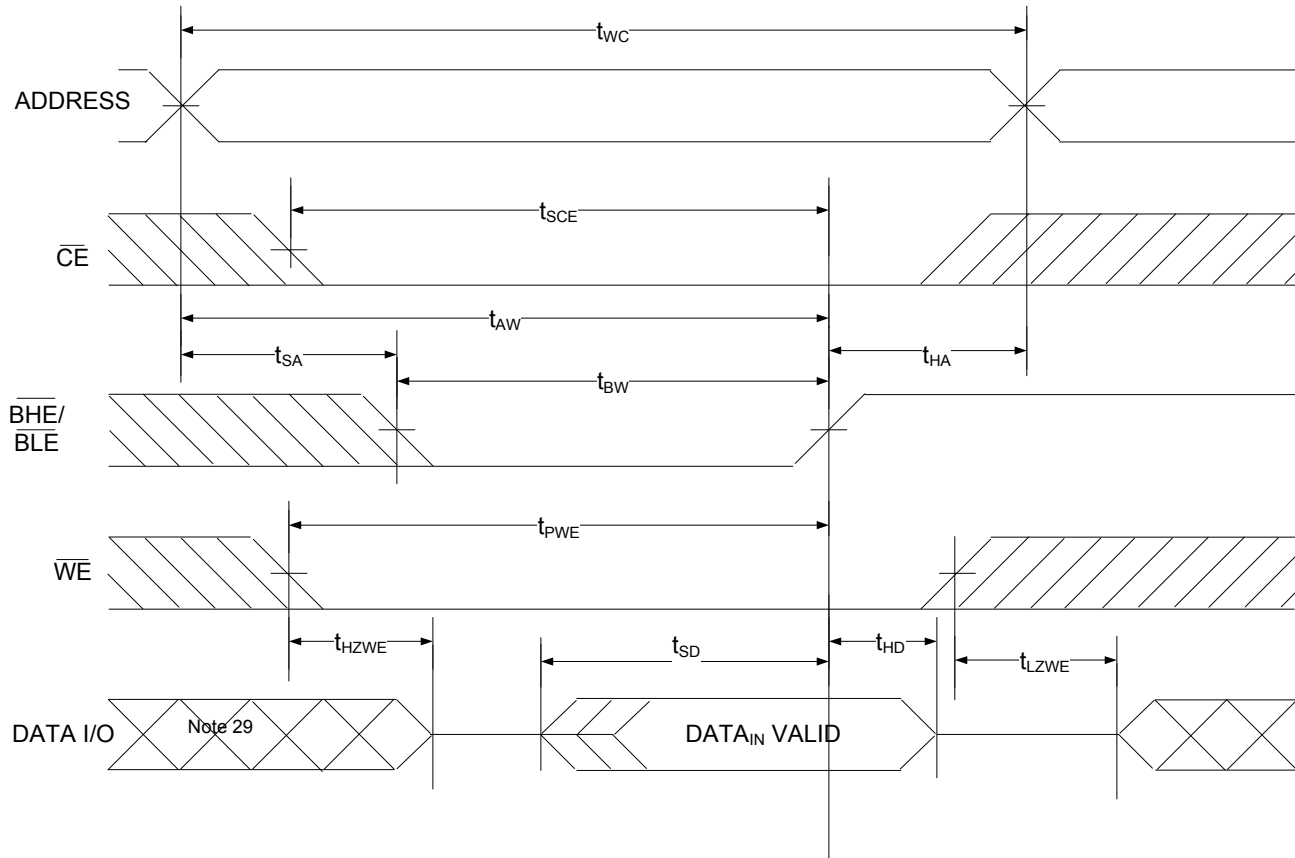
24. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

26. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)^[27, 28]



Notes

27. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

28. Data I/O is in high-impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

29. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X ^[30]	X ^[30]	X ^[30]	X ^[30]	High Z	High Z	Power down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

Note

30. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

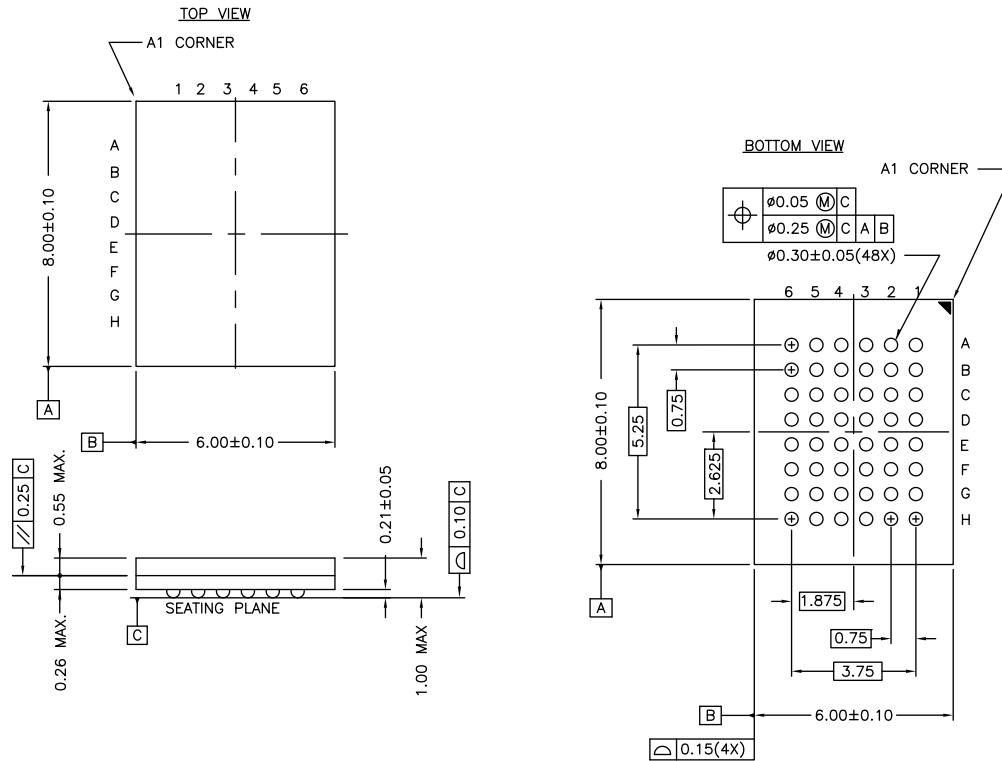
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1061G30-10BV1XE	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Automotive-E
		CY7C1061G30-10BV1XET			
		CY7C1061G30-10ZXE	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free)	
		CY7C1061G30-10ZXET			

Ordering Code Definitions

CY	7	C	1	06	1	G	XX	-	10	XX	1	X	E	X
X: Tape and Reel or Bulk; T = Tape and Reel, Blank = Bulk Temperature Range: E = Automotive-E (–40 °C to 125 °C) Pb-free Chip enables: 1 = Single Chip Enable Package Type: XX = BV or Z BV = 48-ball VFBGA; Z = 48-pin TSOP I Speed: 10 ns Voltage Range: 30 = 2.2 V–3.6 V Revision Code “G”: Process Technology – 65 nm Data Width: 1 = × 16-bits Density: 06 = 16-Mbit Family Code: 1 = Fast Asynchronous SRAM family Technology Code: C = CMOS Marketing Code: 7 = SRAM Company ID: CY = Cypress														

Package Diagrams

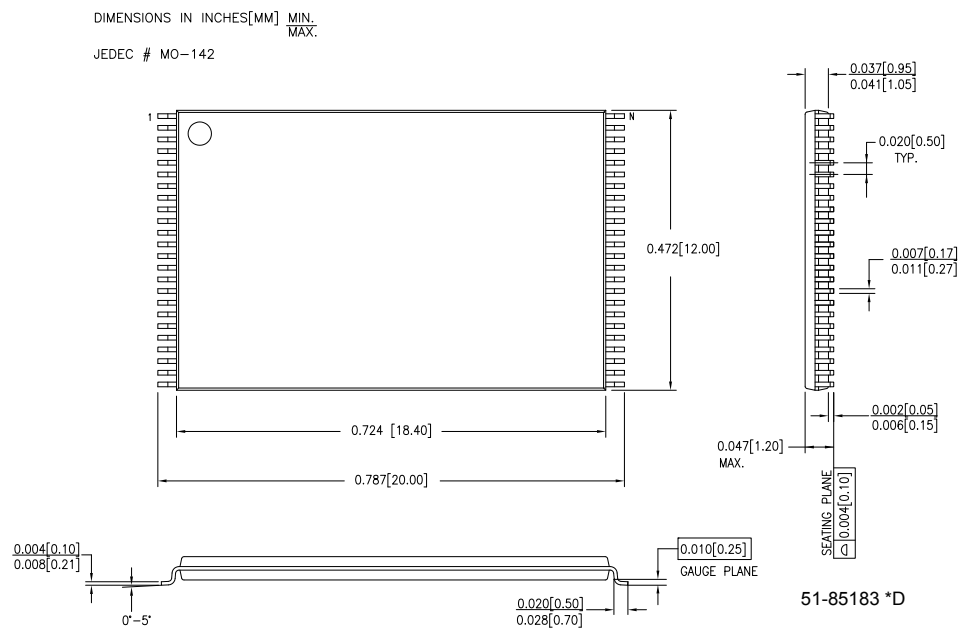
Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84821				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3825225	MEMJ	11/29/2012	New data sheet.
*A	4003550	NILE	05/20/2013	Updated Document Title to read as “CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)”. Updated Features. Updated Functional Description. Removed “Logic Block Diagram – CY7C1061GE”. Updated Logic Diagram for Single Chip Enable. Updated Pin Configurations: Updated Pin diagram to have BV1XE without ERR pin Updated Product Portfolio. Updated Operating Range. Updated Capacitance. Updated Thermal Resistance. Updated Data Retention Characteristics. Updated AC Switching Characteristics: Removed 12 ns, 17 ns speed bin related information and included 10 ns speed bin related information. Updated Switching Waveforms. Removed “ERR Output – CY7C1061GE”. Updated Package Diagrams: Added 48-pin TSOP I Package Diagram (Figure 11).
*B	4292074	MEMJ	02/28/2014	Updated Features: Mentioned frequency of measurement for I_{CC} (typical). Updated Functional Description: Replaced “an error detection” with “a single-bit error detection”. Added Note 1 (for ECC) and referred the same note in CY7C1061G. Updated Product Portfolio: Replaced CY7C1061G with CY7C1061G30. Updated Operating Range: Replaced Automotive with Automotive-E. Updated DC Electrical Characteristics: Added typical value for I_{CC} parameter (90 mA). Added typical value for I_{SB2} parameter (20 mA). Added Note 5 and referred the same note in “Typ” column. Updated AC Switching Characteristics: Added t_{POWER} parameter and its details. Added Note 11 and referred the same note in description of t_{POWER} parameter. Added Note 13 and referred the same note in description of t_{LZOE}, t_{HZOE}, t_{LZCE}, t_{HZCE}, t_{LZBE}, t_{HZBE}, t_{LZWE}, and t_{HZWE} parameters. Added Note 16 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 22 and referred the same note in Figure 7 and Figure 8. Added Note 23 and referred the same note in Figure 8. Added Figure 9. Added Note 26 and referred the same note in Figure 9 (to indicate that I/Os are in output state). Added Note 29 and referred the same note in Figure 10 (to indicate that I/Os are in output state).

Document History Page (continued)

Document Title: CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84821				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B (cont.)	4292074	MEMJ	02/28/2014	Updated Truth Table : Added Note 30 and referred the same note in "X" corresponding to Power down mode. Added condition to place outputs in disable state by making both $\overline{BHE}$ and $\overline{BLE}$ HIGH. Added Errata. Updated to new template.
*C	4330547	AJU	04/02/2014	No technical updates.
*D	4397546	AJU	06/03/2014	Updated AC Switching Characteristics : Updated Note 12 (Removed t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} ; and added Hi-Z, Lo-Z transition).
*E	4469360	NILE	09/18/2014	No technical updates.
*F	4576640	VINI	11/21/2014	No technical updates.
*G	4800949	NILE	09/30/2015	Updated Logic Block Diagram – CY7C1061G . Updated Package Diagrams : spec 51-85183 – Changed revision from *C to *D. Removed Errata. Updated to new template.
*H	4983893	NILE	10/28/2015	Changed status from Preliminary to Final.
*I	5435164	VINI	09/13/2016	Updated DC Electrical Characteristics : Updated the V _{OH} values. Updated Note 4. Updated Ordering Code Definitions : Added Tape and Reel parts. Updated Copyright and Disclaimer.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/Rf	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Cypress Semiconductor:](#)

[CY7C1061G30-10BV1XE](#)