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# 16-bit Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90860E Series

### MB90867E(S)/F867E(S)/V340E-101/V340E-102

#### ■ DESCRIPTION

The MB90860E series with integrated Flash ROM is a general-purpose Fujitsu 16-bit microcontroller designed for automotive and other industrial applications. By utilizing new 0.35 μm CMOS technology, Fujitsu Microelectronics now offers a 128KBytes of on-chip Flash ROM program memory.

Furthermore, the 3 V power supply of the internal MCU core is supplied by an internal regulator circuit, making this a vastly superior product in terms of reliability and power consumption.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

#### ■ FEATURES

##### • CPU

- Optimal instruction suitable for controller applications
  - Wide range of data types (bit, byte, word, and long word)
  - Wide range of addressing modes (23 types)
  - Enhanced multiplication and division instructions, and enhanced RETI instruction
  - Enhanced high-precision calculations using a 32-bit accumulator
- Instruction set level support for high level languages (C language) and multitask
  - Equipped with a system stack pointer
  - A variety of enhanced pointer indirect instructions
  - Barrel shift instructions
- Increased processing speed
  - 4-byte instruction queue

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The information for microcontroller supports is shown in the following homepage.  
Be sure to refer to the "Check Sheet" for the latest cautions on development.

#### "Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

<http://edevic.fujitsu.com/micom/en-support/>

# MB90860E Series

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- **Serial interface**

- LIN-UART : 4 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous and clock-synchronous serial transmission are available
- I<sup>2</sup>C interface : 2 channels
  - Up to 400 kbps transfer rate

- **Interrupt controller**

- Powerful interrupt function with 8 levels and 34 sources
- Supports up to 16 external interrupts
- CPU-independent automatic data transfer function
  - Expanded intelligent I/O service function (EI<sup>2</sup>OS) : up to 16 channels

- **I/O ports**

- General-purpose input/output ports (CMOS output)
  - 80 ports (devices without an S suffix in the part number - devices that support a sub clock)
  - 82 ports (devices with an S suffix in the part number - devices that do not support a sub clock)

- **8/10-bit A/D converter : 24 channels**

- Resolution is selectable between 8-bit and 10-bit.
- Can be activated by an external trigger.
- Conversion time : 3  $\mu$ s (at 24-MHz machine clock, including sampling time)

- **Address match detection (program patch) function**

- Address match detection for 6 address pointers

- **Timers**

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit  $\times$  16 channels or 16-bit  $\times$  8 channels
- 16-bit reload timer : 4 channels
- 16-bit I/O timer
  - 16-bit free run timer : 2 channel (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture (ICU) : 8 channels
  - 16-bit output compare (OCU) : 8 channels

- **Low power consumption (standby) modes**

- Sleep mode (a mode where the CPU operating clock stops)
- Time-base timer mode (a mode where only the oscillator clock, sub clock, time-base timer, and watch timer operate)
- Watch mode (a mode where only the sub clock and watch timer operate)
- Stop mode (a mode where the oscillator clock and sub clock stop)
- CPU blocking operation mode

- **Clock modulator**

- **Technology**

- 0.35  $\mu$ m CMOS technology

## ■ PRODUCT LINEUP

| Part Number<br>Parameter             | MB90867E(S)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | MB90F867E(S)                                                                                                                          | MB90V340E-101/102                                                     |
|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|
| CPU                                  | F <sup>2</sup> MC-16LX CPU                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                       |                                                                       |
| Type                                 | MASK ROM product                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Flash memory product                                                                                                                  | Evaluation product                                                    |
| System clock                         | On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                       |                                                                       |
| ROM                                  | MASK ROM<br>128 Kbytes                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Flash memory<br>128 Kbytes                                                                                                            | External                                                              |
| RAM                                  | 6 Kbytes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 6 Kbytes                                                                                                                              | 30 Kbytes                                                             |
| Dedicated power supply for emulator* | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                       | Yes                                                                   |
| Technology                           | 0.35 μm CMOS with on-chip voltage regulator for internal power supply                                                                                                                                                                                                                                                                                                                                                                                                                          | 0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with on-chip charge pump for programming voltage | 0.35 μm CMOS with on-chip voltage regulator for internal power supply |
| Operating voltage range              | 3.5 V to 5.5 V : during normal operation (not using A/D converter)<br>4.0 V to 5.5 V : when using A/D converter/Flash programming<br>4.5 V to 5.5 V : when using external bus                                                                                                                                                                                                                                                                                                                  |                                                                                                                                       | 5 V ± 10%                                                             |
| Temperature range                    | −40 °C to +105 °C                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                       | —                                                                     |
| Package                              | QFP-100, LQFP-100                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                       | PGA-299                                                               |
| LIN-UART                             | 4 channels                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                       | 5 channels                                                            |
|                                      | Wide range of baud rate settings using a dedicated baud rate generator (reload timer)<br>Special synchronous options for adapting to different synchronous serial protocols<br>LIN functionality can operate as either master or slave LIN device                                                                                                                                                                                                                                              |                                                                                                                                       |                                                                       |
| I <sup>2</sup> C (400 kbps)          | 2 channels                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                       |                                                                       |
| 8/10-bit A/D converter               | 24 channels                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                       |                                                                       |
|                                      | 10-bit or 8-bit resolution<br>Conversion time : Min 3 μs include sample time (per one channel)                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                       |                                                                       |
| 16-bit reload timer (4 channels)     | Operation clock frequency : fsys/2 <sup>1</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>5</sup> (fsys = Machine clock frequency)<br>Supports External Event Count function                                                                                                                                                                                                                                                                                                                         |                                                                                                                                       |                                                                       |
| 16-bit free run timer (2 channels)   | Generates an interrupt on overflow<br>Supports Timer Clear when a match with Output Compare (ch.0, ch.4)<br>Operation clock freq. : fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> , fsys/2 <sup>5</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>7</sup> (fsys = Machine clock freq.)<br>Free run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3<br>Free run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7 |                                                                                                                                       |                                                                       |
| 16-bit output compare (8 channels)   | Generates an interrupt when the 16-bit free run timer matches the output compare register.<br>Multiple compare registers can be used to generate an output signal.                                                                                                                                                                                                                                                                                                                             |                                                                                                                                       |                                                                       |
| 16-bit input capture (8 channels)    | Captures the value of the 16-bit free run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).                                                                                                                                                                                                                                                                                                                        |                                                                                                                                       |                                                                       |

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# MB90860E Series

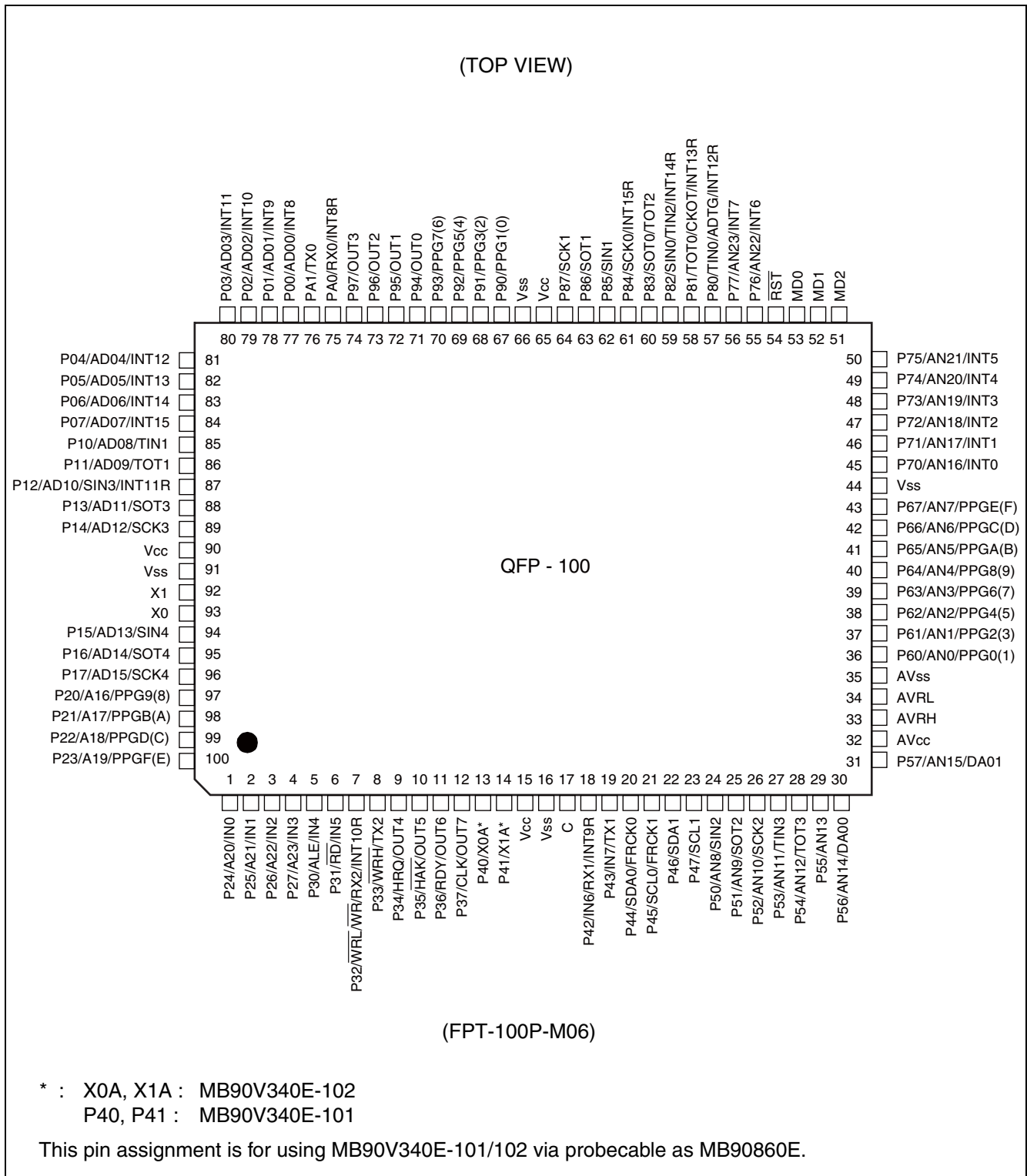
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| Part Number<br>Parameter                           | MB90867E(S)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | MB90F867E(S) | MB90V340E-101/102      |
|----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------------------|
| 8/16-bit programmable pulse generator (8 channels) | 8 channels (16-bit) or 16 channels (8-bit)<br>8-bit reload counter × 16<br>8-bit reload registers for lower part × 16<br>8-bit reload registers for upper part × 16<br>Supports 8-bit and 16-bit operating modes<br>A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as an 8-bit prescaler plus an 8-bit reload counter<br>Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ or 128 $\mu s$ @ $f_{osc} = 4$ MHz<br>( $f_{sys}$ = Machine clock frequency, $f_{osc}$ = Oscillation clock frequency) |              |                        |
| CAN interface                                      | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |              | 3 channels             |
| External interrupt (16 channels)                   | Can be triggered by rising edge, falling edge, or H/L level inputs, external interrupts can be used by expanded intelligent I/O services (EI <sup>2</sup> OS) and DMA                                                                                                                                                                                                                                                                                                                                                                                                               |              |                        |
| D/A converter                                      | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |              | 2 channels             |
| Sub clock (maximum 100 kHz)                        | Devices without 'S' suffix in the part number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              | Only for MB90V340E-102 |
| I/O ports                                          | Virtually all external pins can be used as general-purpose I/O ports<br>All push-pull outputs<br>Bitwise configurable as input/output or peripheral signal<br>Configurable in blocks of 8 pins as CMOS schmitt trigger or automotive inputs<br>Configurable as TTL input levels for an external bus (only applies to the 32 external bus pins)                                                                                                                                                                                                                                      |              |                        |
| Flash memory                                       | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>Equipped with a flag indicating completion of the algorithm<br>Number of erase cycles : 10,000 times<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash                                                                                                                                               |              | —                      |

\* : Configured by the jumper switch (TOOL VCC) when the emulator (MB2147-01) is used.  
Please refer to the Emulator hardware manual for details.

## PIN ASSIGNMENTS

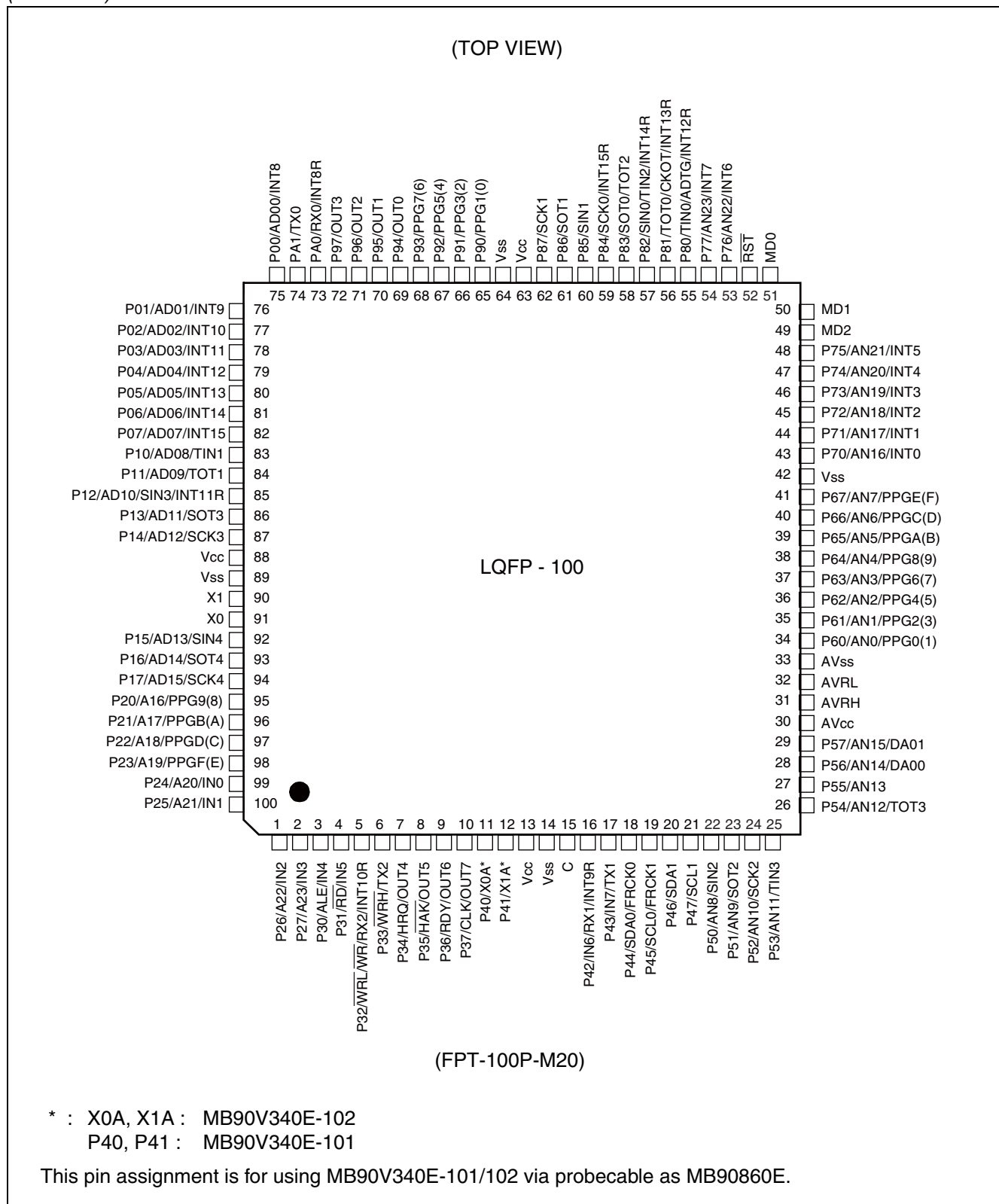
- MB90V340E-101/102



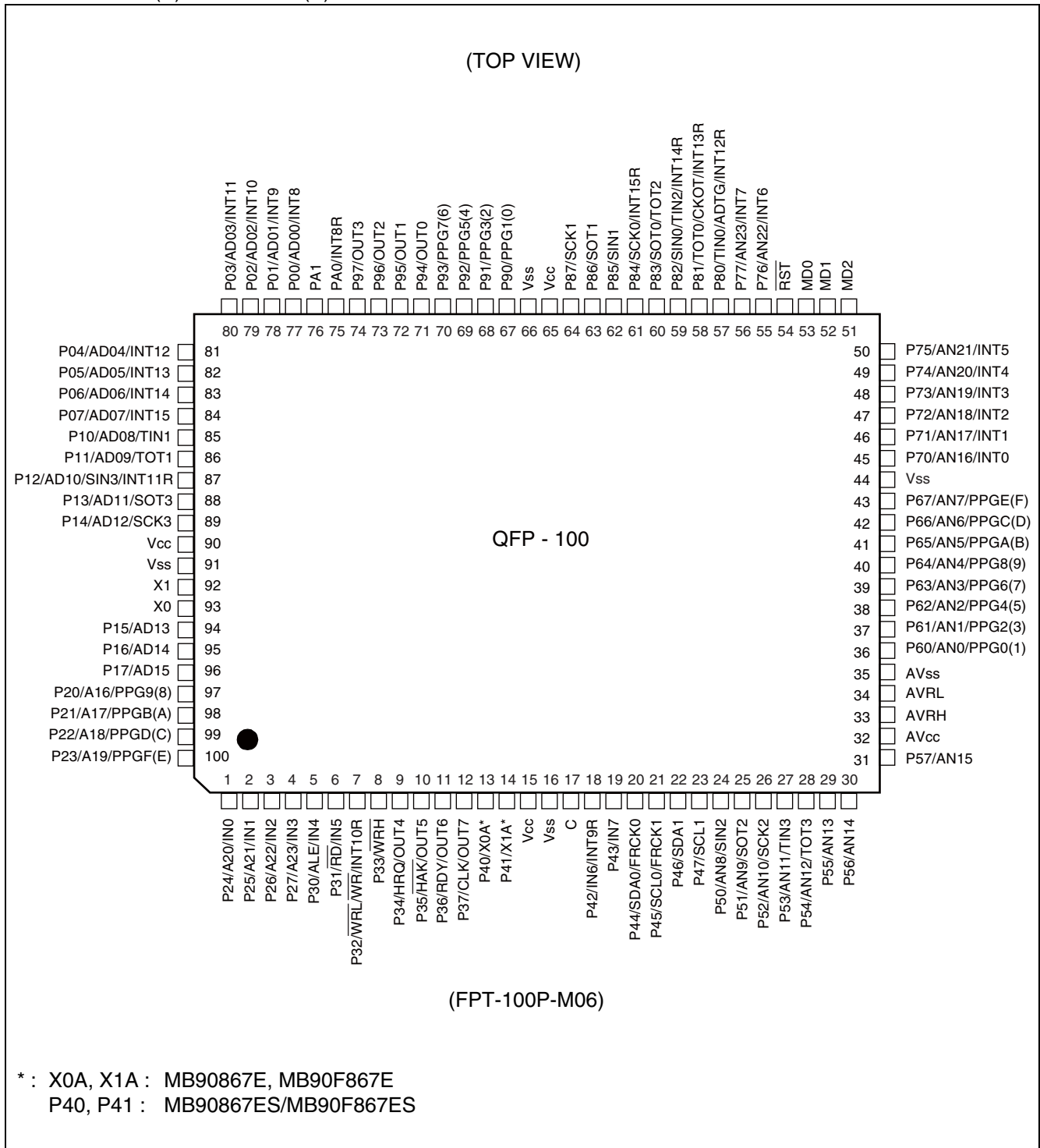
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# MB90860E Series

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- MB90867E(S)/MB90F867E(S)

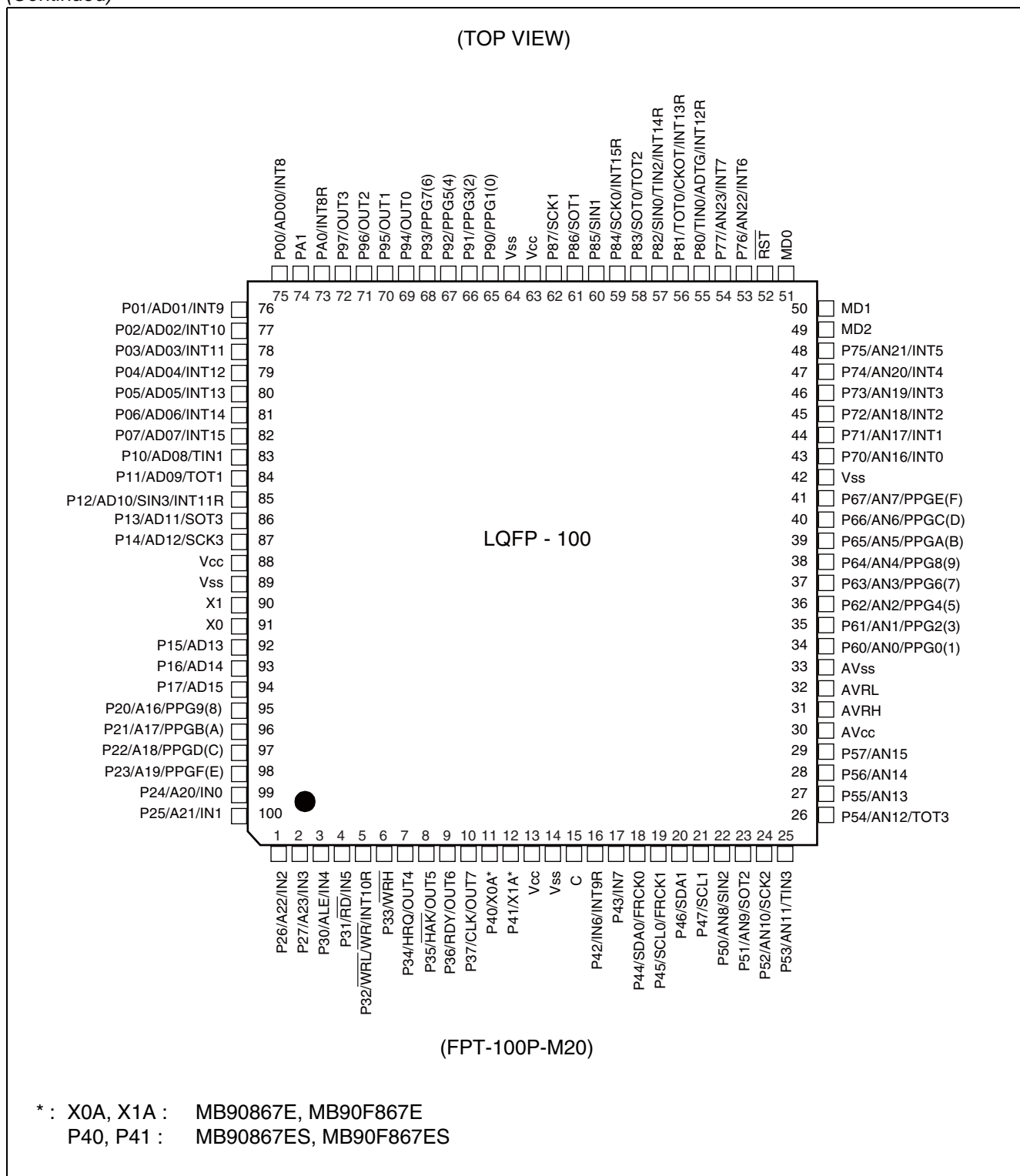


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# MB90860E Series

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## ■ PIN DESCRIPTION

| Pin No.  |           | Pin name                         | I/O<br>Circuit<br>type*3 | Function                                                                                                                                                                                                                                                                                                                                                                        |
|----------|-----------|----------------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1 | LQFP100*2 |                                  |                          |                                                                                                                                                                                                                                                                                                                                                                                 |
| 1 to 4   | 99 to 2   | P24 to P27                       | G                        | General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. In external bus mode, each pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.                                                                                       |
|          |           | A20 to A23                       |                          | External address bus output pins. When the corresponding bits in the external address output control register (HACR) are 0, the pins are enabled as high address output pins (A20 to A23).                                                                                                                                                                                      |
|          |           | IN0 to IN3                       |                          | Trigger input pins for input captures 0 to 3.                                                                                                                                                                                                                                                                                                                                   |
| 5        | 3         | P30                              | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.                                                                                                                                                                                                          |
|          |           | ALE                              |                          | Address latch enable output pin. This function is enabled when the external bus is enabled.                                                                                                                                                                                                                                                                                     |
|          |           | IN4                              |                          | Trigger input pin for input capture 4.                                                                                                                                                                                                                                                                                                                                          |
| 6        | 4         | P31                              | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.                                                                                                                                                                                                          |
|          |           | $\overline{RD}$                  |                          | External read strobe output pin. This function is enabled when the external bus is enabled.                                                                                                                                                                                                                                                                                     |
|          |           | IN5                              |                          | Trigger input pin for input capture 5.                                                                                                                                                                                                                                                                                                                                          |
| 7        | 5         | P32                              | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the $\overline{WR}/\overline{WRL}$ pin output disabled.                                                                                                                                    |
|          |           | $\overline{WR} / \overline{WRL}$ |                          | Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}/\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used as a write strobe output for the lower 8 bits of the data bus in 16-bit access while $\overline{WR}$ is used as the write strobe for the 8 bits of the data bus in 8-bit access. |
|          |           | INT10R                           |                          | External interrupt request input pin (sub) .                                                                                                                                                                                                                                                                                                                                    |
| 8        | 6         | P33                              | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output disabled.                                                                                                                                                  |
|          |           | $\overline{WRH}$                 |                          | Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, and the external bus is in 16-bit mode, and the $\overline{WRH}$ output pin is enabled.                                                                                                                                                       |

(Continued)

# MB90860E Series

| Pin No.  |           | Pin name                | I/O<br>Circuit<br>type*3 | Function                                                                                                                                                                                                                      |
|----------|-----------|-------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1 | LQFP100*2 |                         |                          |                                                                                                                                                                                                                               |
| 9        | 7         | P34                     | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the hold function is disabled.           |
|          |           | HRQ                     |                          | Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.                                                                                                                |
|          |           | OUT4                    |                          | Waveform output pin for output compare 4.                                                                                                                                                                                     |
| 10       | 8         | P35                     | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the hold function is disabled.           |
|          |           | $\overline{\text{HAK}}$ |                          | Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.                                                                                                           |
|          |           | OUT5                    |                          | Waveform output pin for output compare 5.                                                                                                                                                                                     |
| 11       | 9         | P36                     | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the external ready function is disabled. |
|          |           | RDY                     |                          | External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.                                                                                                    |
|          |           | OUT6                    |                          | Waveform output pin for output compare 6.                                                                                                                                                                                     |
| 12       | 10        | P37                     | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when clock output is disabled.                |
|          |           | CLK                     |                          | Clock output pin. This function is enabled when both the external bus and clock output are enabled.                                                                                                                           |
|          |           | OUT7                    |                          | Waveform output pin for output compare 7.                                                                                                                                                                                     |
| 13, 14   | 11, 12    | P40, P41                | F                        | General-purpose I/O pins (devices with an "S" suffix in the part number).                                                                                                                                                     |
|          |           | X0A, X1A                | B                        | Input pins for sub-clock (devices without an "S" suffix in the part number).                                                                                                                                                  |
| 15       | 13        | V <sub>CC</sub>         | —                        | Power (3.5 V to 5.5 V) input pin.                                                                                                                                                                                             |
| 16       | 14        | V <sub>SS</sub>         | —                        | GND pin.                                                                                                                                                                                                                      |
| 17       | 15        | C                       | K                        | This is the power supply stabilization capacitor pin. It should be connected to a ceramic capacitor with a capacitance of 0.1 $\mu\text{F}$ or higher.                                                                        |
| 18       | 16        | P42                     | F                        | General-purpose I/O pin.                                                                                                                                                                                                      |
|          |           | IN6                     |                          | Trigger input pin for input capture 6.                                                                                                                                                                                        |
|          |           | INT9R                   |                          | External interrupt request input pin (sub) .                                                                                                                                                                                  |

(Continued)

| Pin No.  |           | Pin name         | I/O<br>Circuit<br>type*3 | Function                                      |
|----------|-----------|------------------|--------------------------|-----------------------------------------------|
| QFP100*1 | LQFP100*2 |                  |                          |                                               |
| 19       | 17        | P43              | F                        | General-purpose I/O pin.                      |
|          |           | IN7              |                          | Trigger input pin for input capture 7.        |
| 20       | 18        | P44              | H                        | General-purpose I/O pin.                      |
|          |           | SDA0             |                          | Serial data I/O pin for I <sup>2</sup> C 0.   |
|          |           | FRCK0            |                          | Input pin for 16-bit free run timer 0.        |
| 21       | 19        | P45              | H                        | General-purpose I/O pin.                      |
|          |           | SCL0             |                          | Serial clock I/O pin for I <sup>2</sup> C 0.  |
|          |           | FRCK1            |                          | Input pin for 16-bit free run timer 1.        |
| 22       | 20        | P46              | H                        | General-purpose I/O pin.                      |
|          |           | SDA1             |                          | Serial data I/O pin for I <sup>2</sup> C 1.   |
| 23       | 21        | P47              | H                        | General-purpose I/O pin.                      |
|          |           | SCL1             |                          | Serial clock I/O pin for I <sup>2</sup> C 1.  |
| 24       | 22        | P50              | O                        | General-purpose I/O pin.                      |
|          |           | AN8              |                          | Analog input pin for the A/D converter.       |
|          |           | SIN2             |                          | Serial data input pin for UART2.              |
| 25       | 23        | P51              | I                        | General-purpose I/O pin.                      |
|          |           | AN9              |                          | Analog input pin for the A/D converter.       |
|          |           | SOT2             |                          | Serial data output pin for UART2.             |
| 26       | 24        | P52              | I                        | General-purpose I/O pin.                      |
|          |           | AN10             |                          | Analog input pin for the A/D converter.       |
|          |           | SCK2             |                          | Clock I/O pin for UART2.                      |
| 27       | 25        | P53              | I                        | General-purpose I/O pin.                      |
|          |           | AN11             |                          | Analog input pin for the A/D converter.       |
|          |           | TIN3             |                          | Event input pin for reload timer 3.           |
| 28       | 26        | P54              | I                        | General-purpose I/O pin.                      |
|          |           | AN12             |                          | Analog input pin for the A/D converter.       |
|          |           | TOT3             |                          | Output pin for reload timer 3.                |
| 29       | 27        | P55              | I                        | General-purpose I/O pin.                      |
|          |           | AN13             |                          | Analog input pin for the A/D converter.       |
| 30, 31   | 28, 29    | P56, P57         | J                        | General-purpose I/O pins.                     |
|          |           | AN14, AN15       |                          | Analog input pin for the A/D converter.       |
| 32       | 30        | AV <sub>CC</sub> | K                        | Analog power input pin for the A/D converter. |

(Continued)

# MB90860E Series

| Pin No.  |           | Pin name                     | I/O<br>Circuit<br>type*3 | Function                                                                                                                                                                    |
|----------|-----------|------------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1 | LQFP100*2 |                              |                          |                                                                                                                                                                             |
| 33       | 31        | AVRH                         | L                        | Reference voltage input pin for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV <sub>CC</sub> . |
| 34       | 32        | AVRL                         | K                        | Lower reference voltage input pin for the A/D converter.                                                                                                                    |
| 35       | 33        | AV <sub>SS</sub>             | K                        | Analog GND pin for the A/D converter.                                                                                                                                       |
| 36 to 43 | 34 to 41  | P60 to P67                   | I                        | General-purpose I/O pins.                                                                                                                                                   |
|          |           | AN0 to AN7                   |                          | Analog input pins for the A/D converter.                                                                                                                                    |
|          |           | PPG0, 2, 4, 6, 8,<br>A, C, E |                          | PPG output pins.                                                                                                                                                            |
| 44       | 42        | V <sub>SS</sub>              | —                        | GND pin.                                                                                                                                                                    |
| 45 to 50 | 43 to 48  | P70 to P75                   | I                        | General-purpose I/O pins.                                                                                                                                                   |
|          |           | AN16 to AN21                 |                          | Analog input pins for the A/D converter.                                                                                                                                    |
|          |           | INT0 to INT5                 |                          | External interrupt request input pins.                                                                                                                                      |
| 51       | 49        | MD2                          | D                        | Input pin for specifying the operating mode.                                                                                                                                |
| 52, 53   | 50, 51    | MD1, MD0                     | C                        | Input pins for specifying the operating mode.                                                                                                                               |
| 54       | 52        | RST                          | E                        | Reset input.                                                                                                                                                                |
| 55, 56   | 53, 54    | P76, P77                     | I                        | General-purpose I/O pins.                                                                                                                                                   |
|          |           | AN22, AN23                   |                          | Analog input pins for the A/D converter.                                                                                                                                    |
|          |           | INT6, INT7                   |                          | External interrupt request input pins.                                                                                                                                      |
| 57       | 55        | P80                          | F                        | General-purpose I/O pin.                                                                                                                                                    |
|          |           | TIN0                         |                          | Event input pin for reload timer 0.                                                                                                                                         |
|          |           | ADTG                         |                          | Trigger input pin for the A/D converter.                                                                                                                                    |
|          |           | INT12R                       |                          | External interrupt request input pin (sub) .                                                                                                                                |
| 58       | 56        | P81                          | F                        | General-purpose I/O pin.                                                                                                                                                    |
|          |           | TOT0                         |                          | Output pin for reload timer 0.                                                                                                                                              |
|          |           | CKOT                         |                          | Output pin for the clock monitor.                                                                                                                                           |
|          |           | INT13R                       |                          | External interrupt request input pin (sub) .                                                                                                                                |
| 59       | 57        | P82                          | M                        | General-purpose I/O pin.                                                                                                                                                    |
|          |           | SIN0                         |                          | Serial data input pin for UART0.                                                                                                                                            |
|          |           | TIN2                         |                          | Event input pin for reload timer 2.                                                                                                                                         |
|          |           | INT14R                       |                          | External interrupt request input pin (sub) .                                                                                                                                |
| 60       | 58        | P83                          | F                        | General-purpose I/O pin.                                                                                                                                                    |
|          |           | SOT0                         |                          | Serial data output pin for UART0.                                                                                                                                           |
|          |           | TOT2                         |                          | Output pin for reload timer 2.                                                                                                                                              |

(Continued)

# MB90860E Series

| Pin No.  |           | Pin name        | I/O Circuit type*3 | Function                                                                                                                                                                |
|----------|-----------|-----------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1 | LQFP100*2 |                 |                    |                                                                                                                                                                         |
| 61       | 59        | P84             | F                  | General-purpose I/O pin.                                                                                                                                                |
|          |           | SCK0            |                    | Clock I/O pin for UART0.                                                                                                                                                |
|          |           | INT15R          |                    | External interrupt request input pin (sub) .                                                                                                                            |
| 62       | 60        | P85             | M                  | General-purpose I/O pin.                                                                                                                                                |
|          |           | SIN1            |                    | Serial data input pin for UART1.                                                                                                                                        |
| 63       | 61        | P86             | F                  | General-purpose I/O pin.                                                                                                                                                |
|          |           | SOT1            |                    | Serial data output pin for UART1.                                                                                                                                       |
| 64       | 62        | P87             | F                  | General-purpose I/O pin.                                                                                                                                                |
|          |           | SCK1            |                    | Clock I/O pin for UART1.                                                                                                                                                |
| 65       | 63        | V <sub>CC</sub> | —                  | Power (3.5 V to 5.5 V) input pins.                                                                                                                                      |
| 66       | 64        | V <sub>SS</sub> | —                  | GND pins.                                                                                                                                                               |
| 67 to 70 | 65 to 68  | P90 to P93      | F                  | General-purpose I/O pins.                                                                                                                                               |
|          |           | PPG1, 3, 5, 7   |                    | PPG output pins.                                                                                                                                                        |
| 71 to 74 | 69 to 72  | P94 to P97      | F                  | General-purpose I/O pins.                                                                                                                                               |
|          |           | OUT0 to OUT3    |                    | Waveform output pins for output compare 0 to 3. This function is enabled when waveform output is enabled.                                                               |
| 75       | 73        | PA0             | F                  | General-purpose I/O pin.                                                                                                                                                |
|          |           | INT8R           |                    | External interrupt request input pin (sub) .                                                                                                                            |
| 76       | 74        | PA1             | F                  | General-purpose I/O pin.                                                                                                                                                |
| 77 to 84 | 75 to 82  | P00 to P07      | G                  | General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD00 to AD07    |                    | I/O pins for the lower 8 bits of the external address/data bus. This function is enabled when the external bus is enabled.                                              |
|          |           | INT8 to INT15   |                    | External interrupt request input pins.                                                                                                                                  |
| 85       | 83        | P10             | G                  | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.  |
|          |           | AD08            |                    | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                   |
|          |           | TIN1            |                    | Event input pin for reload timer 1.                                                                                                                                     |

(Continued)

# MB90860E Series

| Pin No.  |           | Pin name        | I/O<br>Circuit<br>type*3 | Function                                                                                                                                                               |
|----------|-----------|-----------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1 | LQFP100*2 |                 |                          |                                                                                                                                                                        |
| 86       | 84        | P11             | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD09            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |
|          |           | TOT1            |                          | Output pin for reload timer 1.                                                                                                                                         |
| 87       | 85        | P12             | N                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD10            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |
|          |           | SIN3            |                          | Serial data input pin for UART3.                                                                                                                                       |
|          |           | INT11R          |                          | External interrupt request input pin (sub) .                                                                                                                           |
| 88       | 86        | P13             | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD11            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |
|          |           | SOT3            |                          | Serial data output pin for UART3.                                                                                                                                      |
| 89       | 87        | P14             | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD12            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |
|          |           | SCK3            |                          | Clock I/O pin for UART3.                                                                                                                                               |
| 90       | 88        | V <sub>CC</sub> | —                        | Power (3.5 V to 5.5 V) input pin.                                                                                                                                      |
| 91       | 89        | V <sub>SS</sub> | —                        | GND pin.                                                                                                                                                               |
| 92       | 90        | X1              | A                        | Main clock output pin.                                                                                                                                                 |
| 93       | 91        | X0              |                          | Main clock input pin.                                                                                                                                                  |
| 94       | 92        | P15             | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD13            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |
| 95       | 93        | P16             | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode. |
|          |           | AD14            |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                  |

(Continued)

(Continued)

| Pin No.   |           | Pin name      | I/O<br>Circuit<br>type*3 | Function                                                                                                                                                                                                                                                                                  |
|-----------|-----------|---------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFP100*1  | LQFP100*2 |               |                          |                                                                                                                                                                                                                                                                                           |
| 96        | 94        | P17           | G                        | General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.                                                                                                                    |
|           |           | AD15          |                          | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.                                                                                                                                                                                     |
| 97 to 100 | 95 to 98  | P20 to P23    | G                        | General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. In external bus mode, each pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
|           |           | A16 to A19    |                          | Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).                                                                                           |
|           |           | PPG9, B, D, F |                          | PPG output pins.                                                                                                                                                                                                                                                                          |

\*1 : FPT-100P-M06

\*2 : FPT-100P-M20

\*3 : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.



# MB90860E Series

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks                                                                                                                                                                                                               |
|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A    |         | <p>Oscillator circuit</p> <p>High-speed oscillator feedback resistance = approx. 1 MΩ</p>                                                                                                                             |
| B    |         | <p>Oscillator circuit</p> <p>Low-speed oscillator feedback resistance = approx. 10 MΩ</p>                                                                                                                             |
| C    |         | <ul style="list-style-type: none"> <li>Mask ROM and evaluation device: CMOS hysteresis input pin</li> <li>Flash memory device: CMOS input pin</li> </ul>                                                              |
| D    |         | <ul style="list-style-type: none"> <li>Mask ROM and evaluation device: CMOS hysteresis input pin<br/>Pull-down resistor value: approx. 50 kΩ</li> <li>Flash memory device: CMOS input pin<br/>No pull-down</li> </ul> |
| E    |         | <p>CMOS hysteresis input pin</p> <p>Pull-up resistor value: approx. 50 kΩ</p>                                                                                                                                         |

(Continued)

| Type | Circuit | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> </ul>                                                                                                                                      |
| G    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> <li>• TTL input (with input shutdown in standby mode)</li> <li>• Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> </ul> |
| H    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>• CMOS hysteresis input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> </ul>                                                                                                                                      |

(Continued)

# MB90860E Series

| Type | Circuit | Remarks                                                                                                                                                                                                                                                                                                                                                     |
|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS hysteresis input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> <li>• A/D converter analog input</li> </ul>                              |
| J    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• D/A analog output</li> <li>• CMOS hysteresis input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> <li>• A/D converter analog input</li> </ul> |
| K    |         | Power supply input protection circuit                                                                                                                                                                                                                                                                                                                       |
| L    |         | <ul style="list-style-type: none"> <li>• A/D converter reference voltage power supply input pin with protection circuit</li> <li>• Flash devices do not have a protection circuit against <math>V_{CC}</math> for pin AVRH</li> </ul>                                                                                                                       |

(Continued)

(Continued)

| Type | Circuit | Remarks                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| M    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> </ul>                                                                                                                                 |
| N    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> <li>• TTL input (with input shutdown in standby mode)</li> </ul> <p>Programmable pull-up resistor: 50 k<math>\Omega</math> approx</p> |
| O    |         | <ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>• CMOS input (with input shutdown in standby mode)</li> <li>• Automotive input (with input shutdown in standby mode)</li> <li>• A/D converter analog input</li> </ul>                                                                                           |

## ■ HANDLING DEVICES

### 1. Preventing latch-up

Latch-up may occur in a CMOS IC under the following conditions :

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Therefore, be very careful not to apply analog power-supply voltages in excess of the digital power-supply voltages.

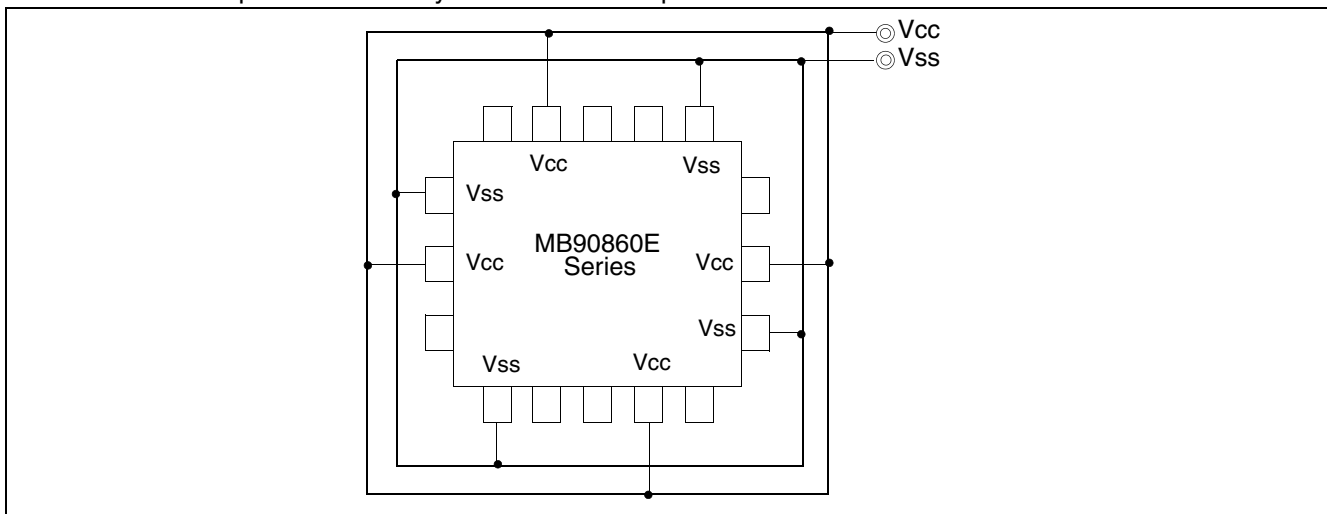
### 2. Handling unused pins

Leaving unused input pins open may cause malfunctions or permanent damages. Unused input pins must therefore be connected to a pull-up or pull-down resistor, with a resistance of 2 k $\Omega$  or more.

Unused bidirectional pins should be set to the output state and can then be left open, or set to the input state and handled as described above.

### 3. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.  
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally. Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



### 4. Mode pins (MD0 to MD2)

Connect the mode pins directly to the  $V_{CC}$  or  $V_{SS}$  pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.

## 5. Sequence for turning on the A/D converter power supply and analog inputs

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AVRH$ ,  $AVRL$ ) and analog inputs ( $AN0$  to  $AN23$ ) after turning on the digital power supply ( $V_{CC}$ ).

Turn off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed  $AVRH$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 6. Handling A/D converter pins when the A/D converter is not used

When the A/D converter is not used, connect the pins such that  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = AVRL = V_{SS}$ .

## 7. Crystal oscillator circuit

Noise near the  $X0$ ,  $X1$ ,  $X0A$ , and  $X1A$  pins can cause the device to malfunction. Design the printed circuit board such that the crystal oscillators (or ceramic oscillators) are as close to the  $X0$  and  $X1$  pins, and  $X0A$  and  $X1A$  pins as possible, and that the bypass capacitor to ground is as close to the device as possible. Furthermore, try as much as possible to prevent the wiring for these components from crossing over the wiring of other circuitry.

It is highly recommended that the printed circuit board artwork is designed such that the  $X0$ ,  $X1$  pins and  $X0A$ ,  $X1A$  pins are surrounded by ground plane, as this is expected to produce more stable operation.

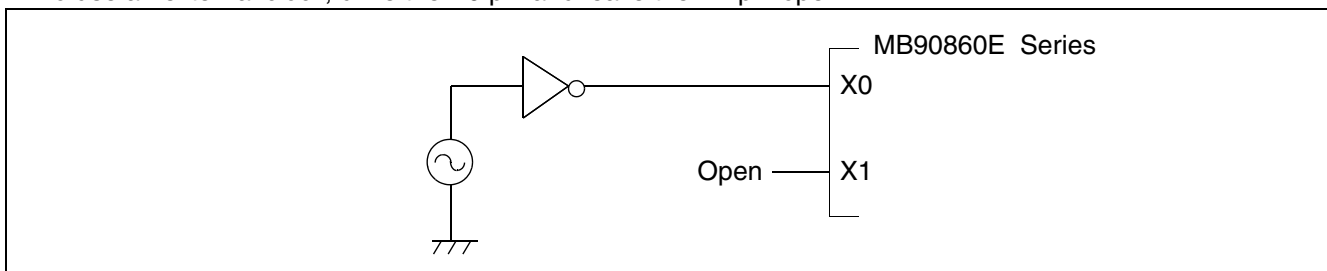
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

## 8. Pull-up/down resistors

The MB90860E series does not support internal pull-up/down resistors (however, port 0 to port 3 have built-in pull-up resistors). Use external components where needed.

## 9. Using external clock

To use an external clock, drive the  $X0$  pin and leave the  $X1$  pin open.



## 10. Precautions when not using a sub clock signal

If you do not connect pins  $X0A$  and  $X1A$  to an oscillator, connect the  $X0A$  pin to a pull-down resistance and leave the  $X1A$  pin open.

## 11. Precautions when operating in PLL clock mode

In the MB90860E series, if the oscillator is disconnected or the clock input is stopped while operating in PLL mode, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit contained in the PLL. However, operation under these circumstances is not guaranteed.

## 12. Precautions when turning the power on

To prevent the internal regulator circuit from malfunctioning, ensure that the time over which the voltage rises when the power is turned on is 50 or more  $\mu s$  (0.2 V to 2.7 V)

## 13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified  $V_{CC}$  supply voltage operating range. Therefore, the  $V_{CC}$  supply voltage should be stabilized.

As a reference, stabilize the supply voltage by meeting the following standards.

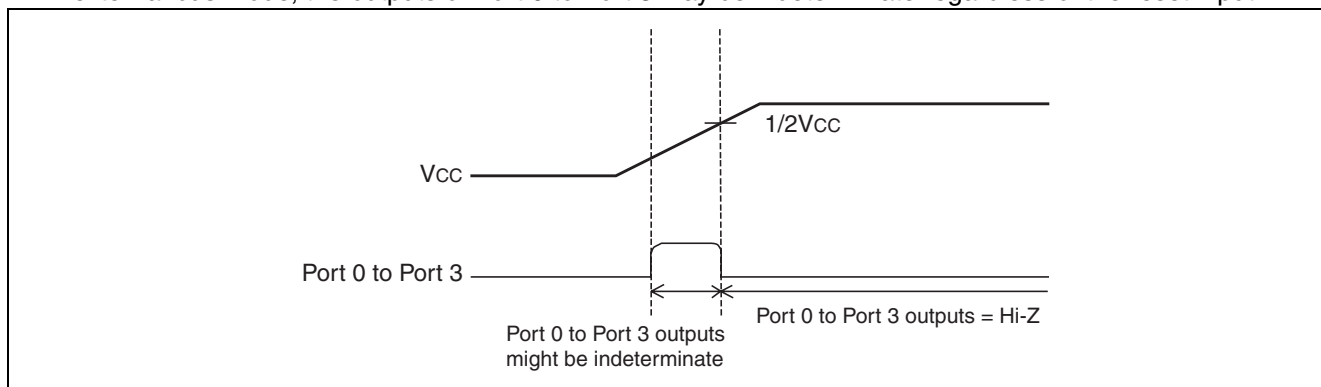
- $V_{CC}$  ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard  $V_{CC}$  supply voltage
- The coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

## 14. Initialization

The device has internal registers that are only initialized by a power-on reset only. To initialize these registers, turn on the power again.

## 15. Port 0 to port 3 output during power-on (external bus mode)

In external bus mode, the outputs of Port 0 to Port 3 may be indeterminate regardless of the reset input.



## 16. Flash security function

The security bit is located in the flash memory area. If protection code 01<sub>H</sub> is written to the security bit, the security function is applied to the flash memory.

Therefore do not write 01<sub>H</sub> to this address if you do not use the security function.

Please refer to following table for the address of the security bit.

|              | Flash memory size            | Address of security bit |
|--------------|------------------------------|-------------------------|
| MB90F867E(S) | Embedded 1 Mbit Flash Memory | FE0001 <sub>H</sub>     |

## 17. Serial communication

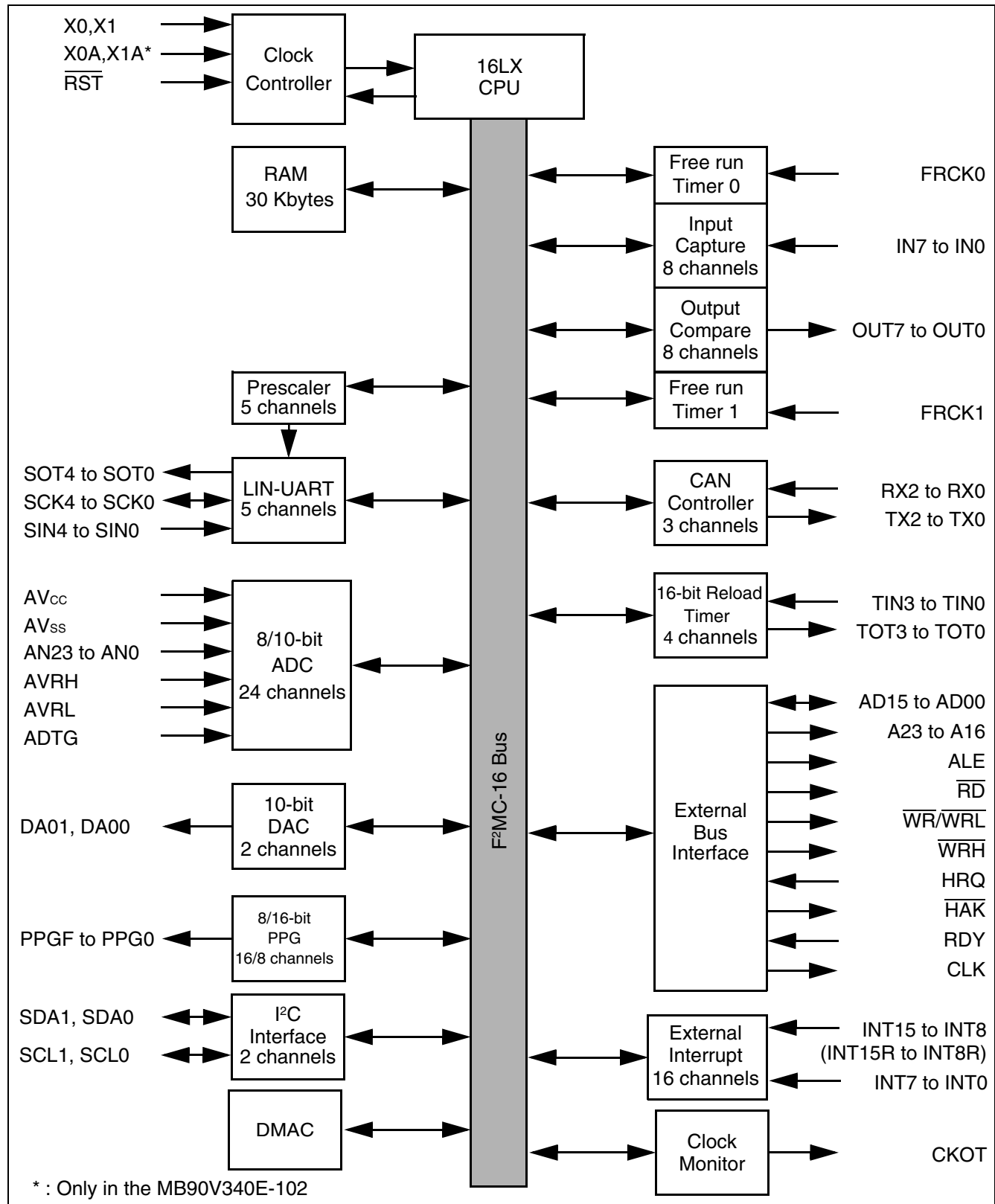
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

## ■ BLOCK DIAGRAMS

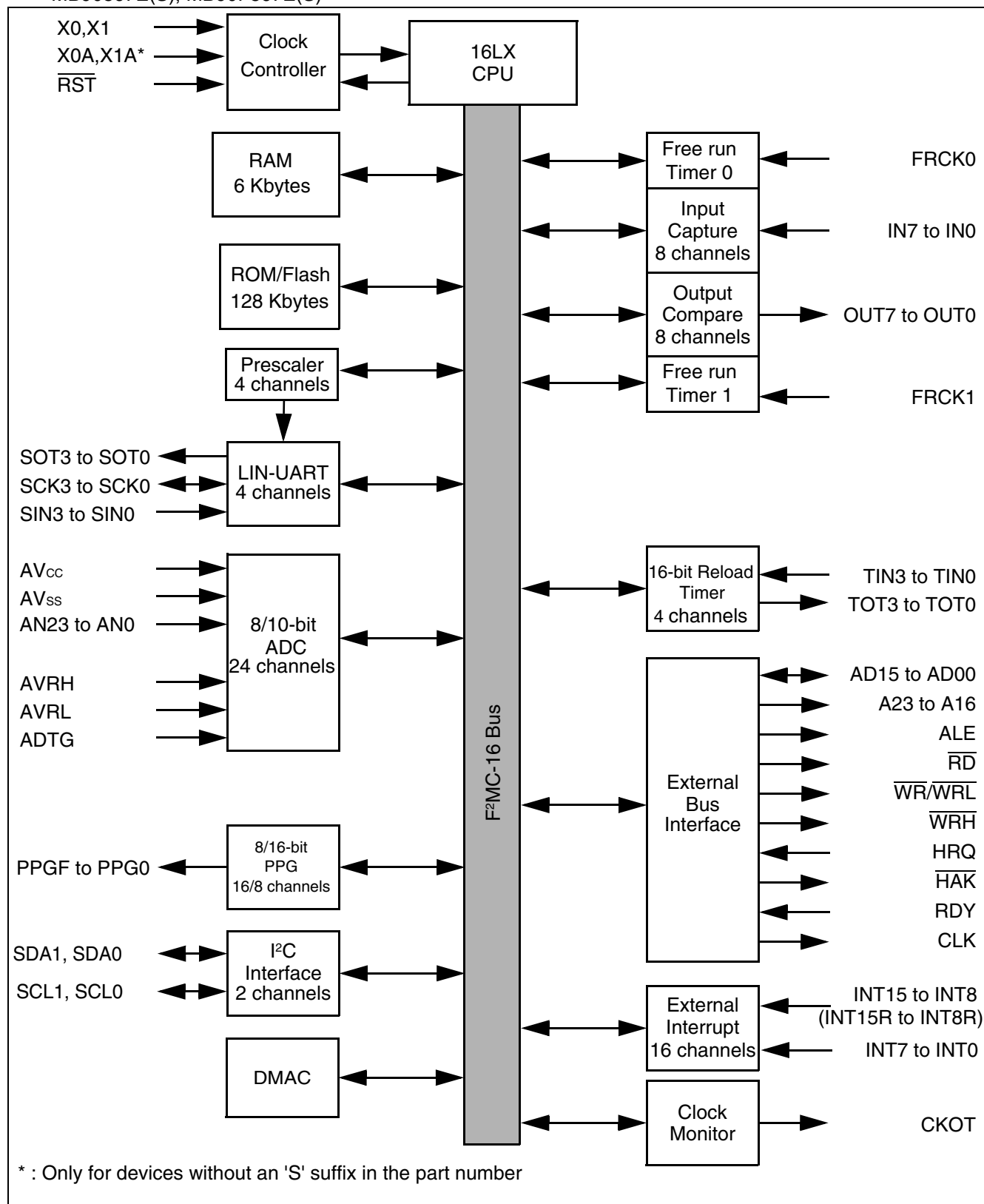
• MB90V340E-101/102



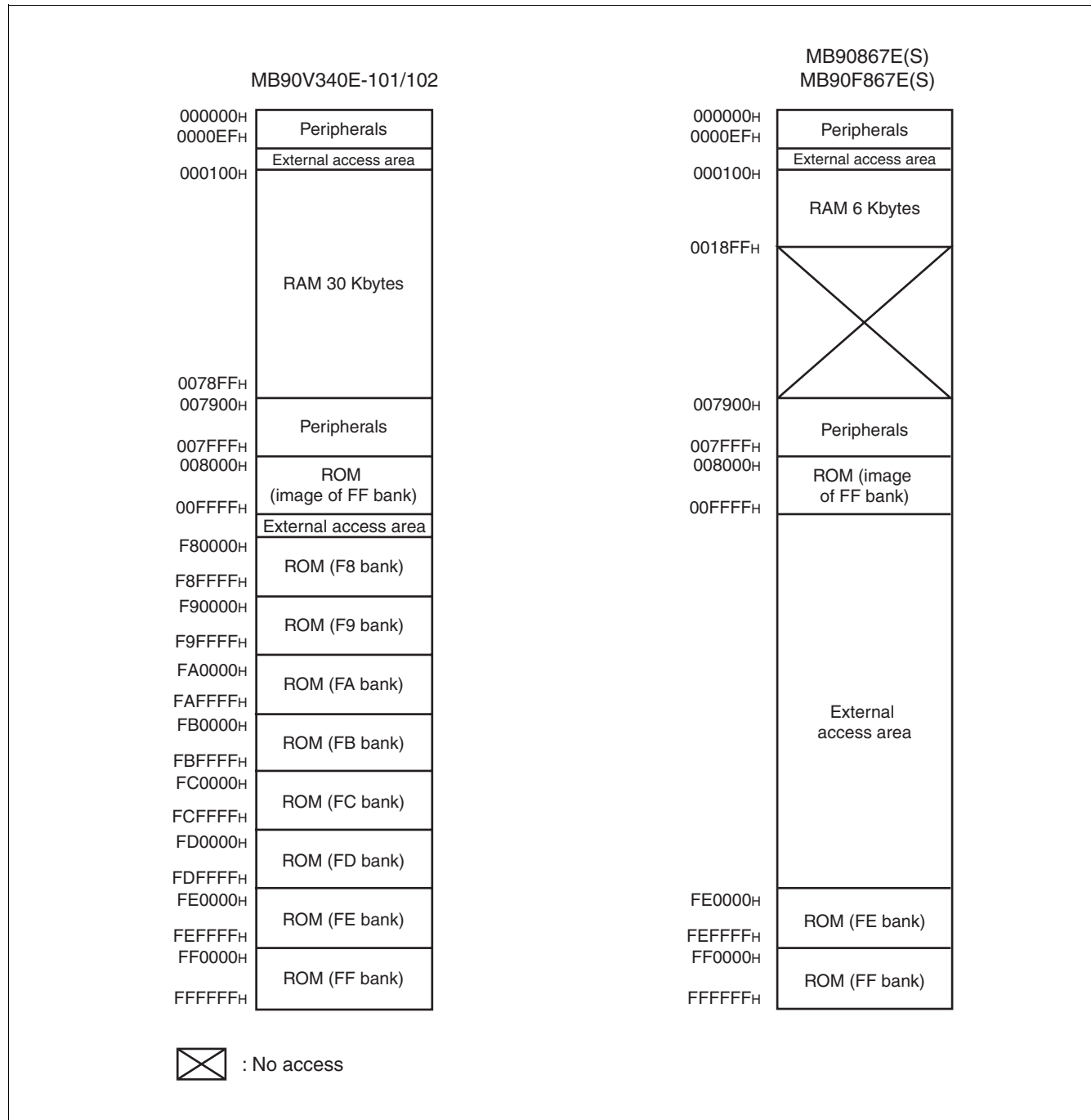


# MB90860E Series

- MB90867E(S), MB90F867E(S)



## ■ MEMORY MAP



Note : An image of the FF bank ROM data is visible in the upper part of bank 00. This makes it possible to use the C compiler small memory model. Because the lower 16 bits of addresses in the 00 bank and the FF bank are the same, tables in ROM can be referenced without using the far specifier in the pointer declarations. For example, an attempt to access 00C000H accesses the value at FFC000H in ROM. The ROM area in bank FF exceeds 32 Kbytes, and therefore, the entire image is not visible in bank 00. The image between FF8000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

# MB90860E Series

## ■ I/O MAP

| Address             | Register                            | Abbrevia-<br>tion | Access | Resource name | Initial value         |
|---------------------|-------------------------------------|-------------------|--------|---------------|-----------------------|
| 000000 <sub>H</sub> | Port 0 Data Register                | PDR0              | R/W    | Port 0        | XXXXXXXX <sub>B</sub> |
| 000001 <sub>H</sub> | Port 1 Data Register                | PDR1              | R/W    | Port 1        | XXXXXXXX <sub>B</sub> |
| 000002 <sub>H</sub> | Port 2 Data Register                | PDR2              | R/W    | Port 2        | XXXXXXXX <sub>B</sub> |
| 000003 <sub>H</sub> | Port 3 Data Register                | PDR3              | R/W    | Port 3        | XXXXXXXX <sub>B</sub> |
| 000004 <sub>H</sub> | Port 4 Data Register                | PDR4              | R/W    | Port 4        | XXXXXXXX <sub>B</sub> |
| 000005 <sub>H</sub> | Port 5 Data Register                | PDR5              | R/W    | Port 5        | XXXXXXXX <sub>B</sub> |
| 000006 <sub>H</sub> | Port 6 Data Register                | PDR6              | R/W    | Port 6        | XXXXXXXX <sub>B</sub> |
| 000007 <sub>H</sub> | Port 7 Data Register                | PDR7              | R/W    | Port 7        | XXXXXXXX <sub>B</sub> |
| 000008 <sub>H</sub> | Port 8 Data Register                | PDR8              | R/W    | Port 8        | XXXXXXXX <sub>B</sub> |
| 000009 <sub>H</sub> | Port 9 Data Register                | PDR9              | R/W    | Port 9        | XXXXXXXX <sub>B</sub> |
| 00000A <sub>H</sub> | Port A Data Register                | PDRA              | R/W    | Port A        | XXXXXXXX <sub>B</sub> |
| 00000B <sub>H</sub> | Port 5 Analog Input Enable Register | ADER5             | R/W    | Port 5, A/D   | 11111111 <sub>B</sub> |
| 00000C <sub>H</sub> | Port 6 Analog Input Enable Register | ADER6             | R/W    | Port 6, A/D   | 11111111 <sub>B</sub> |
| 00000D <sub>H</sub> | Port 7 Analog Input Enable Register | ADER7             | R/W    | Port 7, A/D   | 11111111 <sub>B</sub> |
| 00000E <sub>H</sub> | Input Level Select Register 0       | ILSR0             | R/W    | Ports         | XXXXXXXX <sub>B</sub> |
| 00000F <sub>H</sub> | Input Level Select Register 1       | ILSR1             | R/W    | Ports         | XXXX0XXX <sub>B</sub> |
| 000010 <sub>H</sub> | Port 0 Direction Register           | DDR0              | R/W    | Port 0        | 00000000 <sub>B</sub> |
| 000011 <sub>H</sub> | Port 1 Direction Register           | DDR1              | R/W    | Port 1        | 00000000 <sub>B</sub> |
| 000012 <sub>H</sub> | Port 2 Direction Register           | DDR2              | R/W    | Port 2        | 00000000 <sub>B</sub> |
| 000013 <sub>H</sub> | Port 3 Direction Register           | DDR3              | R/W    | Port 3        | 00000000 <sub>B</sub> |
| 000014 <sub>H</sub> | Port 4 Direction Register           | DDR4              | R/W    | Port 4        | 00000000 <sub>B</sub> |
| 000015 <sub>H</sub> | Port 5 Direction Register           | DDR5              | R/W    | Port 5        | 00000000 <sub>B</sub> |
| 000016 <sub>H</sub> | Port 6 Direction Register           | DDR6              | R/W    | Port 6        | 00000000 <sub>B</sub> |
| 000017 <sub>H</sub> | Port 7 Direction Register           | DDR7              | R/W    | Port 7        | 00000000 <sub>B</sub> |
| 000018 <sub>H</sub> | Port 8 Direction Register           | DDR8              | R/W    | Port 8        | 00000000 <sub>B</sub> |
| 000019 <sub>H</sub> | Port 9 Direction Register           | DDR9              | R/W    | Port 9        | 00000000 <sub>B</sub> |
| 00001A <sub>H</sub> | Port A Direction Register           | DDRA              | R/W    | Port A        | 00000100 <sub>B</sub> |
| 00001B <sub>H</sub> | Reserved                            |                   |        |               |                       |
| 00001C <sub>H</sub> | Port 0 Pull-up Control Register     | PUCR0             | R/W    | Port 0        | 00000000 <sub>B</sub> |
| 00001D <sub>H</sub> | Port 1 Pull-up Control Register     | PUCR1             | R/W    | Port 1        | 00000000 <sub>B</sub> |
| 00001E <sub>H</sub> | Port 2 Pull-up Control Register     | PUCR2             | R/W    | Port 2        | 00000000 <sub>B</sub> |
| 00001F <sub>H</sub> | Port 3 Pull-up Control Register     | PUCR3             | W, R/W | Port 3        | 00000000 <sub>B</sub> |

(Continued)

# MB90860E Series

| Address             | Register                                  | Abbrevia-<br>tion | Access      | Resource name             | Initial value         |
|---------------------|-------------------------------------------|-------------------|-------------|---------------------------|-----------------------|
| 000020 <sub>H</sub> | Serial Mode Register 0                    | SMR0              | W,R/W       | UART0                     | 00000000 <sub>B</sub> |
| 000021 <sub>H</sub> | Serial Control Register 0                 | SCR0              | W,R/W       |                           | 00000000 <sub>B</sub> |
| 000022 <sub>H</sub> | Receive/Transmit Data Register 0          | RDR0/<br>TDR0     | R/W         |                           | 00000000 <sub>B</sub> |
| 000023 <sub>H</sub> | Serial Status Register 0                  | SSR0              | R,R/W       |                           | 00001000 <sub>B</sub> |
| 000024 <sub>H</sub> | Extended Communication Control Register 0 | ECCR0             | R,W,<br>R/W |                           | 000000XX <sub>B</sub> |
| 000025 <sub>H</sub> | Extended Status/Control Register 0        | ESCR0             | R/W         |                           | 00000100 <sub>B</sub> |
| 000026 <sub>H</sub> | Baud Rate Generator Register 00           | BGR00             | R/W         |                           | 00000000 <sub>B</sub> |
| 000027 <sub>H</sub> | Baud Rate Generator Register 01           | BGR01             | R/W         |                           | 00000000 <sub>B</sub> |
| 000028 <sub>H</sub> | Serial Mode Register 1                    | SMR1              | W,R/W       | UART1                     | 00000000 <sub>B</sub> |
| 000029 <sub>H</sub> | Serial Control Register 1                 | SCR1              | W,R/W       |                           | 00000000 <sub>B</sub> |
| 00002A <sub>H</sub> | Receive/Transmit Data Register 1          | RDR1/<br>TDR1     | R/W         |                           | 00000000 <sub>B</sub> |
| 00002B <sub>H</sub> | Serial Status Register 1                  | SSR1              | R,R/W       |                           | 00001000 <sub>B</sub> |
| 00002C <sub>H</sub> | Extended Communication Control Register 1 | ECCR1             | R,W,<br>R/W |                           | 000000XX <sub>B</sub> |
| 00002D <sub>H</sub> | Extended Status/Control Register 1        | ESCR1             | R/W         |                           | 00000100 <sub>B</sub> |
| 00002E <sub>H</sub> | Baud Rate Generator Register 10           | BGR10             | R/W         |                           | 00000000 <sub>B</sub> |
| 00002F <sub>H</sub> | Baud Rate Generator Register 11           | BGR11             | R/W         |                           | 00000000 <sub>B</sub> |
| 000030 <sub>H</sub> | PPG 0 Operation Mode Control Register     | PPGC0             | W,R/W       | 16-bit PPG 0/1            | 0X000XX1 <sub>B</sub> |
| 000031 <sub>H</sub> | PPG 1 Operation Mode Control Register     | PPGC1             | W,R/W       |                           | 0X000001 <sub>B</sub> |
| 000032 <sub>H</sub> | PPG 0/PPG 1 Count Clock Select Register   | PPG01             | R/W         |                           | 000000X0 <sub>B</sub> |
| 000033 <sub>H</sub> | Reserved                                  |                   |             |                           |                       |
| 000034 <sub>H</sub> | PPG 2 Operation Mode Control Register     | PPGC2             | W,R/W       | 16-bit PPG 2/3            | 0X000XX1 <sub>B</sub> |
| 000035 <sub>H</sub> | PPG 3 Operation Mode Control Register     | PPGC3             | W,R/W       |                           | 0X000001 <sub>B</sub> |
| 000036 <sub>H</sub> | PPG 2/PPG 3 Count Clock Select Register   | PPG23             | R/W         |                           | 000000X0 <sub>B</sub> |
| 000037 <sub>H</sub> | Reserved                                  |                   |             |                           |                       |
| 000038 <sub>H</sub> | PPG 4 Operation Mode Control Register     | PPGC4             | W,R/W       | 16-bit PPG 4/5            | 0X000XX1 <sub>B</sub> |
| 000039 <sub>H</sub> | PPG 5 Operation Mode Control Register     | PPGC5             | W,R/W       |                           | 0X000001 <sub>B</sub> |
| 00003A <sub>H</sub> | PPG 4/PPG 5 Clock Select Register         | PPG45             | R/W         |                           | 000000X0 <sub>B</sub> |
| 00003B <sub>H</sub> | Address Detect Control Register 1         | PACSR1            | R/W         | Address Match Detection 1 | 00000000 <sub>B</sub> |
| 00003C <sub>H</sub> | PPG 6 Operation Mode Control Register     | PPGC6             | W,R/W       | 16-bit PPG 6/7            | 0X000XX1 <sub>B</sub> |
| 00003D <sub>H</sub> | PPG 7 Operation Mode Control Register     | PPGC7             | W,R/W       |                           | 0X000001 <sub>B</sub> |
| 00003E <sub>H</sub> | PPG 6/PPG 7 Count Clock Control Register  | PPG67             | R/W         |                           | 000000X0 <sub>B</sub> |
| 00003F <sub>H</sub> | Reserved                                  |                   |             |                           |                       |

(Continued)

# MB90860E Series

| Address             | Register                                 | Abbrevia-<br>tion | Access | Resource name      | Initial value         |
|---------------------|------------------------------------------|-------------------|--------|--------------------|-----------------------|
| 000040 <sub>H</sub> | PPG 8 Operation Mode Control Register    | PPGC8             | W,R/W  | 16-bit PPG 8/9     | 0X000XX1 <sub>B</sub> |
| 000041 <sub>H</sub> | PPG 9 Operation Mode Control Register    | PPGC9             | W,R/W  |                    | 0X000001 <sub>B</sub> |
| 000042 <sub>H</sub> | PPG 8/PPG 9 Count Clock Control Register | PPG89             | R/W    |                    | 000000X0 <sub>B</sub> |
| 000043 <sub>H</sub> | Reserved                                 |                   |        |                    |                       |
| 000044 <sub>H</sub> | PPG A Operation Mode Control Register    | PPGCA             | W,R/W  | 16-bit PPG A/B     | 0X000XX1 <sub>B</sub> |
| 000045 <sub>H</sub> | PPG B Operation Mode Control Register    | PPGCB             | W,R/W  |                    | 0X000001 <sub>B</sub> |
| 000046 <sub>H</sub> | PPG A/PPG B Count Clock Select Register  | PPGAB             | R/W    |                    | 000000X0 <sub>B</sub> |
| 000047 <sub>H</sub> | Reserved                                 |                   |        |                    |                       |
| 000048 <sub>H</sub> | PPG C Operation Mode Control Register    | PPGCC             | W,R/W  | 16-bit PPG C/D     | 0X000XX1 <sub>B</sub> |
| 000049 <sub>H</sub> | PPG D Operation Mode Control Register    | PPGCD             | W,R/W  |                    | 0X000001 <sub>B</sub> |
| 00004A <sub>H</sub> | PPG C/PPG D Count Clock Select Register  | PPGCD             | R/W    |                    | 000000X0 <sub>B</sub> |
| 00004B <sub>H</sub> | Reserved                                 |                   |        |                    |                       |
| 00004C <sub>H</sub> | PPG E Operation Mode Control Register    | PPGCE             | W,R/W  | 16-bit PPG E/F     | 0X000XX1 <sub>B</sub> |
| 00004D <sub>H</sub> | PPG F Operation Mode Control Register    | PPGCF             | W,R/W  |                    | 0X000001 <sub>B</sub> |
| 00004E <sub>H</sub> | PPG E/PPG F Count Clock Select Register  | PPGEF             | R/W    |                    | 000000X0 <sub>B</sub> |
| 00004F <sub>H</sub> | Reserved                                 |                   |        |                    |                       |
| 000050 <sub>H</sub> | Input Capture Control Status 0/1         | ICS01             | R/W    | Input Capture 0/1  | 00000000 <sub>B</sub> |
| 000051 <sub>H</sub> | Input Capture Edge 0/1                   | ICE01             | R/W, R |                    | XXX0X0XX <sub>B</sub> |
| 000052 <sub>H</sub> | Input Capture Control Status 2/3         | ICS23             | R/W    | Input Capture 2/3  | 00000000 <sub>B</sub> |
| 000053 <sub>H</sub> | Input Capture Edge 2/3                   | ICE23             | R      |                    | XXXXXXXX <sub>B</sub> |
| 000054 <sub>H</sub> | Input Capture Control Status 4/5         | ICS45             | R/W    | Input Capture 4/5  | 00000000 <sub>B</sub> |
| 000055 <sub>H</sub> | Input Capture Edge 4/5                   | ICE45             | R      |                    | XXXXXXXX <sub>B</sub> |
| 000056 <sub>H</sub> | Input Capture Control Status 6/7         | ICS67             | R/W    | Input Capture 6/7  | 00000000 <sub>B</sub> |
| 000057 <sub>H</sub> | Input Capture Edge 6/7                   | ICE67             | R/W, R |                    | XXX000XX <sub>B</sub> |
| 000058 <sub>H</sub> | Output Compare Control Status 0          | OCS0              | R/W    | Output Compare 0/1 | 0000XX00 <sub>B</sub> |
| 000059 <sub>H</sub> | Output Compare Control Status 1          | OCS1              | R/W    |                    | 0XX00000 <sub>B</sub> |
| 00005A <sub>H</sub> | Output Compare Control Status 2          | OCS2              | R/W    | Output Compare 2/3 | 0000XX00 <sub>B</sub> |
| 00005B <sub>H</sub> | Output Compare Control Status 3          | OCS3              | R/W    |                    | 0XX00000 <sub>B</sub> |
| 00005C <sub>H</sub> | Output Compare Control Status 4          | OCS4              | R/W    | Output Compare 4/5 | 0000XX00 <sub>B</sub> |
| 00005D <sub>H</sub> | Output Compare Control Status 5          | OCS5              | R/W    |                    | 0XX00000 <sub>B</sub> |
| 00005E <sub>H</sub> | Output Compare Control Status 6          | OCS6              | R/W    | Output Compare 6/7 | 0000XX00 <sub>B</sub> |
| 00005F <sub>H</sub> | Output Compare Control Status 7          | OCS7              | R/W    |                    | 0XX00000 <sub>B</sub> |

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# MB90860E Series

| Address                                          | Register                                               | Abbrevia-<br>tion | Access | Resource name                | Initial value          |
|--------------------------------------------------|--------------------------------------------------------|-------------------|--------|------------------------------|------------------------|
| 000060 <sub>H</sub>                              | Timer Control Status 0                                 | TMCSR0            | R/W    | 16-bit Reload<br>Timer 0     | 00000000 <sub>B</sub>  |
| 000061 <sub>H</sub>                              | Timer Control Status 0                                 | TMCSR0            | R/W    |                              | XXXX0000 <sub>B</sub>  |
| 000062 <sub>H</sub>                              | Timer Control Status 1                                 | TMCSR1            | R/W    | 16-bit Reload<br>Timer 1     | 00000000 <sub>B</sub>  |
| 000063 <sub>H</sub>                              | Timer Control Status 1                                 | TMCSR1            | R/W    |                              | XXXX0000 <sub>B</sub>  |
| 000064 <sub>H</sub>                              | Timer Control Status 2                                 | TMCSR2            | R/W    | 16-bit Reload<br>Timer 2     | 00000000 <sub>B</sub>  |
| 000065 <sub>H</sub>                              | Timer Control Status 2                                 | TMCSR2            | R/W    |                              | XXXX0000 <sub>B</sub>  |
| 000066 <sub>H</sub>                              | Timer Control Status 3                                 | TMCSR3            | R/W    | 16-bit Reload<br>Timer 3     | 00000000 <sub>B</sub>  |
| 000067 <sub>H</sub>                              | Timer Control Status 3                                 | TMCSR3            | R/W    |                              | XXXX0000 <sub>B</sub>  |
| 000068 <sub>H</sub>                              | A/D Control Status 0                                   | ADCS0             | R/W    | A/D Converter                | 000XXXX0 <sub>B</sub>  |
| 000069 <sub>H</sub>                              | A/D Control Status 1                                   | ADCS1             | R/W    |                              | 0000000X <sub>B</sub>  |
| 00006A <sub>H</sub>                              | A/D Data 0                                             | ADCR0             | R      |                              | 00000000 <sub>B</sub>  |
| 00006B <sub>H</sub>                              | A/D Data 1                                             | ADCR1             | R      |                              | XXXXXX00 <sub>B</sub>  |
| 00006C <sub>H</sub>                              | ADC Setting 0                                          | ADSR0             | R/W    |                              | 00000000 <sub>B</sub>  |
| 00006D <sub>H</sub>                              | ADC Setting 1                                          | ADSR1             | R/W    |                              | 00000000 <sub>B</sub>  |
| 00006E <sub>H</sub>                              | Reserved                                               |                   |        |                              |                        |
| 00006F <sub>H</sub>                              | ROM Mirror Function Select                             | ROMM              | W      | ROM Mirror                   | XXXXXXXX1 <sub>B</sub> |
| 000070 <sub>H</sub><br>to<br>00009A <sub>H</sub> | Reserved                                               |                   |        |                              |                        |
| 00009B <sub>H</sub>                              | DMA Descriptor Channel Selection Register              | DCSR              | R/W    | DMA                          | 00000000 <sub>B</sub>  |
| 00009C <sub>H</sub>                              | DMA Status L Register                                  | DSRL              | R/W    |                              | 00000000 <sub>B</sub>  |
| 00009D <sub>H</sub>                              | DMA Status H Register                                  | DSRH              | R/W    |                              | 00000000 <sub>B</sub>  |
| 00009E <sub>H</sub>                              | Address Detect Control Register 0                      | PACSR0            | R/W    | Address Match<br>Detection 0 | 00000000 <sub>B</sub>  |
| 00009F <sub>H</sub>                              | Delayed Interrupt Source Generate/<br>Release Register | DIRR              | R/W    | Delayed Interrupt            | XXXXXXXX0 <sub>B</sub> |
| 0000A0 <sub>H</sub>                              | Low-power Mode Control Register                        | LPMCR             | W,R/W  | Low Power<br>Control Circuit | 00011000 <sub>B</sub>  |
| 0000A1 <sub>H</sub>                              | Clock Selection Register                               | CKSCR             | R,R/W  | Low Power<br>Control Circuit | 11111100 <sub>B</sub>  |
| 0000A2 <sub>H</sub> ,<br>0000A3 <sub>H</sub>     | Reserved                                               |                   |        |                              |                        |
| 0000A4 <sub>H</sub>                              | DMA Stop Status Register                               | DSSR              | R/W    | DMA                          | 00000000 <sub>B</sub>  |
| 0000A5 <sub>H</sub>                              | Automatic Ready Function Select Register               | ARSR              | W      | External Memory<br>Access    | 0011XX00 <sub>B</sub>  |
| 0000A6 <sub>H</sub>                              | External Address Output Control Register               | HACR              | W      |                              | 00000000 <sub>B</sub>  |
| 0000A7 <sub>H</sub>                              | Bus Control Signal Selection Register                  | ECSR              | W      |                              | 0000000X <sub>B</sub>  |

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# MB90860E Series

| Address                                      | Register                                                                     | Abbrevia-<br>tion | Access | Resource name        | Initial value          |
|----------------------------------------------|------------------------------------------------------------------------------|-------------------|--------|----------------------|------------------------|
| 0000A8 <sub>H</sub>                          | Watchdog Control Register                                                    | WDTC              | R,W    | Watchdog Timer       | XXXXXX111 <sub>B</sub> |
| 0000A9 <sub>H</sub>                          | Time Base Timer Control Register                                             | TBTC              | W,R/W  | Time Base Timer      | 1XX00100 <sub>B</sub>  |
| 0000AA <sub>H</sub>                          | Watch Timer Control Register                                                 | WTC               | R,R/W  | Watch Timer          | 1X001000 <sub>B</sub>  |
| 0000AB <sub>H</sub>                          | Reserved                                                                     |                   |        |                      |                        |
| 0000AC <sub>H</sub>                          | DMA Enable L Register                                                        | DERL              | R/W    | DMA                  | 00000000 <sub>B</sub>  |
| 0000AD <sub>H</sub>                          | DMA Enable H Register                                                        | DERH              | R/W    |                      | 00000000 <sub>B</sub>  |
| 0000AE <sub>H</sub>                          | Flash Control Status Register<br>(Flash Devices only.<br>Otherwise reserved) | FMCS              | R,R/W  | Flash Memory         | 000X0000 <sub>B</sub>  |
| 0000AF <sub>H</sub>                          | Reserved                                                                     |                   |        |                      |                        |
| 0000B0 <sub>H</sub>                          | Interrupt Control Register 00                                                | ICR00             | W,R/W  | Interrupt Control    | 00000111 <sub>B</sub>  |
| 0000B1 <sub>H</sub>                          | Interrupt Control Register 01                                                | ICR01             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B2 <sub>H</sub>                          | Interrupt Control Register 02                                                | ICR02             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B3 <sub>H</sub>                          | Interrupt Control Register 03                                                | ICR03             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B4 <sub>H</sub>                          | Interrupt Control Register 04                                                | ICR04             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B5 <sub>H</sub>                          | Interrupt Control Register 05                                                | ICR05             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B6 <sub>H</sub>                          | Interrupt Control Register 06                                                | ICR06             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B7 <sub>H</sub>                          | Interrupt Control Register 07                                                | ICR07             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B8 <sub>H</sub>                          | Interrupt Control Register 08                                                | ICR08             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000B9 <sub>H</sub>                          | Interrupt Control Register 09                                                | ICR09             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BA <sub>H</sub>                          | Interrupt Control Register 10                                                | ICR10             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BB <sub>H</sub>                          | Interrupt Control Register 11                                                | ICR11             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BC <sub>H</sub>                          | Interrupt Control Register 12                                                | ICR12             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BD <sub>H</sub>                          | Interrupt Control Register 13                                                | ICR13             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BE <sub>H</sub>                          | Interrupt Control Register 14                                                | ICR14             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000BF <sub>H</sub>                          | Interrupt Control Register 15                                                | ICR15             | W,R/W  |                      | 00000111 <sub>B</sub>  |
| 0000C0 <sub>H</sub>                          | D/A Converter Data 0 Register                                                | DAT0              | R/W    | D/A Converter        | XXXXXXXXX <sub>B</sub> |
| 0000C1 <sub>H</sub>                          | D/A Converter Data 1 Register                                                | DAT1              | R/W    |                      | XXXXXXXXX <sub>B</sub> |
| 0000C2 <sub>H</sub>                          | D/A Control 0 Register                                                       | DACR0             | R/W    |                      | XXXXXXXX0 <sub>B</sub> |
| 0000C3 <sub>H</sub>                          | D/A Control 1 Register                                                       | DACR1             | R/W    |                      | XXXXXXXX0 <sub>B</sub> |
| 0000C4 <sub>H</sub> ,<br>0000C5 <sub>H</sub> | Reserved                                                                     |                   |        |                      |                        |
| 0000C6 <sub>H</sub>                          | External Interrupt Enable 0                                                  | ENIR0             | R/W    | External Interrupt 0 | 00000000 <sub>B</sub>  |
| 0000C7 <sub>H</sub>                          | External Interrupt Source 0                                                  | EIRR0             | R/W    |                      | XXXXXXXXX <sub>B</sub> |
| 0000C8 <sub>H</sub>                          | External Interrupt Level Setting 0                                           | ELVR0             | R/W    |                      | 00000000 <sub>B</sub>  |
| 0000C9 <sub>H</sub>                          | External Interrupt Level Setting 0                                           | ELVR0             | R/W    |                      | 00000000 <sub>B</sub>  |

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| Address                                          | Register                                  | Abbrevia-<br>tion | Access      | Resource name        | Initial value         |
|--------------------------------------------------|-------------------------------------------|-------------------|-------------|----------------------|-----------------------|
| 0000CA <sub>H</sub>                              | External Interrupt Enable 1               | ENIR1             | R/W         | External Interrupt 1 | 00000000 <sub>B</sub> |
| 0000CB <sub>H</sub>                              | External Interrupt Source 1               | EIRR1             | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000CC <sub>H</sub>                              | External Interrupt Level Setting 1        | ELVR1             | R/W         |                      | 00000000 <sub>B</sub> |
| 0000CD <sub>H</sub>                              | External Interrupt Level Setting 1        | ELVR1             | R/W         |                      | 00000000 <sub>B</sub> |
| 0000CE <sub>H</sub>                              | External Interrupt Source Select          | EISSR             | R/W         |                      | 00000000 <sub>B</sub> |
| 0000CF <sub>H</sub>                              | PLL/Sub Clock Control Register            | PSCCR             | W           | PLL                  | XXXX0000 <sub>B</sub> |
| 0000D0 <sub>H</sub>                              | DMA Buffer Address Pointer L Register     | BAPL              | R/W         | DMA                  | XXXXXXXX <sub>B</sub> |
| 0000D1 <sub>H</sub>                              | DMA Buffer Address Pointer M Register     | BAPM              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D2 <sub>H</sub>                              | DMA Buffer Address Pointer H Register     | BAPH              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D3 <sub>H</sub>                              | DMA Control Register                      | DMACS             | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D4 <sub>H</sub>                              | I/O Register Address Pointer L Register   | IOAL              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D5 <sub>H</sub>                              | I/O Register Address Pointer H Register   | IOAH              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D6 <sub>H</sub>                              | Data Counter L Register                   | DCTL              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D7 <sub>H</sub>                              | Data Counter H Register                   | DCTH              | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 0000D8 <sub>H</sub>                              | Serial Mode Register 2                    | SMR2              | W,R/W       | UART2                | 00000000 <sub>B</sub> |
| 0000D9 <sub>H</sub>                              | Serial Control Register 2                 | SCR2              | W,R/W       |                      | 00000000 <sub>B</sub> |
| 0000DA <sub>H</sub>                              | Receive/Transmit Data Register 2          | RDR2/<br>TDR2     | R/W         |                      | 00000000 <sub>B</sub> |
| 0000DB <sub>H</sub>                              | Serial Status Register 2                  | SSR2              | R,R/W       |                      | 00001000 <sub>B</sub> |
| 0000DC <sub>H</sub>                              | Extended Communication Control Register 2 | ECCR2             | R,W,<br>R/W |                      | 000000XX <sub>B</sub> |
| 0000DD <sub>H</sub>                              | Extended Status Control Register 2        | ESCR2             | R/W         |                      | 00000100 <sub>B</sub> |
| 0000DE <sub>H</sub>                              | Baud Rate Generator Register 20           | BGR20             | R/W         |                      | 00000000 <sub>B</sub> |
| 0000DF <sub>H</sub>                              | Baud Rate Generator Register 21           | BGR21             | R/W         |                      | 00000000 <sub>B</sub> |
| 0000E0 <sub>H</sub><br>to<br>0000FF <sub>H</sub> | External area                             |                   |             |                      |                       |
| 007900 <sub>H</sub>                              | Reload Register L0                        | PRLLO             | R/W         | 16-bit PPG 0/1       | XXXXXXXX <sub>B</sub> |
| 007901 <sub>H</sub>                              | Reload Register H0                        | PRLH0             | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 007902 <sub>H</sub>                              | Reload Register L1                        | PRLLO1            | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 007903 <sub>H</sub>                              | Reload Register H1                        | PRLH1             | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 007904 <sub>H</sub>                              | Reload Register L2                        | PRLLO2            | R/W         | 16-bit PPG 2/3       | XXXXXXXX <sub>B</sub> |
| 007905 <sub>H</sub>                              | Reload Register H2                        | PRLH2             | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 007906 <sub>H</sub>                              | Reload Register L3                        | PRLLO3            | R/W         |                      | XXXXXXXX <sub>B</sub> |
| 007907 <sub>H</sub>                              | Reload Register H3                        | PRLH3             | R/W         |                      | XXXXXXXX <sub>B</sub> |

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# MB90860E Series

| Address             | Register           | Abbrevia-<br>tion | Access | Resource name     | Initial value         |
|---------------------|--------------------|-------------------|--------|-------------------|-----------------------|
| 007908 <sub>H</sub> | Reload Register L4 | PRLL4             | R/W    | 16-bit PPG 4/5    | XXXXXXXX <sub>B</sub> |
| 007909 <sub>H</sub> | Reload Register H4 | PRLH4             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00790A <sub>H</sub> | Reload Register L5 | PRLL5             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00790B <sub>H</sub> | Reload Register H5 | PRLH5             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00790C <sub>H</sub> | Reload Register L6 | PRLL6             | R/W    | 16-bit PPG 6/7    | XXXXXXXX <sub>B</sub> |
| 00790D <sub>H</sub> | Reload Register H6 | PRLH6             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00790E <sub>H</sub> | Reload Register L7 | PRLL7             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00790F <sub>H</sub> | Reload Register H7 | PRLH7             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007910 <sub>H</sub> | Reload Register L8 | PRLL8             | R/W    | 16-bit PPG 8/9    | XXXXXXXX <sub>B</sub> |
| 007911 <sub>H</sub> | Reload Register H8 | PRLH8             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007912 <sub>H</sub> | Reload Register L9 | PRLL9             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007913 <sub>H</sub> | Reload Register H9 | PRLH9             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007914 <sub>H</sub> | Reload Register LA | PRLLA             | R/W    | 16-bit PPG A/B    | XXXXXXXX <sub>B</sub> |
| 007915 <sub>H</sub> | Reload Register HA | PRLHA             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007916 <sub>H</sub> | Reload Register LB | PRLLB             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007917 <sub>H</sub> | Reload Register HB | PRLHB             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007918 <sub>H</sub> | Reload Register LC | PRLLC             | R/W    | 16-bit PPG C/D    | XXXXXXXX <sub>B</sub> |
| 007919 <sub>H</sub> | Reload Register HC | PRLHC             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00791A <sub>H</sub> | Reload Register LD | PRLLD             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00791B <sub>H</sub> | Reload Register HD | PRLHD             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00791C <sub>H</sub> | Reload Register LE | PRLLE             | R/W    | 16-bit PPG E/F    | XXXXXXXX <sub>B</sub> |
| 00791D <sub>H</sub> | Reload Register HE | PRLHE             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00791E <sub>H</sub> | Reload Register LF | PRLLF             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 00791F <sub>H</sub> | Reload Register HF | PRLHF             | R/W    |                   | XXXXXXXX <sub>B</sub> |
| 007920 <sub>H</sub> | Input Capture 0    | IPCP0             | R      | Input Capture 0/1 | XXXXXXXX <sub>B</sub> |
| 007921 <sub>H</sub> | Input Capture 0    | IPCP0             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007922 <sub>H</sub> | Input Capture 1    | IPCP1             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007923 <sub>H</sub> | Input Capture 1    | IPCP1             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007924 <sub>H</sub> | Input Capture 2    | IPCP2             | R      | Input Capture 2/3 | XXXXXXXX <sub>B</sub> |
| 007925 <sub>H</sub> | Input Capture 2    | IPCP2             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007926 <sub>H</sub> | Input Capture 3    | IPCP3             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007927 <sub>H</sub> | Input Capture 3    | IPCP3             | R      |                   | XXXXXXXX <sub>B</sub> |
| 007928 <sub>H</sub> | Input Capture 4    | IPCP4             | R      | Input Capture 4/5 | XXXXXXXX <sub>B</sub> |
| 007929 <sub>H</sub> | Input Capture 4    | IPCP4             | R      |                   | XXXXXXXX <sub>B</sub> |
| 00792A <sub>H</sub> | Input Capture 5    | IPCP5             | R      |                   | XXXXXXXX <sub>B</sub> |
| 00792B <sub>H</sub> | Input Capture 5    | IPCP5             | R      |                   | XXXXXXXX <sub>B</sub> |

(Continued)

| Address             | Register               | Abbrevia-<br>tion | Access | Resource name            | Initial value          |
|---------------------|------------------------|-------------------|--------|--------------------------|------------------------|
| 00792C <sub>H</sub> | Input Capture 6        | IPCP6             | R      | Input Capture 6/7        | XXXXXXXX <sub>B</sub>  |
| 00792D <sub>H</sub> | Input Capture 6        | IPCP6             | R      |                          | XXXXXXXX <sub>B</sub>  |
| 00792E <sub>H</sub> | Input Capture 7        | IPCP7             | R      |                          | XXXXXXXX <sub>B</sub>  |
| 00792F <sub>H</sub> | Input Capture 7        | IPCP7             | R      |                          | XXXXXXXX <sub>B</sub>  |
| 007930 <sub>H</sub> | Output Compare 0       | OCCP0             | R/W    | Output Compare 0/1       | XXXXXXXX <sub>B</sub>  |
| 007931 <sub>H</sub> | Output Compare 0       | OCCP0             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007932 <sub>H</sub> | Output Compare 1       | OCCP1             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007933 <sub>H</sub> | Output Compare 1       | OCCP1             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007934 <sub>H</sub> | Output Compare 2       | OCCP2             | R/W    | Output Compare 2/3       | XXXXXXXX <sub>B</sub>  |
| 007935 <sub>H</sub> | Output Compare 2       | OCCP2             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007936 <sub>H</sub> | Output Compare 3       | OCCP3             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007937 <sub>H</sub> | Output Compare 3       | OCCP3             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007938 <sub>H</sub> | Output Compare 4       | OCCP4             | R/W    | Output Compare 4/5       | XXXXXXXX <sub>B</sub>  |
| 007939 <sub>H</sub> | Output Compare 4       | OCCP4             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00793A <sub>H</sub> | Output Compare 5       | OCCP5             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00793B <sub>H</sub> | Output Compare 5       | OCCP5             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00793C <sub>H</sub> | Output Compare 6       | OCCP6             | R/W    | Output Compare 6/7       | XXXXXXXX <sub>B</sub>  |
| 00793D <sub>H</sub> | Output Compare 6       | OCCP6             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00793E <sub>H</sub> | Output Compare 7       | OCCP7             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00793F <sub>H</sub> | Output Compare 7       | OCCP7             | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 007940 <sub>H</sub> | Timer Data 0           | TCDT0             | R/W    | Free-run Timer 0         | 00000000 <sub>B</sub>  |
| 007941 <sub>H</sub> | Timer Data 0           | TCDT0             | R/W    |                          | 00000000 <sub>B</sub>  |
| 007942 <sub>H</sub> | Timer Control Status 0 | TCCSL0            | R/W    |                          | 00000000 <sub>B</sub>  |
| 007943 <sub>H</sub> | Timer Control Status 0 | TCCSH0            | R/W    |                          | 0XXXXXXXX <sub>B</sub> |
| 007944 <sub>H</sub> | Timer Data 1           | TCDT1             | R/W    | Free-run Timer 1         | 00000000 <sub>B</sub>  |
| 007945 <sub>H</sub> | Timer Data 1           | TCDT1             | R/W    |                          | 00000000 <sub>B</sub>  |
| 007946 <sub>H</sub> | Timer Control Status 1 | TCCSL1            | R/W    |                          | 00000000 <sub>B</sub>  |
| 007947 <sub>H</sub> | Timer Control Status 1 | TCCSH1            | R/W    |                          | 0XXXXXXXX <sub>B</sub> |
| 007948 <sub>H</sub> | Timer 0/Reload 0       | TMR0/             | R/W    | 16-bit Reload<br>Timer 0 | XXXXXXXX <sub>B</sub>  |
| 007949 <sub>H</sub> |                        | TMRLR0            | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00794A <sub>H</sub> | Timer 1/Reload 1       | TMR1/             | R/W    | 16-bit Reload<br>Timer 1 | XXXXXXXX <sub>B</sub>  |
| 00794B <sub>H</sub> |                        | TMRLR1            | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00794C <sub>H</sub> | Timer 2/Reload 2       | TMR2/             | R/W    | 16-bit Reload<br>Timer 2 | XXXXXXXX <sub>B</sub>  |
| 00794D <sub>H</sub> |                        | TMRLR2            | R/W    |                          | XXXXXXXX <sub>B</sub>  |
| 00794E <sub>H</sub> | Timer 3/Reload 3       | TMR3/             | R/W    | 16-bit Reload<br>Timer 3 | XXXXXXXX <sub>B</sub>  |
| 00794F <sub>H</sub> |                        | TMRLR3            | R/W    |                          | XXXXXXXX <sub>B</sub>  |

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# MB90860E Series

| Address                                          | Register                                              | Abbrevia-<br>tion | Access      | Resource name                | Initial value         |
|--------------------------------------------------|-------------------------------------------------------|-------------------|-------------|------------------------------|-----------------------|
| 007950 <sub>H</sub>                              | Serial Mode Register 3                                | SMR3              | W,R/W       | UART3                        | 00000000 <sub>B</sub> |
| 007951 <sub>H</sub>                              | Serial Control Register 3                             | SCR3              | W,R/W       |                              | 00000000 <sub>B</sub> |
| 007952 <sub>H</sub>                              | Receive/Transmit Data Register 3                      | RDR3/<br>TDR3     | R/W         |                              | 00000000 <sub>B</sub> |
| 007953 <sub>H</sub>                              | Serial Status Register 3                              | SSR3              | R,R/W       |                              | 00001000 <sub>B</sub> |
| 007954 <sub>H</sub>                              | Extended Communication Control Register 3             | ECCR3             | R,W,<br>R/W |                              | 000000XX <sub>B</sub> |
| 007955 <sub>H</sub>                              | Extended Status Control Register                      | ESCR3             | R/W         |                              | 00000100 <sub>B</sub> |
| 007956 <sub>H</sub>                              | Baud Rate Generator Register 30                       | BGR30             | R/W         |                              | 00000000 <sub>B</sub> |
| 007957 <sub>H</sub>                              | Baud Rate Generator Register 31                       | BGR31             | R/W         |                              | 00000000 <sub>B</sub> |
| 007958 <sub>H</sub>                              | Serial Mode Register 4                                | SMR4              | W,R/W       | UART4                        | 00000000 <sub>B</sub> |
| 007959 <sub>H</sub>                              | Serial Control Register 4                             | SCR4              | W,R/W       |                              | 00000000 <sub>B</sub> |
| 00795A <sub>H</sub>                              | Receive/Transmit Data Register 4                      | RDR4/<br>TDR4     | R/W         |                              | 00000000 <sub>B</sub> |
| 00795B <sub>H</sub>                              | Serial Status Register 4                              | SSR4              | R,R/W       |                              | 00001000 <sub>B</sub> |
| 00795C <sub>H</sub>                              | Extended Communication Control Register 4             | ECCR4             | R,W,<br>R/W |                              | 000000XX <sub>B</sub> |
| 00795D <sub>H</sub>                              | Extended Status Control Register                      | ESCR4             | R/W         |                              | 00000100 <sub>B</sub> |
| 00795E <sub>H</sub>                              | Baud Rate Generator Register 40                       | BGR40             | R/W         |                              | 00000000 <sub>B</sub> |
| 00795F <sub>H</sub>                              | Baud Rate Generator Register 41                       | BGR41             | R/W         |                              | 00000000 <sub>B</sub> |
| 007960 <sub>H</sub><br>to<br>00796B <sub>H</sub> | Reserved                                              |                   |             |                              |                       |
| 00796C <sub>H</sub>                              | Clock Output Enable Register                          | CLKR              | R/W         | Clock Monitor                | XXXX0000 <sub>B</sub> |
| 00796D <sub>H</sub><br>to<br>00796F <sub>H</sub> | Reserved                                              |                   |             |                              |                       |
| 007970 <sub>H</sub>                              | I <sup>2</sup> C Bus Status Register 0                | IBSR0             | R           | I <sup>2</sup> C Interface 0 | 00000000 <sub>B</sub> |
| 007971 <sub>H</sub>                              | I <sup>2</sup> C bus Control Register 0               | IBCR0             | W,R/W       |                              | 00000000 <sub>B</sub> |
| 007972 <sub>H</sub>                              | I <sup>2</sup> C 10-bit Slave Address Register 0      | ITBAL0            | R/W         |                              | 00000000 <sub>B</sub> |
| 007973 <sub>H</sub>                              |                                                       | ITBAH0            | R/W         |                              | 00000000 <sub>B</sub> |
| 007974 <sub>H</sub>                              | I <sup>2</sup> C 10-bit Slave Address Mask Register 0 | ITMKL0            | R/W         |                              | 11111111 <sub>B</sub> |
| 007975 <sub>H</sub>                              |                                                       | ITMKH0            | R/W         |                              | 00111111 <sub>B</sub> |
| 007976 <sub>H</sub>                              | I <sup>2</sup> C 7-bit Slave Address Register 0       | ISBA0             | R/W         |                              | 00000000 <sub>B</sub> |
| 007977 <sub>H</sub>                              | I <sup>2</sup> C 7-bit Slave Address Mask Register 0  | ISMK0             | R/W         |                              | 01111111 <sub>B</sub> |
| 007978 <sub>H</sub>                              | I <sup>2</sup> C Data Register 0                      | IDAR0             | R/W         |                              | 00000000 <sub>B</sub> |
| 007979 <sub>H</sub> ,<br>00797A <sub>H</sub>     | Reserved                                              |                   |             |                              |                       |

(Continued)

| Address                                          | Register                                              | Abbrevia-<br>tion | Access | Resource name                | Initial value         |
|--------------------------------------------------|-------------------------------------------------------|-------------------|--------|------------------------------|-----------------------|
| 00797B <sub>H</sub>                              | I <sup>2</sup> C Clock Control Register 0             | ICCR0             | R/W    | I <sup>2</sup> C Interface 0 | 00011111 <sub>B</sub> |
| 00797C <sub>H</sub><br>to<br>00797F <sub>H</sub> | Reserved                                              |                   |        |                              |                       |
| 007980 <sub>H</sub>                              | I <sup>2</sup> C Bus Status Register 1                | IBSR1             | R      | I <sup>2</sup> C Interface 1 | 00000000 <sub>B</sub> |
| 007981 <sub>H</sub>                              | I <sup>2</sup> C Bus Control Register 1               | IBCR1             | W,R/W  |                              | 00000000 <sub>B</sub> |
| 007982 <sub>H</sub>                              | I <sup>2</sup> C 10-bit Slave Address Register 1      | ITBAL1            | R/W    |                              | 00000000 <sub>B</sub> |
| 007983 <sub>H</sub>                              |                                                       | ITBAH1            | R/W    |                              | 00000000 <sub>B</sub> |
| 007984 <sub>H</sub>                              | I <sup>2</sup> C 10-bit Slave Address Mask Register 1 | ITMKL1            | R/W    |                              | 11111111 <sub>B</sub> |
| 007985 <sub>H</sub>                              |                                                       | ITMKH1            | R/W    |                              | 00111111 <sub>B</sub> |
| 007986 <sub>H</sub>                              | I <sup>2</sup> C 7-bit Slave Address Register 1       | ISBA1             | R/W    |                              | 00000000 <sub>B</sub> |
| 007987 <sub>H</sub>                              | I <sup>2</sup> C 7-bit Slave Address Mask Register 1  | ISMK1             | R/W    |                              | 01111111 <sub>B</sub> |
| 007988 <sub>H</sub>                              | I <sup>2</sup> C Data Register 1                      | IDAR1             | R/W    |                              | 00000000 <sub>B</sub> |
| 007989 <sub>H</sub> ,<br>00798A <sub>H</sub>     | Reserved                                              |                   |        |                              |                       |
| 00798B <sub>H</sub>                              | I <sup>2</sup> C Clock Control Register 1             | ICCR1             | R/W    | I <sup>2</sup> C Interface 1 | 00011111 <sub>B</sub> |
| 00798C <sub>H</sub><br>to<br>0079C1 <sub>H</sub> | Reserved                                              |                   |        |                              |                       |
| 0079C2 <sub>H</sub>                              | Clock Modulator Control Register                      | CMCR              | R, R/W | Clock Modulator              | 0001X000 <sub>B</sub> |
| 0079C3 <sub>H</sub><br>to<br>0079DF <sub>H</sub> | Reserved                                              |                   |        |                              |                       |
| 0079E0 <sub>H</sub>                              | Detect Address Setting 0                              | PADR0             | R/W    | Address Match Detection 0    | XXXXXXXX <sub>B</sub> |
| 0079E1 <sub>H</sub>                              | Detect Address Setting 0                              | PADR0             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E2 <sub>H</sub>                              | Detect Address Setting 0                              | PADR0             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E3 <sub>H</sub>                              | Detect Address Setting 1                              | PADR1             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E4 <sub>H</sub>                              | Detect Address Setting 1                              | PADR1             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E5 <sub>H</sub>                              | Detect Address Setting 1                              | PADR1             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E6 <sub>H</sub>                              | Detect Address Setting 2                              | PADR2             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E7 <sub>H</sub>                              | Detect Address Setting 2                              | PADR2             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E8 <sub>H</sub>                              | Detect Address Setting 2                              | PADR2             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079E9 <sub>H</sub><br>to<br>0079EF <sub>H</sub> | Reserved                                              |                   |        |                              |                       |

(Continued)

# MB90860E Series

(Continued)

| Address                                          | Register                 | Abbrevia-<br>tion | Access | Resource name                | Initial value         |
|--------------------------------------------------|--------------------------|-------------------|--------|------------------------------|-----------------------|
| 0079F0 <sub>H</sub>                              | Detect Address Setting 3 | PADR3             | R/W    | Address Match<br>Detection 1 | XXXXXXXX <sub>B</sub> |
| 0079F1 <sub>H</sub>                              | Detect Address Setting 3 | PADR3             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F2 <sub>H</sub>                              | Detect Address Setting 3 | PADR3             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F3 <sub>H</sub>                              | Detect Address Setting 4 | PADR4             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F4 <sub>H</sub>                              | Detect Address Setting 4 | PADR4             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F5 <sub>H</sub>                              | Detect Address Setting 4 | PADR4             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F6 <sub>H</sub>                              | Detect Address Setting 5 | PADR5             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F7 <sub>H</sub>                              | Detect Address Setting 5 | PADR5             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F8 <sub>H</sub>                              | Detect Address Setting 5 | PADR5             | R/W    |                              | XXXXXXXX <sub>B</sub> |
| 0079F9 <sub>H</sub><br>to<br>007FFF <sub>H</sub> | Reserved                 |                   |        |                              |                       |

- Notes :
- Initial value of “X” represents undefined value.
  - Do not write to the reserved areas in the I/O map. Reading from reserved addresses will return undefined values.

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

| Interrupt source                             | EI <sup>2</sup> OS clear | DMA ch number | Interrupt vector |                     | Interrupt control register |                     |
|----------------------------------------------|--------------------------|---------------|------------------|---------------------|----------------------------|---------------------|
|                                              |                          |               | Number           | Address             | Number                     | Address             |
| Reset                                        | N                        | —             | #08              | FFFFDC <sub>H</sub> | —                          | —                   |
| INT9 instruction                             | N                        | —             | #09              | FFFFD8 <sub>H</sub> | —                          | —                   |
| Exception                                    | N                        | —             | #10              | FFFFD4 <sub>H</sub> | —                          | —                   |
| (Reserved)                                   | N                        | —             | #11              | FFFFD0 <sub>H</sub> | ICR00                      | 0000B0 <sub>H</sub> |
| (Reserved)                                   | N                        | —             | #12              | FFFFCC <sub>H</sub> |                            |                     |
| Input Capture 6                              | Y1                       | —             | #13              | FFFFC8 <sub>H</sub> | ICR01                      | 0000B1 <sub>H</sub> |
| Input Capture 7                              | Y1                       | —             | #14              | FFFFC4 <sub>H</sub> |                            |                     |
| I <sup>2</sup> C0                            | N                        | —             | #15              | FFFFC0 <sub>H</sub> | ICR02                      | 0000B2 <sub>H</sub> |
| (Reserved)                                   | N                        | —             | #16              | FFFFBC <sub>H</sub> |                            |                     |
| 16-bit Reload Timer 0                        | Y1                       | 0             | #17              | FFFFB8 <sub>H</sub> | ICR03                      | 0000B3 <sub>H</sub> |
| 16-bit Reload Timer 1                        | Y1                       | 1             | #18              | FFFFB4 <sub>H</sub> |                            |                     |
| 16-bit Reload Timer 2                        | Y1                       | 2             | #19              | FFFFB0 <sub>H</sub> | ICR04                      | 0000B4 <sub>H</sub> |
| 16-bit Reload Timer 3                        | Y1                       | —             | #20              | FFFFAC <sub>H</sub> |                            |                     |
| PPG 0/1/4/5                                  | N                        | —             | #21              | FFFFA8 <sub>H</sub> | ICR05                      | 0000B5 <sub>H</sub> |
| PPG 2/3/6/7                                  | N                        | —             | #22              | FFFFA4 <sub>H</sub> |                            |                     |
| PPG 8/9/C/D                                  | N                        | —             | #23              | FFFFA0 <sub>H</sub> | ICR06                      | 0000B6 <sub>H</sub> |
| PPG A/B/E/F                                  | N                        | —             | #24              | FFFF9C <sub>H</sub> |                            |                     |
| Time Base Timer                              | N                        | —             | #25              | FFFF98 <sub>H</sub> | ICR07                      | 0000B7 <sub>H</sub> |
| External Interrupt 0 to 3, 8 to 11           | Y1                       | 3             | #26              | FFFF94 <sub>H</sub> |                            |                     |
| Watch Timer                                  | N                        | —             | #27              | FFFF90 <sub>H</sub> | ICR08                      | 0000B8 <sub>H</sub> |
| External Interrupt 4 to 7, 12 to 15          | Y1                       | 4             | #28              | FFFF8C <sub>H</sub> |                            |                     |
| 8/10-bit A/D Converter                       | Y1                       | 5             | #29              | FFFF88 <sub>H</sub> | ICR09                      | 0000B9 <sub>H</sub> |
| Free-run Timer 0, Free-run Timer 1           | N                        | —             | #30              | FFFF84 <sub>H</sub> |                            |                     |
| Input Capture 4/5, I <sup>2</sup> C1         | Y1                       | 6             | #31              | FFFF80 <sub>H</sub> | ICR10                      | 0000BA <sub>H</sub> |
| Output Compare 0/1/4/5                       | Y1                       | 7             | #32              | FFFF7C <sub>H</sub> |                            |                     |
| Input Capture 0 to 3                         | Y1                       | 8             | #33              | FFFF78 <sub>H</sub> | ICR11                      | 0000BB <sub>H</sub> |
| Output Compare 2/3/6/7                       | Y1                       | 9             | #34              | FFFF74 <sub>H</sub> |                            |                     |
| UART 0 Reception                             | Y2                       | 10            | #35              | FFFF70 <sub>H</sub> | ICR12                      | 0000BC <sub>H</sub> |
| UART 0 Transmission                          | Y1                       | 11            | #36              | FFFF6C <sub>H</sub> |                            |                     |
| UART 1 Reception /<br>UART 3 Reception       | Y2                       | 12            | #37              | FFFF68 <sub>H</sub> | ICR13                      | 0000BD <sub>H</sub> |
| UART 1 Transmission /<br>UART 3 Transmission | Y1                       | 13            | #38              | FFFF64 <sub>H</sub> |                            |                     |

(Continued)

# MB90860E Series

(Continued)

| Interrupt source                             | EI <sup>2</sup> OS clear | DMA ch number | Interrupt vector |                     | Interrupt control register |                     |
|----------------------------------------------|--------------------------|---------------|------------------|---------------------|----------------------------|---------------------|
|                                              |                          |               | Number           | Address             | Number                     | Address             |
| UART 2 Reception /<br>UART 4 Reception       | Y2                       | 14            | #39              | FFFF60 <sub>H</sub> | ICR14                      | 0000BE <sub>H</sub> |
| UART 2 Transmission /<br>UART 4 Transmission | Y1                       | 15            | #40              | FFFF5C <sub>H</sub> |                            |                     |
| Flash Memory                                 | N                        | —             | #41              | FFFF58 <sub>H</sub> | ICR15                      | 0000BF <sub>H</sub> |
| Delayed interrupt                            | N                        | —             | #42              | FFFF54 <sub>H</sub> |                            |                     |

Y1 : Usable

Y2 : Usable, with EI<sup>2</sup>OS stop function

N : Unusable

- Notes :
- Peripheral resources that share an ICR register have the same interrupt level.
  - When two peripheral resources share an ICR register, only one can use Extended Intelligent I/O Service at a time.
  - When either of the two peripheral resources sharing an ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter                                | Symbol               | Rating         |                | Unit | Remarks                                                      |
|------------------------------------------|----------------------|----------------|----------------|------|--------------------------------------------------------------|
|                                          |                      | Min            | Max            |      |                                                              |
| Power supply voltage*1                   | $V_{CC}$             | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    |                                                              |
|                                          | $AV_{CC}$            | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $V_{CC} = AV_{CC}$ *2                                        |
|                                          | AVRH, AVRL           | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $AV_{CC} \geq AVRH$ , $AV_{CC} \geq AVRL$ , $AVRH \geq AVRL$ |
| Input voltage*1                          | $V_I$                | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *3                                                           |
| Output voltage*1                         | $V_O$                | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *3                                                           |
| Maximum clamp current                    | $I_{CLAMP}$          | -4.0           | +4.0           | mA   | *5                                                           |
| Total maximum clamp current              | $\Sigma  I_{CLAMP} $ | —              | 40             | mA   | *5                                                           |
| “L” level maximum output current         | $I_{OL}$             | —              | 15             | mA   | *4                                                           |
| “L” level average output current         | $I_{OLAV}$           | —              | 4              | mA   | *4                                                           |
| “L” level maximum overall output current | $\Sigma I_{OL}$      | —              | 100            | mA   | *4                                                           |
| “L” level average overall output current | $\Sigma I_{OLAV}$    | —              | 50             | mA   | *4                                                           |
| “H” level maximum output current         | $I_{OH}$             | —              | -15            | mA   | *4                                                           |
| “H” level average output current         | $I_{OHAV}$           | —              | -4             | mA   | *4                                                           |
| “H” level maximum overall output current | $\Sigma I_{OH}$      | —              | -100           | mA   | *4                                                           |
| “H” level average overall output current | $\Sigma I_{OHAV}$    | —              | -50            | mA   | *4                                                           |
| Power consumption                        | $P_D$                | —              | 340            | mW   |                                                              |
| Operating temperature                    | $T_A$                | -40            | +105           | °C   |                                                              |
| Storage temperature                      | $T_{STG}$            | -55            | +150           | °C   |                                                              |

\*1 : This parameter is based on  $V_{SS} = AV_{SS} = 0$  V.

\*2 : Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.

\*3 :  $V_I$  and  $V_O$  must not exceed  $V_{CC} + 0.3$  V.  $V_I$  must not exceed the specified ratings. However if the maximum current to/from an input is limited by some means using external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.

\*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, and PA1

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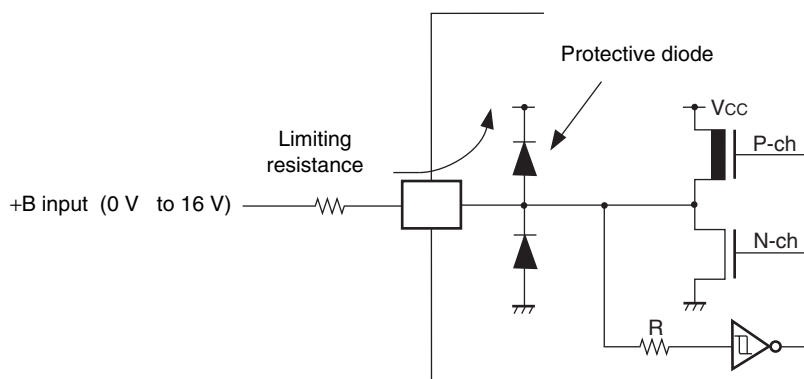


# MB90860E Series

(Continued)

- \*5 : • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (evaluation device : P50 to P55), P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, and PA1
- Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied by placing a limiting resistance between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed the rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , power may be supplied through the +B pin, resulting in incomplete operation of the microcontroller.
  - Note that if the +B input is applied during power-on, the power supplied via the +B pin may result in the supply voltage being insufficient to activate the power-on reset.
  - Care must be taken not to leave +B input pins open.
  - Sample recommended circuits:

- Input/output equivalent circuits



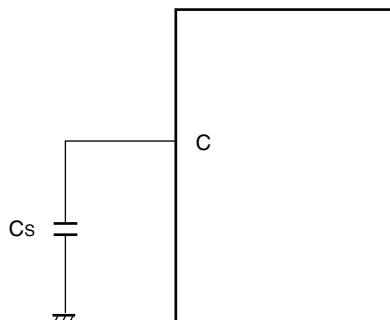
**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter             | Symbol            | Value |     |      | Unit               | Remarks                                                                                                                                                                      |
|-----------------------|-------------------|-------|-----|------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                       |                   | Min   | Typ | Max  |                    |                                                                                                                                                                              |
| Power supply voltage  | $V_{CC}, AV_{CC}$ | 4.0   | 5.0 | 5.5  | V                  | During normal operation                                                                                                                                                      |
|                       |                   | 3.5   | 5.0 | 5.5  | V                  | During normal operation, when not using the A/D converter and not Flash programming.                                                                                         |
|                       |                   | 4.5   | 5.0 | 5.5  | V                  | When using an external bus                                                                                                                                                   |
|                       |                   | 3.0   | —   | 5.5  | V                  | Maintains RAM data in stop mode                                                                                                                                              |
| Smoothing capacitor   | $C_S$             | 0.1   | —   | 1.0  | $\mu\text{F}$      | Use a ceramic capacitor or a capacitor with similar AC characteristics. The bypass capacitor used on the $V_{CC}$ pin should have a greater capacitance than this capacitor. |
| Operating temperature | $T_A$             | -40   | —   | +105 | $^{\circ}\text{C}$ |                                                                                                                                                                              |

### • C Pin Connection Diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB90860E Series

## 3. DC Characteristics

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                               | Symbol    | Pin                              | Condition                                              | Value          |     |                | Unit | Remarks                                                                                                  |
|---------------------------------------------------------|-----------|----------------------------------|--------------------------------------------------------|----------------|-----|----------------|------|----------------------------------------------------------------------------------------------------------|
|                                                         |           |                                  |                                                        | Min            | Typ | Max            |      |                                                                                                          |
| Input H voltage<br>(At $V_{CC} = 5\text{ V} \pm 10\%$ ) | $V_{IHS}$ | —                                | —                                                      | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V    | Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85) |
|                                                         | $V_{IHA}$ | —                                | —                                                      | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V    | Port inputs if automotive input levels are selected                                                      |
|                                                         | $V_{IHT}$ | —                                | —                                                      | 2.0            | —   | $V_{CC} + 0.3$ | V    | Port inputs if TTL input levels are selected                                                             |
|                                                         | $V_{IHS}$ | —                                | —                                                      | $0.7 V_{CC}$   | —   | $V_{CC} + 0.3$ | V    | P12, P50, P82, P85 inputs if CMOS input levels are selected                                              |
|                                                         | $V_{IHI}$ | —                                | —                                                      | $0.7 V_{CC}$   | —   | $V_{CC} + 0.3$ | V    | P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected                                   |
|                                                         | $V_{IHR}$ | —                                | —                                                      | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V    | $\overline{RST}$ input pin (CMOS hysteresis)                                                             |
|                                                         | $V_{IHM}$ | —                                | —                                                      | $V_{CC} - 0.3$ | —   | $V_{CC} + 0.3$ | V    | MD input pin                                                                                             |
| Input L voltage<br>(At $V_{CC} = 5\text{ V} \pm 10\%$ ) | $V_{ILS}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $0.2 V_{CC}$   | V    | Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85) |
|                                                         | $V_{ILA}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $0.5 V_{CC}$   | V    | Port inputs if automotive input levels are selected                                                      |
|                                                         | $V_{ILT}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | 0.8            | V    | Port inputs if TTL input levels are selected                                                             |
|                                                         | $V_{ILS}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $0.3 V_{CC}$   | V    | P12, P50, P82, P85 inputs if CMOS input levels are selected                                              |
|                                                         | $V_{ILI}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $0.3 V_{CC}$   | V    | P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected                                   |
|                                                         | $V_{ILR}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $0.2 V_{CC}$   | V    | $\overline{RST}$ input pin (CMOS hysteresis)                                                             |
|                                                         | $V_{ILM}$ | —                                | —                                                      | $V_{SS} - 0.3$ | —   | $V_{SS} + 0.3$ | V    | MD input pin                                                                                             |
| Output H voltage                                        | $V_{OH}$  | Normal outputs                   | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OH} = -4.0\text{ mA}$ | $V_{CC} - 0.5$ | —   | —              | V    |                                                                                                          |
| Output H voltage                                        | $V_{OHI}$ | I <sup>2</sup> C current outputs | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OH} = -3.0\text{ mA}$ | $V_{CC} - 0.5$ | —   | —              | V    |                                                                                                          |
| Output L voltage                                        | $V_{OL}$  | Normal outputs                   | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OL} = 4.0\text{ mA}$  | —              | —   | 0.4            | V    |                                                                                                          |
| Output L voltage                                        | $V_{OLI}$ | I <sup>2</sup> C current outputs | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OL} = 3.0\text{ mA}$  | —              | —   | 0.4            | V    |                                                                                                          |

(Continued)

(Continued)

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter             | Symbol        | Pin                                                                                  | Condition                                                                                                     | Value |     |     | Unit          | Remarks              |
|-----------------------|---------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|-------|-----|-----|---------------|----------------------|
|                       |               |                                                                                      |                                                                                                               | Min   | Typ | Max |               |                      |
| Input leak current    | $I_{IL}$      | —                                                                                    | $V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_i < V_{CC}$                                                             | -1    | —   | +1  | $\mu\text{A}$ |                      |
| Pull-up resistance    | $R_{UP}$      | P00 to P07,<br>P10 to P17,<br>P20 to P27,<br>P30 to P37,<br>$\overline{RST}$         | —                                                                                                             | 25    | 50  | 100 | $k\Omega$     |                      |
| Pull-down resistance  | $R_{DOWN}$    | MD2                                                                                  | —                                                                                                             | 25    | 50  | 100 | $k\Omega$     | Except Flash devices |
| Power supply current* | $I_{CC}$      | $V_{CC}$                                                                             | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 24 MHz,<br>during normal operation.                         | —     | 55  | 70  | mA            |                      |
|                       |               |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 24 MHz,<br>when writing FLASH memory.                       | —     | 70  | 85  | mA            | Flash devices        |
|                       |               |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 24 MHz,<br>when erasing FLASH memory.                       | —     | 75  | 90  | mA            | Flash devices        |
|                       | $I_{CCS}$     |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 24 MHz,<br>in Sleep mode.                                   | —     | 25  | 35  | mA            |                      |
|                       | $I_{CTS}$     |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 2 MHz,<br>in Main Timer mode                                | —     | 0.3 | 0.8 | mA            |                      |
|                       | $I_{CTSPLL6}$ |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>Internal frequency : 24 MHz,<br>in PLL Timer mode,<br>external frequency = 4 MHz | —     | 4   | 7   | mA            |                      |
|                       | $I_{CCL}$     |                                                                                      | $V_{CC} = 5.0\text{ V}$<br>Internal frequency : 8 kHz,<br>during sub operation<br>$T_A = +25^{\circ}\text{C}$ | —     | 70  | 140 | $\mu\text{A}$ |                      |
|                       | $I_{CCLS}$    |                                                                                      | $V_{CC} = 5.0\text{ V}$<br>Internal frequency : 8 kHz,<br>during sub sleep<br>$T_A = +25^{\circ}\text{C}$     | —     | 20  | 50  | $\mu\text{A}$ |                      |
|                       | $I_{CCT}$     |                                                                                      | $V_{CC} = 5.0\text{ V}$<br>Internal frequency : 8 kHz,<br>in watch mode<br>$T_A = +25^{\circ}\text{C}$        | —     | 10  | 35  | $\mu\text{A}$ |                      |
|                       | $I_{CCH}$     |                                                                                      | $V_{CC} = 5.0\text{ V}$ ,<br>in Stop mode,<br>$T_A = +25^{\circ}\text{C}$                                     | —     | 7   | 25  | $\mu\text{A}$ |                      |
| Input capacitance     | $C_{IN}$      | Other than C,<br>$AV_{CC}$ , $AV_{SS}$ ,<br>$AVRH$ , $AVRL$ ,<br>$V_{CC}$ , $V_{SS}$ | —                                                                                                             | —     | 5   | 15  | pF            |                      |

\* : Power supply currents were measured under test conditions using an external clock.

# MB90860E Series

## 4. AC Characteristics

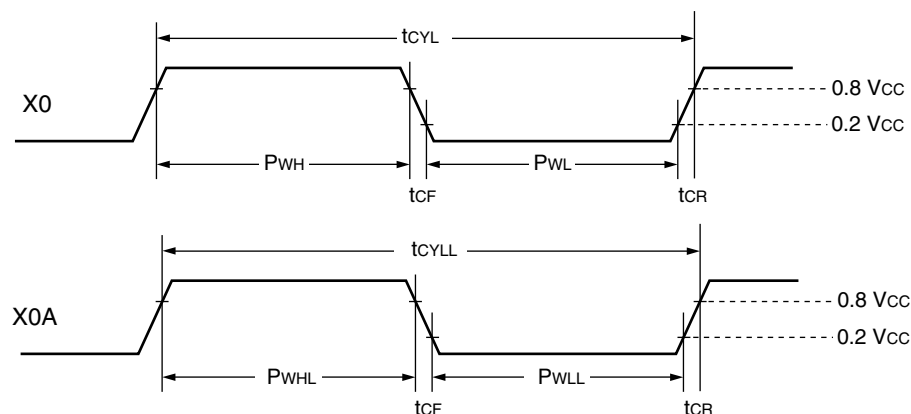
### (1) Clock Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

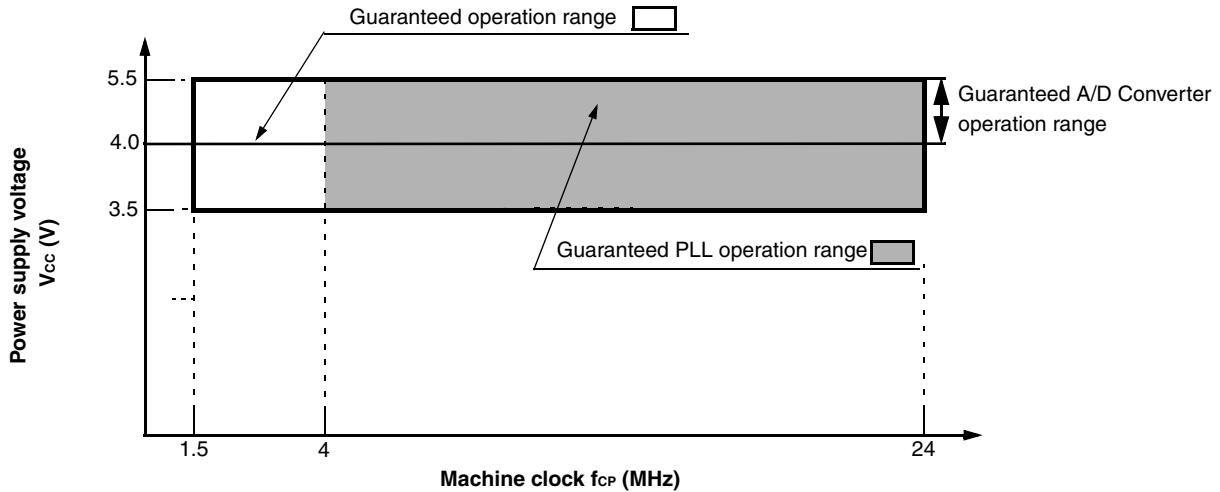
| Parameter                                           | Symbol             | Pin      | Value |        |     | Unit          | Remarks                                                  |
|-----------------------------------------------------|--------------------|----------|-------|--------|-----|---------------|----------------------------------------------------------|
|                                                     |                    |          | Min   | Typ    | Max |               |                                                          |
| Clock frequency                                     | $f_c$              | X0, X1   | 3     | —      | 16  | MHz           | 1/2 (at PLL stop)<br>When using an oscillator circuit    |
|                                                     |                    |          | 4     | —      | 16  | MHz           | PLL multiplied by 1<br>When using an oscillator circuit* |
|                                                     |                    |          | 4     | —      | 12  | MHz           | PLL multiplied by 2<br>When using an oscillator circuit* |
|                                                     |                    |          | 4     | —      | 8   | MHz           | PLL multiplied by 3<br>When using an oscillator circuit* |
|                                                     |                    |          | 4     | —      | 6   | MHz           | PLL multiplied by 4<br>When using an oscillator circuit* |
|                                                     |                    |          | —     | —      | 4   | MHz           | PLL multiplied by 6<br>When using an oscillator circuit* |
|                                                     | $f_{CL}$           | X0A, X1A | —     | 32.768 | 100 | kHz           | When using an external clock                             |
| Clock cycle time                                    | $t_{CYL}$          | X0, X1   | 62.5  | —      | 333 | ns            | When using an oscillator circuit                         |
|                                                     |                    | X0, X1   | 41.67 | —      | 333 | ns            | When using an external clock                             |
|                                                     | $t_{CYLL}$         | X0A, X1A | 10    | 30.5   | —   | $\mu\text{s}$ |                                                          |
| Input clock pulse width                             | $P_{WH}, P_{WL}$   | X0       | 10    | —      | —   | ns            | Duty ratio is about 30% to 70%.                          |
|                                                     | $P_{WHL}, P_{WLL}$ | X0A      | 5     | 15.2   | —   | $\mu\text{s}$ |                                                          |
| Input clock rise and fall time                      | $t_{CR}, t_{CF}$   | X0       | —     | —      | 5   | ns            | When using external clock                                |
| Internal operating clock frequency (machine clock)  | $f_{CP}$           | —        | 1.5   | —      | 24  | MHz           | When using main clock                                    |
|                                                     | $f_{CPL}$          | —        | —     | 8.192  | 50  | kHz           | When using sub clock                                     |
| Internal operating clock cycle time (machine clock) | $t_{CP}$           | —        | 41.67 | —      | 666 | ns            | When using main clock                                    |
|                                                     | $t_{CPL}$          | —        | 20    | 122.1  | —   | $\mu\text{s}$ | When using sub clock                                     |

\* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".

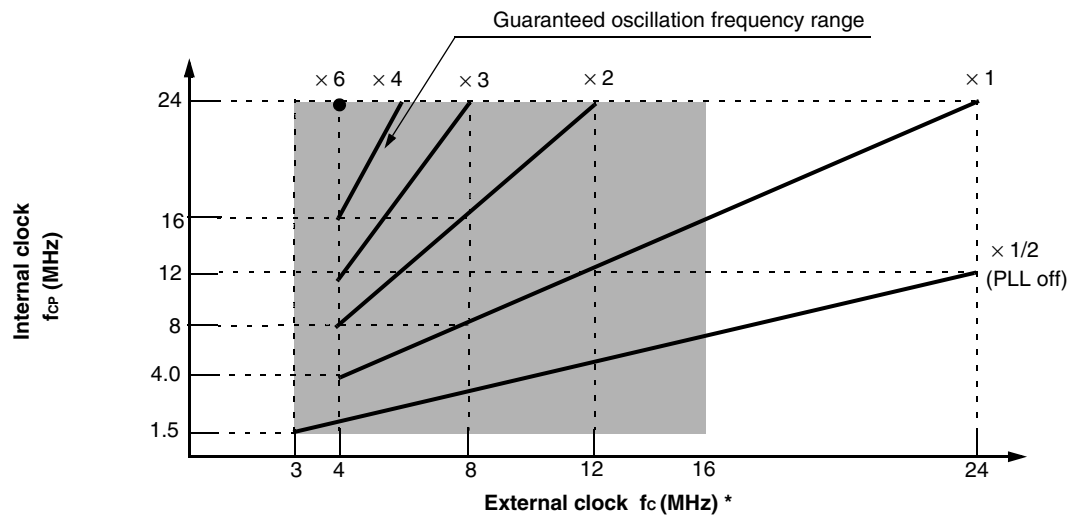
#### • Clock Timing



- Guaranteed PLL operation range



## Guaranteed operation range of MB90860E series



\* : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

# MB90860E Series

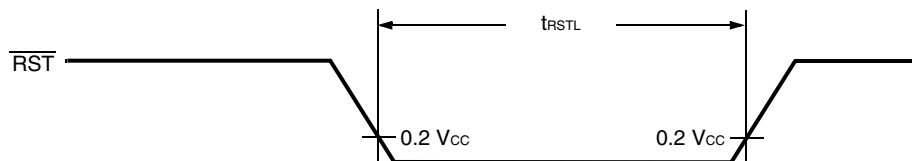
## (2) Reset Standby Input

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

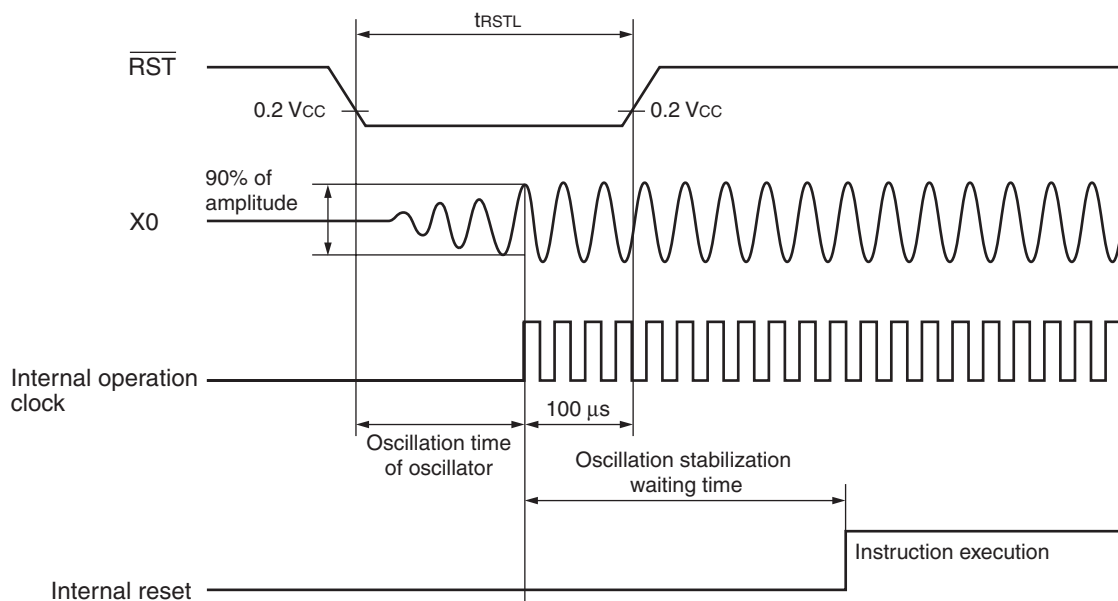
| Parameter        | Symbol     | Pin              | Value                                                  |     | Unit          | Remarks                                                     |
|------------------|------------|------------------|--------------------------------------------------------|-----|---------------|-------------------------------------------------------------|
|                  |            |                  | Min                                                    | Max |               |                                                             |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500                                                    | —   | ns            | During normal operation                                     |
|                  |            |                  | Oscillation time of oscillator*<br>+ 100 $\mu\text{s}$ | —   | $\mu\text{s}$ | In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode |
|                  |            |                  | 100                                                    | —   | $\mu\text{s}$ | In Time Timer mode                                          |

\* : The oscillation time of the oscillator is the time it takes for the amplitude to reach 90%. In crystal oscillators, the oscillation time is between several ms and to tens of ms. In crystal oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. For an external clock, the oscillation time is 0 ms.

During normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode, Power-on:



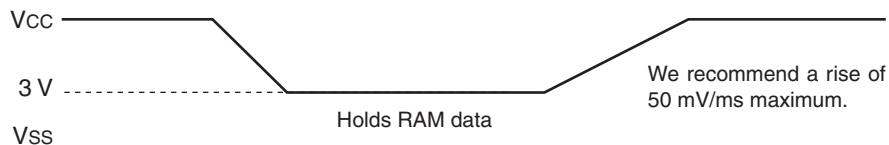
## (3) Power On Reset

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

| Parameter          | Symbol    | Pin      | Condition | Value |     | Unit | Remarks                     |
|--------------------|-----------|----------|-----------|-------|-----|------|-----------------------------|
|                    |           |          |           | Min   | Max |      |                             |
| Power on rise time | $t_R$     | $V_{CC}$ | —         | 0.05  | 30  | ms   |                             |
| Power off time     | $t_{OFF}$ | $V_{CC}$ |           | 1     | —   | ms   | Waiting time until power-on |



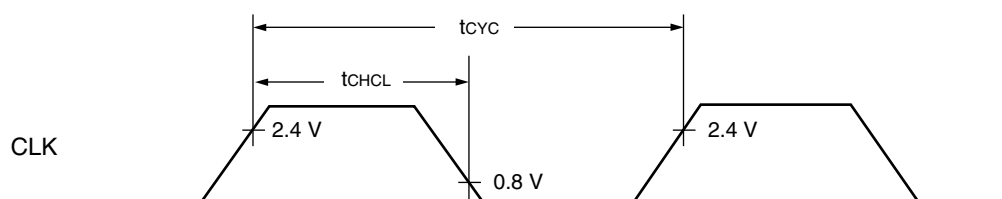
If you change the power supply voltage too rapidly, a power on reset may occur. If the power supply voltage is varied while the device is operating, it is recommended that variation be limited such that the supply voltage rises smoothly as shown in the following diagram. The supply voltage should be changed while the PLL clock is not being used. However, the device can be operated while the PLL is being used if the rate of change is less than 1 V/s.



## (4) Clock Output Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

| Parameter                                   | Symbol     | Pin | Condition | Value |     | Unit | Remarks                  |
|---------------------------------------------|------------|-----|-----------|-------|-----|------|--------------------------|
|                                             |            |     |           | Min   | Max |      |                          |
| Cycle time                                  | $t_{CYC}$  | CLK | —         | 62.5  | —   | ns   | $f_{CP} = 16\text{ MHz}$ |
|                                             |            |     |           | 41.67 | —   | ns   | $f_{CP} = 24\text{ MHz}$ |
| CLK $\uparrow \rightarrow$ CLK $\downarrow$ | $t_{CHCL}$ | CLK | —         | 20    | —   | ns   | $f_{CP} = 16\text{ MHz}$ |
|                                             |            |     |           | 13    | —   | ns   | $f_{CP} = 24\text{ MHz}$ |



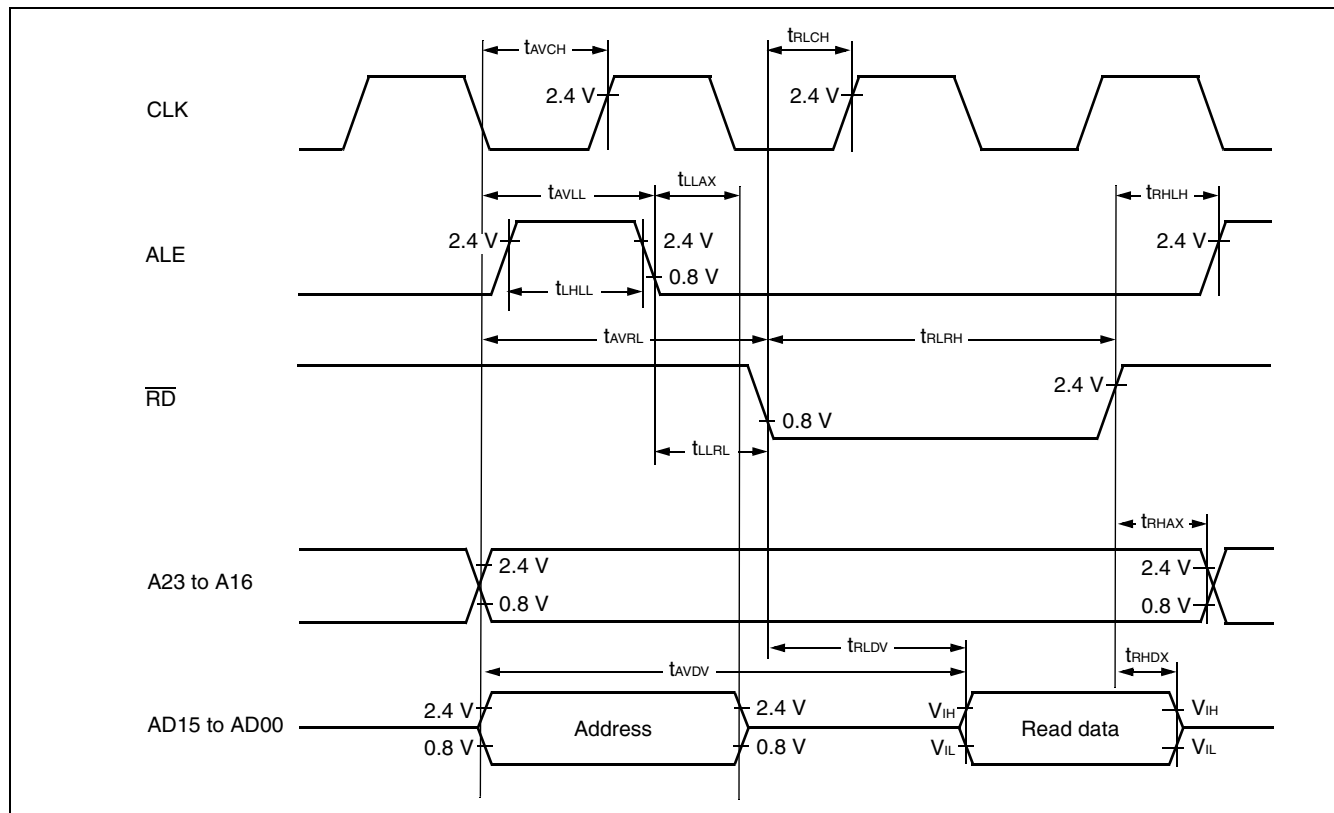


# MB90860E Series

## (5) Bus Timing (Read)

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

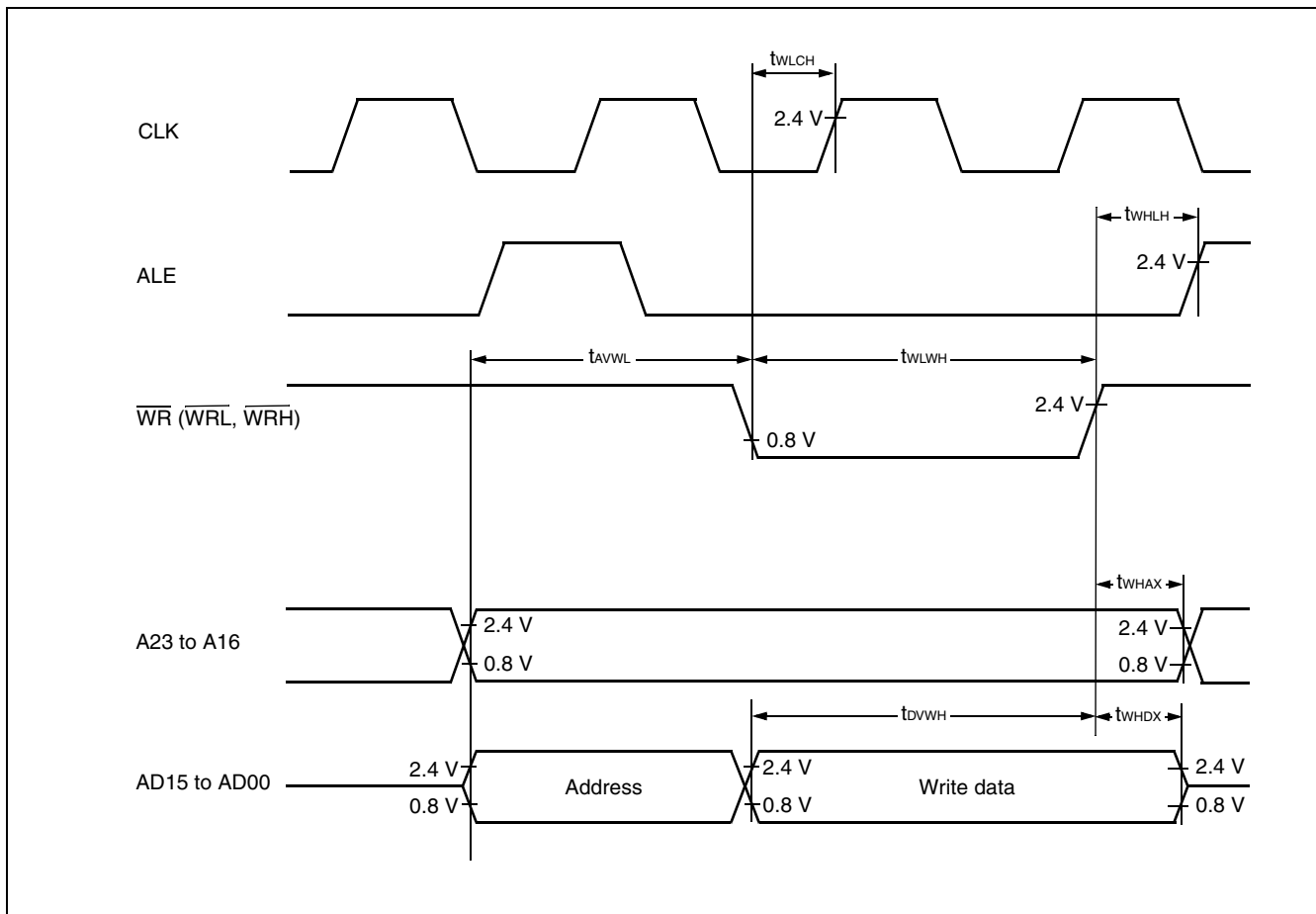
| Parameter                                                  | Symbol     | Pin                                       | Condition | Value             |                   | Unit |
|------------------------------------------------------------|------------|-------------------------------------------|-----------|-------------------|-------------------|------|
|                                                            |            |                                           |           | Min               | Max               |      |
| ALE pulse width                                            | $t_{LHLL}$ | ALE                                       | —         | $t_{CP}/2 - 10$   | —                 | ns   |
| Valid address $\rightarrow$ ALE $\downarrow$ time          | $t_{AVLL}$ | ALE, A23 to A16, AD15 to AD00             |           | $t_{CP}/2 - 20$   | —                 | ns   |
| ALE $\downarrow \rightarrow$ Address valid time            | $t_{LLAX}$ | ALE, AD15 to AD00                         |           | $t_{CP}/2 - 15$   | —                 | ns   |
| Valid address $\rightarrow \overline{RD} \downarrow$ time  | $t_{AVRL}$ | A23 to A16, AD15 to AD00, $\overline{RD}$ |           | $t_{CP} - 15$     | —                 | ns   |
| Valid address $\rightarrow$ Valid data input               | $t_{AVDV}$ | A23 to A16, AD15 to AD00                  |           | —                 | $5 t_{CP}/2 - 60$ | ns   |
| $\overline{RD}$ pulse width                                | $t_{RLRH}$ | $\overline{RD}$                           |           | $3 t_{CP}/2 - 20$ | —                 | ns   |
| $\overline{RD} \downarrow \rightarrow$ Valid data input    | $t_{RLDV}$ | $\overline{RD}$ , AD15 to AD00            |           | —                 | $3 t_{CP}/2 - 50$ | ns   |
| $\overline{RD} \uparrow \rightarrow$ Data hold time        | $t_{RHDX}$ | $\overline{RD}$ , AD15 to AD00            |           | 0                 | —                 | ns   |
| $\overline{RD} \uparrow \rightarrow$ ALE $\uparrow$ time   | $t_{RHLH}$ | $\overline{RD}$ , ALE                     |           | $t_{CP}/2 - 15$   | —                 | ns   |
| $\overline{RD} \uparrow \rightarrow$ Address valid time    | $t_{RHAX}$ | $\overline{RD}$ , A23 to A16              |           | $t_{CP}/2 - 10$   | —                 | ns   |
| Valid address $\rightarrow$ CLK $\uparrow$ time            | $t_{AVCH}$ | A23 to A16, AD15 to AD00, CLK             |           | $t_{CP}/2 - 16$   | —                 | ns   |
| $\overline{RD} \downarrow \rightarrow$ CLK $\uparrow$ time | $t_{RLCH}$ | $\overline{RD}$ , CLK                     |           | $t_{CP}/2 - 15$   | —                 | ns   |
| ALE $\downarrow \rightarrow \overline{RD} \downarrow$ time | $t_{LLRL}$ | ALE, $\overline{RD}$                      |           | $t_{CP}/2 - 15$   | —                 | ns   |



## (6) Bus Timing (Write)

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

| Parameter                                                   | Symbol     | Pin                                             | Condition | Value             |     | Unit |
|-------------------------------------------------------------|------------|-------------------------------------------------|-----------|-------------------|-----|------|
|                                                             |            |                                                 |           | Min               | Max |      |
| Valid address $\rightarrow \overline{WR} \downarrow$ time   | $t_{AVWL}$ | A23 to A16,<br>AD15 to AD00,<br>$\overline{WR}$ | —         | $t_{CP}-15$       | —   | ns   |
| $\overline{WR}$ pulse width                                 | $t_{WLWH}$ | $\overline{WR}$                                 |           | $3 t_{CP}/2 - 20$ | —   | ns   |
| Valid data output $\rightarrow \overline{WR} \uparrow$ time | $t_{DVWH}$ | AD15 to AD00,<br>$\overline{WR}$                |           | $3 t_{CP}/2 - 20$ | —   | ns   |
| $\overline{WR} \uparrow \rightarrow$ Data hold time         | $t_{WHDX}$ | AD15 to AD00,<br>$\overline{WR}$                |           | 15                | —   | ns   |
| $\overline{WR} \uparrow \rightarrow$ Address valid time     | $t_{WHAX}$ | A23 to A16, $\overline{WR}$                     |           | $t_{CP}/2 - 10$   | —   | ns   |
| $\overline{WR} \uparrow \rightarrow$ ALE $\uparrow$ time    | $t_{WHLH}$ | $\overline{WR}$ , ALE                           |           | $t_{CP}/2 - 15$   | —   | ns   |
| $\overline{WR} \downarrow \rightarrow$ CLK $\uparrow$ time  | $t_{WLCH}$ | $\overline{WR}$ , CLK                           |           | $t_{CP}/2 - 15$   | —   | ns   |



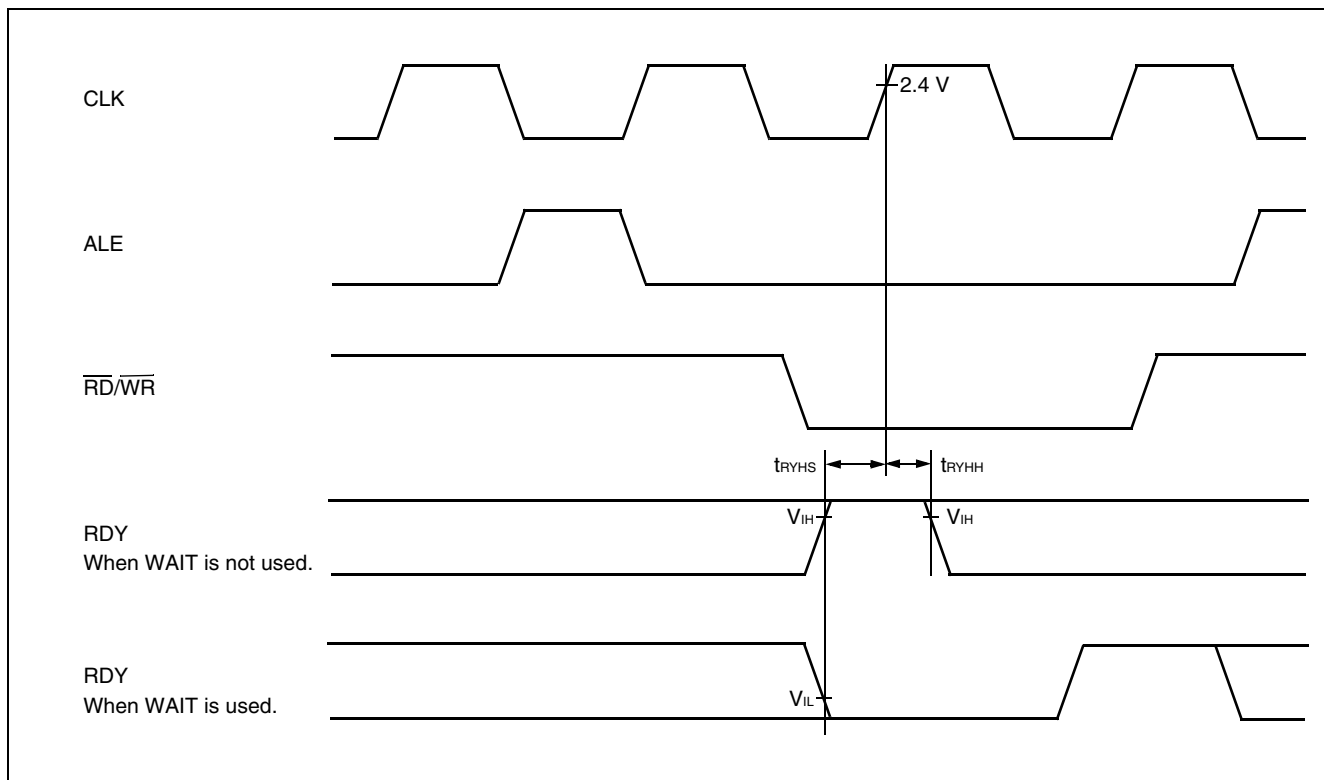
# MB90860E Series

## (7) Ready Input Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

| Parameter      | Symbol     | Pin | Condition | Rated Value |     | Units | Remarks                  |
|----------------|------------|-----|-----------|-------------|-----|-------|--------------------------|
|                |            |     |           | Min         | Max |       |                          |
| RDY setup time | $t_{RYHS}$ | RDY | —         | 45          | —   | ns    | $f_{CP} = 16\text{ MHz}$ |
|                |            |     |           | 32          | —   | ns    | $f_{CP} = 24\text{ MHz}$ |
| RDY hold time  | $t_{RYHH}$ | RDY |           | 0           | —   | ns    |                          |

Note : If the RDY setup time is insufficient, use the auto-ready function.

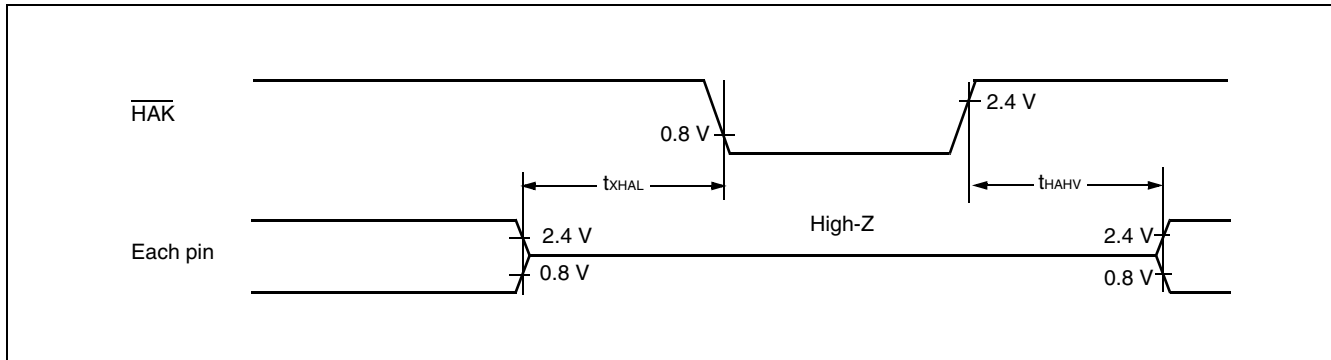


## (8) Hold Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

| Parameter                                                          | Symbol     | Pin                     | Condition | Value    |            | Units |
|--------------------------------------------------------------------|------------|-------------------------|-----------|----------|------------|-------|
|                                                                    |            |                         |           | Min      | Max        |       |
| Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time   | $t_{XHAL}$ | $\overline{\text{HAK}}$ | —         | 30       | $t_{CP}$   | ns    |
| $\overline{\text{HAK}} \uparrow$ time $\rightarrow$ Pin valid time | $t_{HAHV}$ | $\overline{\text{HAK}}$ |           | $t_{CP}$ | $2 t_{CP}$ | ns    |

Note : It takes at least one machine clock cycle from when an HRQ is accepted until  $\overline{\text{HAK}}$  changes.



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## (9) LIN-UART0/1/2/3

- Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

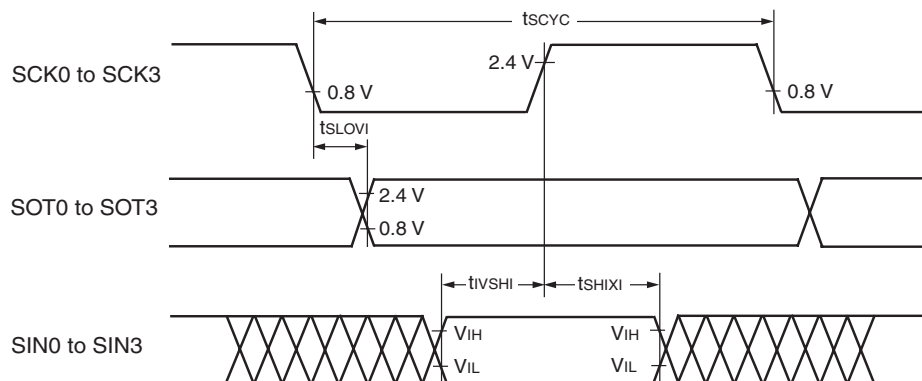
| Parameter                    | Symbol      | Pin                          | Condition                                                                       | Value             |                  | Unit |
|------------------------------|-------------|------------------------------|---------------------------------------------------------------------------------|-------------------|------------------|------|
|                              |             |                              |                                                                                 | Min               | Max              |      |
| Serial clock cycle time      | $t_{SCYC}$  | SCK0 to SCK3                 | Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $5\ t_{CP}$       | —                | ns   |
| SCK ↓ → SOT delay time       | $t_{SLOVI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                 | −50               | +50              | ns   |
| Valid SIN → SCK ↑            | $t_{IVSHI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | $t_{CP} + 80$     | —                | ns   |
| SCK ↑ → Valid SIN hold time  | $t_{SHIXI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | 0                 | —                | ns   |
| Serial clock “L” pulse width | $t_{SHSL}$  | SCK0 to SCK3                 | External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $3\ t_{CP} - t_R$ | —                | ns   |
| Serial clock “H” pulse width | $t_{SLSH}$  | SCK0 to SCK3                 |                                                                                 | $t_{CP} + 10$     | —                | ns   |
| SCK ↓ → SOT delay time       | $t_{SLOVE}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                 | —                 | $2\ t_{CP} + 60$ | ns   |
| Valid SIN → SCK ↑            | $t_{IVSHE}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | 30                | —                | ns   |
| SCK ↑ → Valid SIN hold time  | $t_{SHIXE}$ | SCK0, SCK1,<br>SIN0 to SIN3  |                                                                                 | $t_{CP} + 30$     | —                | ns   |
| SCK fall time                | $t_F$       | SCK0 to SCK3                 |                                                                                 | —                 | 10               | ns   |
| SCK rise time                | $t_R$       | SCK0 to SCK3                 |                                                                                 | —                 | 10               | ns   |

Notes : • AC characteristic in CLK synchronized mode.

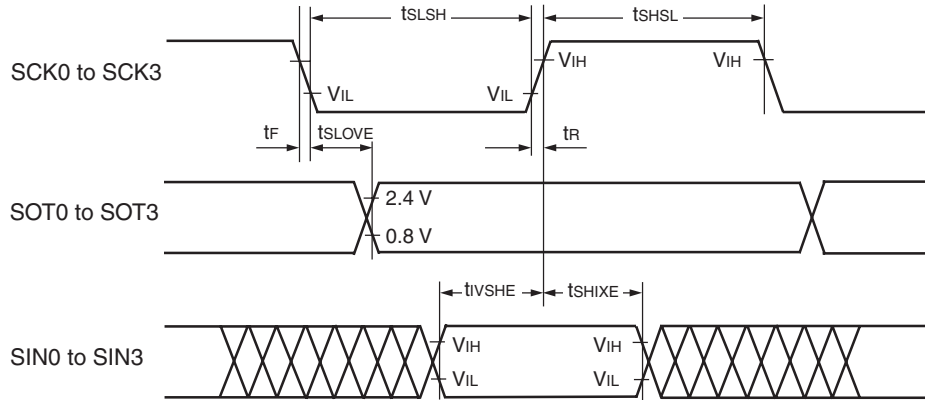
•  $C_L$  is load capacity value of pins when testing.

•  $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

### • Internal Shift Clock Mode



• External Shift Clock Mode



• Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

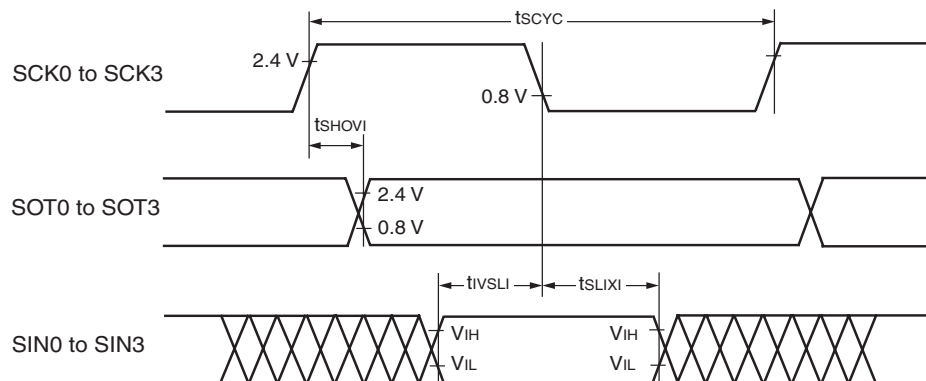
| Parameter                                          | Symbol      | Pin                          | Condition                                                                       | Value                   |                        | Unit |
|----------------------------------------------------|-------------|------------------------------|---------------------------------------------------------------------------------|-------------------------|------------------------|------|
|                                                    |             |                              |                                                                                 | Min                     | Max                    |      |
| Serial clock cycle time                            | $t_{SCYC}$  | SCK0 to SCK3                 | Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $5\text{ }t_{CP}$       | —                      | ns   |
| SCK $\uparrow$ $\rightarrow$ SOT delay time        | $t_{SHOVI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                 | -50                     | +50                    | ns   |
| Valid SIN $\rightarrow$ SCK $\downarrow$           | $t_{IVSLI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | $t_{CP} + 80$           | —                      | ns   |
| SCK $\downarrow$ $\rightarrow$ Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | 0                       | —                      | ns   |
| Serial clock "H" pulse width                       | $t_{SHSL}$  | SCK0 to SCK3                 | External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $3\text{ }t_{CP} - t_R$ | —                      | ns   |
| Serial clock "L" pulse width                       | $t_{SLSH}$  | SCK0 to SCK3                 |                                                                                 | $t_{CP} + 10$           | —                      | ns   |
| SCK $\uparrow$ $\rightarrow$ SOT delay time        | $t_{SHOVE}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                 | —                       | $2\text{ }t_{CP} + 60$ | ns   |
| Valid SIN $\rightarrow$ SCK $\downarrow$           | $t_{IVSLE}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | 30                      | —                      | ns   |
| SCK $\downarrow$ $\rightarrow$ Valid SIN hold time | $t_{SLIXE}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                 | $t_{CP} + 30$           | —                      | ns   |
| SCK fall time                                      | $t_F$       | SCK0 to SCK3                 |                                                                                 | —                       | 10                     | ns   |
| SCK rise time                                      | $t_R$       | SCK0 to SCK3                 |                                                                                 | —                       | 10                     | ns   |

Notes : •  $C_L$  is load capacity value of pins when testing.

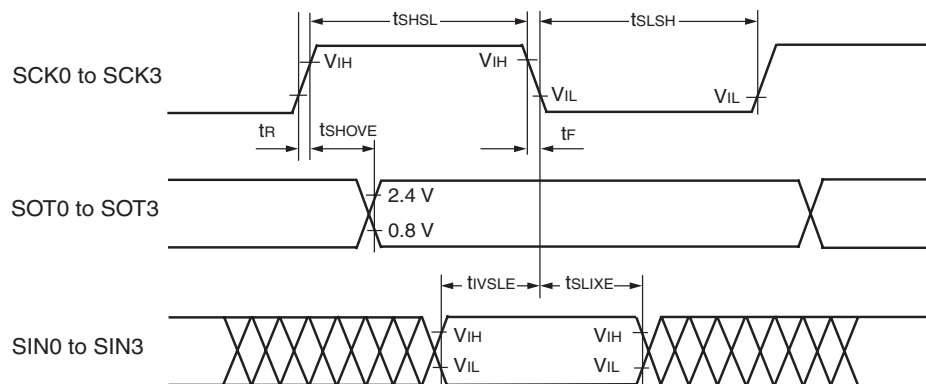
•  $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

# MB90860E Series

## • Internal Shift Clock Mode



## • External Shift Clock Mode



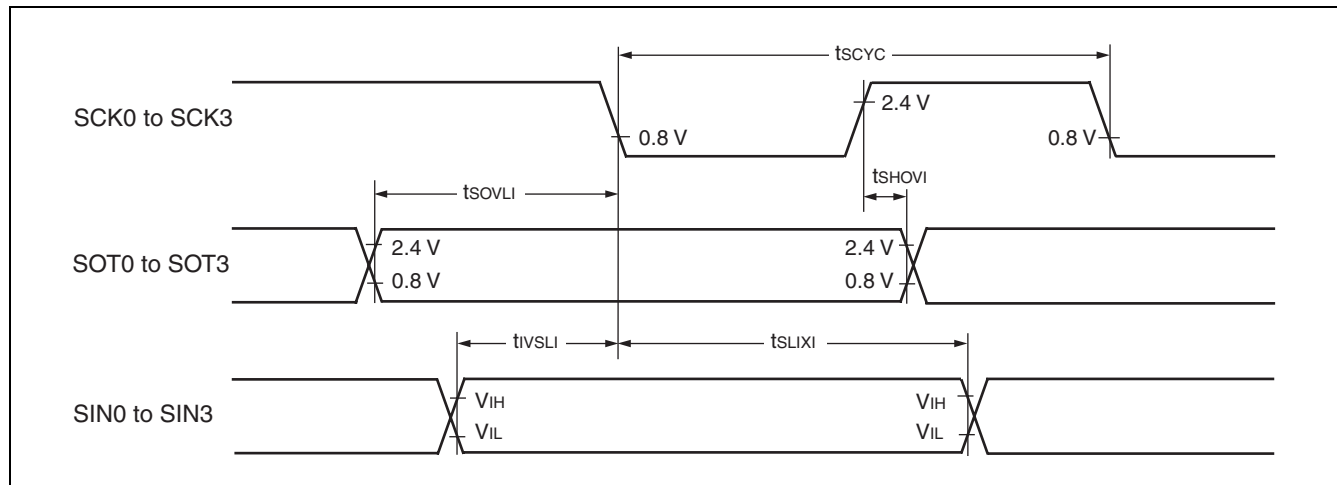
- Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                          | Symbol      | Pin                          | Condition                                                                            | Value            |     | Unit |
|----------------------------------------------------|-------------|------------------------------|--------------------------------------------------------------------------------------|------------------|-----|------|
|                                                    |             |                              |                                                                                      | Min              | Max |      |
| Serial clock cycle time                            | $t_{SCYC}$  | SCK0 to SCK3                 | Internal clock operation<br>output pins are<br>$C_L = 80\text{ pF} + 1\text{ TTL}$ . | $5\ t_{CP}$      | —   | ns   |
| SCK $\uparrow$ $\rightarrow$ SOT delay time        | $t_{SHOVI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                      | -50              | +50 | ns   |
| Valid SIN $\rightarrow$ SCK $\downarrow$           | $t_{IVSLI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                      | $t_{CP} + 80$    | —   | ns   |
| SCK $\downarrow$ $\rightarrow$ Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                      | 0                | —   | ns   |
| SOT $\rightarrow$ SCK $\downarrow$ delay time      | $t_{SOVLI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                      | $3\ t_{CP} - 70$ | —   | ns   |

Notes : •  $C_L$  is load capacity value of pins when testing.

- $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.





# MB90860E Series

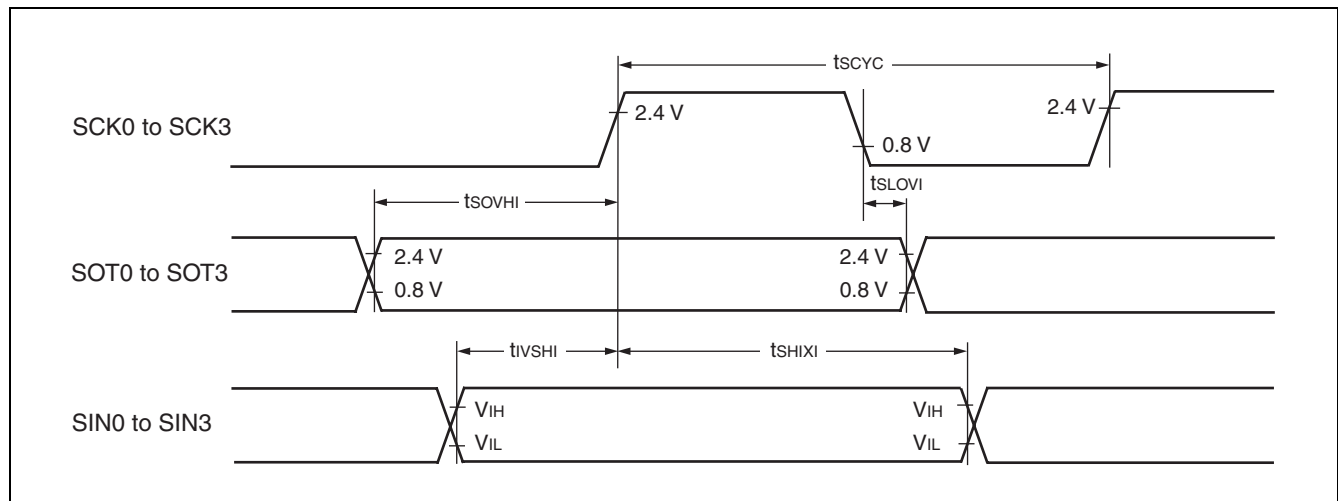
- Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                      | Symbol      | Pin                          | Condition                                                                            | Value            |     | Unit |
|------------------------------------------------|-------------|------------------------------|--------------------------------------------------------------------------------------|------------------|-----|------|
|                                                |             |                              |                                                                                      | Min              | Max |      |
| Serial clock cycle time                        | $t_{SCYC}$  | SCK0 to SCK3                 | Internal clock operation<br>output pins are<br>$C_L = 80\text{ pF} + 1\text{ TTL}$ . | $5\ t_{CP}$      | —   | ns   |
| SCK $\downarrow \rightarrow$ SOT delay time    | $t_{SLOVI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                      | -50              | +50 | ns   |
| Valid SIN $\rightarrow$ SCK $\uparrow$         | $t_{IVSHI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                      | $t_{CP} + 80$    | —   | ns   |
| SCK $\uparrow \rightarrow$ Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3<br>SIN0 to SIN3 |                                                                                      | 0                | —   | ns   |
| SOT $\rightarrow$ SCK $\uparrow$ delay time    | $t_{SOVHI}$ | SCK0 to SCK3<br>SOT0 to SOT3 |                                                                                      | $3\ t_{CP} - 70$ | —   | ns   |

Notes : •  $C_L$  is load capacity value of pins when testing.

- $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.

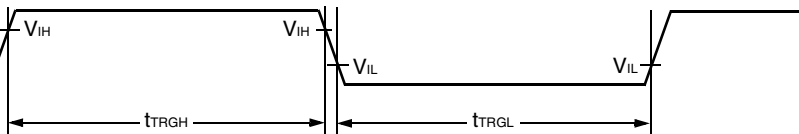


## (10) Trigger Input Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter         | Symbol                   | Pin                                        | Condition | Value       |     | Unit |
|-------------------|--------------------------|--------------------------------------------|-----------|-------------|-----|------|
|                   |                          |                                            |           | Min         | Max |      |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT15,<br>INT8R to INT15R,<br>ADTG | —         | $5\ t_{CP}$ | —   | ns   |

INT0 to INT15,  
INT8R to INT15R,  
ADTG

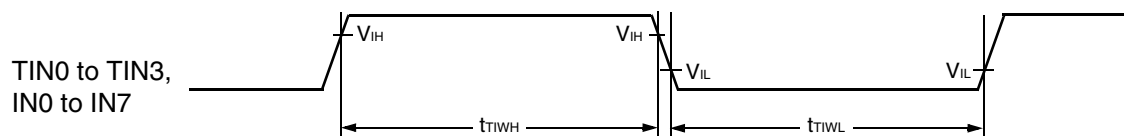


# MB90860E Series

## (11) Timer Related Resource Input Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

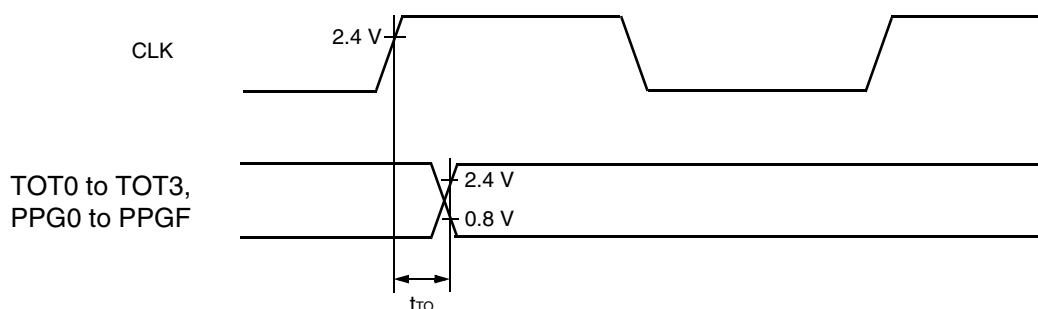
| Parameter         | Symbol     | Pin                         | Condition | Value       |     | Unit |
|-------------------|------------|-----------------------------|-----------|-------------|-----|------|
|                   |            |                             |           | Min         | Max |      |
| Input pulse width | $t_{TIWH}$ | TIN0 to TIN3,<br>IN0 to IN7 | —         | $4\ t_{CP}$ | —   | ns   |
|                   | $t_{TIWL}$ |                             |           |             |     |      |



## (12) Timer Related Resource Output Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0.0\text{ V}$ )

| Parameter                                          | Symbol   | Pin                           | Condition | Value |     | Unit |
|----------------------------------------------------|----------|-------------------------------|-----------|-------|-----|------|
|                                                    |          |                               |           | Min   | Max |      |
| CLK $\uparrow$ $\rightarrow$ $T_{OUT}$ change time | $t_{TO}$ | TOT0 to TOT3,<br>PPG0 to PPGF | —         | 30    | —   | ns   |



## (13) I<sup>2</sup>C Timing

(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V)

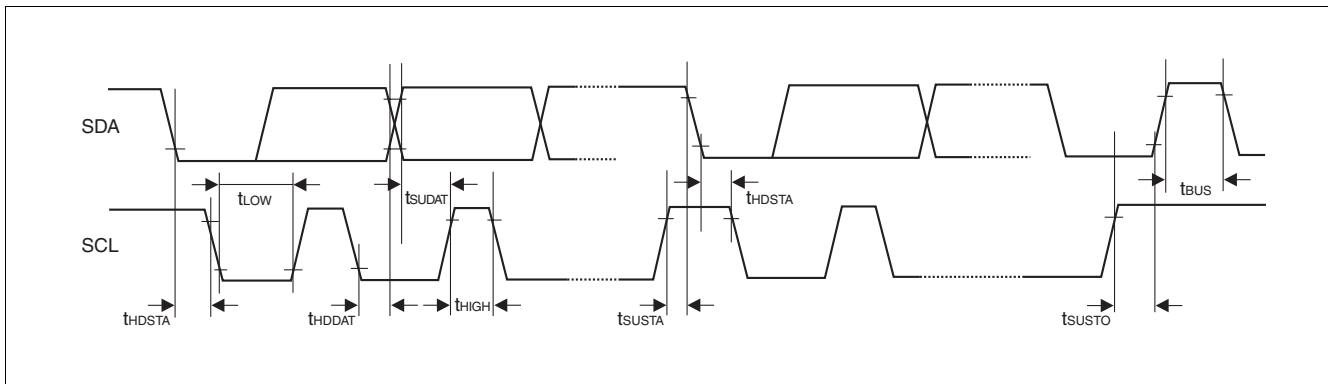
| Parameter                                                   | Symbol             | Condition                              | Standard-mode |                    | Fast-mode* <sup>1</sup> |                   | Unit |
|-------------------------------------------------------------|--------------------|----------------------------------------|---------------|--------------------|-------------------------|-------------------|------|
|                                                             |                    |                                        | Min           | Max                | Min                     | Max               |      |
| SCL clock frequency                                         | f <sub>SCL</sub>   | R = 1.7 kΩ,<br>C = 50 pF* <sup>2</sup> | 0             | 100                | 0                       | 400               | kHz  |
| Hold time (repeated) START condition<br>SDA ↓ → SCL ↓       | t <sub>HDSTA</sub> |                                        | 4.0           | —                  | 0.6                     | —                 | μs   |
| “L” width of the SCL clock                                  | t <sub>LOW</sub>   |                                        | 4.7           | —                  | 1.3                     | —                 | μs   |
| “H” width of the SCL clock                                  | t <sub>HIGH</sub>  |                                        | 4.0           | —                  | 0.6                     | —                 | μs   |
| Set-up time for a repeated START condition<br>SCL ↑ → SDA ↓ | t <sub>SUSTA</sub> |                                        | 4.7           | —                  | 0.6                     | —                 | μs   |
| Data hold time<br>SCL ↓ → SDA ↓ ↑                           | t <sub>HDDAT</sub> |                                        | 0             | 3.45* <sup>3</sup> | 0                       | 0.9* <sup>4</sup> | μs   |
| Data set-up time<br>SDA ↓ ↑ → SCL ↑                         | t <sub>SUDAT</sub> |                                        | 250           | —                  | 100                     | —                 | ns   |
| Set-up time for STOP condition<br>SCL ↑ → SDA ↑             | t <sub>SUSTO</sub> |                                        | 4.0           | —                  | 0.6                     | —                 | μs   |
| Bus free time between a STOP and START condition            | t <sub>BUS</sub>   |                                        | 4.7           | —                  | 1.3                     | —                 | μs   |

\*1 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

\*2 : R,C : Pull-up resistance and load capacitance of the SCL and SDA lines.

\*3 : The maximum t<sub>HDDAT</sub> must be satisfied if the device does not extend the “L” width (t<sub>LOW</sub>) of the SCL signal.

\*4 : A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SUDAT</sub> ≥ 250 ns must then be met.



# MB90860E Series

## 5. A/D Converter

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

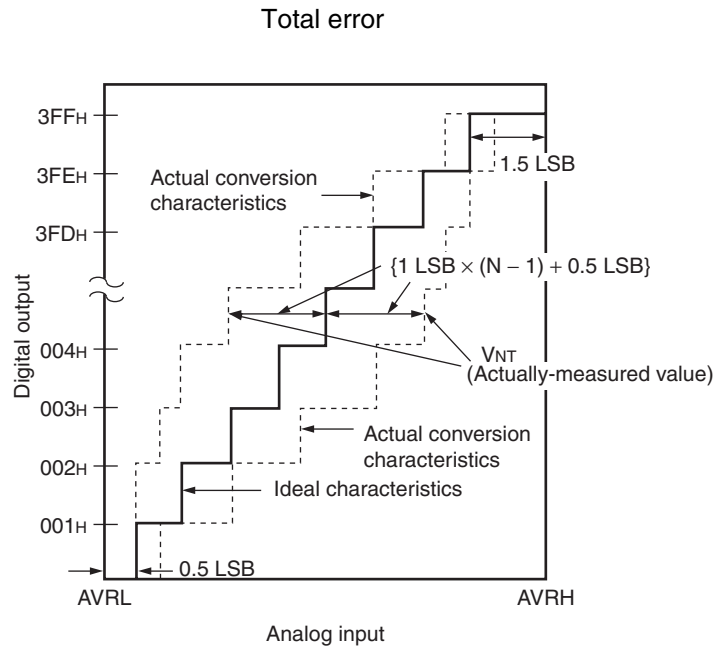
| Parameter                        | Symbol    | Pin              | Value                                 |                                       |                                       | Unit          | Remarks                                              |
|----------------------------------|-----------|------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------|------------------------------------------------------|
|                                  |           |                  | Min                                   | Typ                                   | Max                                   |               |                                                      |
| Resolution                       | —         | —                | —                                     | —                                     | 10                                    | bit           |                                                      |
| Total error                      | —         | —                | —                                     | —                                     | $\pm 3.0$                             | LSB           |                                                      |
| Nonlinearity error               | —         | —                | —                                     | —                                     | $\pm 2.5$                             | LSB           |                                                      |
| Differential nonlinearity error  | —         | —                | —                                     | —                                     | $\pm 1.9$                             | LSB           |                                                      |
| Zero reading voltage             | $V_{OT}$  | AN0 to AN23      | $\text{AVRL} - 1.5 \times \text{LSB}$ | $\text{AVRL} + 0.5 \times \text{LSB}$ | $\text{AVRL} + 2.5 \times \text{LSB}$ | V             |                                                      |
| Full scale reading voltage       | $V_{FST}$ | AN0 to AN23      | $\text{AVRH} - 3.5 \times \text{LSB}$ | $\text{AVRH} - 1.5 \times \text{LSB}$ | $\text{AVRH} + 0.5 \times \text{LSB}$ | V             |                                                      |
| Compare time                     | —         | —                | 1.0                                   | —                                     | 16500                                 | $\mu\text{s}$ | $4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$ |
|                                  |           |                  | 2.0                                   |                                       |                                       |               | $4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$    |
| Sampling time                    | —         | —                | 0.5                                   | —                                     | $\infty$                              | $\mu\text{s}$ | $4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$ |
|                                  |           |                  | 1.2                                   |                                       |                                       |               | $4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$    |
| Analog port input current        | $I_{AIN}$ | AN0 to AN23      | -0.3                                  | —                                     | +0.3                                  | $\mu\text{A}$ |                                                      |
| Analog input voltage             | $V_{AIN}$ | AN0 to AN23      | AVRL                                  | —                                     | AVRH                                  | V             |                                                      |
| Reference voltage                | —         | AVRH             | $\text{AVRL} + 2.7$                   | —                                     | $\text{AV}_{CC}$                      | V             |                                                      |
|                                  | —         | AVRL             | 0                                     | —                                     | $\text{AVRH} - 2.7$                   | V             |                                                      |
| Power supply current             | $I_A$     | $\text{AV}_{CC}$ | —                                     | 3.5                                   | 7.5                                   | mA            |                                                      |
|                                  | $I_{AH}$  | $\text{AV}_{CC}$ | —                                     | —                                     | 5                                     | $\mu\text{A}$ | *                                                    |
| Reference voltage current        | $I_R$     | AVRH             | —                                     | 600                                   | 900                                   | $\mu\text{A}$ |                                                      |
|                                  | $I_{RH}$  | AVRH             | —                                     | —                                     | 5                                     | $\mu\text{A}$ | *                                                    |
| Variation between input channels | —         | AN0 to AN23      | —                                     | —                                     | 4                                     | LSB           |                                                      |

\* : This is the current when the A/D converter is not being operated, and the CPU is stopped ( $V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$ ) .

Note : The relative error increases as  $\text{AVRH} - \text{AVRL}$  becomes smaller.

## 6. Definition of A/D Converter Terms

|                              |                                                                                                                                                                                                                                                                     |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Resolution                   | : Analog variation that is recognized by an A/D converter.                                                                                                                                                                                                          |
| Non linearity error          | : Deviation of the actual conversion characteristics from a line that connects the zero transition point ( "00 0000 0000" $\leftarrow \rightarrow$ "00 0000 0001" ) to the full-scale transition point ( "11 1111 1110" $\leftarrow \rightarrow$ "11 1111 1111" ) . |
| Differential linearity error | : Deviation from the ideal value of the input voltage required to change the output code by LSB.                                                                                                                                                                    |
| Total error                  | : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.                                                                                                           |



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : A/D converter digital output value

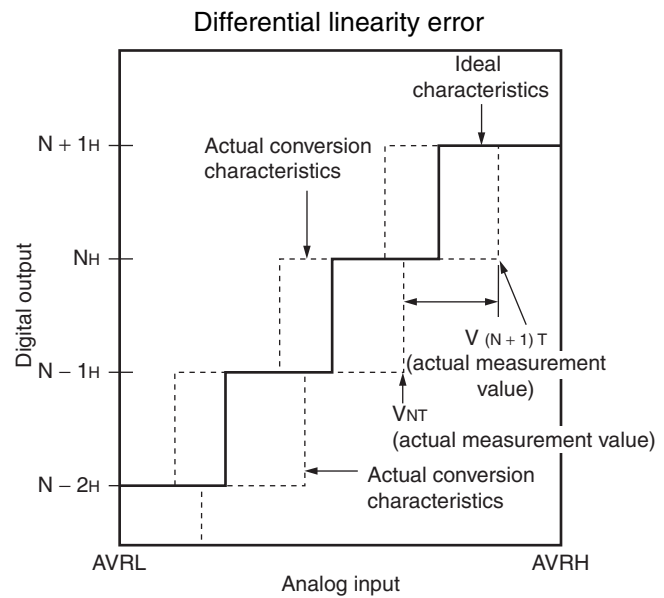
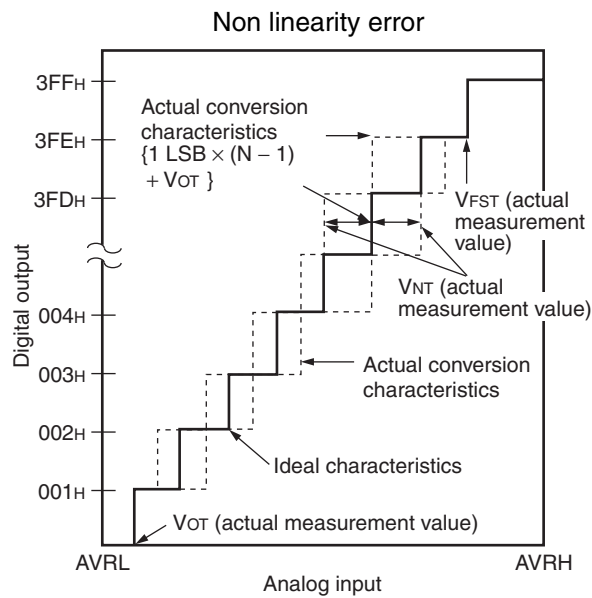
$$V_{OT} \text{ (Ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (Ideal value)} = AVRH - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : The voltage at which the digital output changes from  $(N - 1)_H$  to  $N_H$ .

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} [\text{V}]$$

N : A/D converter digital output value

$V_{OT}$  : The voltage at which the digital output changes from "000<sub>H</sub>" to "001<sub>H</sub>."

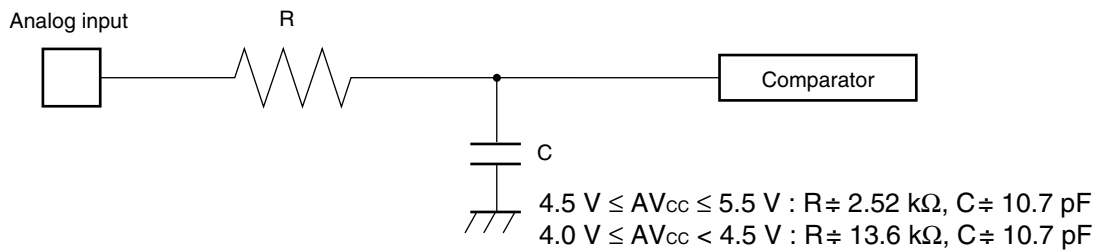
$V_{FST}$  : The voltage at which the digital output changes from "3FE<sub>H</sub>" to "3FF<sub>H</sub>."

## 7. Notes on A/D Converter Unit

Use the device such that the output impedance of the external circuits attached to the analog inputs satisfy the following conditions.

- It is recommended that the output impedance of external circuits are approx. 1.5 kΩ or lower ( $4.0\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$ , sampling period = 0.5 μs)
- If an external capacitor is used, in consideration of the capacitive voltage division effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor is several thousand times greater than the internal capacitor.
- If the output impedance of the external circuit is too high, the sampling period for the analog voltage may be insufficient.

### • Analog input circuit model



Note : The values shown in this figure are reference values.

## 8. Flash Memory Program/Erase Characteristics

| Parameter                            | Conditions                                         | Value |     |      | Unit  | Remarks                                     |
|--------------------------------------|----------------------------------------------------|-------|-----|------|-------|---------------------------------------------|
|                                      |                                                    | Min   | Typ | Max  |       |                                             |
| Sector erase time                    | T <sub>A</sub> = +25 °C<br>V <sub>CC</sub> = 5.0 V | —     | 1   | 15   | s     | Excludes programming prior to erasure       |
| Chip erase time                      |                                                    | —     | 9   | —    | s     | Excludes programming prior to erasure       |
| Word (16-bit width) programming time |                                                    | —     | 16  | 3600 | μs    | Except for the over head time of the system |
| Number of program/erase cycles       | —                                                  | 10000 | —   | —    | cycle |                                             |
| Flash data retention time            | Average<br>T <sub>A</sub> = +85 °C                 | 20    | —   | —    | Year  | *                                           |

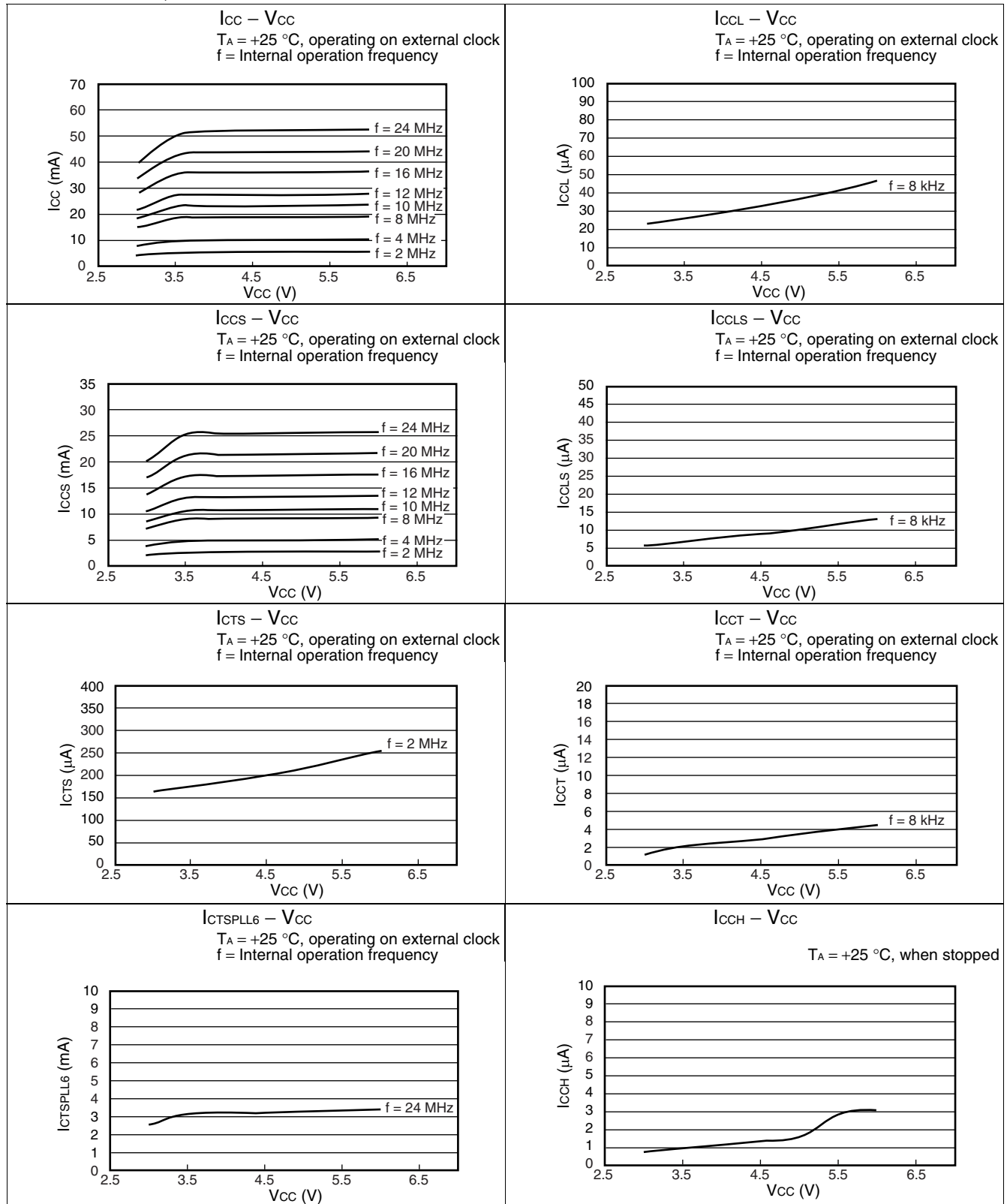
\* : This value is the result of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .



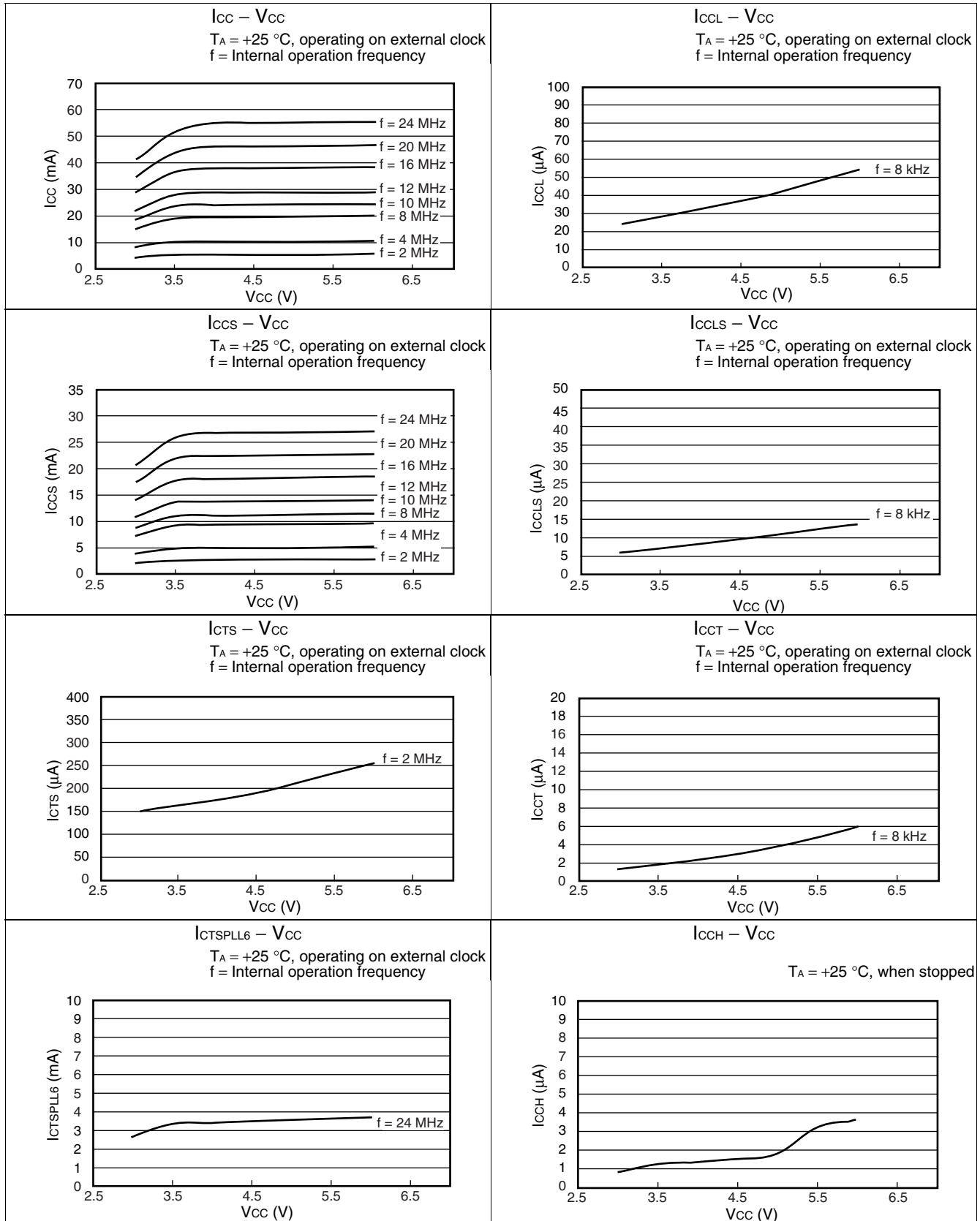
# MB90860E Series

## EXAMPLE CHARACTERISTICS

- MB90F867E, MB90F867ES

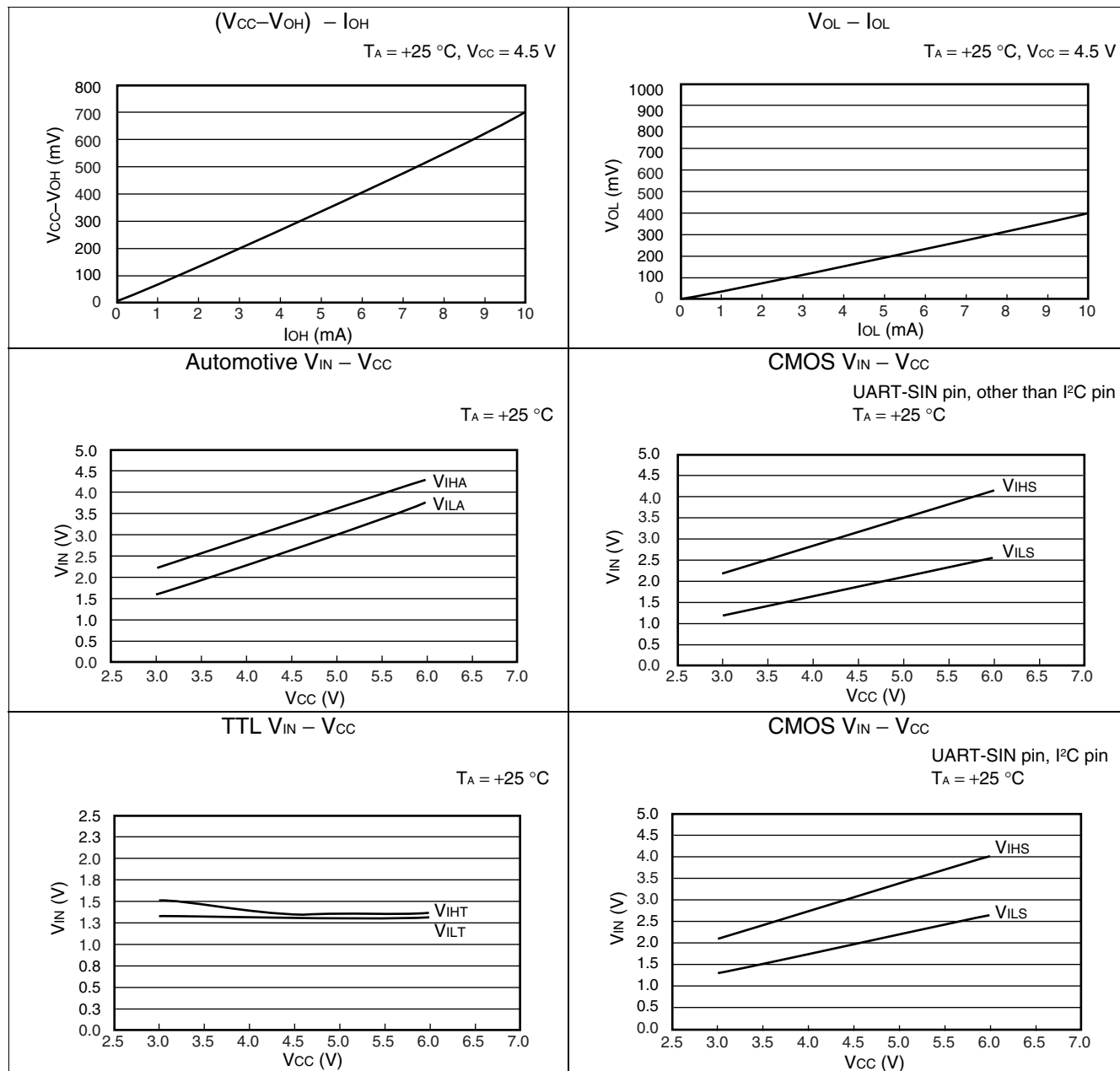


• MB90867E, MB90867ES



# MB90860E Series

## • I/O characteristics

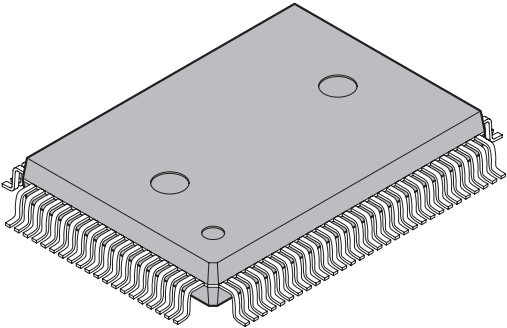


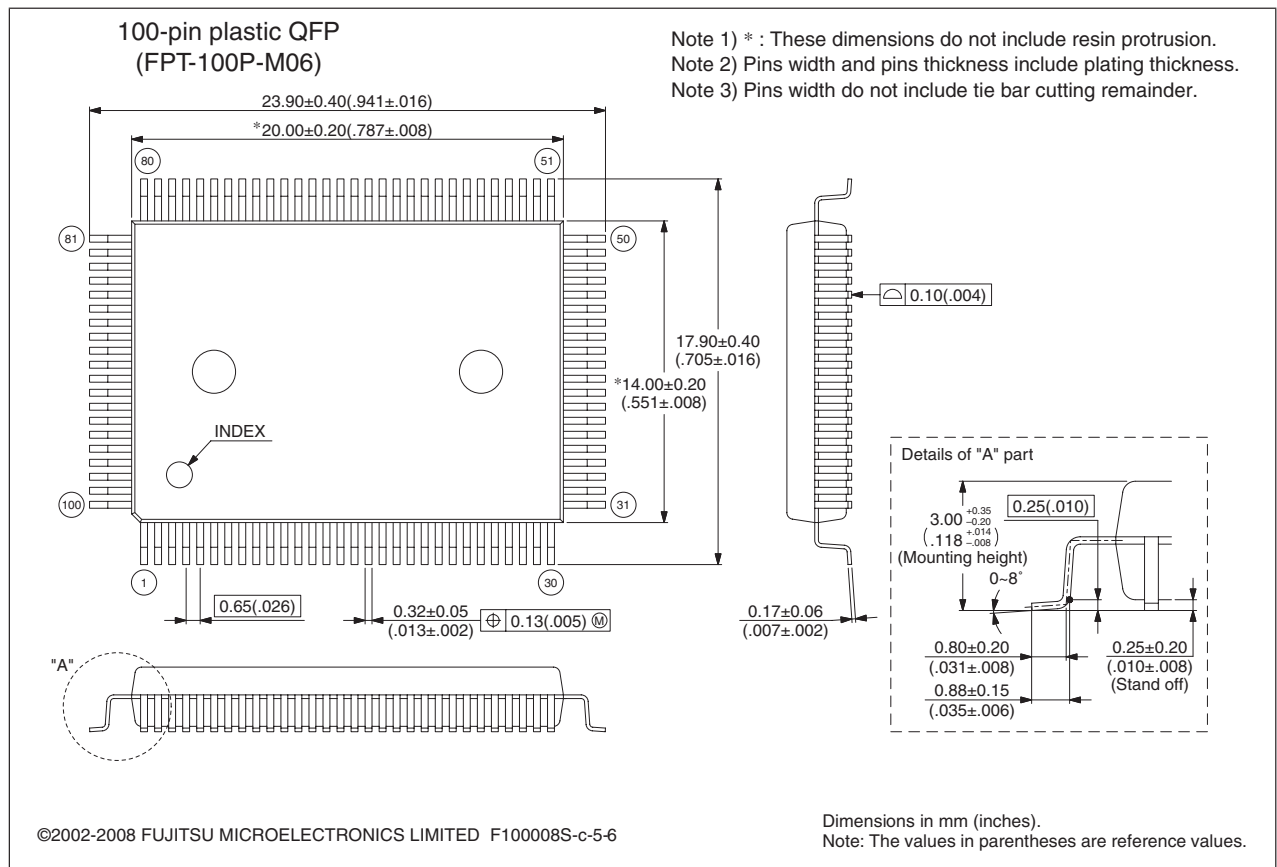
## ■ ORDERING INFORMATION

| Part number     | Package                                | Remarks              |
|-----------------|----------------------------------------|----------------------|
| MB90F867EPF     | 100-pin plastic QFP<br>(FPT-100P-M06)  | Flash memory product |
| MB90F867ESPF    |                                        |                      |
| MB90F867EPMC    | 100-pin plastic LQFP<br>(FPT-100P-M20) |                      |
| MB90F867ESPMC   |                                        |                      |
| MB90867EPF      | 100-pin plastic QFP<br>(FPT-100P-M06)  | MASK ROM product     |
| MB90867ESPF     |                                        |                      |
| MB90867EPMC     | 100-pin plastic LQFP<br>(FPT-100P-M20) |                      |
| MB90867ESPMC    |                                        |                      |
| MB90V340E-101CR | 299-pin ceramic PGA<br>(PGA-299C-A01)  | Evaluation product   |
| MB90V340E-102CR |                                        |                      |

# MB90860E Series

## ■ PACKAGE DIMENSIONS

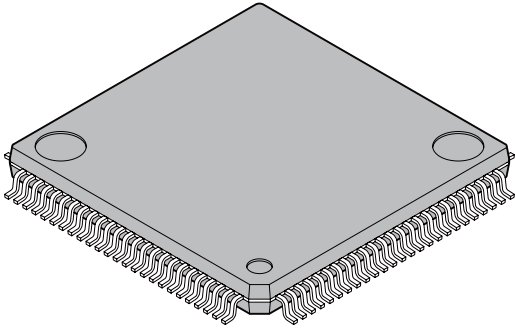
|                                                                                                                                    |                                |                     |
|------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|---------------------|
|  <p>100-pin plastic QFP</p> <p>(FPT-100P-M06)</p> | Lead pitch                     | 0.65 mm             |
|                                                                                                                                    | Package width × package length | 14.00 × 20.00 mm    |
|                                                                                                                                    | Lead shape                     | Gullwing            |
|                                                                                                                                    | Sealing method                 | Plastic mold        |
|                                                                                                                                    | Mounting height                | 3.35 mm MAX         |
|                                                                                                                                    | Code (Reference)               | P-QFP100-14×20-0.65 |
|                                                                                                                                    |                                |                     |

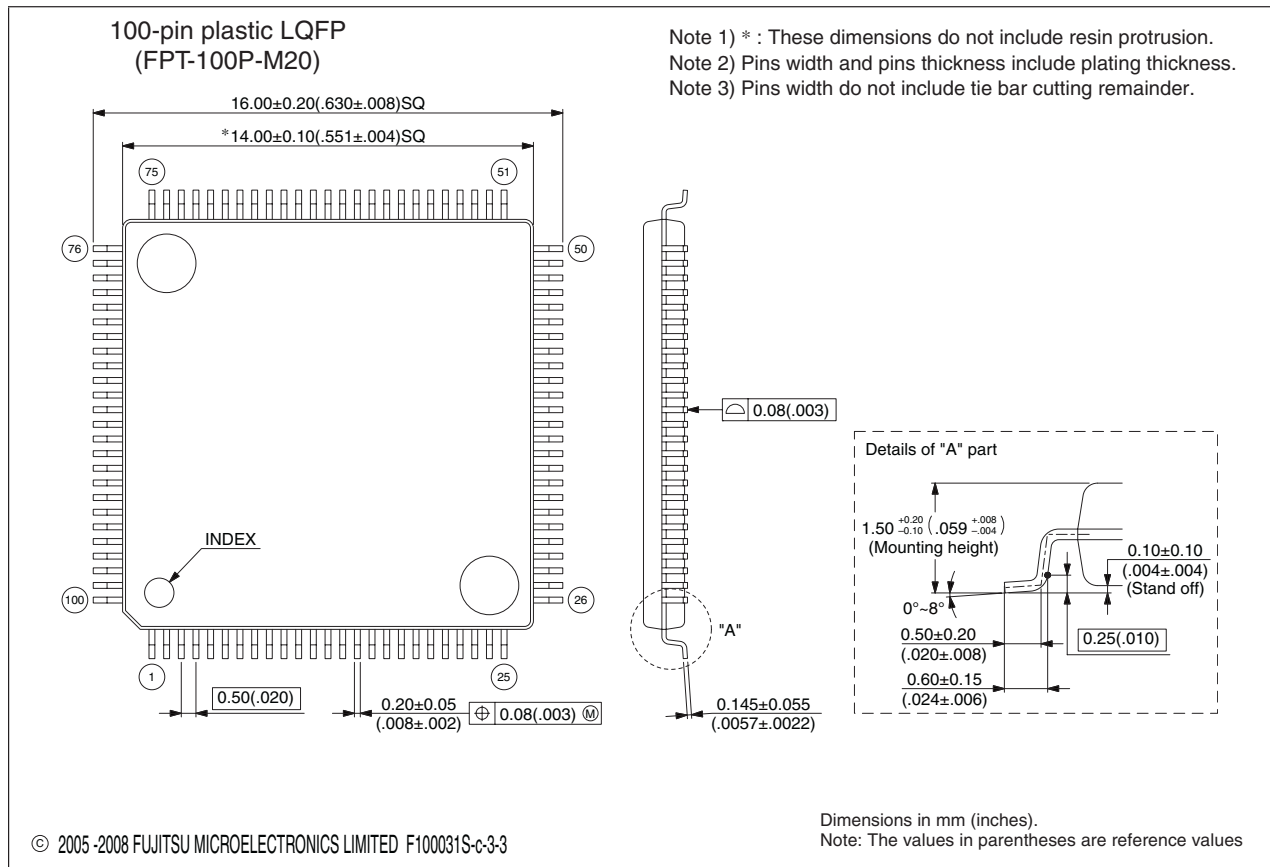


Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

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|                                                                                                                                     |                                |                       |
|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----------------------|
|  <p>100-pin plastic LQFP</p> <p>(FPT-100P-M20)</p> | Lead pitch                     | 0.50 mm               |
|                                                                                                                                     | Package width × package length | 14.0 mm × 14.0 mm     |
|                                                                                                                                     | Lead shape                     | Gullwing              |
|                                                                                                                                     | Sealing method                 | Plastic mold          |
|                                                                                                                                     | Mounting height                | 1.70 mm Max           |
|                                                                                                                                     | Weight                         | 0.65 g                |
|                                                                                                                                     | Code (Reference)               | P-LFQFP100-14×14-0.50 |



Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

# MB90860E Series

## ■ MAIN CHANGES IN THIS EDITION

| Page | Section                                          | Change Results                                                                                                                                                                                                              |
|------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| —    | —                                                | Changed the package.<br>FPT-100P-M05 → FPT-100P-M20                                                                                                                                                                         |
| 60   | ■ ELECTRICAL CHARACTERISTICS<br>5. A/D Converter | Changed the items for “Zero reading voltage” and “Full scale reading voltage”.                                                                                                                                              |
| 67   | ■ ORDERING INFORMATION                           | Changed the part numbers;<br>MB90867EPFV → MB90367EPMC<br>MB90867ESPFV → MB90867ESPMC<br>MB90F867EPFV → MB90F867EPMC<br>MB90F867ESPFV → MB90F867ESPMC<br>MB90V340E-101 → MB90V340E-101CR<br>MB90V340E-102 → MB90V340E-102CR |
| 69   | ■ PACKAGE DIMENSIONS                             | Changed the package's figure.<br>FPT-100P-M05 → FPT-100P-M20                                                                                                                                                                |

The vertical lines marked in the left side of the page show the changes.

**MEMO**



# MB90860E Series

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