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## Features

- Temperature range
  - Automotive: -40 °C to 125 °C
- High speed
  - $t_{AA} = 15 \text{ ns}$
- Optimized voltage range: 2.5 V to 2.7 V
- Automatic power down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed and power
- Package offered: 44-pin TSOP II

## Functional Description

The CY7C1020CV26 is a high performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs LOW. If byte low enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ). If byte high enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ).

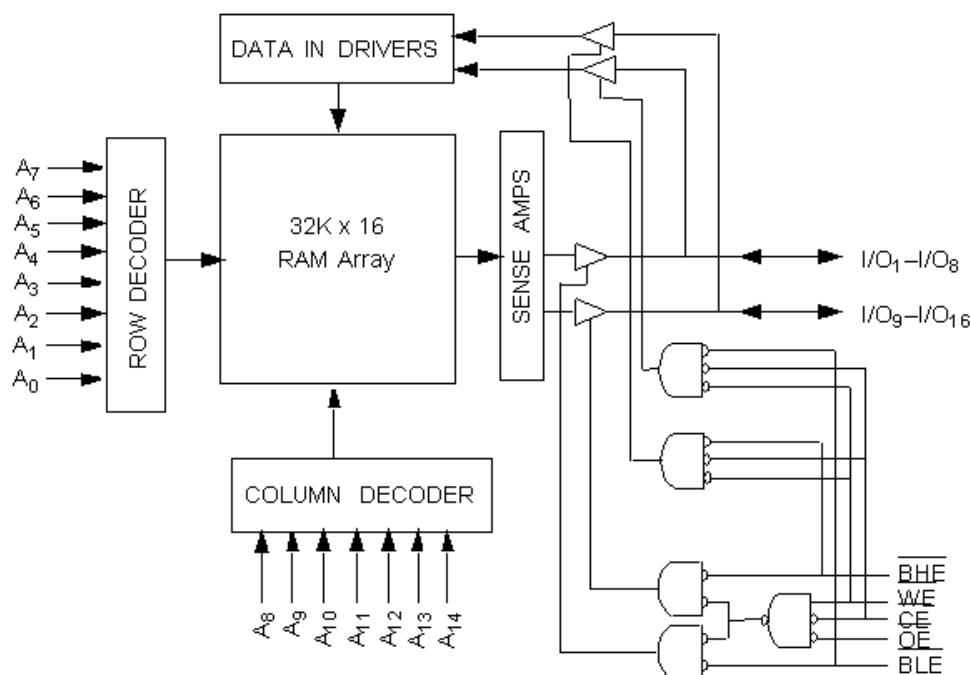
Reading from the device is accomplished by taking chip enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the write enable ( $\overline{WE}$ ) HIGH. If byte low enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_9$  to  $I/O_{16}$ . See the [Truth Table](#) on page 11 for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1020CV26 is available in a standard 44-pin TSOP Type II.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

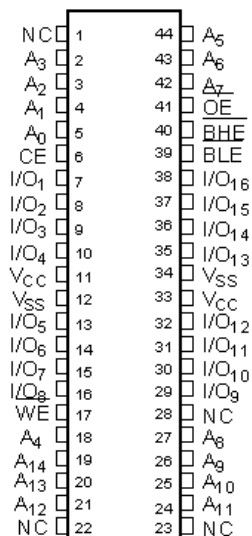


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## Pin Configuration

Figure 1. 44-pin TSOP II pinout (Top View)



## Selection Guide

Description	CY7C1020CV26-15	Unit
Maximum access time	15	ns
Maximum operating current	100	mA
Maximum CMOS standby current	5	mA

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on  $V_{CC}$  to relative GND<sup>[1]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs  
in High-Z State<sup>[1]</sup> ..... -0.5 V to  $V_{CC}+0.5$  V

DC input voltage<sup>[1]</sup> ..... -0.5 V to  $V_{CC}+0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Automotive	-40 °C to +125 °C	2.5 V to 2.7 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7C1020CV26		Unit
			Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Minimum}, I_{OH} = -1.0 \text{ mA}$	2.3	—	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Minimum}, I_{OL} = 1.0 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[1]</sup>		-0.3	0.8	V
$I_{IX}$	Input load current	$GND \leq V_I \leq V_{CC}$	-5	+5	μA
$I_{OZ}$	Output leakage current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-5	+5	μA
$I_{OS}^{[2]}$	Output short circuit current	$V_{CC} = \text{Maximum}, V_{OUT} = GND$	—	-300	mA
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Maximum}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	—	100	mA
$I_{SB1}$	Automatic CE power-down Current – TTL Inputs	Maximum $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	—	40	mA
$I_{SB2}$	Automatic CE power-down Current – CMOS Inputs	Maximum $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$	—	5	mA

### Notes

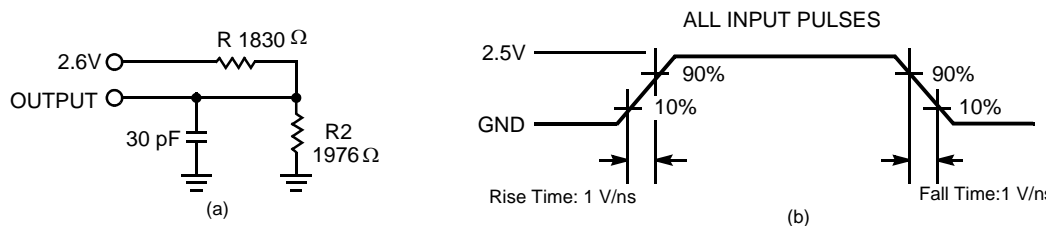
- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

## Capacitance

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 2.6\text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 1V/ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.5 V and transmission line loads as in (a) of Figure 2.

## AC Switching Characteristics

Over the Operating Range

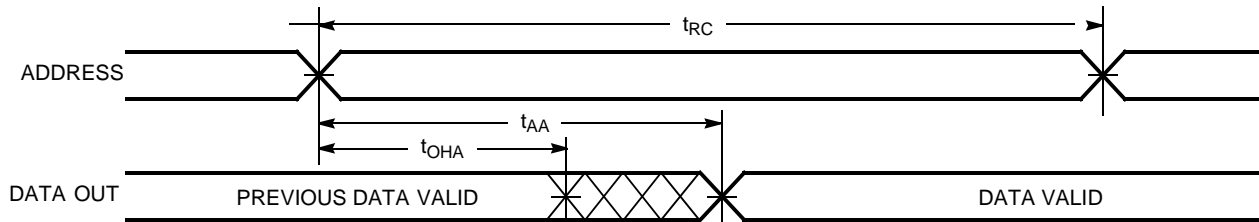
Parameter	Description	CY7C1020CV26		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	15	—	ns
t <sub>AA</sub>	Address to data valid	—	15	ns
t <sub>OHA</sub>	Data hold from address change	3	—	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data valid	—	15	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	—	7	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[5]</sup>	0	—	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[5, 6]</sup>	—	7	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to low Z <sup>[5]</sup>	3	—	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to high Z <sup>[5, 6]</sup>	—	7	ns
t <sub>PU</sub> <sup>[7]</sup>	$\overline{\text{CE}}$ LOW to power-up	0	—	ns
t <sub>PD</sub> <sup>[7]</sup>	$\overline{\text{CE}}$ HIGH to power-down	—	15	ns
t <sub>DBE</sub>	Byte enable to data valid	—	7	ns
t <sub>LZBE</sub>	Byte enable to low Z	0	—	ns
t <sub>HZBE</sub>	Byte disable to high Z	—	7	ns
Write Cycle <sup>[8, 9]</sup>				
t <sub>WC</sub>	Write cycle time	15	—	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end	10	—	ns
t <sub>AW</sub>	Address setup to write end	10	—	ns
t <sub>HA</sub>	Address hold from write end	0	—	ns
t <sub>SA</sub>	Address setup to write start	0	—	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	10	—	ns
t <sub>SD</sub>	Data setup to write end	8	—	ns
t <sub>HD</sub>	Data hold from write end	0	—	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[5]</sup>	3	—	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[5, 6]</sup>	—	4	ns
t <sub>BW</sub>	Byte enable to end of write	10	—	ns

### Notes

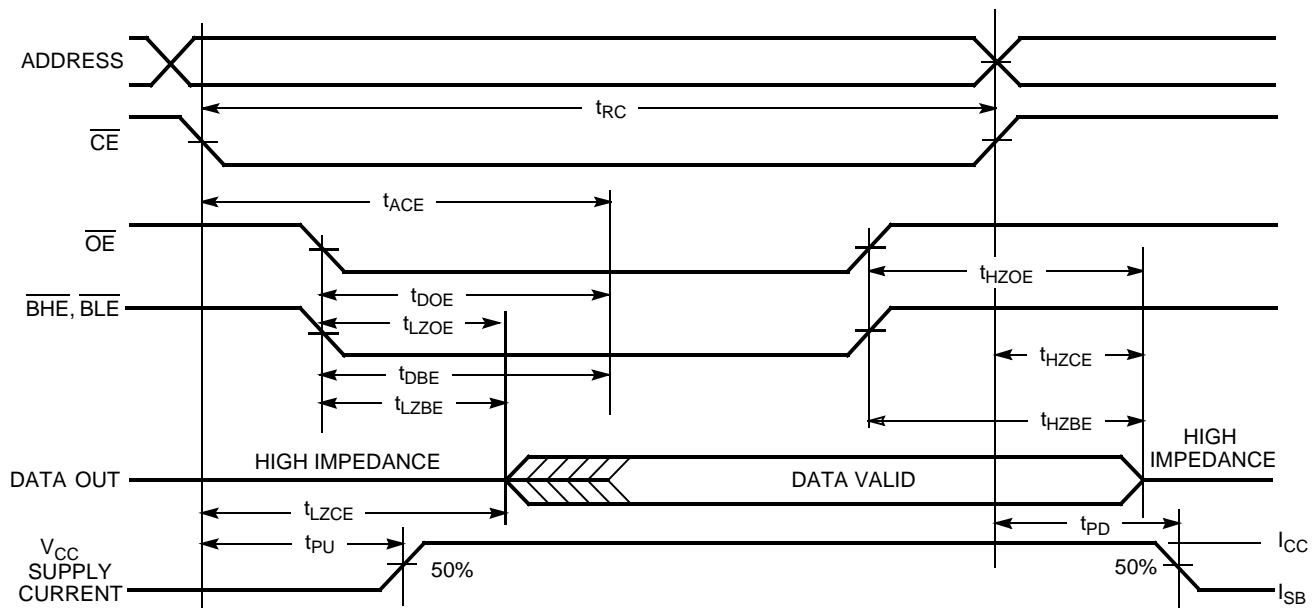
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured  $\pm 500$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}$  /  $\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}$  /  $\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write pulse width for WRITE Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 3. Read Cycle No. 1** [10, 11]



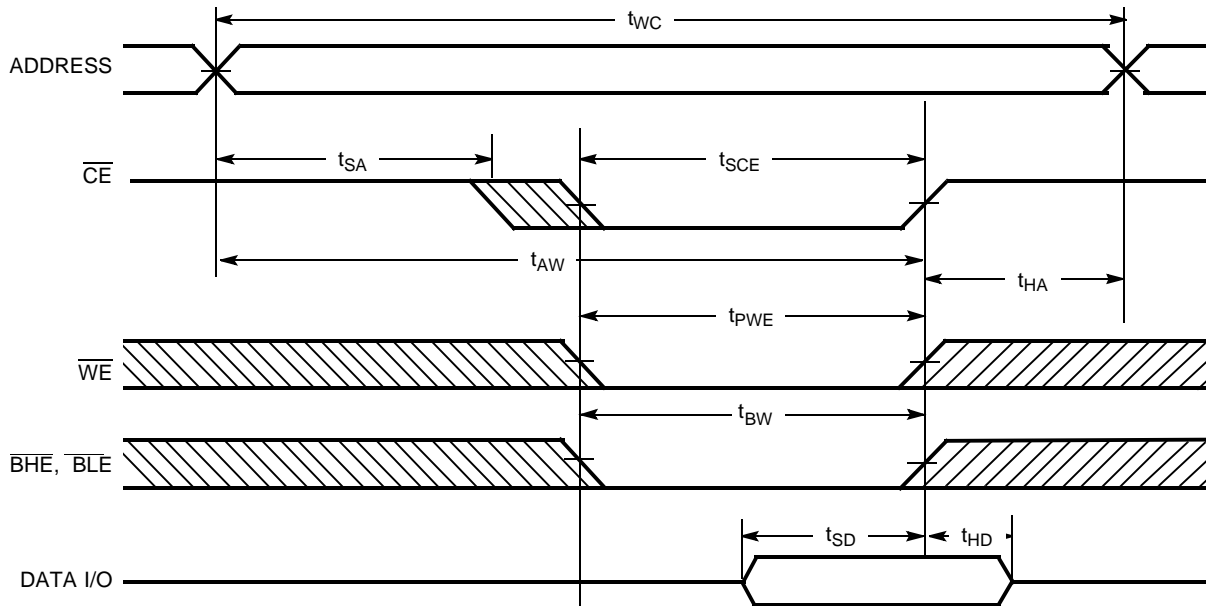
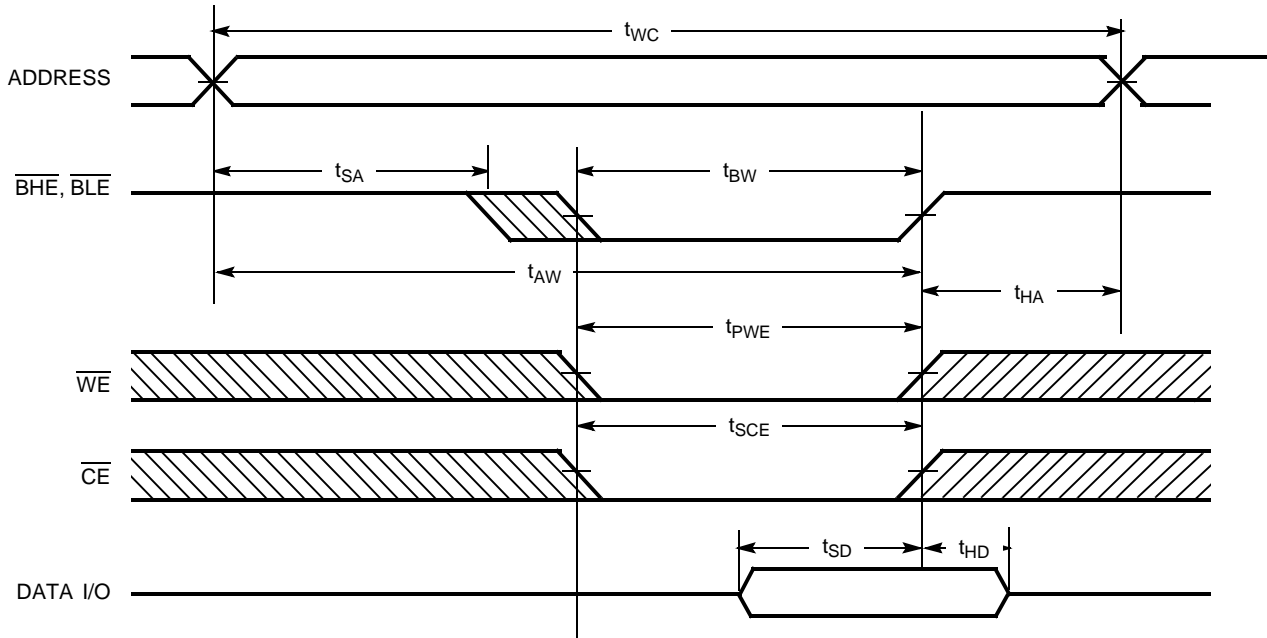
**Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [11, 12]



### Notes

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



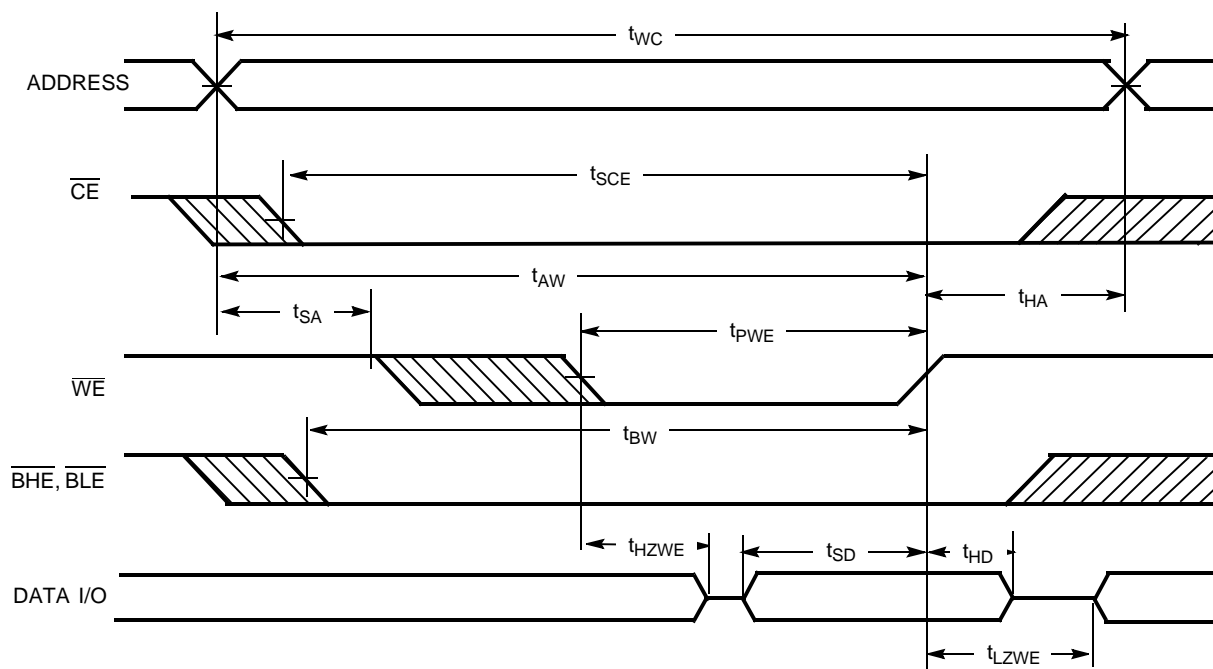
**Switching Waveforms (continued)**
**Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [13, 14]**

**Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes**

 13. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}} = V_{\text{IH}}$ .

 14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

## Switching Waveforms (continued)

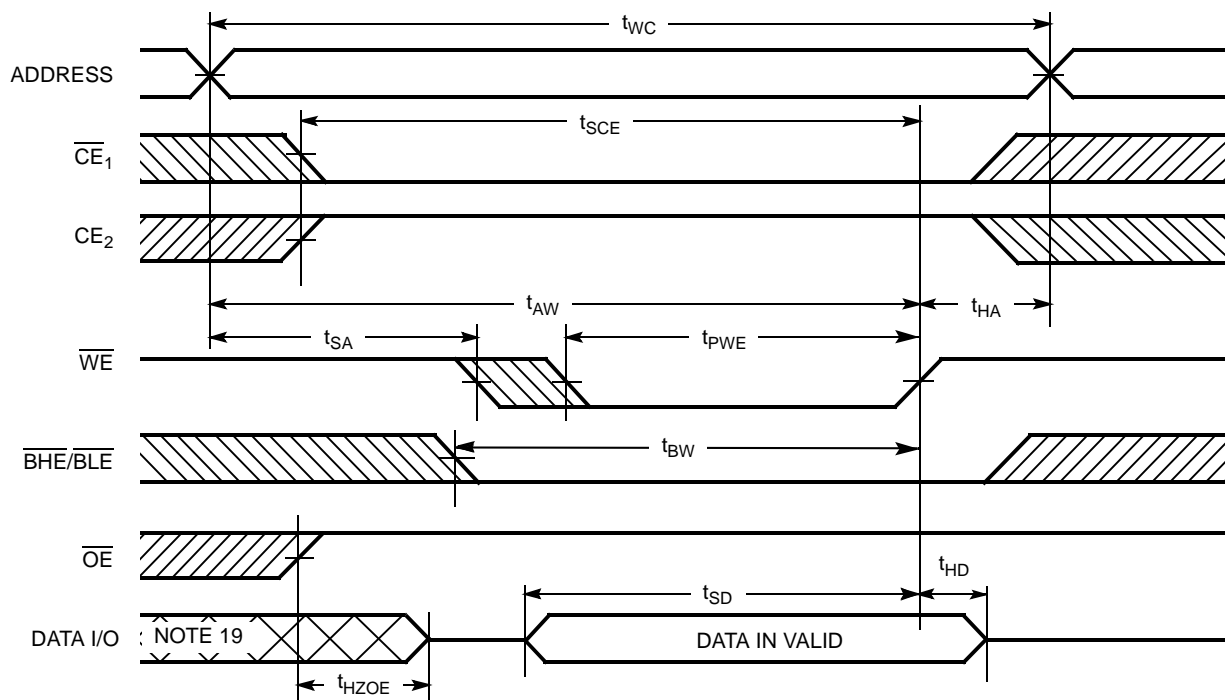
**Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) <sup>[15]</sup>**



### Note

15. The minimum write pulse width for WRITE Cycle No.3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Switching Waveforms** (continued)

**Figure 8. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled)** [16, 17, 18]

**Notes**

16. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
17. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
18. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.
19. During this period the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>1</sub> –I/O <sub>8</sub>	I/O <sub>9</sub> –I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I <sub>CC</sub> )
			L	H	Data Out	High Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data Out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I <sub>CC</sub> )
			L	H	Data In	High Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data In	Write – Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

## Ordering Information

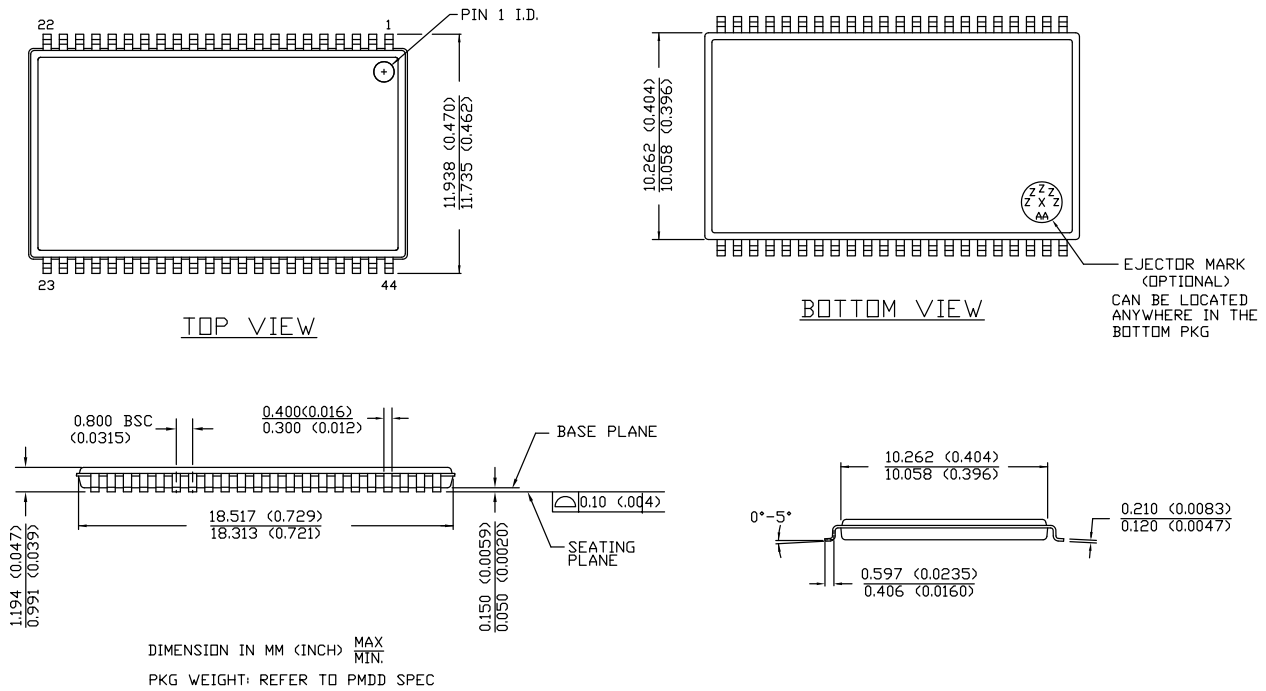
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1020CV26-15ZSX E	Z44	44-pin TSOP Type II (Pb-free)	Automotive

## Ordering Code Definitions

CY	7	C	1	02	0	C	V26	-	15	ZS	X	E	
													Temperature Range:
													E = Automotive
													Pb-free
													Package Type:
													ZS = 44-pin TSOP Type II
													Speed Grade= 15 ns
													Voltage Range: V26 = 2.5 V to 2.7 V
													Process Technology: C = 0.16 $\mu$ m Technology
													Data Width: 0 = x 16-bits
													Density: 02 = 512-Kbit density
													Family Code: 1 = Fast Asynchronous SRAM family
													Technology Code: C = CMOS
													Marketing Code: 7 = SRAM
													Company ID: CY = Cypress

## Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt

## Document History Page

Document Title: CY7C1020CV26, 512-Kbit (32 K × 16) Static RAM Document Number: 38-05406				
Rev.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	128060	07/30/03	EJH	Customized data sheet to meet special requirements for CG5988AF Automotive temperature range: –40°C / +125°C
*A	352999	See ECN	SYT	Updated Document Title (to include the mention of '512Kb'). Removed 'CG5988AF' from the Datasheet. Updated <a href="#">Features</a> (for better structure).
*B	2903127	04/01/2010	VIVG	Updated <a href="#">Package Diagrams</a> . Added <a href="#">Sales, Solutions, and Legal Information</a> . Updated to new template.
*C	3109992	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> .
*D	3346414	08/16/2011	RAME	Updated <a href="#">Ordering Code Definitions</a> .
*E	4499482	09/11/2014	MEMJ	Updated <a href="#">AC Switching Characteristics</a> : Updated Note 7. Added Note 9 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 15 and referred the same note in <a href="#">Figure 7</a> . Updated <a href="#">Package Diagrams</a> : spec 51-85087 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*F	4573200	11/18/2014	MEMJ	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.
*G	4919066	09/14/2015	VINI	Updated <a href="#">Switching Waveforms</a> : Added <a href="#">Figure 8</a> . Added Note 16, 17, 18, 19 and referred the same notes in <a href="#">Figure 8</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template. Completing Sunset Review.



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