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## Features

- Thin small outline package TSOP I configurable as 2M × 16 or as 4M × 8 static RAM (SRAM)
- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V to 3.6 V
- Ultra low standby power
  - Typical standby current: 3 μA
  - Maximum standby current: 25 μA
- Ultra low active power
  - Typical active current: 10 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-pin TSOP I package and 48-ball FBGA package

## Functional Description

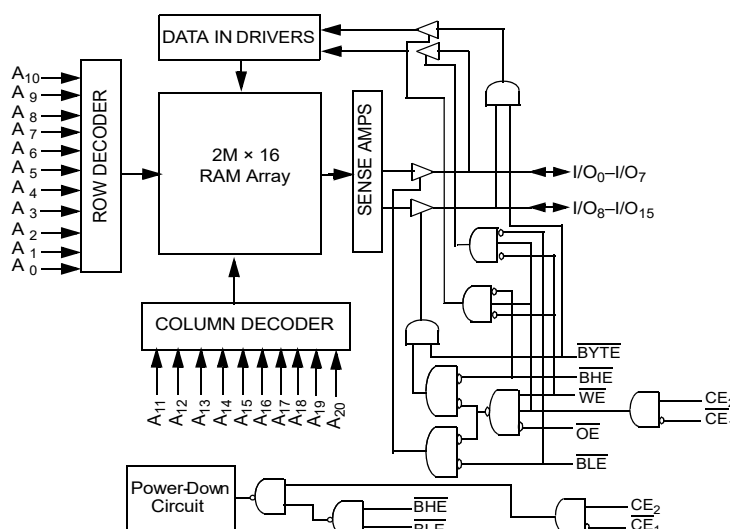
The CY62177EV30 is a high performance CMOS static RAM organized as 2M words by 16 bits and 4M words by 8 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both BHE and BLE are HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and WE LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written to the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>). To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the [Truth Table on page 11](#) for a complete description of read and write modes.

Pin #13 of the 48 TSOP I package is an DNU pin that must be left floating at all times to ensure proper application.

For a complete list of related resources, [click here](#).

## Logic Block Diagram

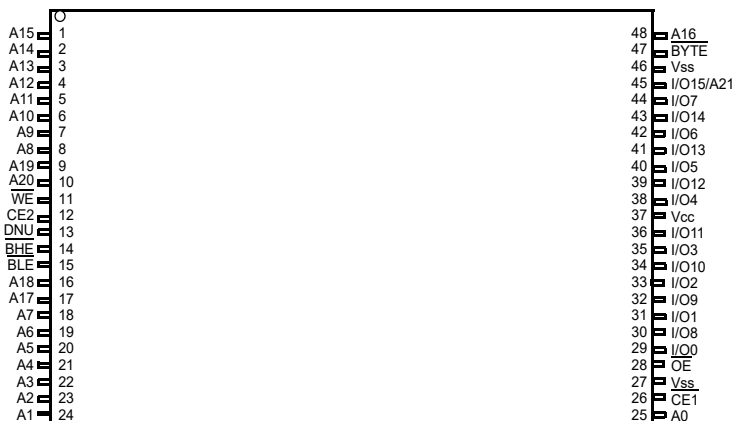


## Contents

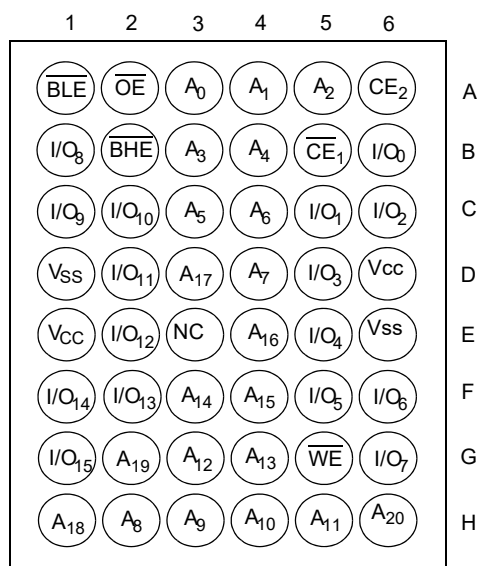
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## Pin Configurations

**Figure 1. 48-pin TSOP I pinout (Front View)** <sup>[1, 2]</sup>



**Figure 2. 48-ball FBGA pinout (Top View)**



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>Max</sub>							
	Min	Typ <sup>[3]</sup>	Max		Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62177EV30LL	2.2	3.0	3.6	55	10	18	35	45	3	25

### Notes

1. DNU Pin# 13 needs to be left floating to ensure proper application.

2. The BYTE pin in the 48-pin TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 2M × 16 SRAM.

The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 4M × 8 configuration, Pin 45 is A21, while BHE, BLE, and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
to ground potential [4, 5] ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC voltage applied to outputs  
in High Z state [4, 5] ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC input voltage [4, 5] ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ [6]
CY62177EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ [7]	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA $V_{CC} = 2.20$ V	2.0	—	—	V
		$I_{OH} = -1.0$ mA $V_{CC} = 2.70$ V	2.4	—	—	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA $V_{CC} = 2.20$ V	—	—	0.4	V
		$I_{OL} = 2.1$ mA $V_{CC} = 2.70$ V	—	—	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V	1.8	—	$V_{CC} + 0.3$	V
		$V_{CC} = 2.7$ V to 3.6 V	2.2	—	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V	-0.3	—	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V	-0.3	—	0.7 [8]	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1	—	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{Max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$	—	35	45	mA
		$f = 1$ MHz $I_{OUT} = 0$ mA CMOS levels	—	10	18	mA
$I_{SB2}$ [9, 10]	Automatic CE power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ( $\overline{BHE}$ and $\overline{BLE}$ ) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.7$ V	—	3	25	μA

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to  $V_{CC}$  (min) and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Under DC conditions the device meets a  $V_{IL}$  of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V.

- The  $\overline{BYTE}$  pin in the 48-pin TSOP I package has to be tied to  $V_{CC}$  to use the device as a 2M × 16 SRAM.

The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the  $\overline{BYTE}$  signal to  $V_{SS}$ . In the 4M × 8 configuration, Pin 45 is A21, while  $\overline{BHE}$ ,  $\overline{BLE}$ , and  $I/O_8$  to  $I/O_{14}$  pins are not used.

- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ),  $\overline{BYTE}$ , and Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

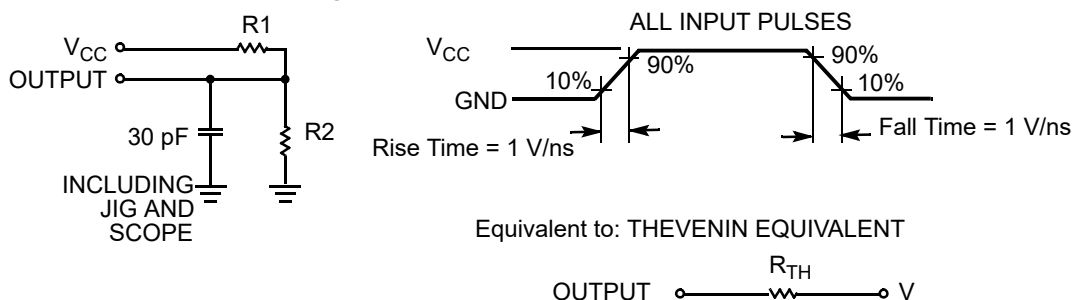
Parameter <sup>[11]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	15	pF
$C_{OUT}$	Output capacitance		15	pF

## Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	FBGA	TSOP I	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	54.8	54.42	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		11.9	9.4	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameter	2.5 V	3.3 V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Note

11. Tested initially and after any design or process changes that may affect these parameters.

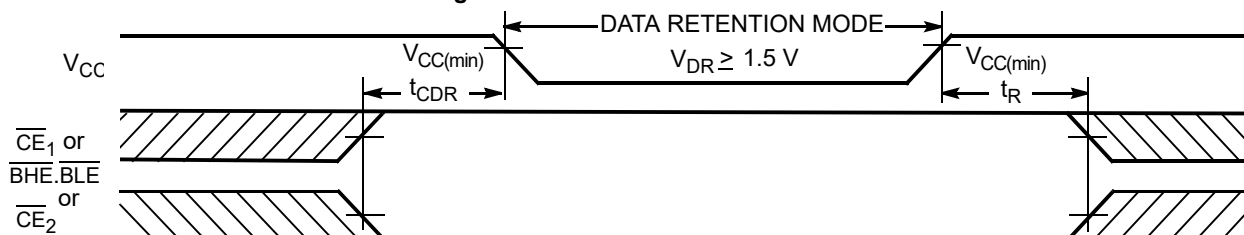
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[12]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}^{[13]}$	Data retention current	$V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	20	$\mu\text{A}$
$t_{CDR}^{[14]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[15]}$	Operation recovery time		55	–	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform<sup>[16]</sup>



### Notes

12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^\circ\text{C}$ .
13. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ),  $\overline{BYTE}$ , Address Pin  $A_{20}$  and Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
16.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip is deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[17]</sup>	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	55	–	ns
t <sub>AA</sub>	Address to data valid	–	55	ns
t <sub>OHA</sub>	Data hold from address change	4	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid	–	55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z <sup>[18]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[18, 19]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[18]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[18, 19]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power up	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power down	–	55	ns
t <sub>DBE</sub>	$\overline{BLE/BHE}$ LOW to data valid	–	55	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low Z <sup>[18]</sup>	10	–	ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to HIGH Z <sup>[18, 19]</sup>	–	18	ns
Write Cycle <sup>[20, 21]</sup>				
t <sub>WC</sub>	Write cycle time	55	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end	40	–	ns
t <sub>AW</sub>	Address setup to write end	40	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	40	–	ns
t <sub>BW</sub>	$\overline{BLE/BHE}$ LOW to write end	40	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from Write End	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[18, 19]</sup>	–	20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[18]</sup>	10	–	ns

### Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{TH}$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in [Figure 3 on page 5](#).

18. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

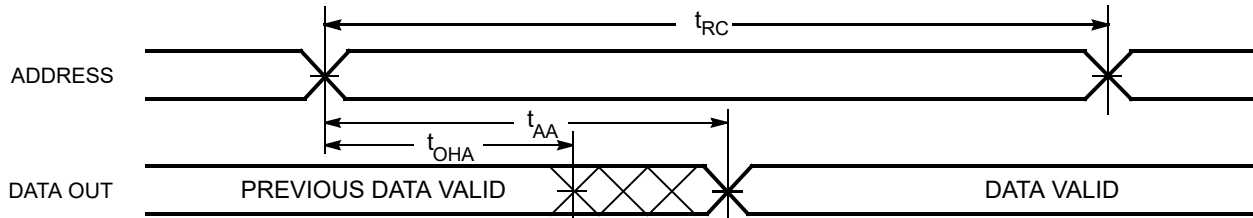
19.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

20. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

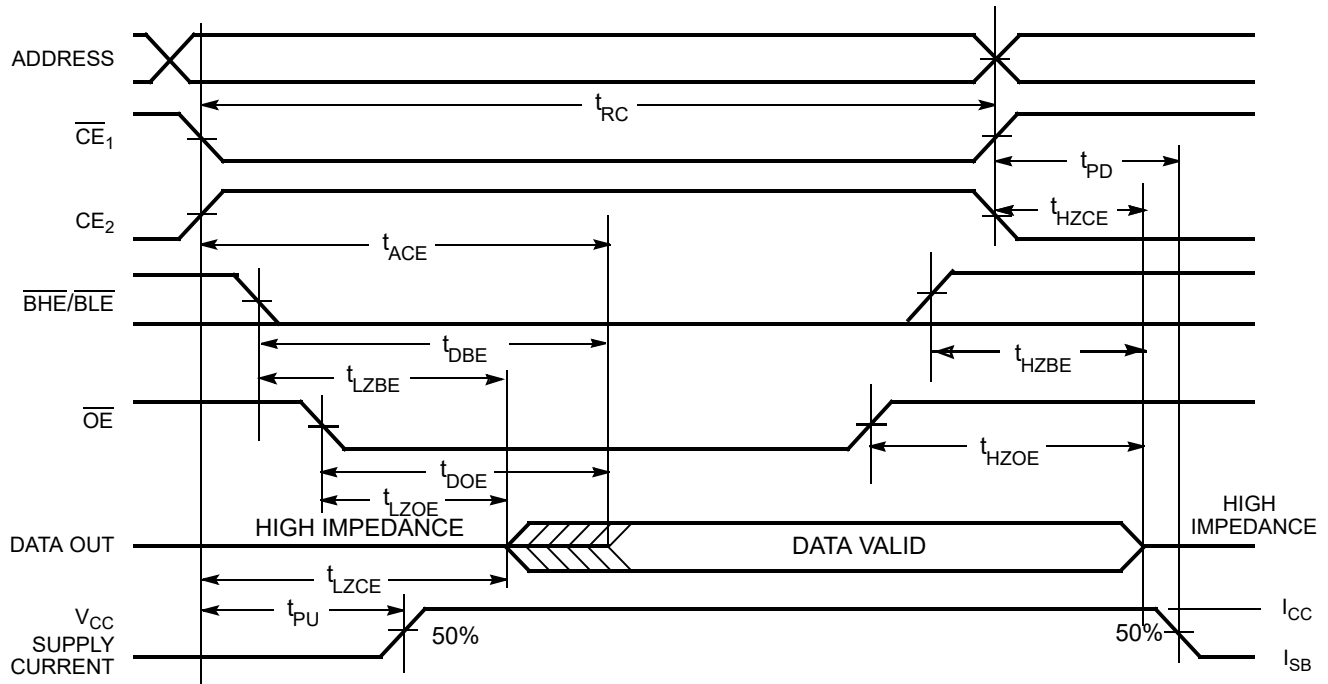
21. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1 (Address Transition Controlled)** [22, 23]



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [23, 24]



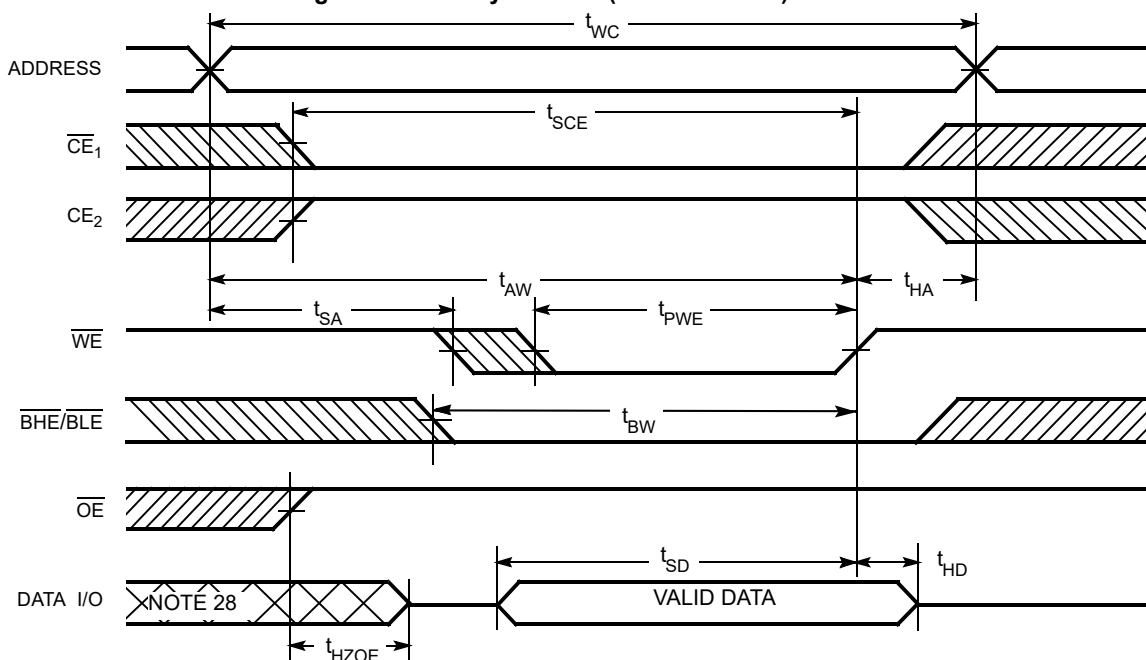
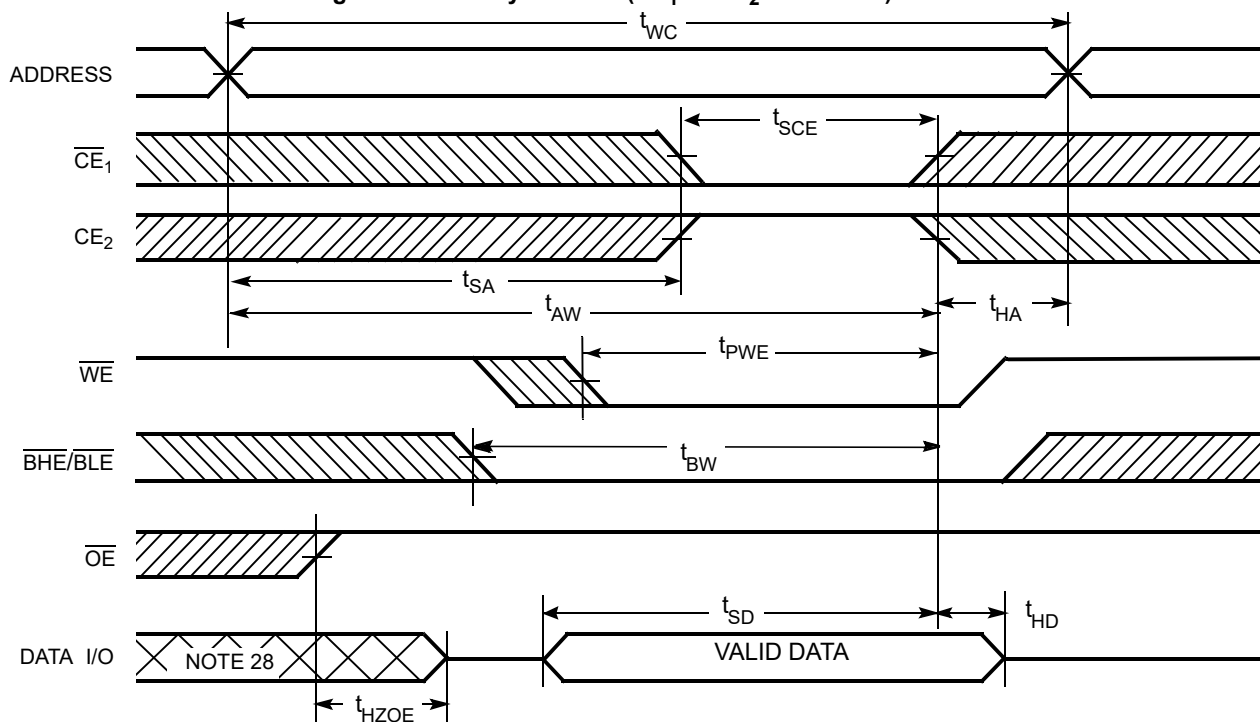
### Notes

22. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .

23.  $\overline{WE}$  is HIGH for read cycle.

24. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{WE}$  Controlled)** [25, 26, 27, 28]

**Figure 8. Write Cycle No. 2 ( $\overline{CE_1}$  or  $\overline{CE_2}$  Controlled)** [25, 26, 27, 28]

**Notes**

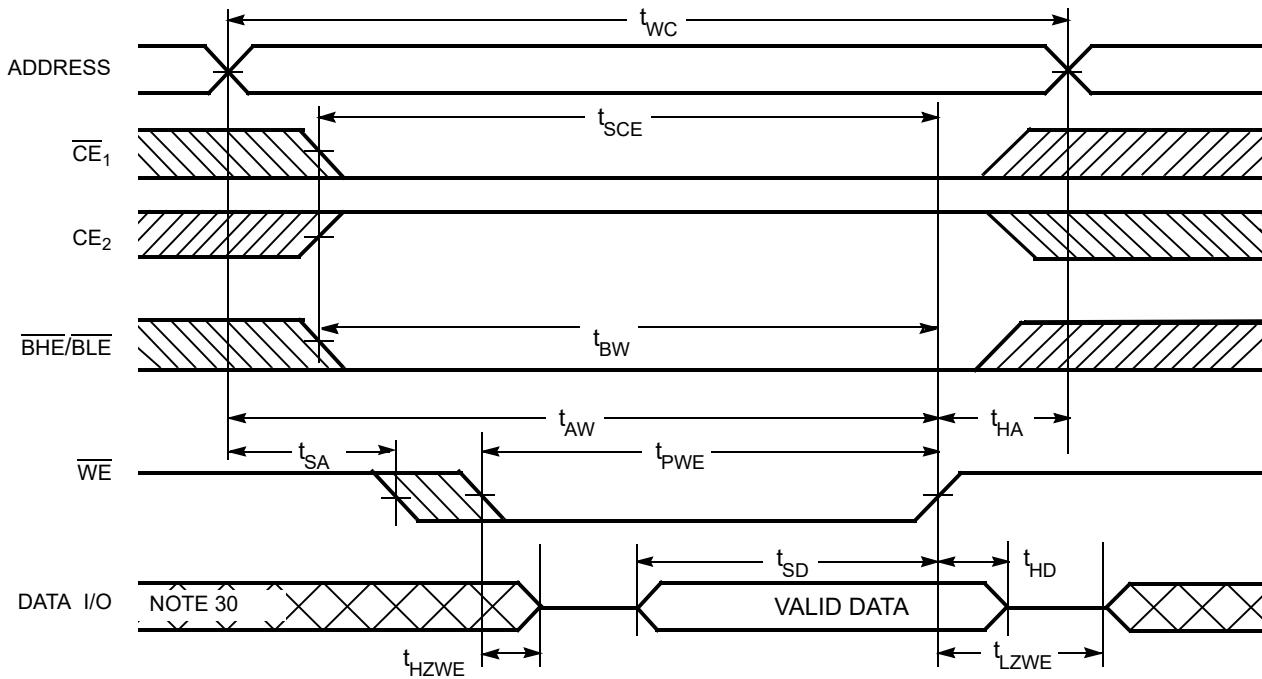
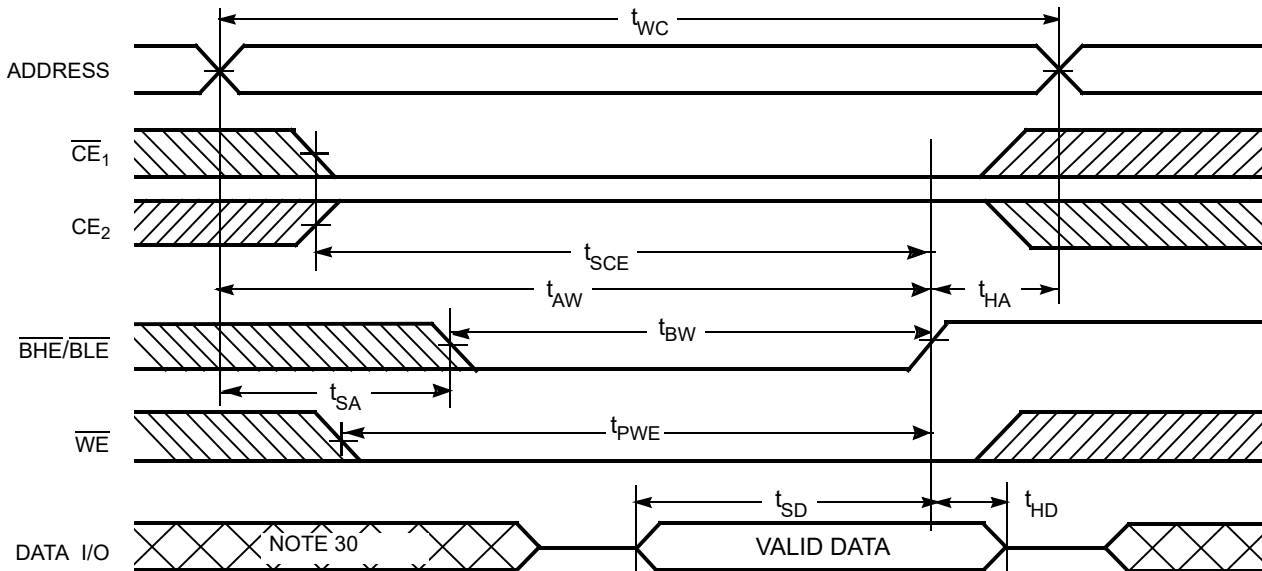
25. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE_1} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

26. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

27. If  $\overline{CE_1}$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

28. During this period the I/Os are in output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [29]**

**Figure 10. Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [29, 32]**

**Notes**

29. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

30. During this period the I/Os are in output state and input signals should not be applied.

31. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Truth Table

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Input/Output	Mode	Power
H	X <sup>[32]</sup>	X	X	X <sup>[32]</sup>	X <sup>[32]</sup>	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	L	X	X	X <sup>[32]</sup>	X <sup>[32]</sup>	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	X <sup>[32]</sup>	X	X	H	H	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data Out ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data In ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )

### Note

32. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

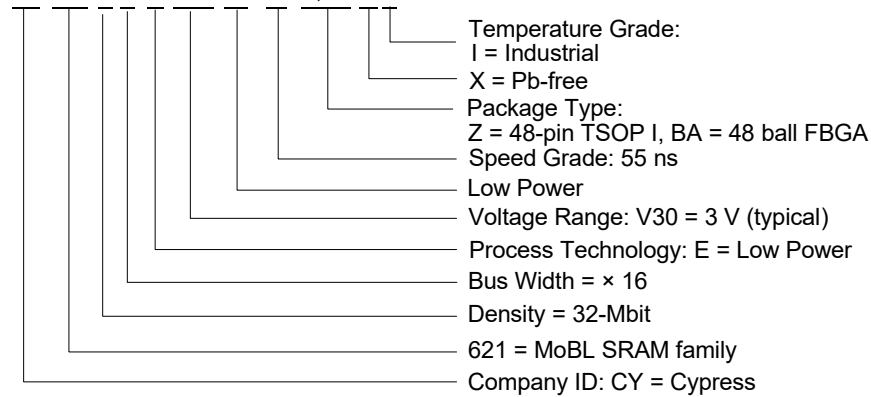
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177EV30LL-55ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) Pb-free	Industrial
55	CY62177EV30LL-55BAXI	51-85191	48 ball FBGA (8 × 9.5 × 1.2 mm) Pb-free	Industrial

Contact your local Cypress sales representative for availability of these parts.

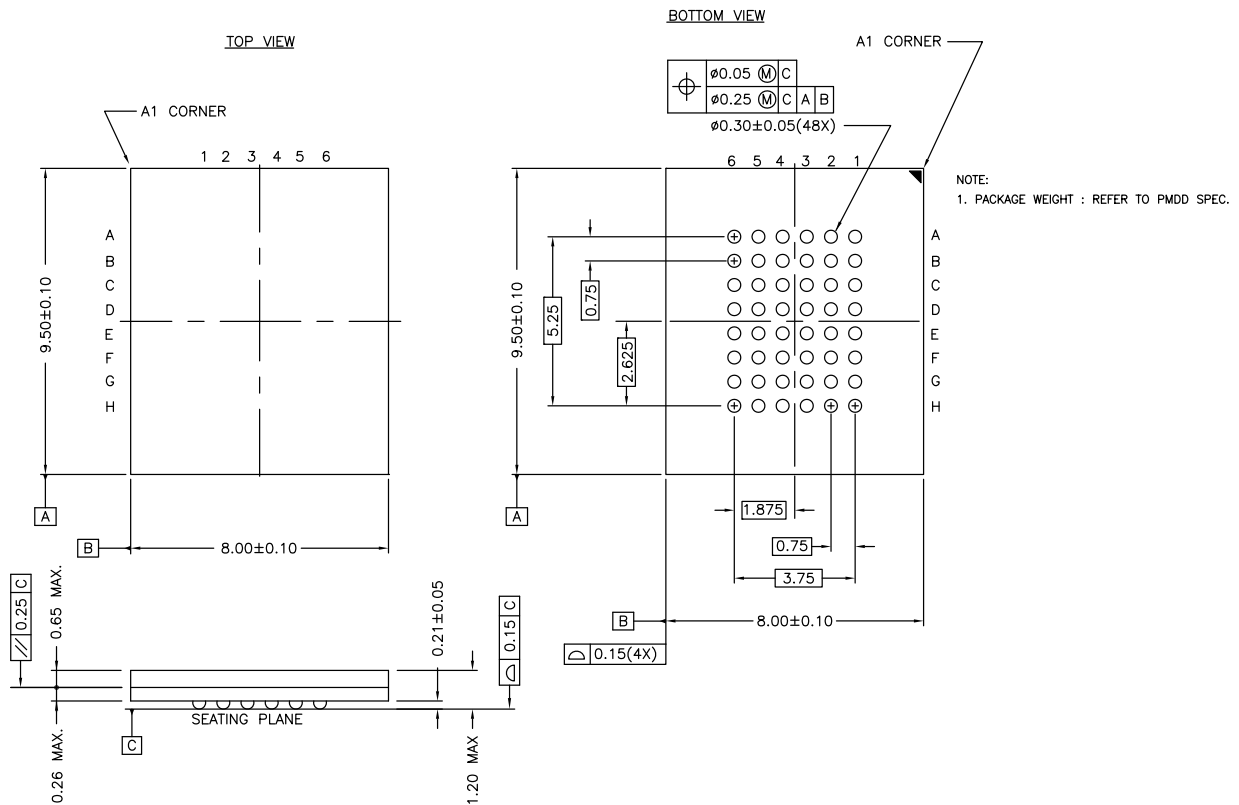
## Ordering Code Definitions

CY 621 7 7 E V30 LL -55 Z,BA X I

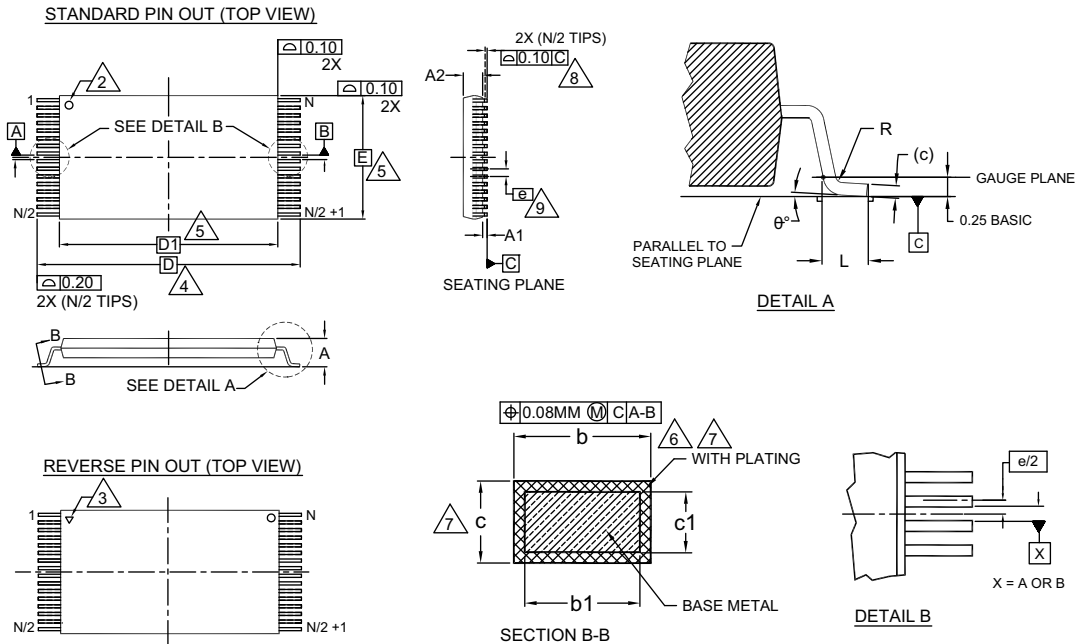


## Package Diagram

**Figure 11. 48-ball FBGA (8 × 9.5 × 1.2 mm) Package Outline, 51-85191**



51-85191 \*C

**Package Diagram (continued)**
**Figure 12. 48-pin TSOP I (12 × 18.4 × 1 mm) Package Outline, 51-85183**


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE  $\overline{C-C}$ . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

## Document History Page

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM Document Number: 001-09880			
Revision	ECN	Submission Date	Description of Change
**	498562	08/31/2006	New data sheet.
*A	2544845	07/29/2008	Added 48-pin TSOP I package related information in all instances across the document. Removed 45 ns speed bin related information in all instances across the document. Added 70 ns speed bin related information in all instances across the document. Updated <a href="#">Electrical Characteristics</a> : Added Note 10 and referred the same note in I <sub>SB2</sub> parameter. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : Added spec 51-85183 *A.
*B	2589750	10/15/2008	Updated <a href="#">Pin Configurations</a> : Updated <a href="#">Figure 1</a> (Changed pin functions of pin 10 from NC to A20 and pin 13 from A20 to DNU).
*C	2668432	03/03/2009	Removed 70 ns speed bin related information in all instances across the document. Added 55 ns speed bin related information in all instances across the document. Replaced 3.6 V with 3.7 V in V <sub>CC</sub> range in all instances across the document. Updated <a href="#">Electrical Characteristics</a> : Changed maximum value of I <sub>CC</sub> parameter from 30 mA to 45 mA corresponding to Test Condition "f = f <sub>(max)</sub> ". Changed maximum value of I <sub>CC</sub> parameter from 2.8 mA to 4.5 mA corresponding to Test Condition "f = 1 MHz". Removed I <sub>SB1</sub> parameter and its details. Changed maximum value of I <sub>SB2</sub> parameter from 17 μA to 25 μA. Referred Note 9 in I <sub>SB2</sub> parameter. Updated Note 10.
*D	2779867	10/06/2009	Changed status from Preliminary to Final. Updated <a href="#">Electrical Characteristics</a> : Added details of V <sub>IL</sub> parameter corresponding to Test Condition "For TSOP I Package". Added Note 8 and referred the same note in maximum value of V <sub>IL</sub> parameter corresponding to Test Condition "For TSOP I Package". Changed typical value of I <sub>CC</sub> parameter from 28 mA to 35 mA corresponding to Test Condition "f = f <sub>(max)</sub> ". Changed typical value of I <sub>CC</sub> parameter from 2.2 mA to 4.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I <sub>CC</sub> parameter from 4.5 mA to 5.5 mA corresponding to Test Condition "f = 1 MHz". Updated <a href="#">Capacitance</a> : Changed maximum value of C <sub>OUT</sub> parameter from 10 pF to 15 pF. Updated <a href="#">Thermal Resistance</a> : Replaced TBD with values in FBGA column. Updated <a href="#">Switching Characteristics</a> : Changed minimum value of t <sub>OHA</sub> parameter from 10 ns to 6 ns. Completing Sunset Review.
*E	2899662	03/26/2010	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : spec 51-85191 – Changed revision from ** to *A. spec 51-85183 – Changed revision from *A to *B.

**Document History Page** *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM Document Number: 001-09880			
Revision	ECN	Submission Date	Description of Change
*F	2927528	05/04/2010	Updated <a href="#">Electrical Characteristics</a> : Updated Note 10. Updated <a href="#">Truth Table</a> : Added Note 32 and referred the same note in respective places. Added <a href="#">Acronyms</a> . Updated to new template.
*G	3177000	02/18/2011	Removed 48-ball FBGA package related information in all instances in the document. Updated <a href="#">Features</a> (Removed 48-ball FBGA package related information). Updated <a href="#">Pin Configurations</a> : Removed 48-ball FBGA package related information. Updated Note 1 (Replaced NC with DNU). Updated <a href="#">Electrical Characteristics</a> (Updated details in “Test Conditions” column of I <sub>SB2</sub> parameter). Updated <a href="#">Thermal Resistance</a> (Removed 48-ball FBGA package related information). Updated <a href="#">Data Retention Characteristics</a> (Updated details in “Conditions” column of I <sub>CCDR</sub> parameter). Updated <a href="#">Ordering Information</a> : No change in part numbers. Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> : Removed spec 51-85191 *A. Updated <a href="#">Acronyms</a> . Added <a href="#">Units of Measure</a> . Updated to new template.
*H	3295175	06/29/2011	Updated <a href="#">Functional Description</a> : Removed Note “For best practice recommendations, refer to the Cypress application note <a href="#">System Design Guidelines</a> .” and its reference. Updated <a href="#">Package Diagram</a> : spec 51-85183 – Changed revision from *B to *C.
*I	3461953	12/22/2011	Included 48-ball FBGA package related information in all instances in the document. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : Added spec 51-85191 *B.
*J	4100342	08/21/2013	Updated <a href="#">Switching Characteristics</a> : Added Note 17 and referred the same note in “Parameter” column. Updated <a href="#">Package Diagram</a> : spec 51-85191 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*K	4111710	09/12/2013	Updated <a href="#">Electrical Characteristics</a> : Updated Note 10. Updated <a href="#">Data Retention Characteristics</a> : Updated Note 13.
*L	4355423	04/29/2014	Updated <a href="#">Electrical Characteristics</a> : Updated Note 10 (Issue is fixed so pin A <sub>20</sub> can be left floating in standby). Updated <a href="#">Switching Characteristics</a> : Added Note <u>21</u> and referred the same note in Write Cycle (for t <sub>PWE</sub> parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW condition). Updated <a href="#">Switching Waveforms</a> : Added Note <u>31</u> and referred the same note in <a href="#">Figure 10</a> (for t <sub>PWE</sub> parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW condition).

**Document History Page** *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM Document Number: 001-09880			
Revision	ECN	Submission Date	Description of Change
*M	4567826	11/12/2014	Updated <a href="#">Features</a> : Included 48-ball FBGA package related information. Updated <a href="#">Functional Description</a> : Added "For a complete list of related resources, <a href="#">click here</a> ." at the end. Updated <a href="#">Maximum Ratings</a> : Referred Notes 4, 5 in "Supply voltage to ground potential". Completing Sunset Review.
*N	5017414	11/17/2015	Updated <a href="#">Thermal Resistance</a> : Replaced "2-layer" with "four-layer" in "Test Conditions" column. Changed value of $\Theta_{JA}$ parameter corresponding to TSOP I package from 44.66 °C/W to 55.91 °C/W. Changed value of $\Theta_{JC}$ parameter corresponding to TSOP I package from 12.12 °C/W to 9.39 °C/W. Updated <a href="#">Package Diagram</a> : spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*O	6073315	02/16/2018	Updated <a href="#">Package Diagram</a> : spec 51-85183 – Changed revision from *D to *F. Updated to new template.
*P	6315809	09/26/2018	Updated <a href="#">Maximum Ratings</a> : Changed value of Latch-up current from "> 200 mA" to "> 140 mA". Updated <a href="#">Operating Range</a> : Replaced "2.2 V to 3.7 V" with "2.2 V to 3.6 V" under " $V_{CC}$ " column. Updated <a href="#">Electrical Characteristics</a> : Changed typical value of $I_{CC}$ parameter from 4.5 mA to 10 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of $I_{CC}$ parameter from 5.5 mA to 12 mA corresponding to Test Condition "f = 1 MHz". Updated <a href="#">Thermal Resistance</a> : Changed value of $\Theta_{JA}$ parameter corresponding to FBGA package from 38.1 °C/W to 54.8 °C/W. Changed value of $\Theta_{JC}$ parameter corresponding to FBGA package from 7.54 °C/W to 11.9 °C/W. Changed value of $\Theta_{JA}$ parameter corresponding to TSOP I package from 55.91 °C/W to 54.42 °C/W. Changed value of $\Theta_{JC}$ parameter corresponding to TSOP I package from 9.39 °C/W to 9.4 °C/W. Updated <a href="#">Data Retention Characteristics</a> : Changed maximum value of $I_{CCDR}$ parameter from 17 $\mu$ A to 20 $\mu$ A. Updated <a href="#">Switching Characteristics</a> : Removed Note "In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note <a href="#">AN66311</a> . However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production." and its reference in "Parameter" column. Changed minimum value of $t_{OHA}$ parameter from 6 ns to 4 ns. Completing Sunset Review.

**Document History Page** *(continued)*

Document Title: CY62177EV30 MoBL, 32-Mbit (2M × 16/4M × 8) Static RAM Document Number: 001-09880			
Revision	ECN	Submission Date	Description of Change
*Q	6692046	10/06/2019	Updated <a href="#">Product Portfolio</a> : Changed maximum value of "Operating I <sub>CC</sub> " under "Power Dissipation" from 12 mA to 18 mA corresponding to "f = 1 MHz". Updated <a href="#">Electrical Characteristics</a> : Changed maximum value of I <sub>CC</sub> parameter from 12 mA to 18 mA corresponding to Test Condition "f = 1 MHz". Updated to new template. Completing Sunset Review.

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