

## Features

- Pin- and function-compatible with CY7C1018CV33 and CY7C1019CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low Active Power
  - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- Available in Pb-free 32-pin 400-Mil wide Molded SOJ, 32-pin TSOP II and 48-ball VFBGA packages

## Functional Description

The CY7C1018DV33/CY7C1019DV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

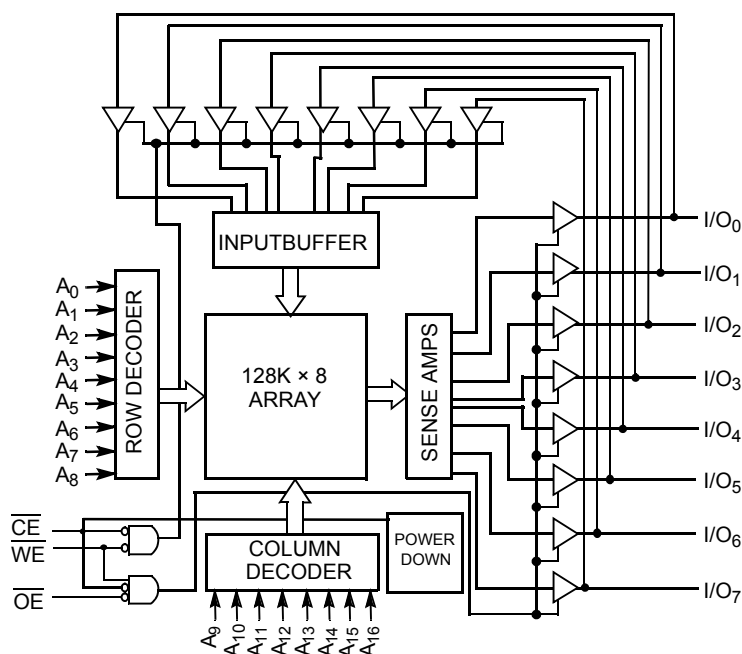
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1018DV33/CY7C1019DV33 are available in Pb-free 32-pin 400-Mil wide Molded SOJ, 32-pin TSOP II and 48-ball VFBGA packages.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



## Contents

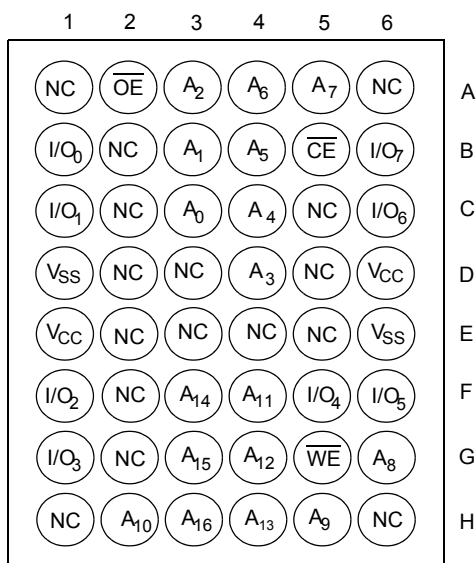
<b>Selection Guide</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>12</b>
<b>Pin Configurations</b> .....	<b>3</b>	Ordering Code Definitions .....	12
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>13</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>17</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>17</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	17
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>18</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>20</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	20
<b>Data Retention Waveform</b> .....	<b>6</b>	Products .....	20
<b>Switching Characteristics</b> .....	<b>7</b>	PSoC® Solutions .....	20
<b>Switching Waveforms</b> .....	<b>8</b>	Cypress Developer Community .....	20
<b>Truth Table</b> .....	<b>11</b>	Technical Support .....	20

## Selection Guide

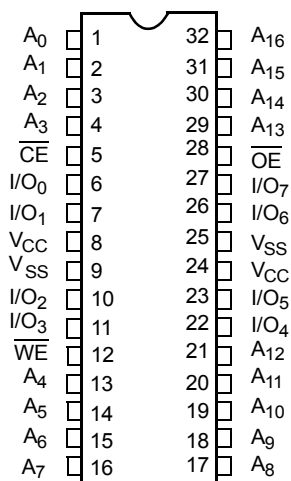
Description	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	60	mA
Maximum Standby Current	3	mA

## Pin Configurations

**Figure 1. 48-ball VFBGA pinout (Top View)** <sup>[1]</sup>



**Figure 2. 32-pin SOJ / TSOP II pinout (Top View)**



### Note

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage on  
 $V_{CC}$  to Relative GND <sup>[2]</sup> ..... -0.3 V to +4.6 V

DC Voltage Applied to Outputs  
in High Z State <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC Input Voltage <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V	10 ns

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial)		Unit
				Min	Max	
V <sub>OH</sub>	Output HIGH voltage	Min V <sub>CC</sub> , I <sub>OH</sub> = −4.0 mA		2.4	–	V
V <sub>OL</sub>	Output LOW voltage	Min V <sub>CC</sub> , I <sub>OL</sub> = 8.0 mA		–	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[2]</sup>			−0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		−1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , output disabled		−1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	–	60	mA
			83 MHz	–	55	mA
			66 MHz	–	45	mA
			40 MHz	–	30	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		–	10	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0		–	3	mA

### Note

2.  $V_{IL(min)}$  = -2.0 V and  $V_{IH(max)}$  =  $V_{CC} + 1$  V for pulse durations of less than 5 ns.

## Capacitance

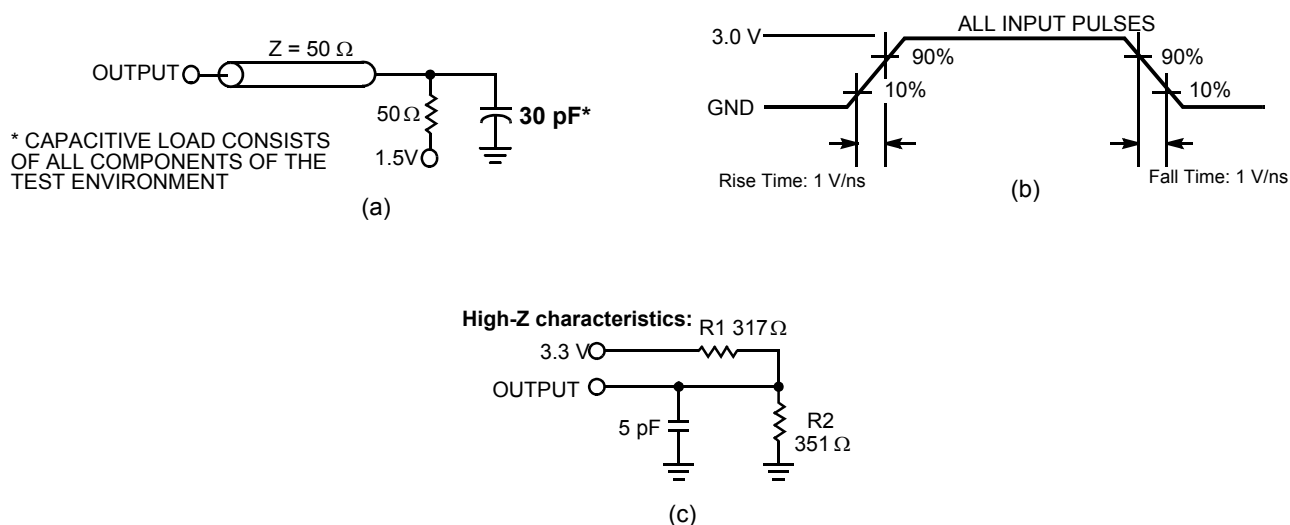
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

## Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	32-pin SOJ	32-pin TSOP II	48-ball VFBGA	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	56.29	62.22	36	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		38.14	21.43	9	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

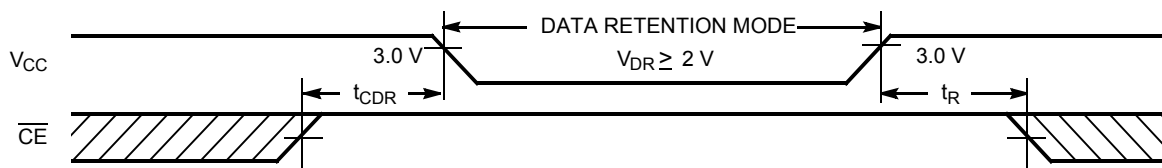
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[5]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[6]}$	Operation recovery time		$t_{RC}$	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

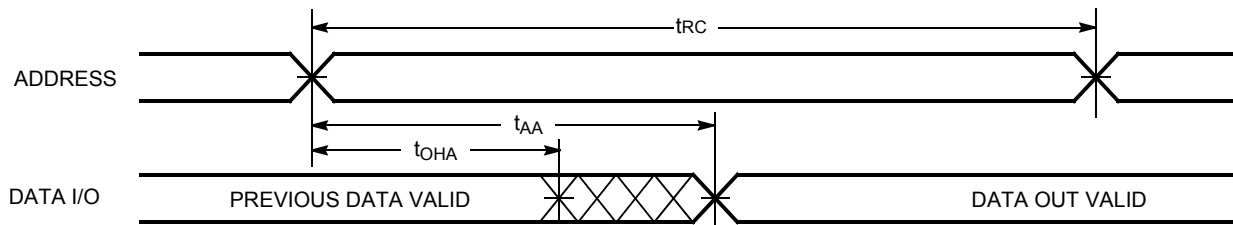
Parameter <sup>[7]</sup>	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub> <sup>[8]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	μs
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub>	Address to data valid	–	10	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[9]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[9, 10]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to low Z <sup>[9]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to high Z <sup>[9, 10]</sup>	–	5	ns
t <sub>PU</sub> <sup>[11]</sup>	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t <sub>PD</sub> <sup>[11]</sup>	$\overline{\text{CE}}$ HIGH to power-down	–	10	ns
Write Cycle <sup>[12, 13]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end	8	–	ns
t <sub>AW</sub>	Address set-up to write end	8	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7	–	ns
t <sub>SD</sub>	Data set-up to write end	5	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to low Z <sup>[9]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to high Z <sup>[9, 10]</sup>	–	5	ns

### Notes

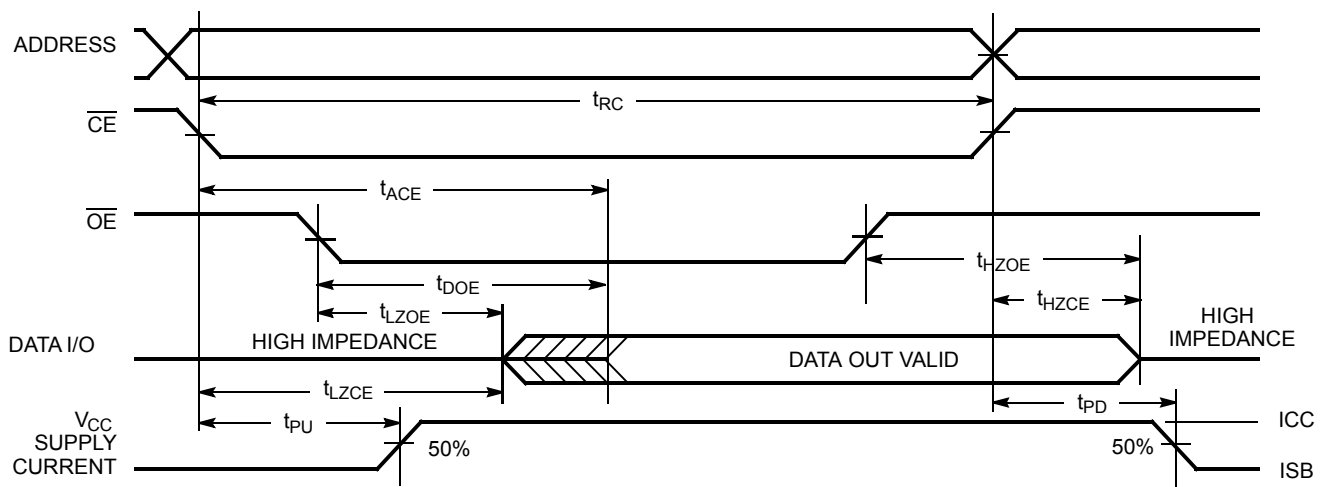
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
8.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
9. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
10.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in [Figure 3 on page 5 \(c\)](#). Transition is measured when the outputs enter a high impedance state.
11. This parameter is guaranteed by design and is not tested.
12. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle no. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1 (Address Transition Controlled)** [14, 15]



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [15, 16]



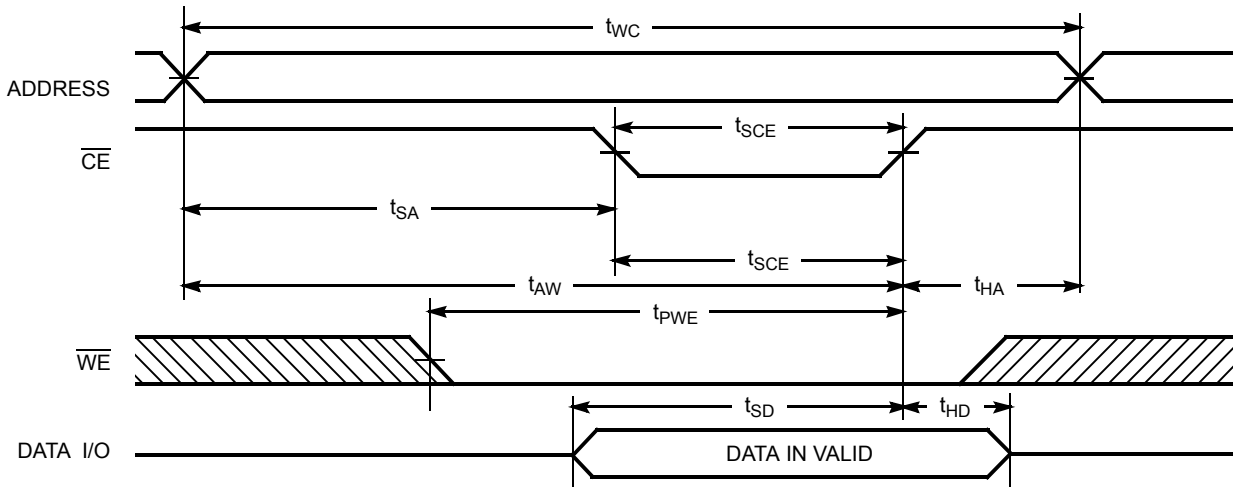
### Notes

- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for Read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

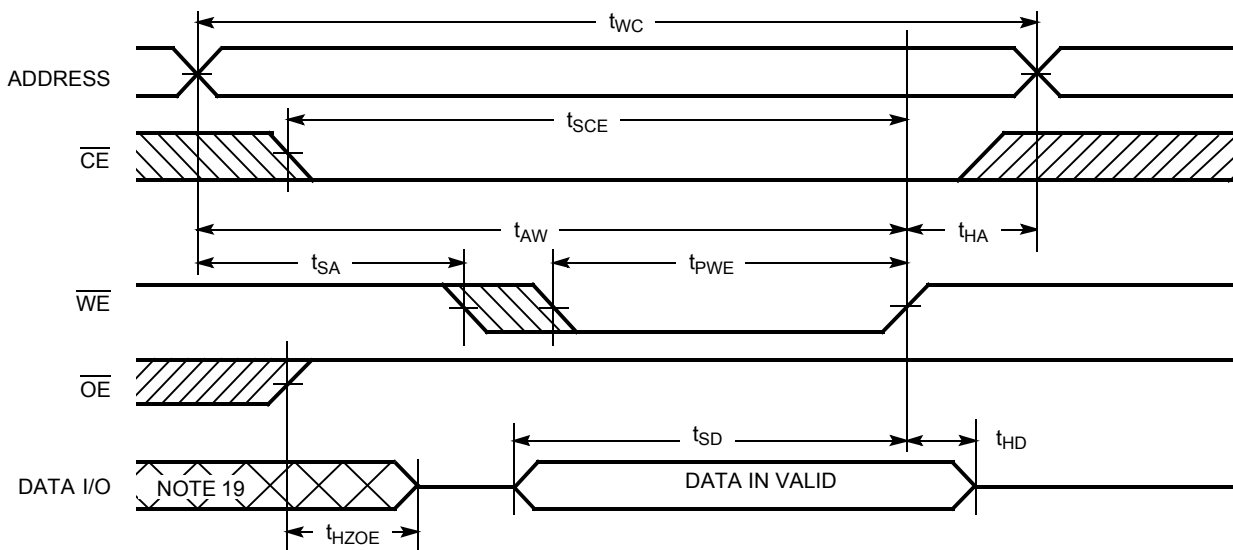


## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [17, 18]



**Figure 8. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)** [17, 18]

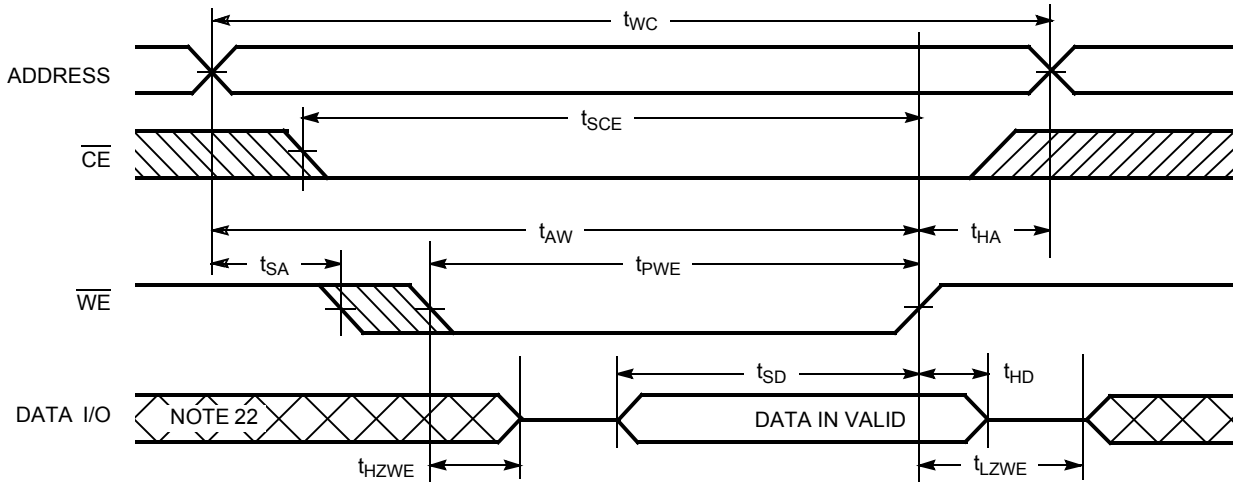


### Notes

17. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
19. During this period the I/Os are in the output state and input signals should not be applied.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [20, 21]**



### Notes

20. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
21. The minimum write cycle time for Write Cycle no. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
22. During this period the I/Os are in the output state and input signals should not be applied.

## Truth Table

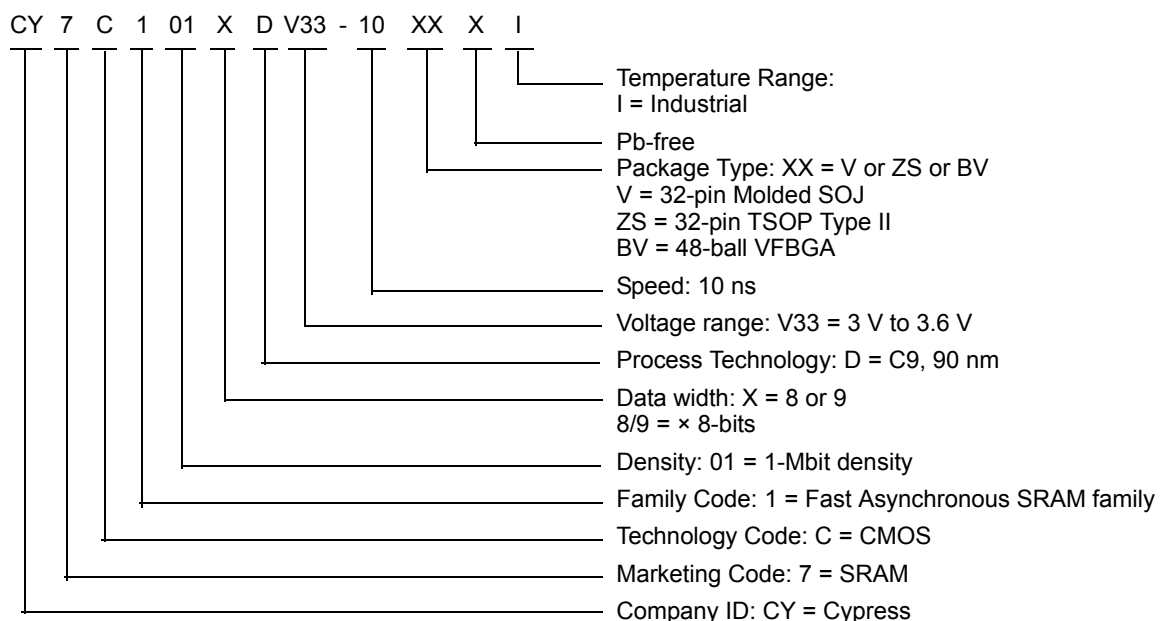
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018DV33-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1019DV33-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1019DV33-10ZSXI	51-85095	32-pin TSOP Type II (Pb-free)	
	CY7C1019DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	

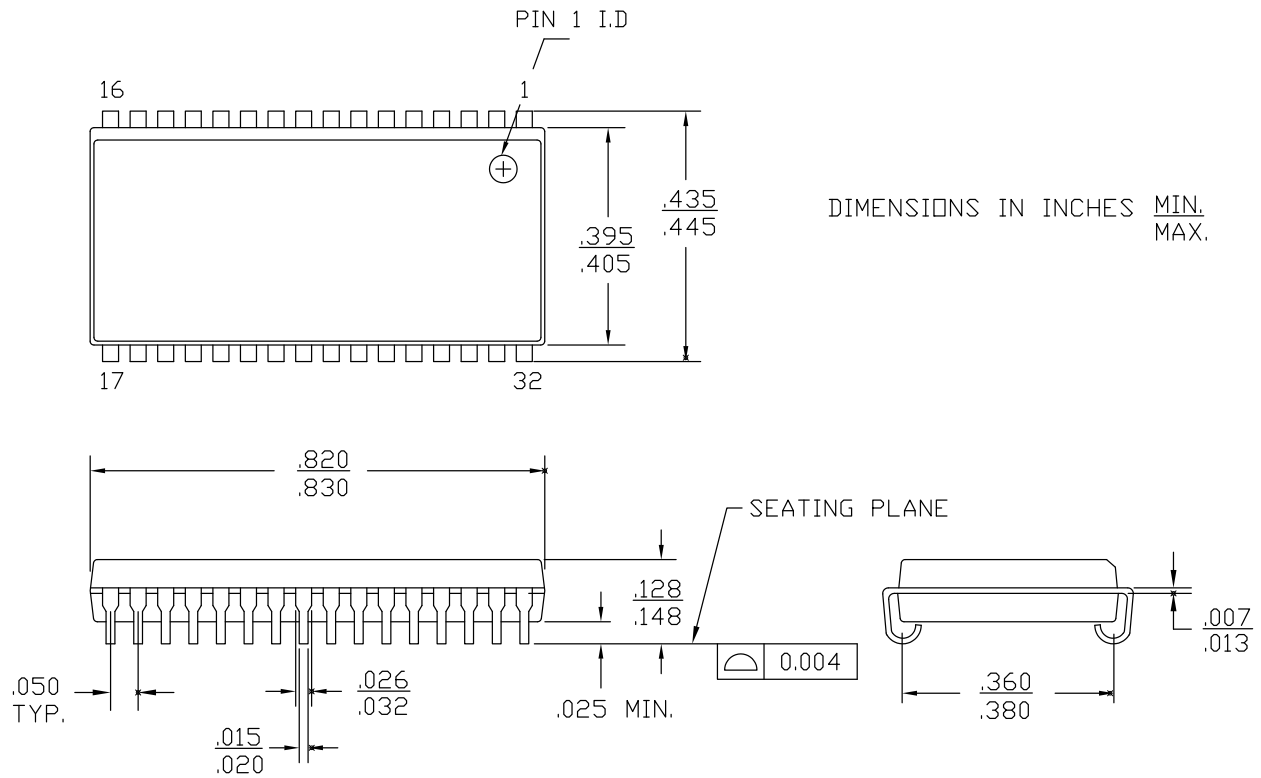
Please contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions



## Package Diagrams

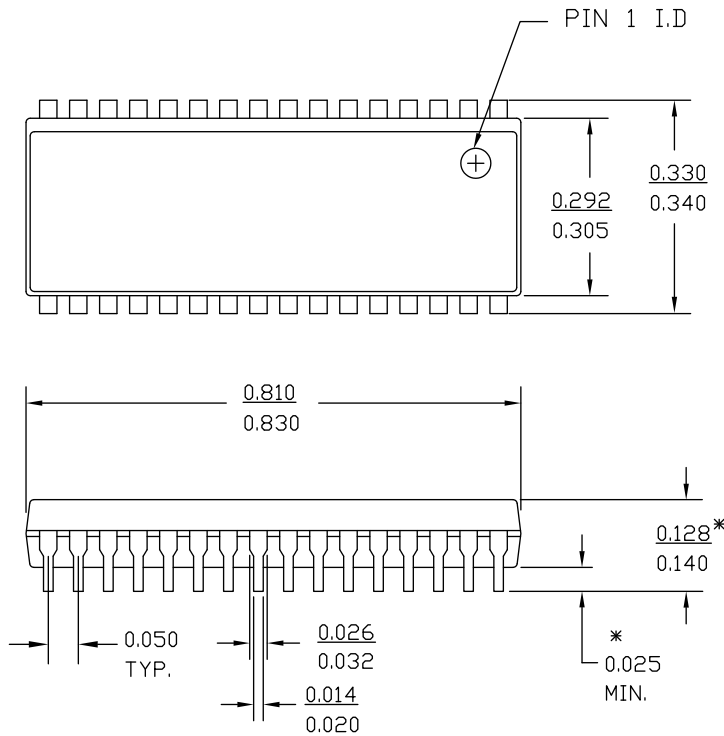
Figure 10. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033



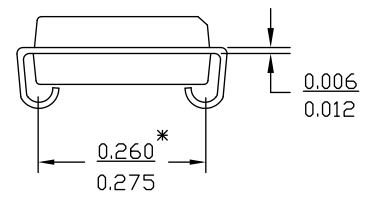
51-85033 \*E

## Package Diagrams (continued)

**Figure 11. 32-pin SOJ (300 Mils) V32.3 (Catalog 32.3 Molded SOJ) Package Outline, 51-85041**



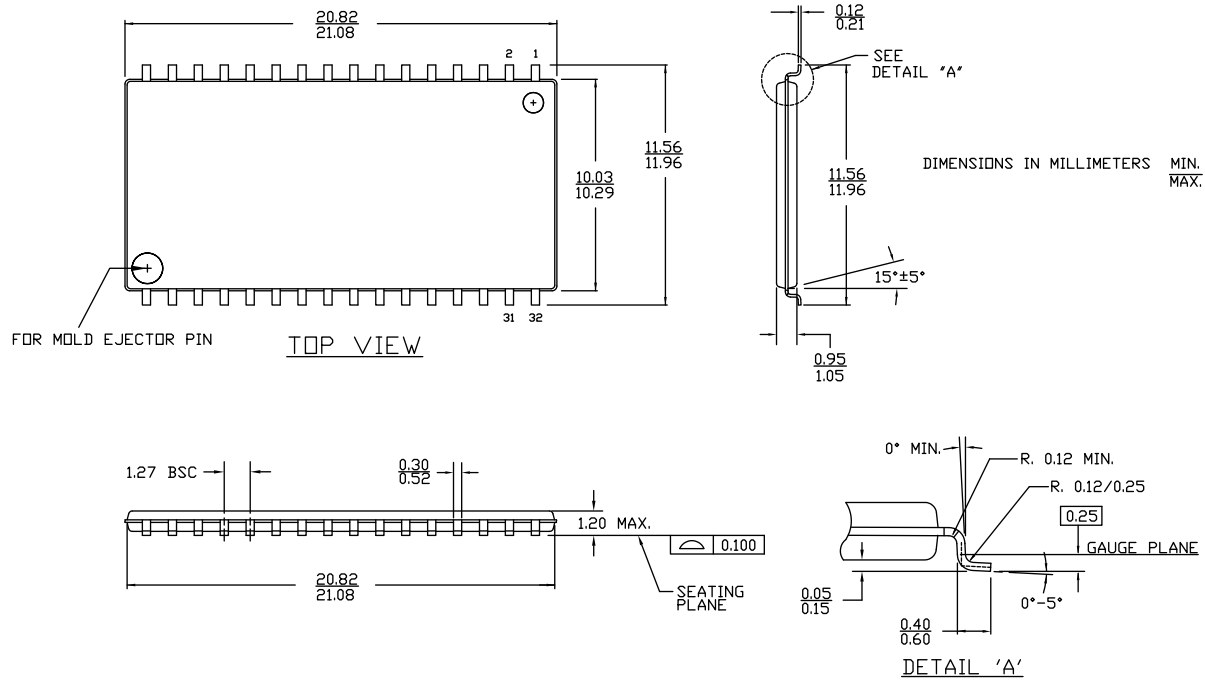
DIMENSIONS IN INCHES MIN. MAX.  
LEAD COPLANARITY 0.004 MAX.



51-85041 \*D

**Package Diagrams** (continued)

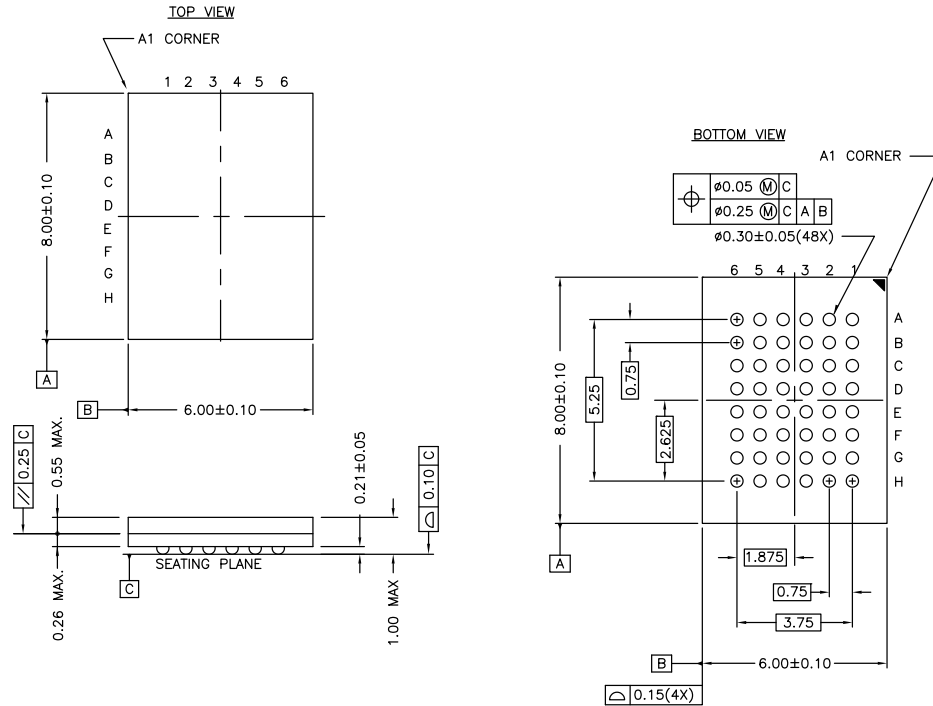
**Figure 12. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095**



51-85095 \*D

## Package Diagrams (continued)

**Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H



## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1018DV33/CY7C1019DV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05481				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233750	See ECN	RKF	Updated <a href="#">Electrical Characteristics</a> : DC parameters modified as per EROS (Spec # 01-02165 Rev *A) Updated <a href="#">Ordering Information</a> : Added Pb-free offering.
*B	262950	See ECN	RKF	Added <a href="#">Data Retention Characteristics</a> . Updated <a href="#">Switching Characteristics</a> : Added T <sub>power</sub> parameter and its details. Updated <a href="#">Ordering Information</a> : Shaded all Pb-free MPNs.
*C	307598	See ECN	RKF	Removed 12 ns speed bin and 15 ns speed bin related information in all instances across the document.
*D	520652	See ECN	VKN	Changed status from Preliminary to Final. Removed Commercial Temperature Range related information in all instances across the document. Removed 8 ns speed bin related information in all instances across the document. Added 48-ball VFBGA package related information in all instances across the document. Updated <a href="#">Electrical Characteristics</a> : Added values of I <sub>CC</sub> parameter (for frequencies 83 MHz, 66 MHz and 40 MHz). Updated Note 2 (Replaced "V <sub>IH(max)</sub> = V <sub>CC</sub> + 2 V" with "V <sub>IH(max)</sub> = V <sub>CC</sub> + 1 V"). Updated <a href="#">Thermal Resistance</a> . Updated <a href="#">Ordering Information</a> . Updated <a href="#">Package Diagrams</a> : Added <a href="#">Figure 13</a> (spec 51-85150).
*E	3110052	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*F	3416342	10/20/2011	TAVA	Updated <a href="#">Functional Description</a> (Removed the Note "For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at <a href="http://www.cypress.com">www.cypress.com</a> link." and its reference in <a href="#">Functional Description</a> ). Updated <a href="#">Electrical Characteristics</a> . Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*G	4324792	03/28/2014	VINI	Added CY7C1018DV33 related information across the document. Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagrams</a> : spec 51-85033 – Changed revision from *D to *E. spec 51-85150 – Changed revision from *G to *H. Updated to new template.
*H	4531367	10/10/2014	NILE	Updated <a href="#">Ordering Information</a> : Replaced "51-85033" with "51-85041" in "Package Diagram" column for CY7C1018DV33-10VXI. Updated <a href="#">Package Diagrams</a> : Added <a href="#">Figure 11</a> (spec 51-85041).

## Document History Page (continued)

Document Title: CY7C1018DV33/CY7C1019DV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05481				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*I	4574311	11/19/2014	NILE	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end. Updated <a href="#">Package Diagrams</a> : spec 51-85041 – Changed revision from *C to *D.
*J	4777177	05/26/2015	NILE	Updated <a href="#">Package Diagrams</a> : spec 51-85095 – Changed revision from *B to *D. Updated to new template.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="#">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="#">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="#">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="#">cypress.com/go/powerpsoc</a>
<a href="#">Memory</a>	<a href="#">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="#">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="#">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="#">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="#">cypress.com/go/wireless</a>

#### PSoC® Solutions

[psoc.cypress.com/solutions](#)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2004-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor:

[CY7C1018DV33-10VXI](#) [CY7C1019DV33-10BVXI](#) [CY7C1019DV33-10VXI](#) [CY7C1019DV33-10ZSXI](#)