

### Features

- High speed: 45 ns
- Temperature ranges
   □ Industrial: -40 °C to +85 °C
   □ Automotive: -40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62126DV30
- Ultra low standby power
   Typical standby current: 1 μA
   Maximum standby current: 4 μA
- Ultra low active power
   Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with CE and OE features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II packages

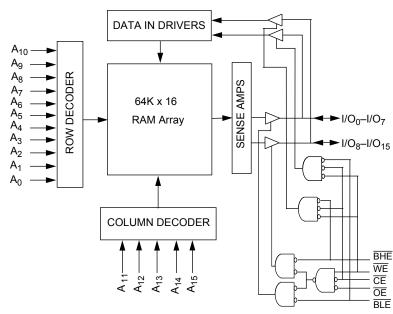
### **Functional Description**

The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life<sup>TM</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}$  HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ , BLE HIGH) or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

To write to the device, take Chip Enable  $\overline{(CE)}$  and Write Enable  $\overline{(WE)}$  inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

To read from the device, take Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the Truth Table on page 11 for a complete description of read and write modes.

### Logic Block Diagram



**Cypress Semiconductor Corporation** Document Number: 38-05486 Rev. \*I 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised May 31, 2011



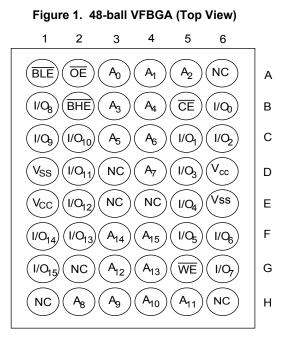
## Contents

| Pin Configuration                                  | 3 |
|--|---|
| Product Portfolio                                  |   |
| Maximum Ratings                                    | 4 |
| Operating Range                                    | 4 |
| Electrical Characteristics                         | 4 |
| Capacitance  | 5 |
| Thermal Resistance                                 | 5 |
| Data Retention Characteristics                     | 6 |
| Switching Characteristics                          |   |
| Switching Waveforms                                | 8 |
| Read Cycle No. 1 (Address transition controlled) . | 8 |
| Read Cycle No. 2 (OE controlled)                   | 8 |
| Write Cycle No. 1 (WE controlled)                  | 9 |
| Write Cycle No. 2 (CE controlled)                  | 9 |
| Write Cycle No. 3 (WE controlled, OE LOW           |   |

| Write Cycle No. 4                       |    |
|---|----|
| (BHE/BLE controlled, OE LOW)            | 10 |
| Truth Table                             |    |
| Ordering Information                    | 12 |
| Ordering Code Definitions               | 12 |
| Package Diagrams                        | 13 |
| Acronyms                                | 15 |
| Document Conventions                    | 15 |
| Units of Measure                        | 15 |
| Document History Page                   | 16 |
| Sales, Solutions, and Legal Information | 18 |
| Worldwide Sales and Design Support      | 18 |
| Products                                | 18 |
| PSoC Solutions                          | 18 |



## **Pin Configuration**



| Figure 2. | 44-pin TSOP | II ( | (Тор | View | <b>)</b> [1] |
|-----------|-------------|------|------|------|--------------|
|           |             |      |      |      |              |

| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | $\begin{array}{c} A_4 & \square \\ A_3 & \square \\ A_2 & \square \\ A_2 & \square \\ 3 \\ A_1 & \square \\ 4 \\ A_0 & \square \\ 5 \\ \hline CE & \square \\ 6 \\  /O_0 \square \\ 7 \\  /O_1 \square \\ 8 \\  /O_2 \square \\ 9 \\  /O_3 \square \\ 10 \\ V_{CC} \square \\ 11 \\ V_{SS} \square \\ 12 \\  /O_4 \square \\ 13 \\  /O_5 \square \\ 14 \\  /O_6 \square \\ 15 \end{array}$ | $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ |
|---|--|---|
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $  |  |   |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   |  |   |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   |  |   |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   |  |   |
| $ \begin{array}{cccccccccccccccccccccccccccccccccccc$   |  | 34 🖂 V <sub>SS</sub>                                  |
|   |  | 33 🗋 V <sub>CC</sub>                                  |
|   | I/O <sub>4</sub> ∐13   | 32 ∐ I/O <sub>11</sub>                                |
|   | I/O <sub>5</sub> 14  | 31 □ I/O <sub>10</sub>                                |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  |  |   |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | I/O <sub>7</sub> ☐ 16  | 29 🏼 I/O <sub>8</sub>                                 |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  |  | 28 🗆 NC   |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$  | A <sub>15</sub> ∐ 18   | 27 🗋 A <sub>8</sub>                                   |
| $\begin{array}{c c} A_{13} \square 20 & 25 \square A_{10} \\ A_{12} \square 21 & 24 \square A_{11} \end{array}$ | A <sub>14</sub> ∐19  | 26 🛛 A <sub>9</sub>                                   |
| $A_{12} \square 21$ 24 $\square A_{11}$   | A <sub>13</sub> ∐20  | 25 🛛 A <sub>10</sub>                                  |
|   |  |   |
|   |  |   |

### **Product Portfolio**

| Broduct       | Product Range V <sub>CC</sub> Range (V) |     | Speed                     |     | Operating | , I <sub>CC</sub> (mA)    | )   | Standby L. (A             |     |                           |     |                                  |  |
|---------------|---|-----|---------------------------|-----|-----------|---------------------------|-----|---------------------------|-----|---------------------------|-----|----------------------------------|--|
| Floudet       | Kaliye                                  |     |                           | ,   |           | (ns)                      |     | f = 1 MHz                 |     | f = f <sub>max</sub>      |     | – Standby, I <sub>SB2</sub> (μΑ) |  |
|               |   | Min | <b>Typ</b> <sup>[2]</sup> | Max |           | <b>Typ</b> <sup>[2]</sup> | Мах | <b>Typ</b> <sup>[2]</sup> | Мах | <b>Typ</b> <sup>[2]</sup> | Max |                                  |  |
| CY62126EV30LL | Industrial                              | 2.2 | 3.0                       | 3.6 | 45        | 1.3                       | 2   | 11                        | 16  | 1                         | 4   |                                  |  |
| CY62126EV30LL | Automotive                              | 2.2 | 3.0                       | 3.6 | 55        | 1.3                       | 4   | 11                        | 35  | 1                         | 30  |                                  |  |

1. NC pins are not connected on the die. 2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.



### **Maximum Ratings**

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

| Storage temperature65 °C to +150 °C  |
|--|
| Ambient temperature with power applied55 °C to +125 °C   |
| Supply voltage to ground potential0.3 V to 3.6 V (V <sub>CCmax</sub> + 0.3 V)                                  |
| DC voltage applied to outputs<br>in High Z state <sup>[3, 4]</sup> 0.3 V to 3.6 V (V <sub>CCmax</sub> + 0.3 V) |

| DC input voltage <sup>[3, 4]</sup> –0.3 V to 3.6 V ( $V_{CC}$ | <sub>Cmax</sub> + 0.3 V) |
|---|--------------------------|
| Output current into outputs (LOW)                             | 20 mA                    |
| Static discharge voltage<br>(MIL-STD-883, Method 3015)        | > 2001 V                 |
| Latch up current  | > 200 mA                 |

### **Operating Range**

| Device        | Range      | Ambient<br>Temperature | <b>V<sub>CC</sub></b> <sup>[5]</sup> |
|---------------|------------|------------------------|--------------------------------------|
| CY62126EV30LL | Industrial | –40 °C to +85 °C       | 2.2 V to 3.6 V                       |
|               | Automotive | –40 °C to +125 °C      |                                      |

## **Electrical Characteristics**

Over the Operating Range

| Devenueter                      | Description  | Test Canditions  |            | 45 ns (Industrial) |                    |                       | 55 ns (Automotive) |                    |                       | Unit |
|---------------------------------|--|--|------------|--------------------|--------------------|-----------------------|--------------------|--------------------|-----------------------|------|
| Parameter                       | Description  | Test Conditions  |            |                    | Typ <sup>[6]</sup> | Max                   | Min                | Typ <sup>[6]</sup> | Max                   | Unit |
| V <sub>OH</sub>                 | Output high voltage                                | I <sub>OH</sub> = -0.1 mA  |            | 2.0                | -                  | _                     | 2.0                | -                  | _                     | V    |
|                                 |  | $I_{OH} = -1.0 \text{ mA}, V_{CC} \ge 2.70 \text{ mA}$   | V          | 2.4                | -                  | _                     | 2.4                | -                  | _                     | V    |
| V <sub>OL</sub>                 | Output low voltage                                 | I <sub>OL</sub> = 0.1 mA   |            | -                  | -                  | 0.4                   | _                  |                    | 0.4                   | V    |
|                                 |  | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70 V   |            | -                  | -                  | 0.4                   | -                  | -                  | 0.4                   | V    |
| V <sub>IH</sub>                 | Input high voltage                                 | V <sub>CC</sub> = 2.2 V to 2.7 V   |            | 1.8                | -                  | V <sub>CC</sub> + 0.3 | 1.8                | -                  | V <sub>CC</sub> + 0.3 | V    |
|                                 |  | V <sub>CC</sub> = 2.7 V to 3.6 V   |            | 2.2                | -                  | V <sub>CC</sub> + 0.3 | 2.2                | -                  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>                 | Input low voltage                                  | V <sub>CC</sub> = 2.2 V to 2.7 V   |            | -0.3               | -                  | 0.6                   | -0.3               | -                  | 0.6                   | V    |
|                                 |  | V <sub>CC</sub> = 2.7 V to 3.6 V   |            | -0.3               | -                  | 0.8                   | -0.3               | -                  | 0.8                   | V    |
| I <sub>IX</sub>                 | Input leakage current                              | $GND \le V_I \le V_{CC}$   |            | -1                 | -                  | +1                    | -4                 | -                  | +4                    | μA   |
| I <sub>OZ</sub>                 | Output leakage current                             | $GND \le V_O \le V_{CC}$ , Output Disabled   |            | –1                 | -                  | +1                    | -4                 | -                  | +4                    | μA   |
| I <sub>CC</sub>                 | V <sub>CC</sub> operating supply                   | $f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC}$   | Cmax       | -                  | 11                 | 16                    | -                  | 11                 | 35                    | mA   |
|                                 | current  | f = 1 MHz I <sub>OUT</sub> = 0 m<br>CMOS lev   | nA<br>vels | -                  | 1.3                | 2.0                   | -                  | 1.3                | 4.0                   |      |
| I <sub>SB1</sub> <sup>[7]</sup> | Automatic CE power<br>down current —CMOS<br>inputs | $\label{eq:constraint} \begin{split} \overline{CE} &\geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} &\geq V_{CC} - 0.2 \text{ V}, \text{ V}_{IN} \leq 0.2 \\ \text{f} &= \text{f}_{\text{max}} (\text{Address and Data } 0 \\ \text{f} &= 0 \; (\overline{OE}, \; \overline{\text{BHE}}, \; \overline{\text{BLE}} \; \text{and } \overline{\text{W}} \\ V_{CC} &= 3.60 \text{ V} \end{split}$ | Only),     | -                  | 1                  | 4                     | -                  | 1                  | 35                    | μA   |
| I <sub>SB2</sub> <sup>[7]</sup> | Automatic CE power<br>down current —CMOS<br>inputs | $\label{eq:constraint} \begin{split} \overline{CE} &\geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} &\geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0 \\ f &= 0, \ V_{CC} = 3.60 \text{ V} \end{split}$  | 0.2 V,     | -                  | 1                  | 4                     | _                  | 1                  | 30                    | μA   |

### Notes

- Notes
  3. V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
  4. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
  5. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>cc</sub>(min) and 200 μs wait time after V<sub>cc</sub> stabilization.
  6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
  7. Chip enable (CE) needs to be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.



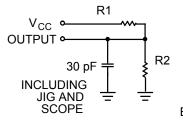
## Capacitance

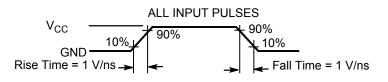
| Parameter <sup>[8]</sup> | Description        | Test Conditions  | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C <sub>IN</sub>          | Input capacitance  | $T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$ | 10  | pF   |
| C <sub>OUT</sub>         | Output capacitance |  | 10  | pF   |

### Thermal Resistance

| Parameter [8]   | Description                              | Test Conditions  | 48-ball VFBGA<br>Package | 44-pin TSOP II<br>Package | Unit |
|-----------------|--|--|--------------------------|---------------------------|------|
| $\Theta_{JA}$   |  | Still Air, soldered on a 4.25 × 1.125 inch,<br>two-layer printed circuit board | 58.85                    | 28.2                      | °C/W |
| Θ <sup>JC</sup> | Thermal resistance<br>(Junction to case) |  | 17.01                    | 3.4                       | °C/W |

Figure 3. AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

R<sub>TH</sub> OUTPUT • V<sub>TH</sub>

| Parameters      | 2.2 V–2.7 V | 2.7 V–3.6 V | Unit |
|-----------------|-------------|-------------|------|
| R1              | 16600       | 1103        | Ω    |
| R2              | 15400       | 1554        | Ω    |
| R <sub>TH</sub> | 8000        | 645         | Ω    |
| V <sub>TH</sub> | 1.2         | 1.75        | V    |

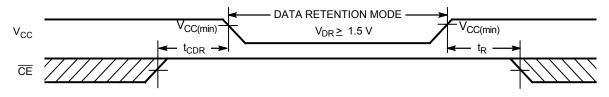


## **Data Retention Characteristics**

### Over the Operating Range

| Parameter                         | Description                          | Conditions   |                  |     | <b>Typ</b> <sup>[9]</sup> | Мах | Unit |
|-----------------------------------|--------------------------------------|--|------------------|-----|---------------------------|-----|------|
| V <sub>DR</sub>                   | V <sub>CC</sub> for data retention   |  |                  | 1.5 | -                         | -   | V    |
| I <sub>CCDR</sub> <sup>[10]</sup> | Data retention current               | $V_{CC} = V_{DR}, \overline{CE} \ge V_{CC} - 0.2 V,$<br>$V_{IN} \ge V_{CC} - 0.2 V \text{ or } V_{IN} \le 0.2 V$ | Industrial       | -   | -                         | 3   | μΑ   |
|                                   |                                      | $V_{\text{IN}} \ge V_{\text{CC}} - 0.2 \text{ V or } V_{\text{IN}} \le 0.2 \text{ V}$                            | Automotive       | _   | -                         | 30  | μΑ   |
| t <sub>CDR</sub> <sup>[11]</sup>  | Chip deselect to data retention time |  |                  | 0   | _                         | _   | ns   |
| t <sub>R</sub> <sup>[12]</sup>    | Operation recovery time              |  | CY62126EV30LL-45 | 45  | -                         | -   | ns   |
|                                   |                                      |  | CY62126EV30LL-55 | 55  | -                         | _   |      |

### Figure 4. Data Retention Waveform



### Notes

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C. 10. Chip enable ( $\overline{CE}$ ) needs to be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters. 12. Full device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} > 100 \ \mu$ s.



### **Switching Characteristics**

Over the Operating Range

| Parameter [13, 14]          | Description                           | 45 ns (li | ndustrial) | 55 ns (Automotive) |     | Unit |
|-----------------------------|---------------------------------------|-----------|------------|--------------------|-----|------|
| Parameter [10, 11]          | Description                           | Min       | Max        | Min                | Max |      |
| Read Cycle                  |                                       |           |            |                    |     |      |
| t <sub>RC</sub>             | Read cycle time                       | 45        | -          | 55                 | -   | ns   |
| t <sub>AA</sub>             | Address to data valid                 | -         | 45         | _                  | 55  | ns   |
| t <sub>OHA</sub>            | Data hold from address change         | 10        | -          | 10                 | _   | ns   |
| t <sub>ACE</sub>            | CE LOW to data valid                  | -         | 45         | _                  | 55  | ns   |
| t <sub>DOE</sub>            | OE LOW to data valid                  | -         | 22         | _                  | 25  | ns   |
| t <sub>LZOE</sub>           | OE LOW to Low Z <sup>[15]</sup>       | 5         | -          | 5                  | -   | ns   |
| t <sub>HZOE</sub>           | OE HIGH to High Z <sup>[15, 16]</sup> | -         | 18         | _                  | 20  | ns   |
| t <sub>LZCE</sub>           | CE LOW to Low Z <sup>[15]</sup>       | 10        | -          | 10                 | _   | ns   |
| t <sub>HZCE</sub>           | CE HIGH to High Z <sup>[15, 16]</sup> | -         | 18         | _                  | 20  | ns   |
| t <sub>PU</sub>             | CE LOW to power up                    | 0         | -          | 0                  | _   | ns   |
| t <sub>PD</sub>             | CE HIGH to power down                 | -         | 45         | _                  | 55  | ns   |
| t <sub>DBE</sub>            | BHE / BLE LOW to data valid           | -         | 22         | _                  | 25  | ns   |
| t <sub>LZBE</sub>           | BHE / BLE LOW to Low Z [15]           | 5         | -          | 5                  | -   | ns   |
| t <sub>HZBE</sub>           | BHE / BLE HIGH to High Z [15, 16]     | -         | 18         | _                  | 20  | ns   |
| Write Cycle <sup>[17]</sup> |                                       |           |            |                    |     |      |
| t <sub>WC</sub>             | Write cycle time                      | 45        | -          | 55                 | -   | ns   |
| t <sub>SCE</sub>            | CE LOW to write end                   | 35        | -          | 40                 | _   | ns   |
| t <sub>AW</sub>             | Address setup to write end            | 35        | -          | 40                 | _   | ns   |
| t <sub>HA</sub>             | Address hold from write end           | 0         | -          | 0                  | _   | ns   |
| t <sub>SA</sub>             | Address setup to write start          | 0         | -          | 0                  | _   | ns   |
| t <sub>PWE</sub>            | WE pulse width                        | 35        | -          | 40                 | _   | ns   |
| t <sub>BW</sub>             | BHE / BLE pulse width                 | 35        | -          | 40                 | _   | ns   |
| t <sub>SD</sub>             | Data setup to write end               | 25        | -          | 25                 | -   | ns   |
| t <sub>HD</sub>             | Data hold from write end              | 0         | -          | 0                  | -   | ns   |
| t <sub>HZWE</sub>           | WE LOW to High Z <sup>[15, 16]</sup>  | _         | 18         | _                  | 20  | ns   |
| t <sub>LZWE</sub>           | WE HIGH to Low Z <sup>[15]</sup>      | 10        | _          | 10                 | _   | ns   |

Notes

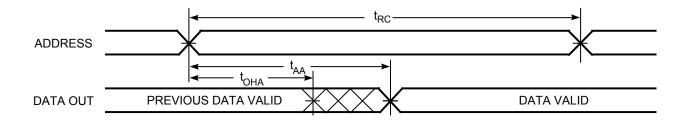
- 13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance. 14. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.

15. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZDE</sub>, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZE</sub> is less than t<sub>LZCE</sub>.
16. t<sub>HZCE</sub>, t<sub>HZCE</sub>, t<sub>HZE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE, BLE or both = V<sub>IL</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.

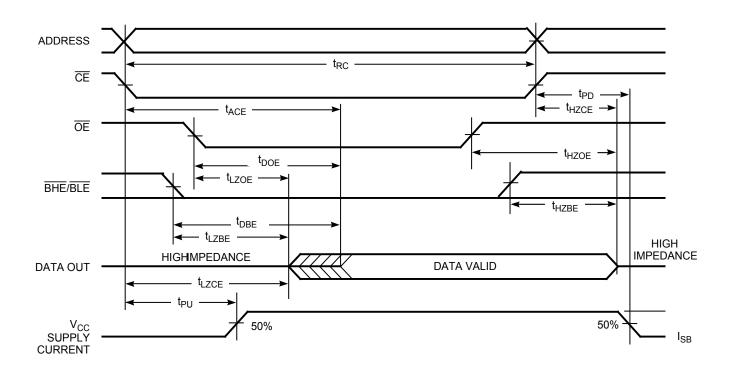


### **Switching Waveforms**

Read Cycle No. 1 (Address transition controlled) <sup>[18, 19]</sup>



### Read Cycle No. 2 (OE controlled) <sup>[19, 20]</sup>



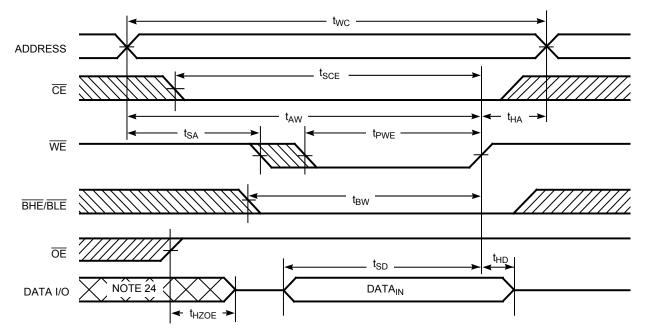
### Notes

18. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ . 19.  $\overline{WE}$  is high for read cycle. 20. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

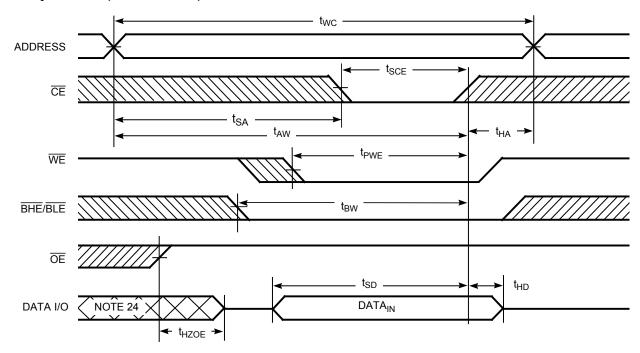


## Switching Waveforms (continued)





Write Cycle No. 2 (CE controlled) <sup>[21, 22, 23]</sup>

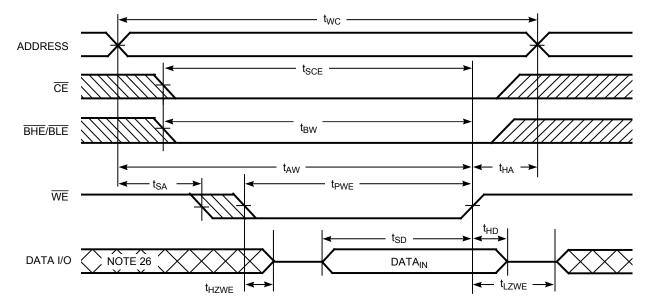


- Notes
  21. The internal write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE, BLE or both = V<sub>IL</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
  22. Data I/O is high impedance if OE = V<sub>IH</sub>.
  23. If CE goes high simultaneously with WE = V<sub>IH</sub>, the output remains in a high impedance state.
  24. During this period, the I/Os are in output state. Do not apply input signals.

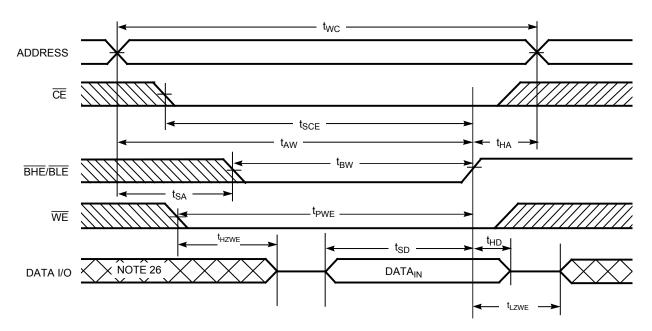


### Switching Waveforms (continued)





## Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$ controlled, $\overline{\text{OE}}$ LOW) [25]



Notes

25. If  $\overline{CE}$  goes high simultaneously with  $\overline{WE} = V_{H}$ , the output remains in a high impedance state. 26. During this period, the I/Os are in output state. Do not apply input signals.





### **Truth Table**

| <b>CE</b> <sup>[27]</sup> | WE | OE | BHE | BLE | Inputs/Outputs   | Mode                | Power                      |
|---------------------------|----|----|-----|-----|--|---------------------|----------------------------|
| Н                         | Х  | X  | Х   | Х   | High Z   | Deselect/power down | Standby (I <sub>SB</sub> ) |
| L                         | Х  | X  | Н   | Н   | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                         | н  | L  | L   | L   | Data out (I/O <sub>0</sub> –I/O <sub>15</sub> )  | Read                | Active (I <sub>CC</sub> )  |
| L                         | Н  | L  | Н   | L   | Data out (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High Z | Read                | Active (I <sub>CC</sub> )  |
| L                         | Н  | L  | L   | Н   | Data out (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High Z | Read                | Active (I <sub>CC</sub> )  |
| L                         | н  | Н  | L   | L   | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                         | н  | Н  | н   | L   | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                         | н  | Н  | L   | Н   | High Z   | Output disabled     | Active (I <sub>CC</sub> )  |
| L                         | L  | X  | L   | L   | Data in (I/O <sub>0</sub> –I/O <sub>15</sub> )   | Write               | Active (I <sub>CC</sub> )  |
| L                         | L  | Х  | Н   | L   | Data in (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High Z  | Write               | Active (I <sub>CC</sub> )  |
| L                         | L  | Х  | L   | Н   | Data in (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High Z  | Write               | Active (I <sub>CC</sub> )  |

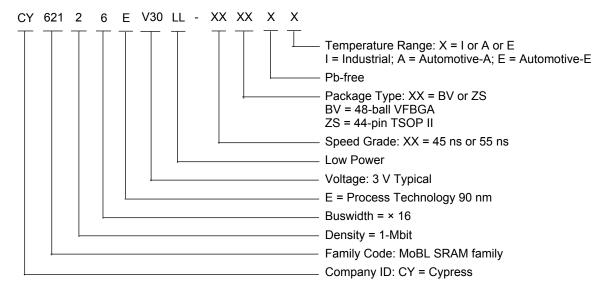


## **Ordering Information**

| Speed<br>(ns) | Ordering Code        | Package<br>Diagram | Package Type             | Operating<br>Range |
|---------------|----------------------|--------------------|--------------------------|--------------------|
| 45            | CY62126EV30LL-45BVXI | 51-85150           | 48-ball VFBGA (Pb-free)  | Industrial         |
|               | CY62126EV30LL-45ZSXI | 51-85087           | 44-pin TSOP II (Pb-free) | Industrial         |
|               | CY62126EV30LL-45ZSXA | 51-85087           | 44-pin TSOP II (Pb-free) | Automotive-A       |
| 55            | CY62126EV30LL-55BVXE | 51-85150           | 48-ball VFBGA (Pb-free)  | Automotive-E       |
|               | CY62126EV30LL-55ZSXE | 51-85087           | 44-pin TSOP II (Pb-free) | Automotive-E       |

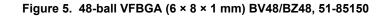
Contact your local Cypress sales representative for availability of other parts.

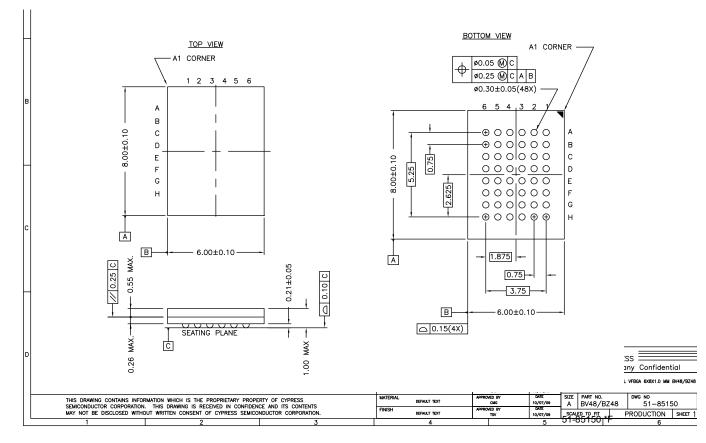
### **Ordering Code Definitions**





### **Package Diagrams**







### Package Diagrams (continued)

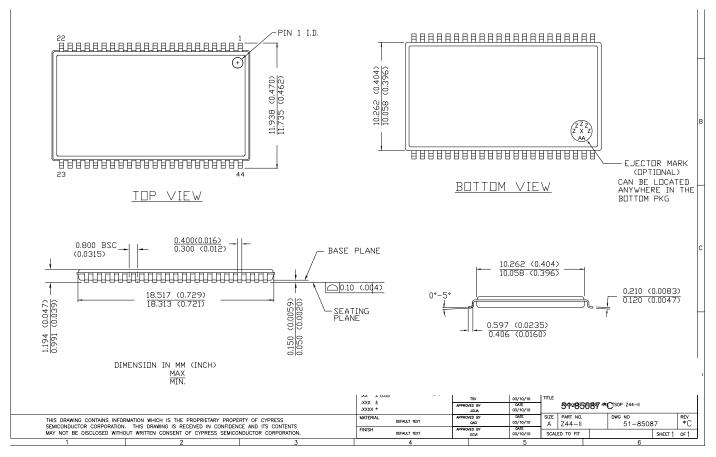


Figure 6. 44-pin TSOP Z44-II, 51-85087





### Acronyms

| Acronym | Description                             |
|---------|---|
| CE      | chip enable                             |
| CMOS    | complementary metal oxide semiconductor |
| I/O     | input/output                            |
| ŌĒ      | output enable                           |
| RAM     | random access memory                    |
| SRAM    | static random access memory             |
| TSOP    | thin small outline package              |
| VFBGA   | very fine-pitch ball grid array         |
| WE      | write enable                            |

### **Document Conventions**

### **Units of Measure**

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celcius  |
| MHz    | Mega Hertz      |
| μA     | micro Amperes   |
| μs     | micro seconds   |
| mA     | milli Amperes   |
| mm     | milli meter     |
| ns     | nano seconds    |
| Ω      | ohms            |
| %      | percent         |
| pF     | pico Farad      |
| V      | Volts           |
| W      | Watts           |



## **Document History Page**

| Rev. | ECN No. | Submission<br>Date | Orig. of<br>Change | Description of Change   |
|------|---------|--------------------|--------------------|---|
| **   | 202760  | See ECN            | AJU                | New data sheet  |
| *A   | 300835  | See ECN            | SYT                | Converted from Advance Information to Preliminary<br>Specified Typical standby power in the Features Section<br>Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package<br>and removed the footnote associated with it on page #2<br>Changed t <sub>OHA</sub> from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively<br>Changed t <sub>DOE</sub> , t <sub>SD</sub> from 15 to 18 ns for 35-ns speed bin<br>Changed t <sub>HZOE</sub> , t <sub>HZBE</sub> , t <sub>HZWE</sub> from 12 and 15 ns to 15 and 18 ns for the 35- and<br>45-ns speed bins, respectively<br>Changed t <sub>HZCE</sub> from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed<br>bins, respectively<br>Changed t <sub>SCE</sub> ,t <sub>BW</sub> from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed<br>bins, respectively<br>Changed t <sub>SCE</sub> ,t <sub>BW</sub> from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bins respectively<br>Changed t <sub>DBE</sub> from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins<br>respectively<br>Changed t <sub>DBE</sub> from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins<br>respectively<br>Removed footnote that read "BHE.BLE is the AND of both BHE and BLE. Chip can<br>be deselected by either disabling the chip enable signals or by disabling both BHE<br>and BLE" on page # 4<br>Removed footnote that read "If both BHE and BLE are toggled together, then t <sub>LZE</sub><br>is 10 ns" on page # 5<br>Added Pb-free package information |
| *B   | 461631  | See ECN            | NXR                | Converted from Preliminary to Final<br>Removed 35 ns Speed Bin<br>Removed "L" version of CY62126EV30<br>Changed I <sub>CC (Typ)</sub> from 8 mA to 11 mA and I <sub>CC (max)</sub> from 12 mA to 16 mA for f = f <sub>max</sub><br>Changed I <sub>CC (max)</sub> from 1.5 mA to 2.0 mA for f = 1 MHz, I <sub>SB1</sub> , I <sub>SB2 (max)</sub> from 1 $\mu$<br>to 4 $\mu$ A, I <sub>SB1</sub> , I <sub>SB2 (Typ)</sub> from 0.5 $\mu$ A to 1 $\mu$ A, I <sub>CCDR (max)</sub> from 1.5 $\mu$ A to 3 $\mu$ A, AC Tes<br>load Capacitance value from 50 pF to 30 pF, t <sub>LZOE</sub> from 3 to 5 ns, t <sub>LZCE</sub> from 6 to<br>10 ns, t <sub>HZCE</sub> from 22 to 18 ns, t <sub>LZBE</sub> from 6 to 5 ns, t <sub>PWE</sub> from 30 to 35 ns, t <sub>SD</sub> from<br>22 to 25 ns, t <sub>LZWE</sub> from 6 to 10 ns, and updated the Ordering Information table.  |
| *C   | 925501  | See ECN            | VKN                | Added footnote #7 related to I <sub>SB2</sub> and I <sub>CCDR</sub><br>Added footnote #11 related AC timing parameters  |
| *D   | 1045260 | See ECN            | VKN                | Added Automotive information<br>Updated Ordering Information table  |
| *E   | 2631771 | 01/07/09           | NXR/PYRS           | Changed $\overline{CE}$ condition from X to L in Truth table for Output Disable mode Updated template   |
| *F   | 2944332 | 06/04/2010         | VKN                | Added Contents<br>Removed byte enable from footnote #2 in Electrical Characteristics<br>Added footnote related to chip enable in Truth Table<br>Updated Package Diagrams<br>Updated links in Sales, Solutions, and Legal Information  |
| *G   | 2996166 | 07/29/2010         | AJU                | Added CY62126EV30LL-45ZSXA part in Ordering Information.<br>Added Ordering Code Definitions.<br>Modified table footnote format.   |
| *H   | 3113864 | 12/17/2010         | PRAS               | Updated Figure 1 and Package Diagram, and fixed Typo in Figure 3  |



## Document History Page (continued)

| Document Title: CY62126EV30 MoBL <sup>®</sup> , 1-Mbit (64 K × 16) Static RAM<br>Document Number: 38-05486 |         |                    |                    |   |  |  |
|--|---------|--------------------|--------------------|---|--|--|
| Rev.   | ECN No. | Submission<br>Date | Orig. of<br>Change | Description of Change   |  |  |
| *  | 3270487 | 05/31/2011         | RAME               | Updated Functional Description (Removed "For best practice recommendations,<br>refer to the Cypress application note AN1064, SRAM System Guidelines.").<br>Updated Electrical Characteristics.<br>Updated Data Retention Characteristics.<br>Added Acronyms and Units of Measure.<br>Updated in new template. |  |  |



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Page 18 of 18

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