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MB9B320M Series

32-bit Arm® Cortex®-M3 FM3 Microcontroller

The MB9B320M Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the Arm® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, DACs and Communication Interfaces (USB, UART, CSIO, I^{2}C, LIN).

The products which are described in this data sheet are placed into TYPE9 product categories in “FM3 Family Peripheral Manual”.

Features

32-bit Arm® Cortex®-M3 Core

- Processor version: r2p1
- Up to 72 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Dual operation Flash memory
  - ☐ Dual Operation Flash memory has the upper bank and the lower bank.
    So, this series could implement erase, write and read operations for each bank simultaneously.
  - ☐ Main area: Up to 256 Kbytes (Up to 240 Kbytes upper bank + 16 Kbytes lower bank)
  - ☐ Work area: 32 Kbytes (lower bank)
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 Kbytes
- SRAM1: Up to 16 Kbytes

USB Interface

The USB interface is composed of Device and Host.
PLL for USB is built-in, USB clock can be generated by multiplication of Main clock.

[USB device]

- USB2.0 Full-Speed supported
- Max 6 EndPoint supported
  - ☐ EndPoint 0 is control transfer
  - ☐ EndPoint 1, 2 can select Bulk-transfer, Interrupt-transfer or Isochronous-transfer
  - ☐ EndPoint 3 to 5 can select Bulk-transfer or Interrupt-transfer
  - ☐ EndPoint 1 to 5 are comprised of Double Buffers.
  - ☐ The size of each endpoint is according to the follows.
    - Endpoint 0, 2 to 5: 64bytes
    - Endpoint 1: 256bytes

[USB host]

- USB2.0 Full/Low-speed supported
- Bulk-transfer, interrupt-transfer and Isochronous-transfer support
- USB Device connected/dis-connected automatic detection
- Automatic processing of the IN/OUT token handshake packet
- Max 256-byte packet-length supported
- Wake-up function supported

Multi-function Serial Interface (Max eight channels)

- 4 channels with 16 steps×9-bit FIFO (ch.0/1/3/4), 4 channels without FIFO (ch.2/5/6/7)
- Operation mode is selectable from the followings for each channel.
  - ☐ UART
  - ☐ CSIO
  - ☐ LIN
  - ☐ I^{2}C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission/reception by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed to 13 to 16-bit length)
- LIN break delimiter generation (can be changed to 1 to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[I^{2}C]

Standard mode (Max 100 kbps) / Fast mode (Max 400 kbps) supported

DMA Controller (Eight channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 26 channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 2units
- Conversion time: 0.8 μs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

D/A Converter (Max two channels)

- R-2R type
- 10-bit resolution

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 65 high-speed general-purpose I/O Ports @ 80 pin Package
- Some ports are 5V tolerant.
- See “List of Pin Functions” and “I/O Circuit Type” to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Quadrature Position/Revolution Counter (QPRC) (Max two channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activation compare × 2ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter

The Watch counter is used for wake up from Sleep and Timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 23 external interrupt input pins @ 80 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in Low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC, Deep Standby Stop modes.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

Main Clock:	4 MHz to 48 MHz
Sub Clock:	32.768 kHz

- Built-in High-speed CR Clock: 4 MHz
- Built-in Low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Six low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC (selectable between keeping the value of RAM and not)
- Deep Standby Stop (selectable between keeping the value of RAM and not)

Debug

Serial Wire JTAG Debug Port (SWJ-DP)

Unique ID

Unique value of the device (41 bits) is set.

Power Supply

Wide range voltage:

VCC	= 2.7 V to 5.5 V
USBVCC	= 3.0 V to 3.6 V (when USB is used)
	= 2.7 V to 5.5 V (when GPIO is used)

Contents

1. Product Lineup

Memory Size

Product name		MB9BF321K/L/M	MB9BF322K/L/M	MB9BF324K/L/M
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

Function

Product name			MB9BF321K MB9BF322K MB9BF324K	MB9BF321L MB9BF322L MB9BF324L	MB9BF321M MB9BF322M MB9BF324M
Pin count			48	64	80/96
CPU			Cortex-M3		
	Freq.		72 MHz		
Power supply voltage range			2.7 V to 5.5 V		
USB2.0 (Device/Host)			1 ch. (Max)		
DMAC			8 ch.		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			4 ch. (Max) ch.0/1/3: FIFO ch.5: No FIFO (In ch.1/5, only UART and LIN are available.)	8 ch. (Max) ch.0/1/3/4 FIFO ch.2/5/6/7: No FIFO (In ch.1, only UART and LIN are available.)	
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF-Timer	A/D activation compare	2 ch.	1 unit		
	Input capture	4 ch.*			
	Free-run timer	3 ch.			
	Output compare	6 ch.			
	Waveform generator	3 ch.			
	PPG	3 ch.			
QPRC			1 ch.	2 ch. (Max)	
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1 ch. (SW) + 1ch. (HW)		
External Interrupts			14 pins (Max) + NMI × 1	19 pins (Max) + NMI × 1	23 pins (Max) + NMI × 1
I/O ports			35 pins (Max)	50 pins (Max)	65 pins (Max)
12-bit A/D converter			14 ch. (2 units)	23 ch. (2 units)	26 ch. (2 units)
10-bit D/A converter			2ch. (Max)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2 ch.		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SWJ-DP		
Unique ID			Yes		

*: The external input channel which can be used is shown as follows.

- ch.0 to ch.3: MB9BF321M/F322M/F324M
- ch.0, ch.2, ch.3: MB9BF321K/F322K/F324K, MB9BF321L/F322L/F324L

Note:

– *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.*
It is necessary to use the port relocate function of the I/O port according to your function use.
See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

2. Packages

Package \ Product name	MB9BF321K MB9BF322K MB9BF324K	MB9BF321L MB9BF322L MB9BF324L	MB9BF321M MB9BF322M MB9BF324M
LQFP: LQA048 (0.5 mm pitch)	❍	-	-
QFN: VNA048 (0.5 mm pitch)	❍	-	-
LQFP: LQD064 (0.5 mm pitch)	-	❍	-
LQFP: LQG064 (0.65 mm pitch)	-	❍	-
QFN: VNC064 (0.5 mm pitch)	-	❍	-
LQFP: LQH080 (0.5 mm pitch)	-	-	❍
LQFP: LQJ080 (0.65 mm pitch)	-	-	❍
BGA: FDG096 (0.5 mm pitch)	-	-	❍

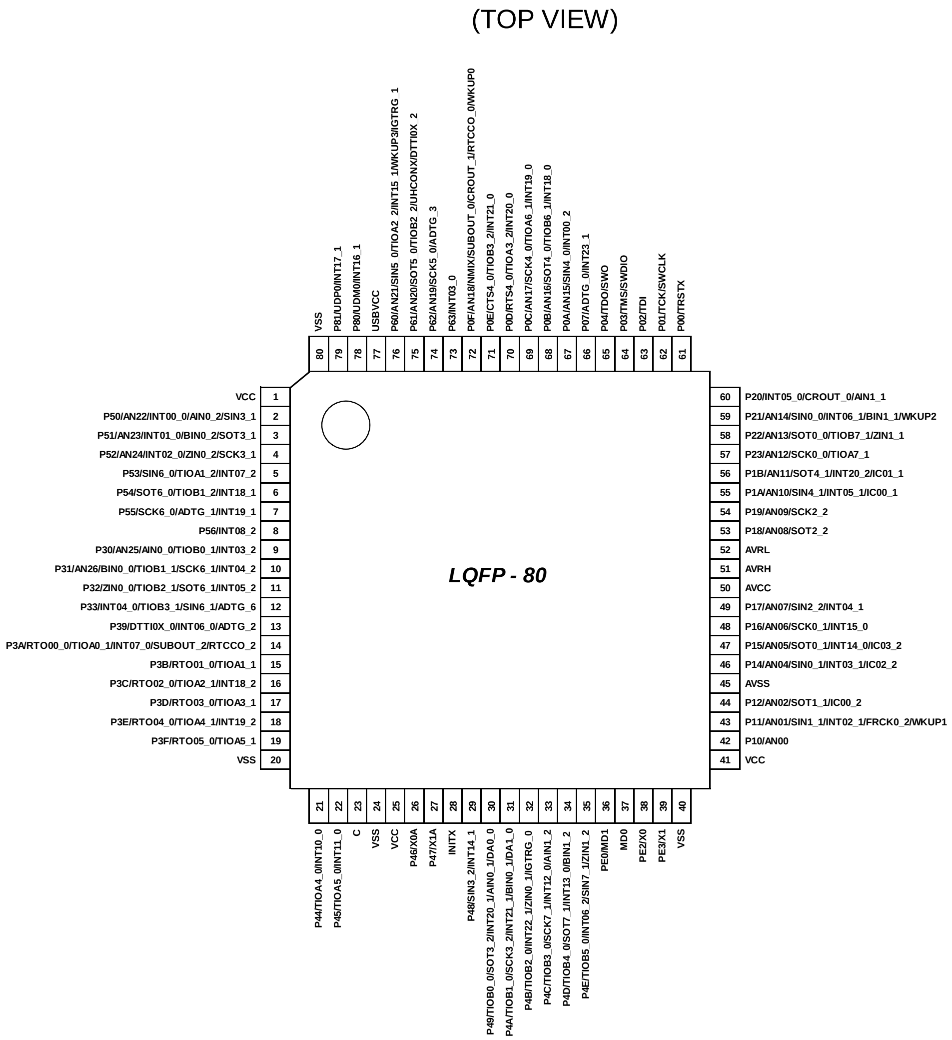
❍: Supported

Note:

– *See “Package Dimensions” for detailed information on each package.*

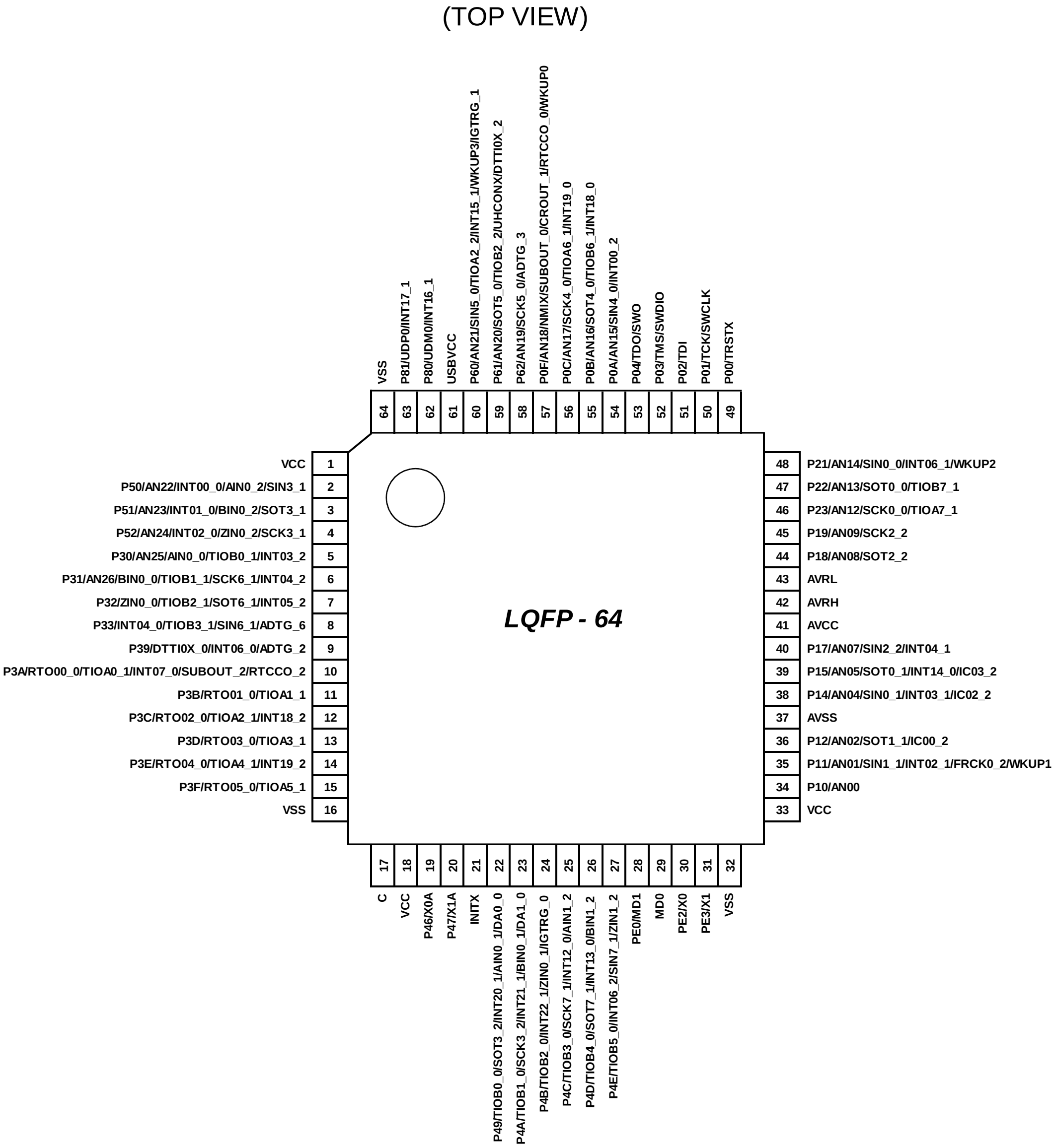
3. Pin Assignment

LQH080/LQJ080



Note:
- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

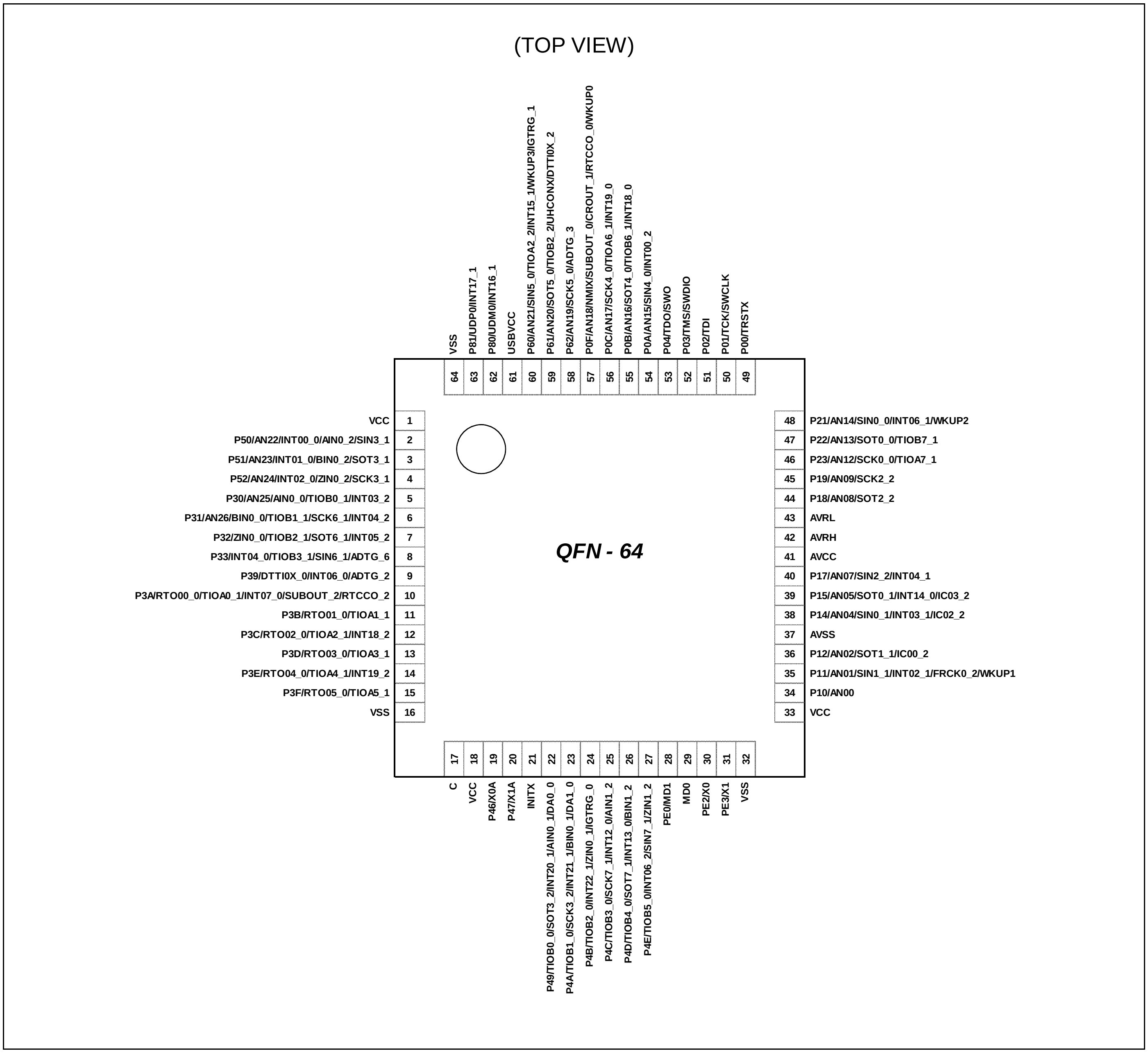
LQD064/LQG064



Note:

– *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

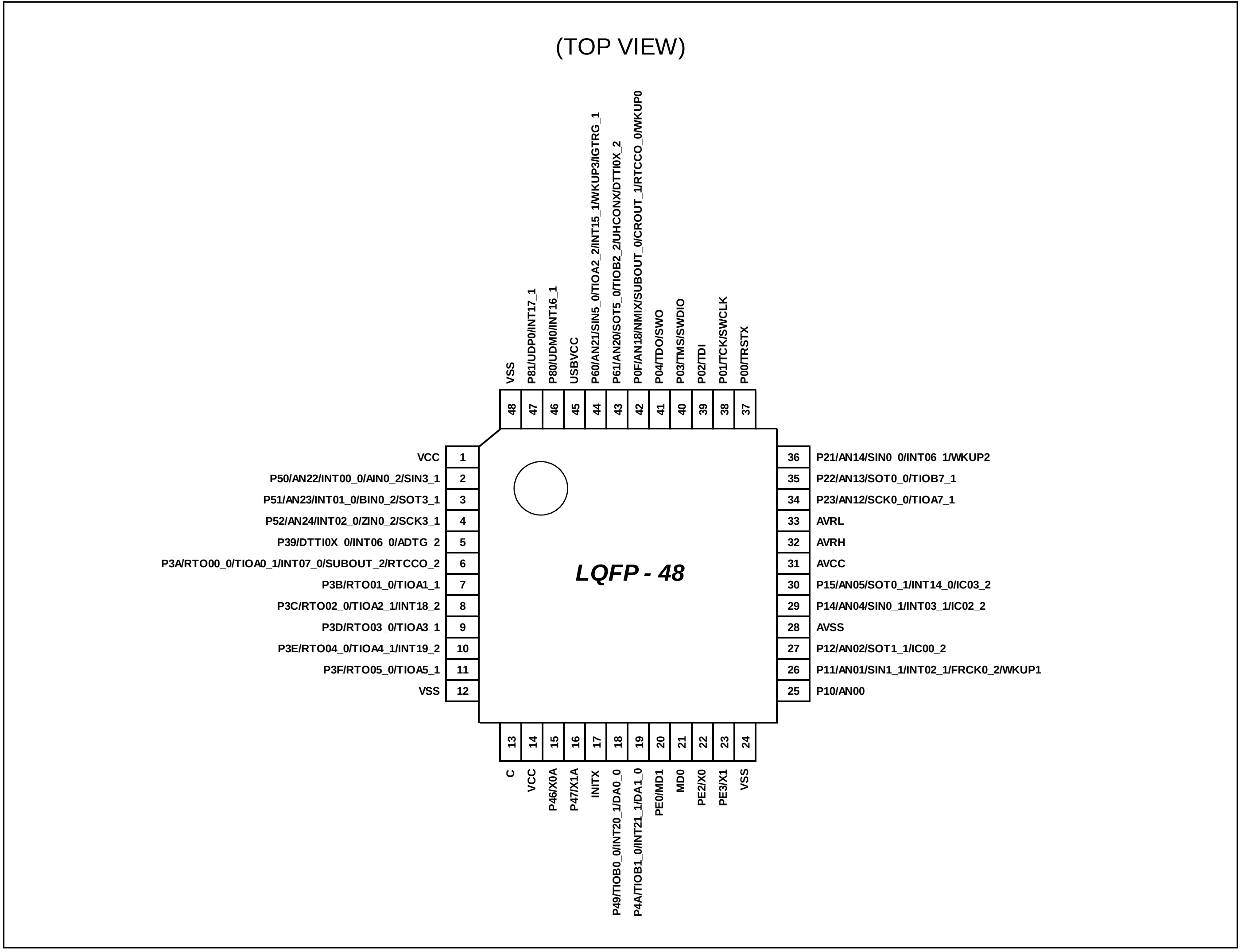
VNC064



Note:

– *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

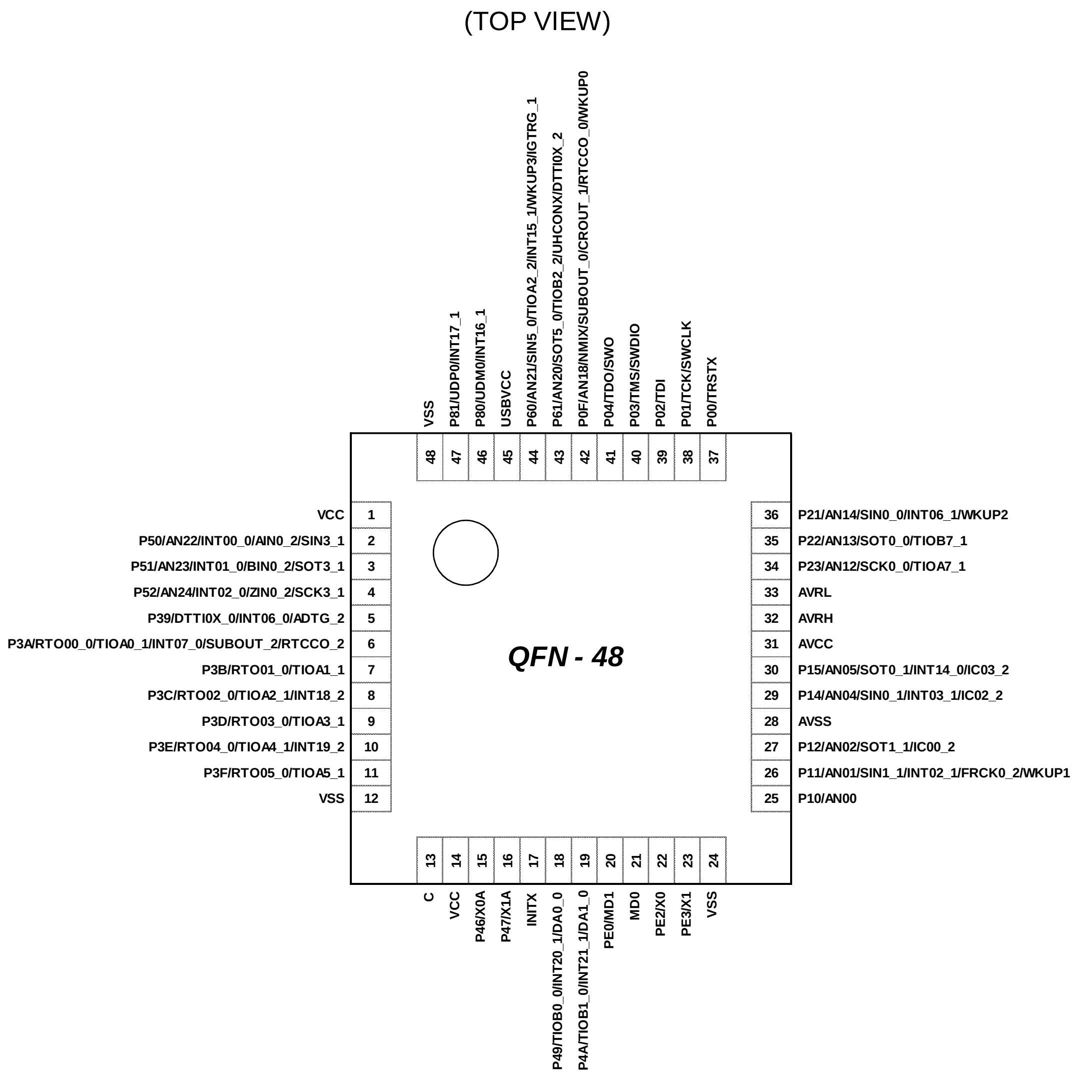
LQA048



Note:

– *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

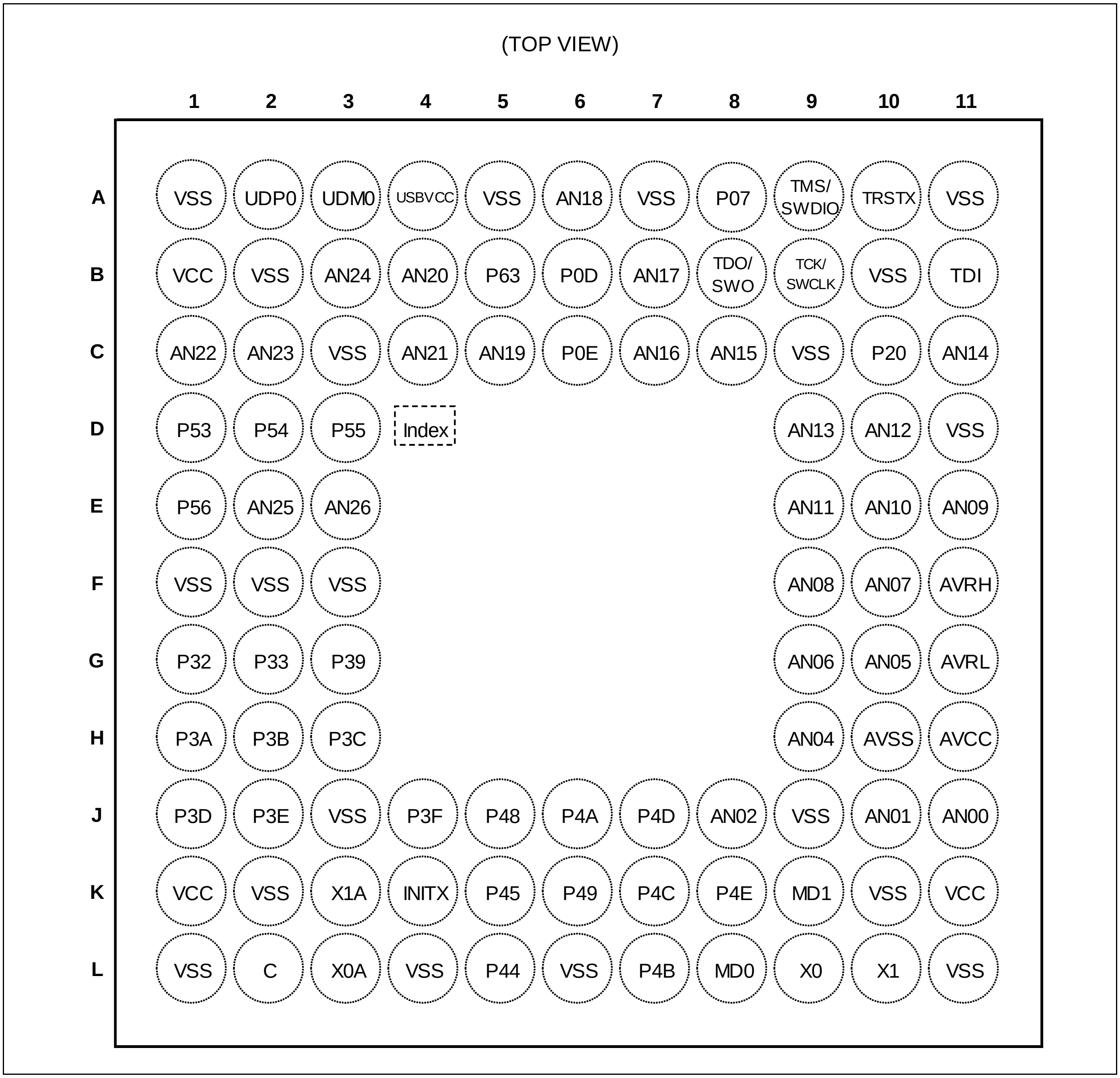
VNA048



Note:

– *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

FDG096



	1	2	3	4	5	6	7	8	9	10	11
A	VSS	UDP0	UDM0	USBVCC	VSS	AN18	VSS	P07	TMS/ SWDIO	TRSTX	VSS
B	VCC	VSS	AN24	AN20	P63	P0D	AN17	TDO/ SWO	TCK/ SWCLK	VSS	TDI
C	AN22	AN23	VSS	AN21	AN19	P0E	AN16	AN15	VSS	P20	AN14
D	P53	P54	P55	Index					AN13	AN12	VSS
E	P56	AN25	AN26						AN11	AN10	AN09
F	VSS	VSS	VSS						AN08	AN07	AVRH
G	P32	P33	P39						AN06	AN05	AVRL
H	P3A	P3B	P3C						AN04	AVSS	AVCC
J	P3D	P3E	VSS	P3F	P48	P4A	P4D	AN02	VSS	AN01	AN00
K	VCC	VSS	X1A	INITX	P45	P49	P4C	P4E	MD1	VSS	VCC
L	VSS	C	X0A	VSS	P44	VSS	P4B	MD0	X0	X1	VSS

Note:

– *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
1	B1	1	1	VCC	-	
2	C1	2	2	P50 INT00_0 AIN0_2 SIN3_1 AN22	F	N
3	C2	3	3	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) AN23	F	N
4	B3	4	4	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) AN24	F	N
5	D1	-	-	P53 SIN6_0 TIOA1_2 INT07_2	E	L
6	D2	-	-	P54 SOT6_0 (SDA6_0) TIOB1_2 INT18_1	E	L
7	D3	-	-	P55 SCK6_0 (SCL6_0) ADTG_1 INT19_1	E	L
8	E1	-	-	P56 INT08_2	E	L
9	E2	5	-	P30 AIN0_0 TIOB0_1 INT03_2 AN25	F	N

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
10	E3	6	-	P31 BIN0_0 TIOB1_1 SCK6_1 (SCL6_1) INT04_2 AN26	F	N
11	G1	7	-	P32 ZIN0_0 TIOB2_1 SOT6_1 (SDA6_1) INT05_2	E	L
12	G2	8	-	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6	E	L
13	G3	9	5	P39 DTTI0X_0 INT06_0 ADTG_2	E	L
14	H1	10	6	P3A RTO00_0 (PPG00_0) TIOA0_1 INT07_0 SUBOUT_2 RTCCO_2	G	L
15	H2	11	7	P3B RTO01_0 (PPG00_0) TIOA1_1	G	K
16	H3	12	8	P3C RTO02_0 (PPG02_0) TIOA2_1 INT18_2	G	L
17	J1	13	9	P3D RTO03_0 (PPG02_0) TIOA3_1	G	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
18	J2	14	10	P3E RTO04_0 (PPG04_0) TIOA4_1 INT19_2	G	L
19	J4	15	11	P3F RTO05_0 (PPG04_0) TIOA5_1	G	K
20	L1	16	12	VSS	-	
21	L5	-	-	P44 TIOA4_0 INT10_0	G	L
22	K5	-	-	P45 TIOA5_0 INT11_0	G	L
23	L2	17	13	C	-	
24	L4	-	-	VSS	-	
25	K1	18	14	VCC	-	
26	L3	19	15	P46 X0A	D	F
27	K3	20	16	P47 X1A	D	G
28	K4	21	17	INITX	B	C
29	J5	-	-	P48 INT14_1 SIN3_2	E	L
30	K6	22	18	P49 TIOB0_0 INT20_1 DA0_0	L	L
			-	SOT3_2 (SDA3_2) AIN0_1		
31	J6	23	19	P4A TIOB1_0 INT21_1 DA1_0	L	L
			-	SCK3_2 (SCL3_2) BIN0_1		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
32	L7	24	-	P4B TIOB2_0 INT22_1 IGTRG_0 ZIN0_1	E	L
33	K7	25	-	P4C TIOB3_0 SCK7_1 (SCL7_1) INT12_0 AIN1_2	I*	L
34	J7	26	-	P4D TIOB4_0 SOT7_1 (SDA7_1) INT13_0 BIN1_2	I*	L
35	K8	27	-	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2	I*	L
36	K9	28	20	MD1 PE0	C	E
37	L8	29	21	MD0	K	D
38	L9	30	22	X0 PE2	A	A
39	L10	31	23	X1 PE3	A	B
40	L11	32	24	VSS	-	
41	K11	33	-	VCC	-	
42	J11	34	25	P10 AN00	F	M
43	J10	35	26	P11 AN01 SIN1_1 INT02_1 FRCK0_2 WKUP1	F	N
44	J8	36	27	P12 AN02 SOT1_1 (SDA1_1) IC00_2	F	M

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
45	H10	37	28	AVSS	-	
46	H9	38	29	P14	F	N
				AN04		
				INT03_1		
				IC02_2		
				SIN0_1		
47	G10	39	30	P15	F	N
				AN05		
				IC03_2		
				SOT0_1 (SDA0_1)		
				INT14_0		
48	G9	-	-	P16	F	N
				AN06		
				SCK0_1 (SCL0_1)		
				INT15_0		
49	F10	40	-	P17	F	N
				AN07		
				SIN2_2		
				INT04_1		
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18	F	M
				AN08		
				SOT2_2 (SDA2_2)		
54	E11	45	-	P19	F	M
				AN09		
				SCK2_2 (SCL2_2)		
55	E10	-	-	P1A	F	N
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
56	E9	-	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 INT20_2	F	N
57	D10	46	34	P23 SCK0_0 (SCL0_0) TIOA7_1 AN12	F	M
58	D9	47	35	P22 SOT0_0 (SDA0_0) TIOB7_1 AN13	F	M
		-	-	ZIN1_1		
59	C11	48	36	P21 SIN0_0 INT06_1 WKUP2 BIN1_1 AN14	F	N
60	C10	-	-	P20 INT05_0 CROUT_0 AIN1_1	E	N
61	A10	49	37	P00 TRSTX	E	J
62	B9	50	38	P01 TCK SWCLK	E	J
63	B11	51	39	P02 TDI	E	J
64	A9	52	40	P03 TMS SWDIO	E	J
65	B8	53	41	P04 TDO SWO	E	J
66	A8	-	-	P07 ADTG_0 INT23_1	E	L

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
67	C8	54	-	P0A SIN4_0 INT00_2 AN15	J*	N
68	C7	55	-	P0B SOT4_0 (SDA4_0) TIOB6_1 AN16 INT18_0	J*	N
69	B7	56	-	P0C SCK4_0 (SCL4_0) TIOA6_1 INT19_0 AN17	J*	N
70	B6	-	-	P0D RTS4_0 TIOA3_2 INT20_0	E	L
71	C6	-	-	P0E CTS4_0 TIOB3_2 INT21_0	E	L
72	A6	57	42	P0F NMIX SUBOUT_0 CROUT_1 RTCCO_0 WKUP0 AN18	F	I
73	B5	-	-	P63 INT03_0	E	L
74	C5	58	-	P62 SCK5_0 (SCL5_0) ADTG_3 AN19	F	M
75	B4	59	43	P61 SOT5_0 (SDA5_0) TIOB2_2 UHCONX DTTI0X_2 AN20	F	M

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
76	C4	60	44	P60	J*	N
				SIN5_0		
				TIOA2_2		
				INT15_1		
				WKUP3		
				IGTRG_1		
				AN21		
77	A4	61	45	USBVCC	-	
78	A3	62	46	P80	H	H
				UDM0		
				INT16_1		
79	A2	63	47	P81	H	H
				UDP0		
				INT17_1		
80	A1	64	48	VSS	-	
-	A5, A7, A11, B2, B10, C3, C9, D11, F1, F2, F3, J3, J9, K2, K10, L6	-	-	VSS	-	

*: 5 V tolerant I/O

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
ADC	ADTG_0	A/D converter external trigger input pin	66	A8	-	-
	ADTG_1		7	D3	-	-
	ADTG_2		13	G3	9	5
	ADTG_3		74	C5	58	-
	ADTG_6		12	G2	8	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	42	J11	34	25
	AN01		43	J10	35	26
	AN02		44	J8	36	27
	AN04		46	H9	38	29
	AN05		47	G10	39	30
	AN06		48	G9	-	-
	AN07		49	F10	40	-
	AN08		53	F9	44	-
	AN09		54	E11	45	-
	AN10		55	E10	-	-
	AN11		56	E9	-	-
	AN12		57	D10	46	34
	AN13		58	D9	47	35
	AN14		59	C11	48	36
	AN15		67	C8	54	-
	AN16		68	C7	55	-
	AN17		69	B7	56	-
	AN18		72	A6	57	42
	AN19		74	C5	58	-
	AN20		75	B4	59	43
	AN21		76	C4	60	44
	AN22		2	C1	2	2
	AN23		3	C2	3	3
	AN24		4	B3	4	4
	AN25		9	E2	5	-
	AN26		10	E3	6	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	14	H1	10	6
	TIOB0_0	Base timer ch.0 TIOB pin	30	K6	22	18
	TIOB0_1		9	E2	5	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	15	H2	11	7
	TIOA1_2		5	D1	-	-
	TIOB1_0	Base timer ch.1 TIOB pin	31	J6	23	19
	TIOB1_1		10	E3	6	-
	TIOB1_2		6	D2	-	-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	16	H3	12	8
	TIOA2_2		76	C4	60	44
	TIOB2_0	Base timer ch.2 TIOB pin	32	L7	24	-
	TIOB2_1		11	G1	7	-
	TIOB2_2		75	B4	59	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	17	J1	13	9
	TIOA3_2		70	B6	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	33	K7	25	-
	TIOB3_1		12	G2	8	-
	TIOB3_2		71	C6	-	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	21	L5	-	-
	TIOA4_1		18	J2	14	10
	TIOB4_0	Base timer ch.4 TIOB pin	34	J7	26	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	22	K5	-	-
	TIOA5_1		19	J4	15	11
	TIOB5_0	Base timer ch.5 TIOB pin	35	K8	27	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	69	B7	56	-
	TIOB6_1	Base timer ch.6 TIOB pin	68	C7	55	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	57	D10	46	34
	TIOB7_1	Base timer ch.7 TIOB pin	58	D9	47	35
Debugger	SWCLK	Serial wire debug interface clock input pin	62	B9	50	38
	SWDIO	Serial wire debug interface data input / output pin	64	A9	52	40
	SWO	Serial wire viewer output pin	65	B8	53	41
	TCK	JTAG test clock input pin	62	B9	50	38
	TDI	JTAG test data input pin	63	B11	51	39
	TDO	JTAG debug data output pin	65	B8	53	41
	TMS	JTAG test mode state input/output pin	64	A9	52	40
	TRSTX	JTAG test reset input pin	61	A10	49	37

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	2
	INT00_2		67	C8	54	-
	INT01_0	External interrupt request 01 input pin	3	C2	3	3
	INT02_0	External interrupt request 02 input pin	4	B3	4	4
	INT02_1		43	J10	35	26
	INT03_0	External interrupt request 03 input pin	73	B5	-	-
	INT03_1		46	H9	38	29
	INT03_2		9	E2	5	-
	INT04_0	External interrupt request 04 input pin	12	G2	8	-
	INT04_1		49	F10	40	-
	INT04_2		10	E3	6	-
	INT05_0	External interrupt request 05 input pin	60	P20	-	-
	INT05_1		55	E10	-	-
	INT05_2		11	G1	7	-
	INT06_0	External interrupt request 06 input pin	13	G3	9	5
	INT06_1		59	C11	48	36
	INT06_2		35	K8	27	-
	INT07_0	External interrupt request 07 input pin	14	H1	10	6
	INT07_2		5	D1	-	-
	INT08_2	External interrupt request 08 input pin	8	E1	-	-
	INT10_0	External interrupt request 10 input pin	21	L5	-	-
	INT11_0	External interrupt request 11 input pin	22	K5	-	-
	INT12_0	External interrupt request 12 input pin	33	K7	25	-
	INT13_0	External interrupt request 13 input pin	34	J7	26	-
	INT14_0	External interrupt request 14 input pin	47	G10	39	30
	INT14_1		29	J5	-	-
	INT15_0	External interrupt request 15 input pin	48	G9	-	-
	INT15_1		76	C4	60	44
	INT16_1	External interrupt request 16 input pin	78	A3	62	46
	INT17_1	External interrupt request 17 input pin	79	A2	63	47
	INT18_0	External interrupt request 18 input pin	68	C7	55	-
	INT18_1		6	D2	-	-
	INT18_2		16	H3	12	8
	INT19_0	External interrupt request 19 input pin	59	C11	56	-
	INT19_1		7	D3	-	-
	INT19_2		18	J2	14	10

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT20_0	External interrupt request 20 input pin	70	B6	-	-
	INT20_1		30	K6	22	18
	INT20_2		56	E9	-	-
	INT21_0	External interrupt request 21 input pin	71	C6	-	-
	INT21_1		31	J6	23	19
	INT22_1	External interrupt request 22 input pin	32	L7	24	-
	INT23_1	External interrupt request 23 input pin	66	A8	-	-
	NMIX	Non-Maskable Interrupt input pin	72	A6	57	42
GPIO	P00	General-purpose I/O port 0	61	A10	49	37
	P01		62	B9	50	38
	P02		63	B11	51	39
	P03		64	A9	52	40
	P04		65	B8	53	41
	P07		66	A8	-	-
	P0A		67	C8	54	-
	P0B		68	C7	55	-
	P0C		69	B7	56	-
	P0D		70	B6	-	-
	P0E		71	C6	-	-
	P0F		72	A6	57	42
	P10	General-purpose I/O port 1	42	J11	34	25
	P11		43	J10	35	26
	P12		44	J8	36	27
	P14		46	H9	38	29
	P15		47	G10	39	30
	P16		48	G9	-	-
	P17		49	F10	40	-
	P18		53	F9	44	-
	P19		54	E11	45	-
	P1A		55	E10	-	-
	P1B		56	E9	-	-
	P20	General-purpose I/O port 2	60	C10	-	-
	P21		59	C11	48	36
	P22		58	D9	47	35
	P23		57	D10	46	34

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
GPIO	P30	General-purpose I/O port 3	9	E2	5	-
	P31		10	E3	6	-
	P32		11	G1	7	-
	P33		12	G2	8	-
	P39		13	G3	9	5
	P3A		14	H1	10	6
	P3B		15	H2	11	7
	P3C		16	H3	12	8
	P3D		17	J1	13	9
	P3E		18	J2	14	10
	P3F		19	J4	15	11
	P44	General-purpose I/O port 4	21	L5	-	-
	P45		22	K5	-	-
	P46		26	L3	19	15
	P47		27	K3	20	16
	P48		29	J5	-	-
	P49		30	K6	22	18
	P4A		31	J6	23	19
	P4B		32	L7	24	-
	P4C		33	K7	25	-
	P4D		34	J7	26	-
	P4E		35	K8	27	-
	P50	General-purpose I/O port 5	2	C1	2	2
	P51		3	C2	3	3
	P52		4	B3	4	4
	P53		5	D1	-	-
	P54		6	D2	-	-
	P55		7	D3	-	-
	P56		8	E1	-	-
	P60	General-purpose I/O port 6	76	C4	60	44
	P61		75	B4	59	43
	P62		74	C5	58	-
	P63		73	B5	-	-
	P80	General-purpose I/O port 8	78	A3	62	46
	P81		79	A2	63	47
	PE0	General-purpose I/O port E	36	K9	28	20
	PE2		38	L9	30	22
	PE3		39	L10	31	23

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	59	C11	48	36
	SIN0_1		46	H9	38	29
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^{2}C (operation mode 4).	58	D9	47	35
	SOT0_1 (SDA0_1)		47	G10	39	30
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^{2}C (operation mode 4).	57	D10	46	34
	SCK0_1 (SCL0_1)		48	G9	-	-
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	43	J10	35	26
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/LIN (operation modes 0,1,3) .	44	J8	36	27
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	49	F10	40	-
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^{2}C (operation mode 4).	53	F9	44	-
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I^{2}C (operation mode 4).	54	E11	45	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	C1	2	2
	SIN3_2		29	J5	-	-
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^{2}C (operation mode 4).	3	C2	3	3
	SOT3_2 (SDA3_2)		30	K6	-	-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I^{2}C (operation mode 4).	4	B3	4	4
	SCK3_2 (SCL3_2)		31	J6	-	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	67	C8	54	-
	SIN4_1		55	E10	-	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	68	C7	55	-
	SOT4_1 (SDA4_1)		56	E9	-	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	69	B7	56	-
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	70	B6	-	-
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	71	C6	-	-
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	76	C4	60	44
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	75	B4	59	43
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	74	C5	58	-
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	D1	-	-
	SIN6_1		12	G2	8	-
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	D2	-	-
	SOT6_1 (SDA6_1)		11	G1	7	-
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	D3	-	-
	SCK6_1 (SCL6_1)		10	E3	6	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	35	K8	27	-
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	34	J7	26	-
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	33	K7	25	-
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0	13	G3	9	5
	DTTI0X_2		75	B4	59	43
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	43	J10	35	26
	IC00_1	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	55	E10	-	-
	IC00_2		44	J8	36	27
	IC01_1		56	E9	-	-
	IC02_2		46	H9	38	29
	IC03_2		47	G10	39	30
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	14	H1	10	6
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	15	H2	11	7
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	16	H3	12	8
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	17	J1	13	9
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	18	J2	14	10
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	19	J4	15	11
	IGTRG_0	PPG IGBT mode external trigger input pin	32	L7	24	-
	IGTRG_1		76	C4	60	44

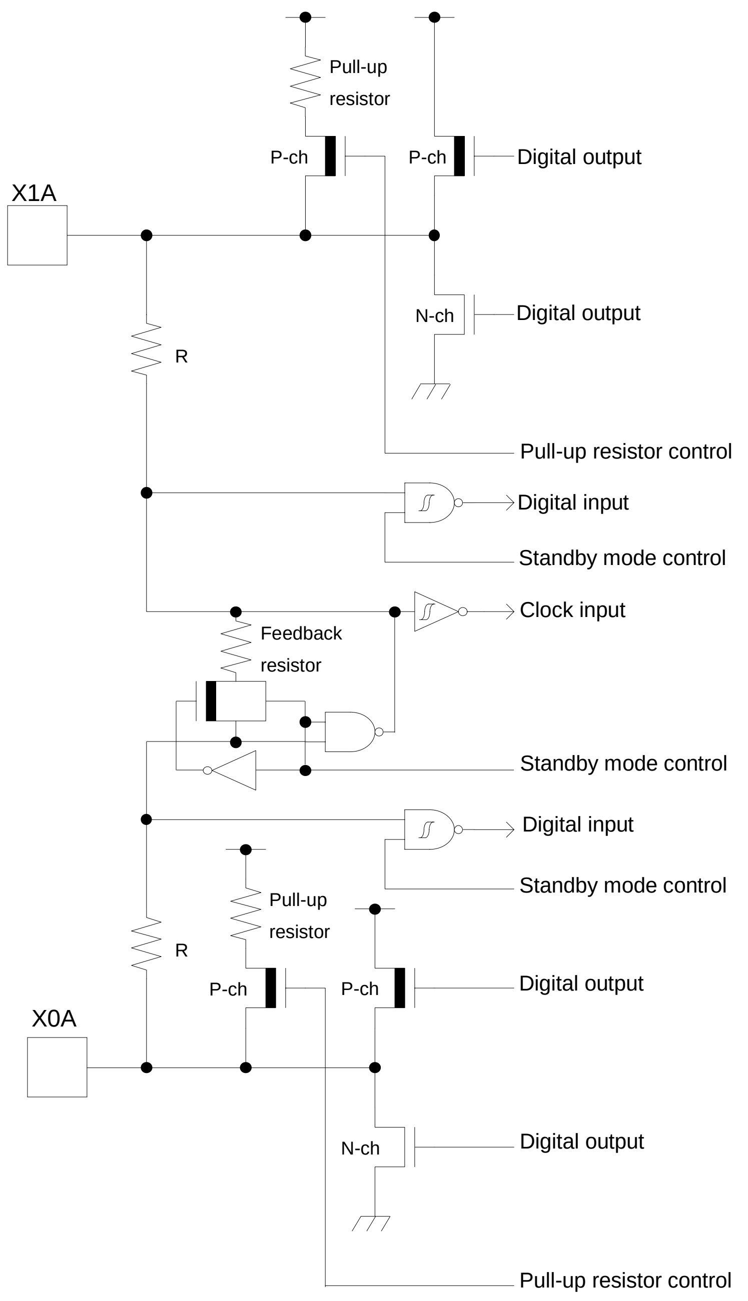
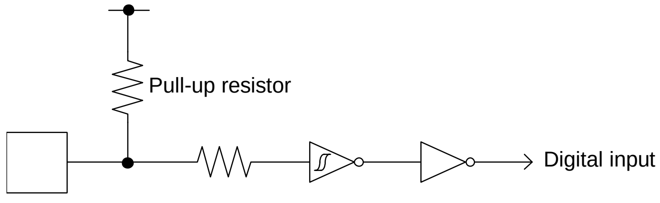
Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	9	E2	5	-
	AIN0_1		30	K6	22	-
	AIN0_2		2	C1	2	2
	BIN0_0	QPRC ch.0 BIN input pin	10	E3	6	-
	BIN0_1		31	J6	23	-
	BIN0_2		3	C2	3	3
	ZIN0_0	QPRC ch.0 ZIN input pin	11	G1	7	-
	ZIN0_1		32	L7	24	-
	ZIN0_2		4	B3	4	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	60	C10	-	-
	AIN1_2		33	K7	25	-
	BIN1_1	QPRC ch.1 BIN input pin	59	C11	-	-
	BIN1_2		34	J7	26	-
	ZIN1_1	QPRC ch.1 ZIN input pin	58	D9	-	-
	ZIN1_2		35	K8	27	-
USB	UDM0	USB device/host D – pin	78	A3	62	46
	UDP0	USB device/host D + pin	79	A2	63	47
	UHCONX	USB external pull-up control pin	75	B4	59	43
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	72	A6	57	42
	RTCCO_2		14	H1	10	6
	SUBOUT_0	Sub clock output pin	72	A6	57	42
	SUBOUT_2		14	H1	10	6
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	72	A6	57	42
	WKUP1	Deep standby mode return signal input pin 1	43	J10	35	26
	WKUP2	Deep standby mode return signal input pin 2	59	C11	48	36
	WKUP3	Deep standby mode return signal input pin 3	76	C4	60	44
DAC	DA0	D/A converter ch.0 analog output pin	30	K6	22	18
	DA1	D/A converter ch.1 analog output pin	31	J6	23	19
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	28	K4	21	17

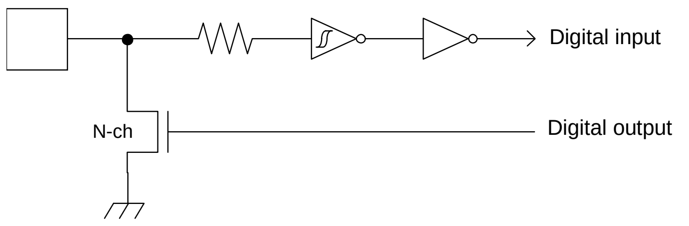
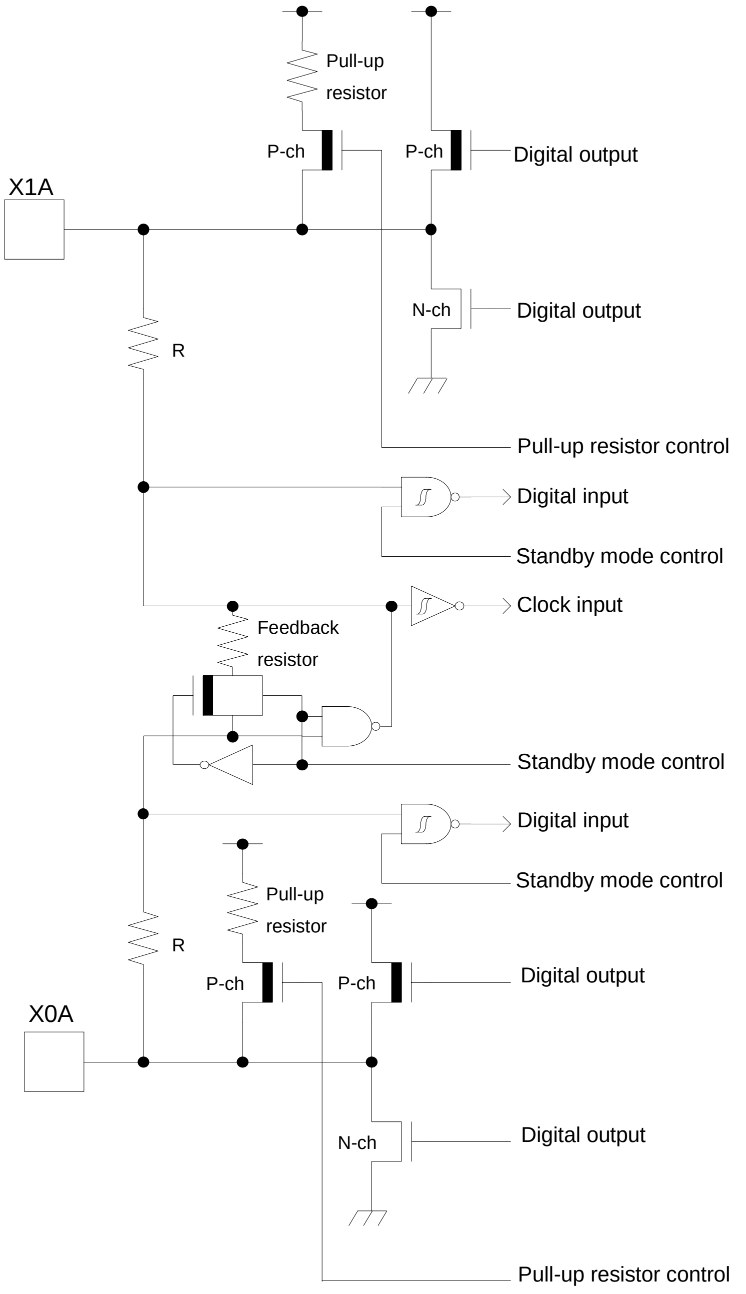
Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	37	L8	29	21
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	36	K9	28	20
Power	VCC	Power supply Pin	1	B1	1	1
	VCC	Power supply Pin	25	K1	18	14
	VCC	Power supply Pin	41	K11	33	-
	USBVCC	3.3V Power supply port for USB I/O	77	A4	61	45
GND	VSS	GND Pin	-	F1	-	-
	VSS	GND Pin	-	F2	-	-
	VSS	GND Pin	-	F3	-	-
	VSS	GND Pin	-	B2	-	-
	VSS	GND Pin	20	L1	16	12
	VSS	GND Pin	-	K2	-	-
	VSS	GND Pin	-	J3	-	-
	VSS	GND Pin	-	L6	-	-
	VSS	GND Pin	24	L4	-	-
	VSS	GND Pin	40	L11	32	24
	VSS	GND Pin	-	K10	-	-
	VSS	GND Pin	-	J9	-	-
	VSS	GND Pin	-	B10	-	-
	VSS	GND Pin	-	C9	-	-
	VSS	GND Pin	-	D11	-	-
	VSS	GND Pin	-	A11	-	-
	VSS	GND Pin	-	A7	-	-
	VSS	GND Pin	-	C3	-	-
	VSS	GND Pin	-	A5	-	-
	VSS	GND Pin	80	A1	64	48
Clock	X0	Main clock (oscillation) input pin	38	L9	30	22
	X0A	Sub clock (oscillation) input pin	26	L3	19	15
	X1	Main clock (oscillation) I/O pin	39	L10	31	23
	X1A	Sub clock (oscillation) I/O pin	27	K3	20	16
	CROUT_0	Built-in high-speed CR-osc clock output port	60	C10	-	-
	CROUT_1		72	A6	57	42
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	50	H11	41	31
	AVRH	A/D converter analog reference voltage input pin	51	F11	42	32
Analog GND	AVSS	A/D converter and D/A converter GND pin	45	H10	37	28
	AVRL	A/D converter analog reference voltage input pin	52	G11	43	33
C pin	C	Power supply stabilization capacity pin	23	L2	17	13

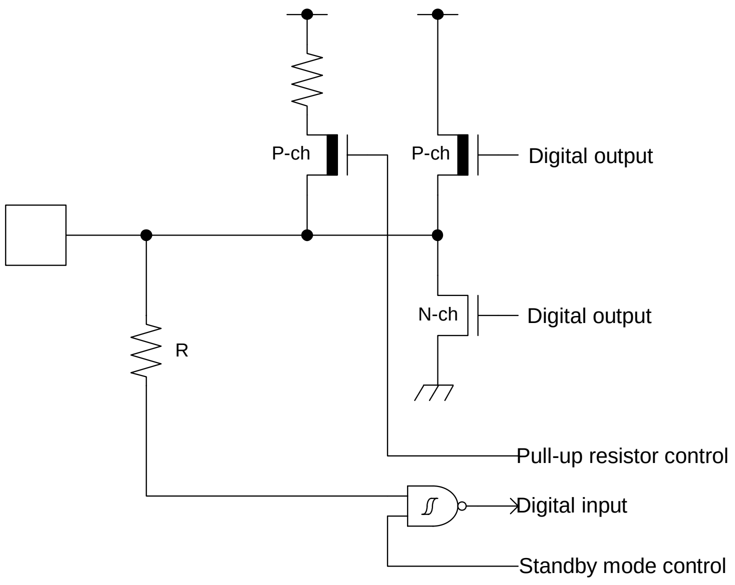
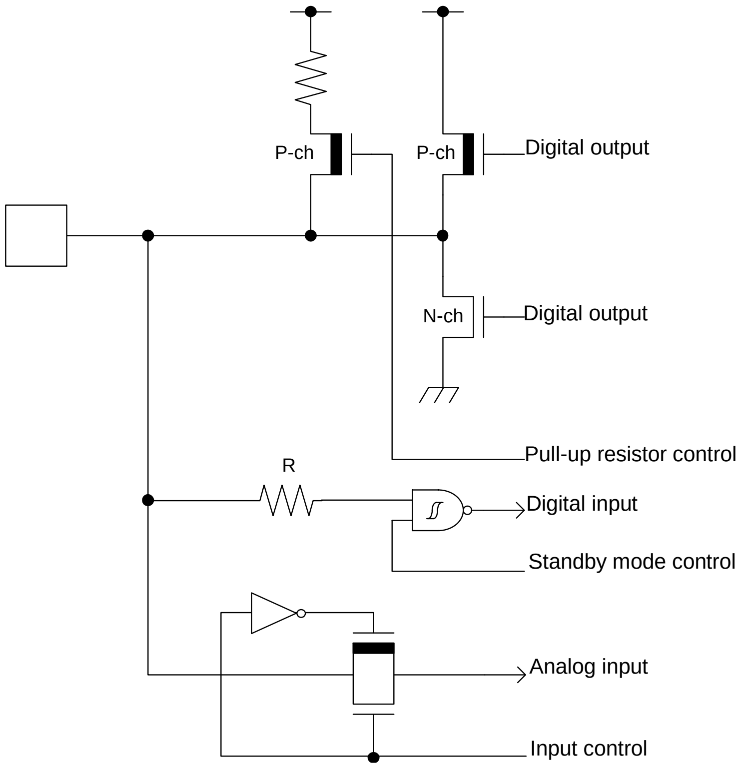
Note:

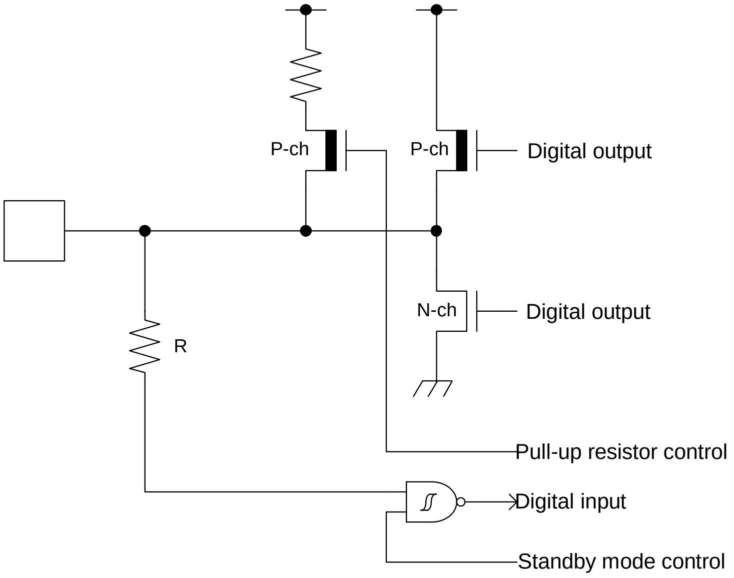
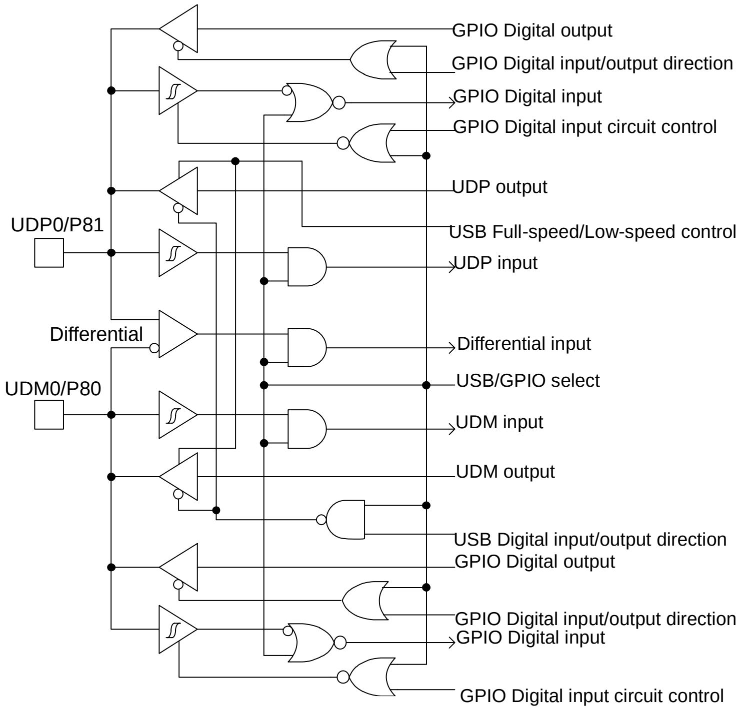
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

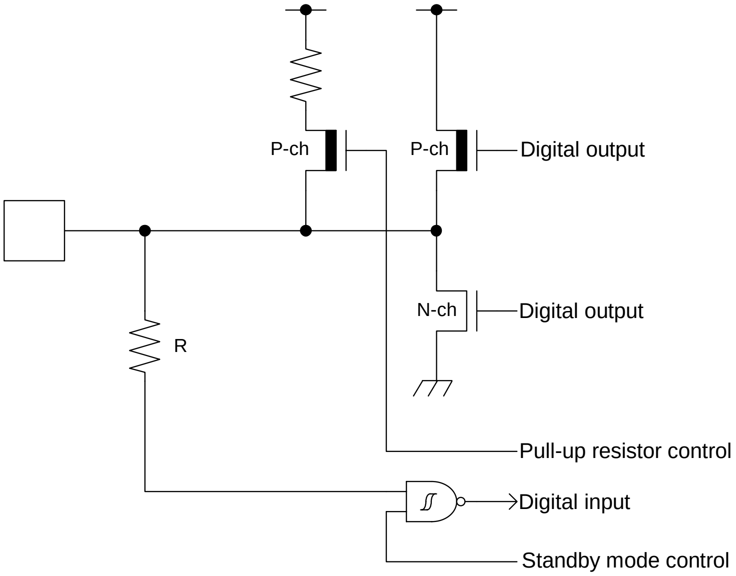
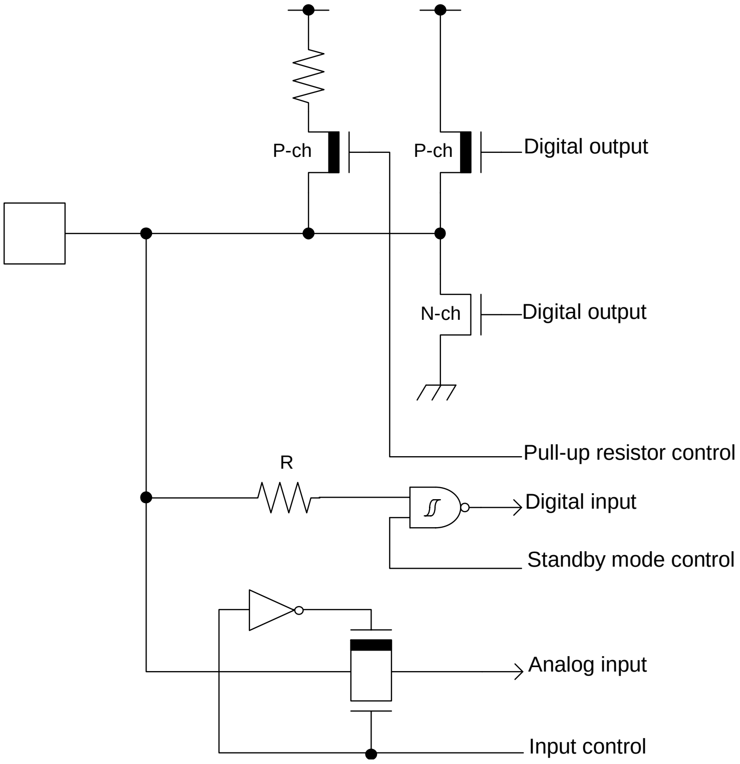
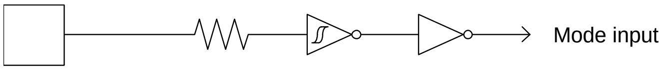
5. I/O Circuit Type

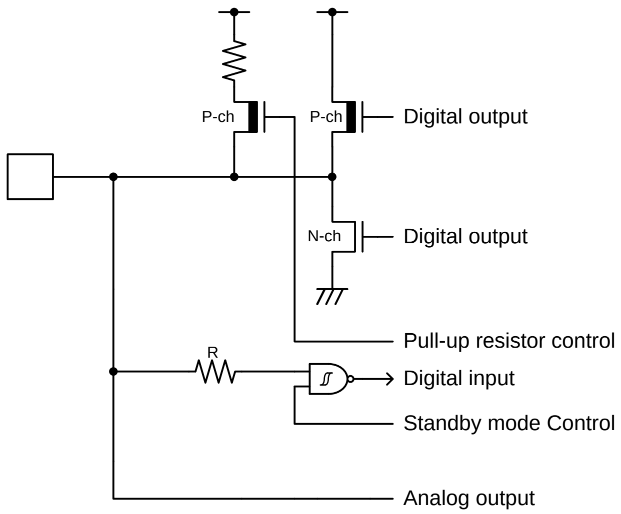
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
C		- Open drain output - CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. - Oscillation feedback resistor : Approximately 5 MΩ - With Standby mode control When the GPIO is selected. - CMOS level output. - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ - I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
E		- CMOS level output - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ - I_{OH}= -4 mA, I_{OL}= 4 mA - When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off - +B input is available
F		- CMOS level output - CMOS level hysteresis input - With input control - Analog input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ - I_{OH}= -4 mA, I_{OL}= 4 mA - When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off - +B input is available

Type	Circuit	Remarks
G		- CMOS level output - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ - I_{OH}= -12 mA, I_{OL}= 12 mA - +B input is available
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. - Full-speed, Low-speed control When the GPIO is selected. - CMOS level output - CMOS level hysteresis input - With standby mode control

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
K		CMOS level hysteresis input

Type	Circuit	Remarks
L		- CMOS level output - CMOS level hysteresis input - With input control - Analog output - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ - I_{OH} = -4 mA, I_{OL} = 4 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin, between AVRH pin and AVRL pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size:	More than 3.2 mm × 1.5 mm
Load capacitance:	Approximately 6 pF to 7 pF

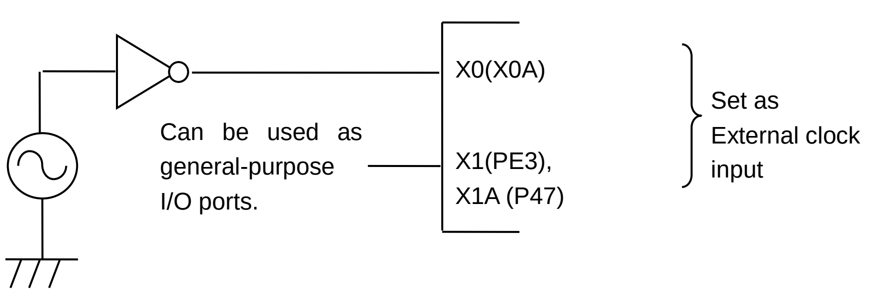
■Lead type

Load capacitance:	Approximately 6 pF to 7 pF

Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

● Example of Using an External Clock

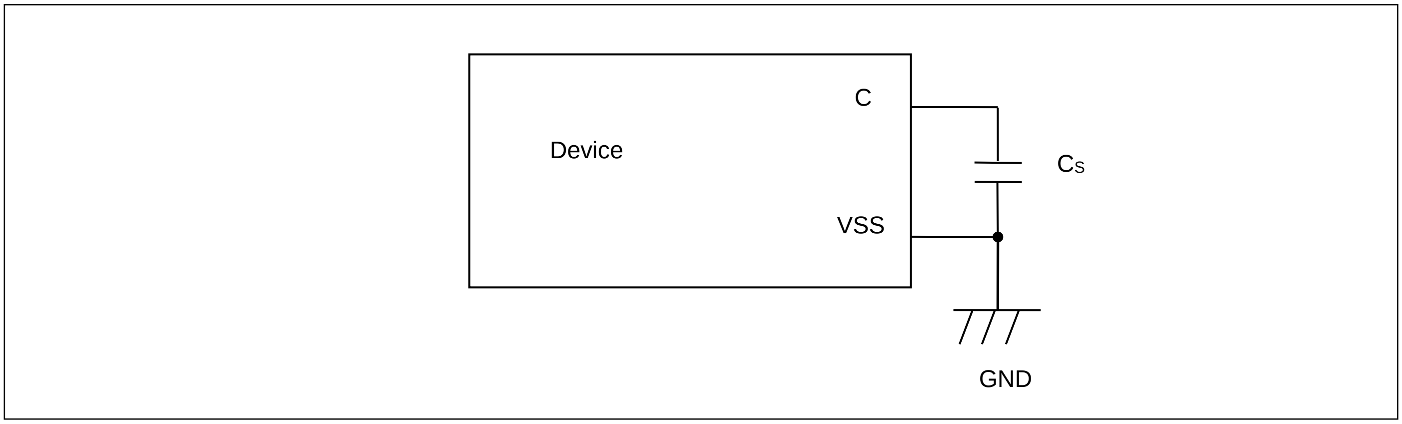


Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 μF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC →USBVCC

VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

USBVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

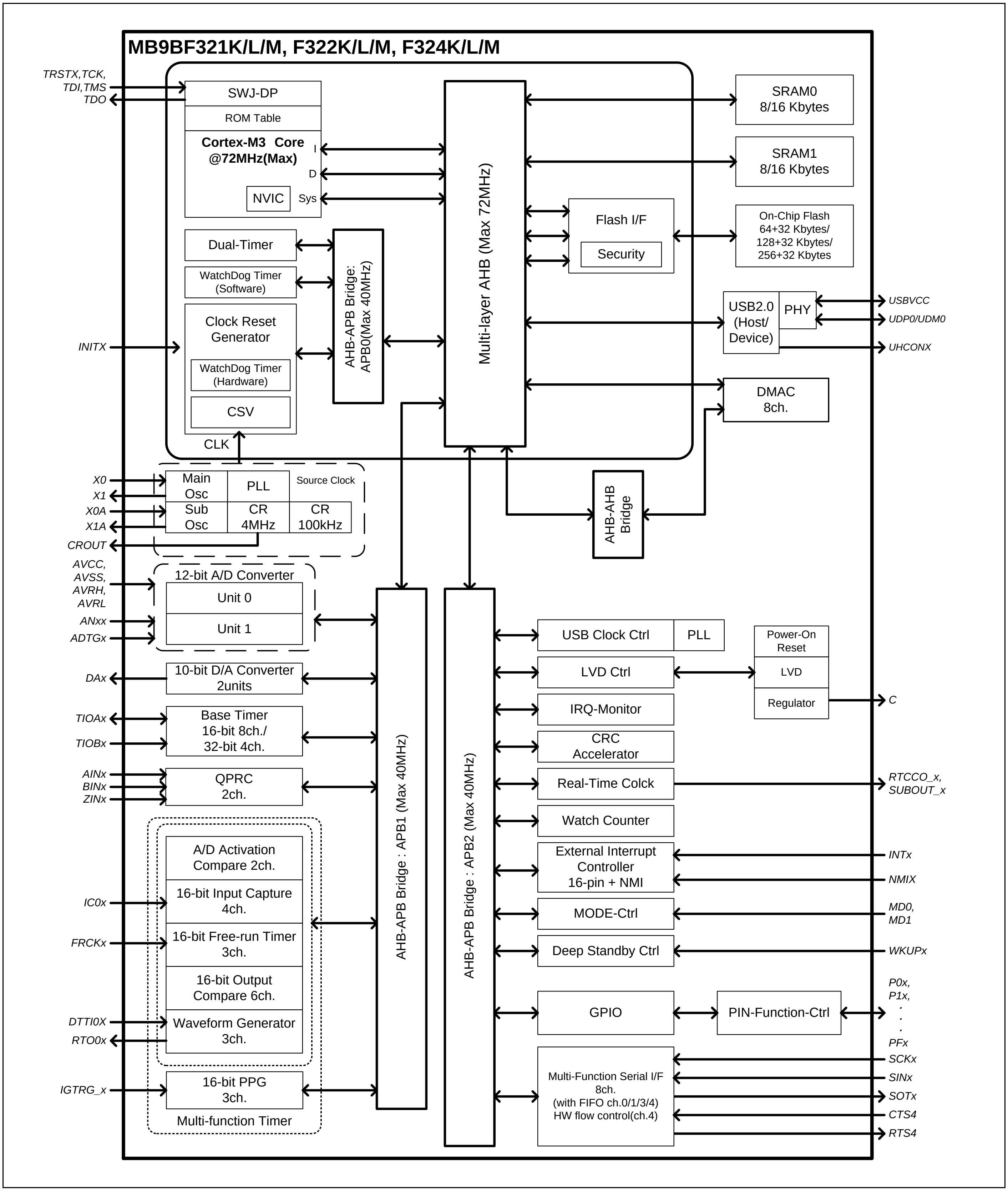
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

8. Block Diagram

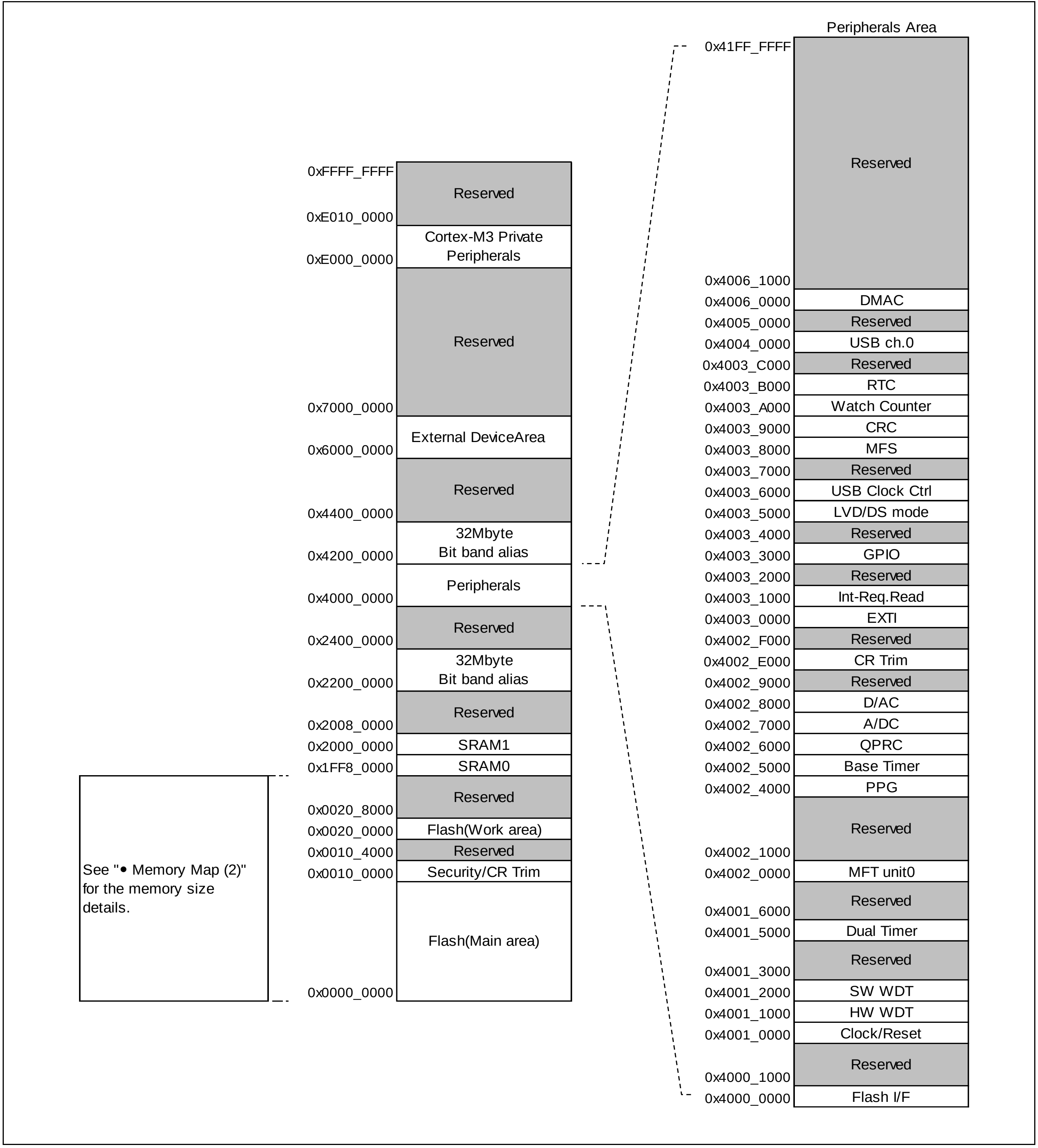


9. Memory Size

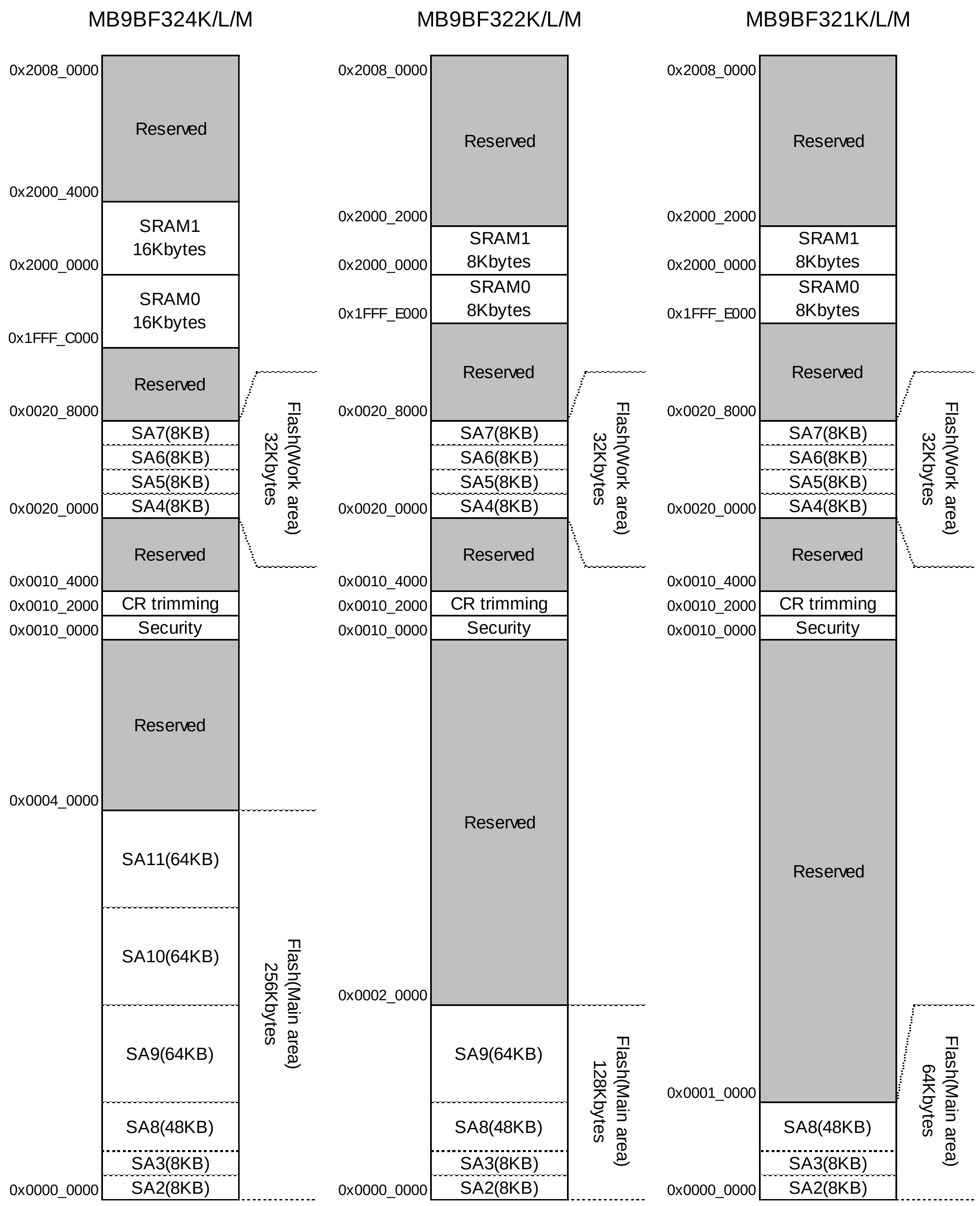
See “Memory size” in “Product Lineup” to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



Refer to the programming manual for the detail of Flash main area.

■MB9AB40N/A40N/340N/140N/150R,MB9B520M/320M/120M Series Flash Programming Manual

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter (QPRC)
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0

This is the period when the INITX pin is the "L" level.

■INITX=1

This is the period when the INITX pin is the "H" level.

■SPL=0

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

■SPL=1

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

■Input enabled

Indicates that the input function can be used.

■Internal input fixed at "0"

This is the status that the input function cannot be used. Internal input is fixed at "L".

■Hi-Z

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled

Indicates that the setting is disabled.

■Maintain previous state

Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled

Indicates that the analog input is enabled.

■Trace output

Indicates that the trace function can be used.

■GPIO selected

In Deep standby mode, pins switch to the general-purpose I/O port.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops^{*1}, Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z/ Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled		Hi-Z at trans-mission/ Input enabled/ Internal input fixed at "0" at reception	Hi-Z at trans-mission/ Input enabled/ Internal input fixed at "0" at reception	Hi-Z / Input enabled	Hi-Z / Input enabled	Hi-Z / Input enabled
I	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled
	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									Maintain previous state
J	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
K	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
L	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External interrupt enabled selected					Maintain previous state	Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									

*1: Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

*3: Maintain previous state at Timer mode. GPIO selected Internal input fixed at "0" at RTC mode, Stop mode.

*4: Maintain previous state at Timer mode. Hi-Z/Internal input fixed at "0" at RTC mode, Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB)*1, * 3	$USBV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB pin
		V_{SS} - 0.5	$USBV_{CC}$ + 0.5 (≤ 6.5 V)	V	USB pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
L level maximum output current*5	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
			39	mA	The pin doubled as USB I/O
L level average output current*6	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
			16.5	mA	The pin doubled as USB I/O
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*5	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
			- 39	mA	The pin doubled as USB I/O
H level average output current*6	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
			- 18	mA	The pin doubled as USB I/O
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}$ must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

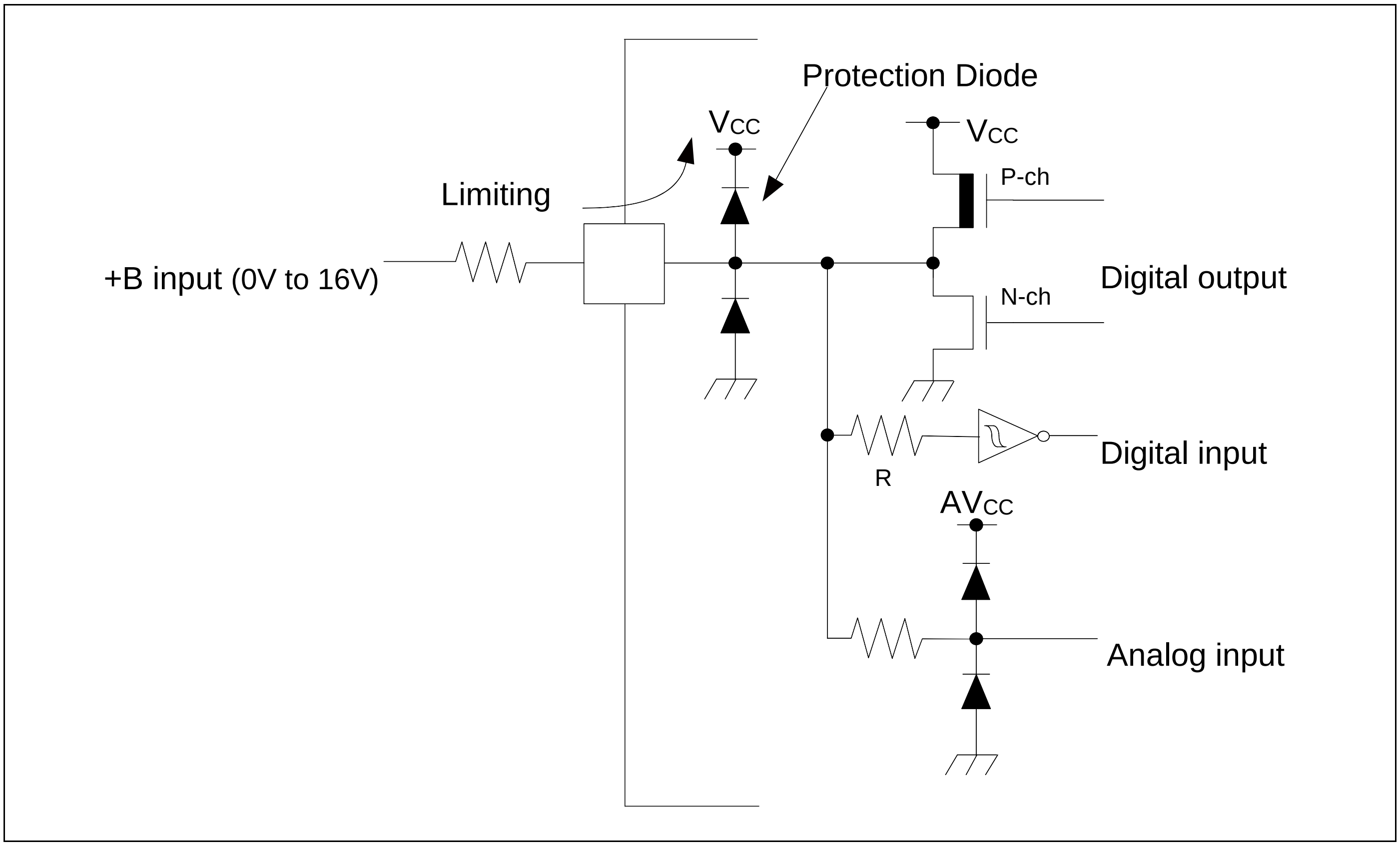
*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

*8:

- See “List of Pin Functions” and “I/O Circuit Type” about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

− *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

12.2 Recommended Operating Conditions

($V_{SS} = AV_{SS} = AVRL = 0.0V$)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*[4]	5.5	V	
Power supply voltage (3V power supply) for USB	$USBV_{CC}$	-	3.0	3.6 (≤ V_{CC})	V	*1
			2.7	5.5 (≤ V_{CC})		*2
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	μF	For Regulator*[3]
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80).

*3: See “C Pin” in “Handling Devices” for the connection of the smoothing capacitor.

*4: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

− *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 *Current Rating*

(V_{CC} = AV_{CC} = $USBV_{CC}$ = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU: 72 MHz, Peripheral: 36 MHz	32.5	41	mA	*1, *5
				CPU:72 MHz, Peripheral clock stops NOP operation	18	23	mA	*1, *5
			High-speed CR Run mode	CPU/ Peripheral: 4 MHz*2	2.5	3.4	mA	*1
			Sub Run mode	CPU/ Peripheral: 32 kHz	110	980	µA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral: 100 kHz	130	1030	µA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral: 36 MHz	22	28	mA	*1, *5
			High-speed CR Sleep mode	Peripheral: 4 MHz*2	1.6	2.6	mA	*1
			Sub Sleep mode	Peripheral: 32 kHz	96	955	µA	*1, *6
			Low-speed CR Sleep mode	Peripheral: 100 kHz	115	975	µA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A = +25°C, V_{CC} = 5.5 V

*4: T_A = +105°C, V_{CC} = 5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

(V_{CC} = AV_{CC} = $USBV_{CC}$ = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
Timer mode current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	4.1	4.8	mA	*1, *4
				T_A = + 105°C, When LVD is off	-	5.4	mA	*1, *4
	I_{CCT}		Sub Timer mode	T_A = + 25°C, When LVD is off	17	66	μA	*1, *5
				T_A = + 105°C, When LVD is off	-	835	μA	*1, *5
RTC mode current	I_{CCR}		RTC mode	T_A = + 25°C, When LVD is off	15	61	μA	*1, *5
				T_A = + 105°C, When LVD is off	-	680	μA	*1, *5
Stop mode current	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	14	53	μA	*1
				T_A = + 105°C, When LVD is off	-	600	μA	*1
Deep Standby mode current	I_{CCRD}		Deep Standby RTC mode	T_A = + 25°C, When LVD is off, When RAM is off	2.2	11	μA	*1, *3, *5
				T_A = + 25°C, When LVD is off, When RAM is on	6.2	23	μA	*1, *3, *5
				T_A = + 105°C, When LVD is off, When RAM is off	-	155	μA	*1, *3, *5
				T_A = + 105°C, When LVD is off, When RAM is on		215	μA	*1, *3, *5
	I_{CCHD}		Deep Standby Stop mode	T_A = + 25°C, When LVD is off, When RAM is off	1.6	9.6	μA	*1, *3
				T_A = + 25°C, When LVD is off, When RAM is on	5.6	22	μA	*1, *3
				T_A = + 105°C, When LVD is off, When RAM is off	-	150	μA	*1, *3
				T_A = + 105°C, When LVD is off, When RAM is on		210	μA	*1, *3

*1: When all ports are fixed.

*2: V_{CC} = 5.5 V

*3: RAM on/off setting is on-chip SRAM only.

*4: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*5: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for reset Vcc = 5.5 V	0.13	0.3	μA	At not detect
			At operation for interrupt Vcc = 5.5 V	0.13	0.3	μA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	*

*: The current at which to write or erase Flash memory, "$I_{CCFLASH}$" is added to "I_{CC}".

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.69	0.90	mA	
			At stop	0.25	25.84	μA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.97	mA	
			At stop	0.2	3.4	μA	

D/A Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*1	I_{DDA}*2	AVCC	At 1unit operation AV_{CC}=3.3 V	250	315	380	μA	
			At 1unit operation AV_{CC}=5.0 V	380	475	580	μA	
	I_{DSA}		At stop	-	-	16	μA	

*1: No-load

*2: Generates the max current by the CODE about 0x200

12.3.2 *Pin Characteristics*

(V_{CC} = USBV_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq$ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} <$ 4.5 V, I_{OH} = - 2 mA					
		12 mA type	$V_{CC} \geq$ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} <$ 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	USB$V_{CC} \geq$ 4.5 V, I_{OH} = - 18.0 mA	USBV_{CC} - 0.4	-	USBV_{CC}	V	
			USB$V_{CC} <$ 4.5 V, I_{OH} = - 12.0 mA					
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq$ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} <$ 4.5 V, I_{OL} = 2 mA					
		12 mA type	$V_{CC} \geq$ 4.5 V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} <$ 4.5 V, I_{OL} = 8 mA					
		The pin doubled as USB I/O	USB$V_{CC} \geq$ 4.5 V, I_{OL} = 16.5 mA	V_{SS}	-	0.4	V	
			USB$V_{CC} <$ 4.5 V, I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	μA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq$ 4.5 V	33	50	90	kΩ	
			$V_{CC} <$ 4.5 V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, USBVCC, VSS, AVCC, AVSS, AVRH, AVRL	-	-	5	15	pF	

12.4 AC Characteristics

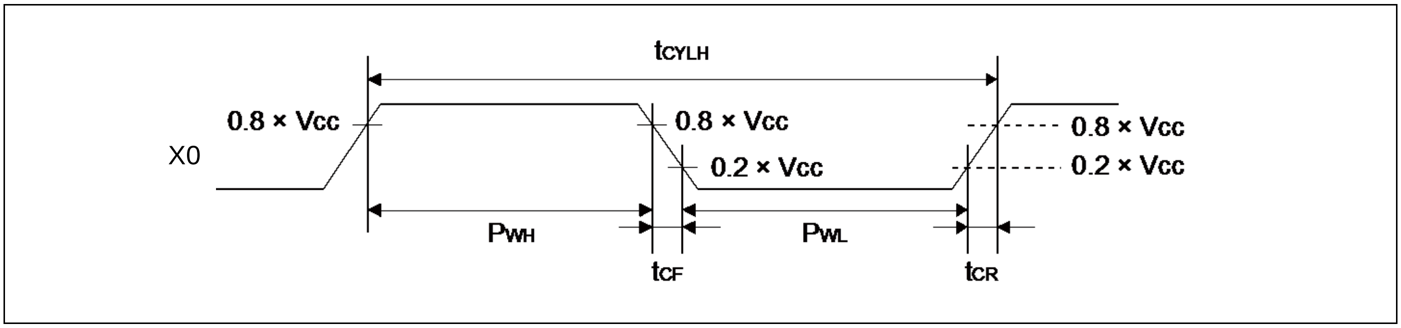
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external Clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external Clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external Clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external Clock
Internal operating clock frequency*1	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock cycle time*1	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see “Chapter 2-1: Clock” in “FM3 Family Peripheral Manual”.

*2: For about each APB bus which each peripheral is connected to, see “Block Diagram” in this data sheet.

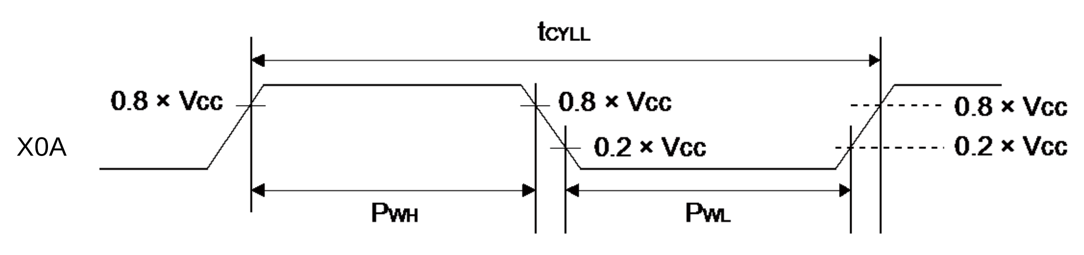


12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		PWH/tCYLL, PWL/tCYLL	45	-	55	%	When using external clock

*: See "Sub crystal oscillator" in "Handling Devices" for the crystal oscillator used.



12.4.3 *Built-in CR Oscillation Characteristics*

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
		T_A = 0°C to + 85°C	3.9	4	4.1		
		T_A = -40°C to + 105°C	3.88	4	4.12		
		T_A = + 25°C $V_{CC} \leq 3.6$ V	3.94	4	4.06		
		T_A = - 20°C to + 85°C $V_{CC} \leq 3.6$ V	3.92	4	4.08		
		T_A = - 20°C to + 105°C $V_{CC} \leq 3.6$ V	3.9	4	4.1		
		T_A = - 40°C to + 105°C	2.8	4	5.2		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	μs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.
This period is able to use high-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main and USB PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*[1] (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*[2]	f_{CLKPLL}	-	-	72	MHz	
USB clock frequency*[3]	$f_{CLKSPLL}$	-	-	48	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter: Clock” in “FM3 Family Peripheral Manual”.

*3: For more information about USB clock, see “Chapter 2-2: USB Clock Generation” in “FM3 Family Peripheral Manual Communication Macro Part”.

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*[1] (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*[2]	f_{CLKPLL}	-	-	72	MHz	

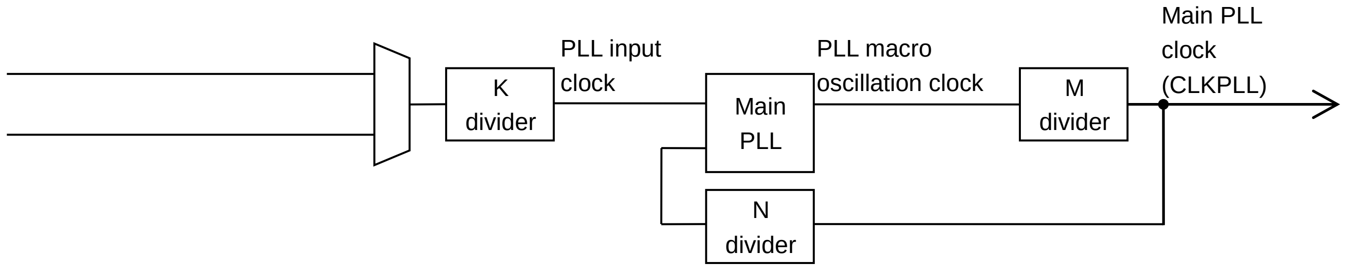
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see “Chapter 2-1: Clock” in “FM3 Family Peripheral Manual”.

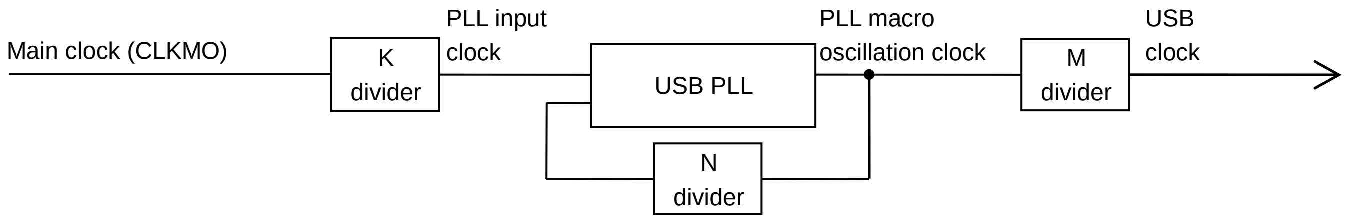
Note:

– *Make sure to input to the Main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.*
When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



USB PLL connection



12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 105°C)

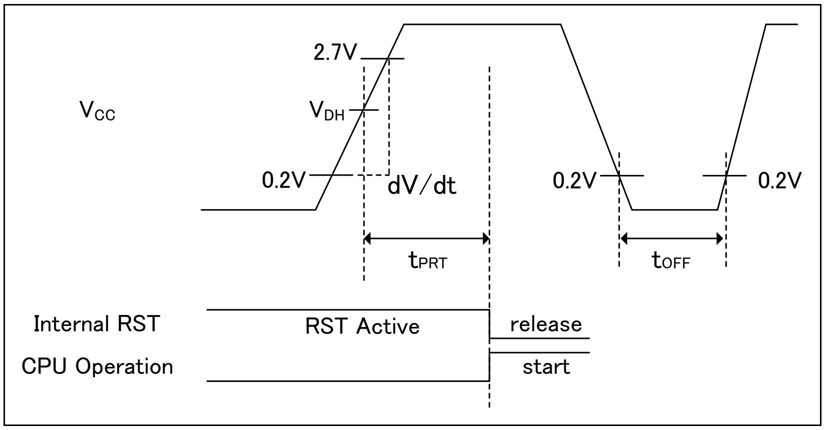
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2 V to 2.70 V	0.3	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	1.34	-	18.6	ms	

*1: V_{CC} must be held below 0.2 V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1 ms).

Note:

– *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12.4.6.*



Glossary

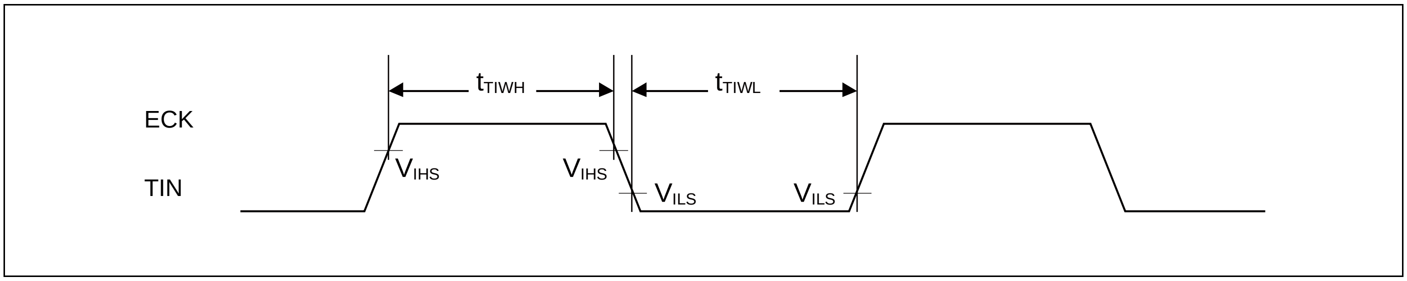
- VDH: detection voltage (when SVHR=00000) of Low-Voltage detection reset. See "12.8. Low-Voltage Detection Characteristics".

12.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

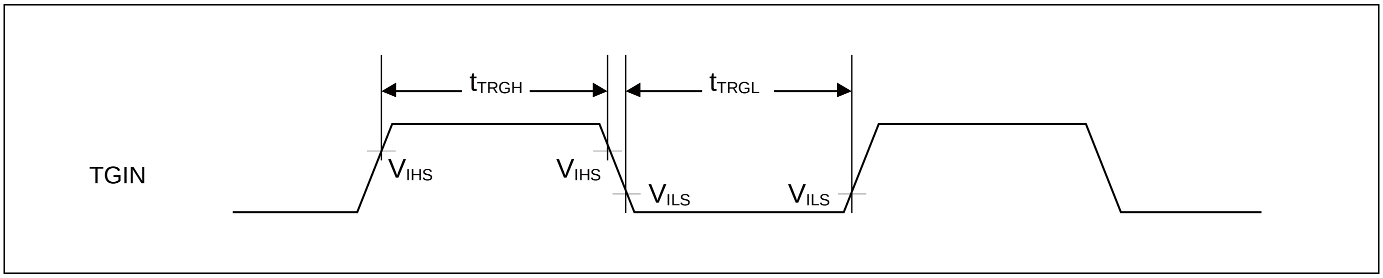
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

– *t_{CYCP} indicates the APB bus clock cycle time.*
About the APB bus number which the Base Timer is connected to, see "Block Diagram" in this data sheet.

12.4.9 CSIO/UART Timing

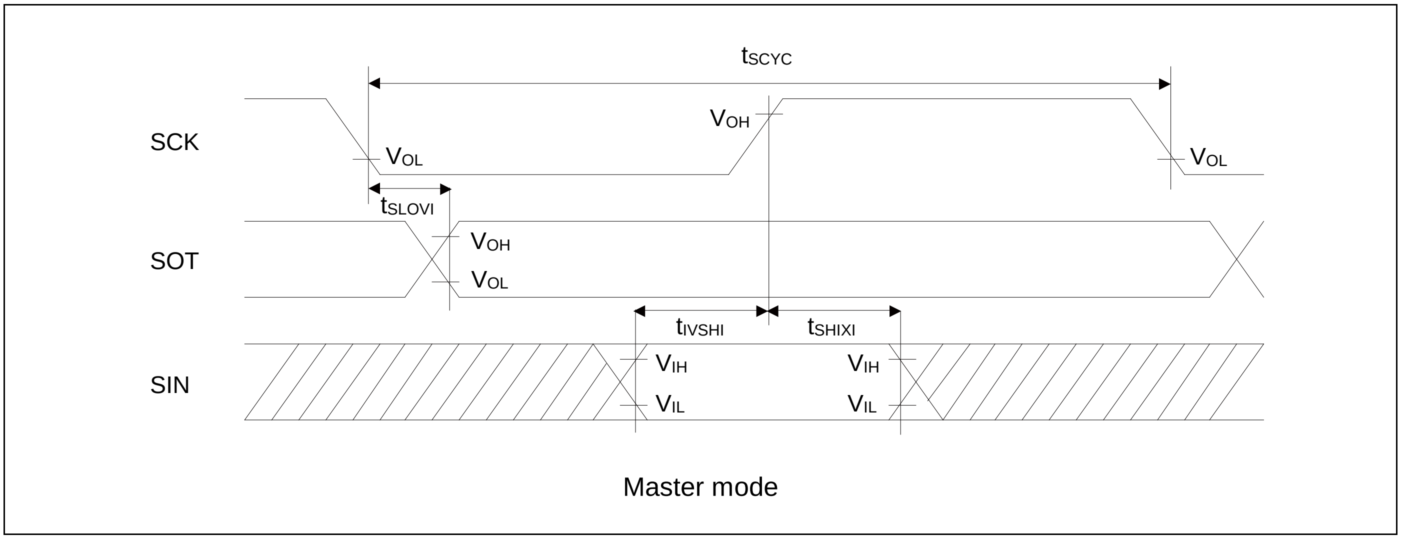
CSIO (SPI = 0, SCINV = 0)

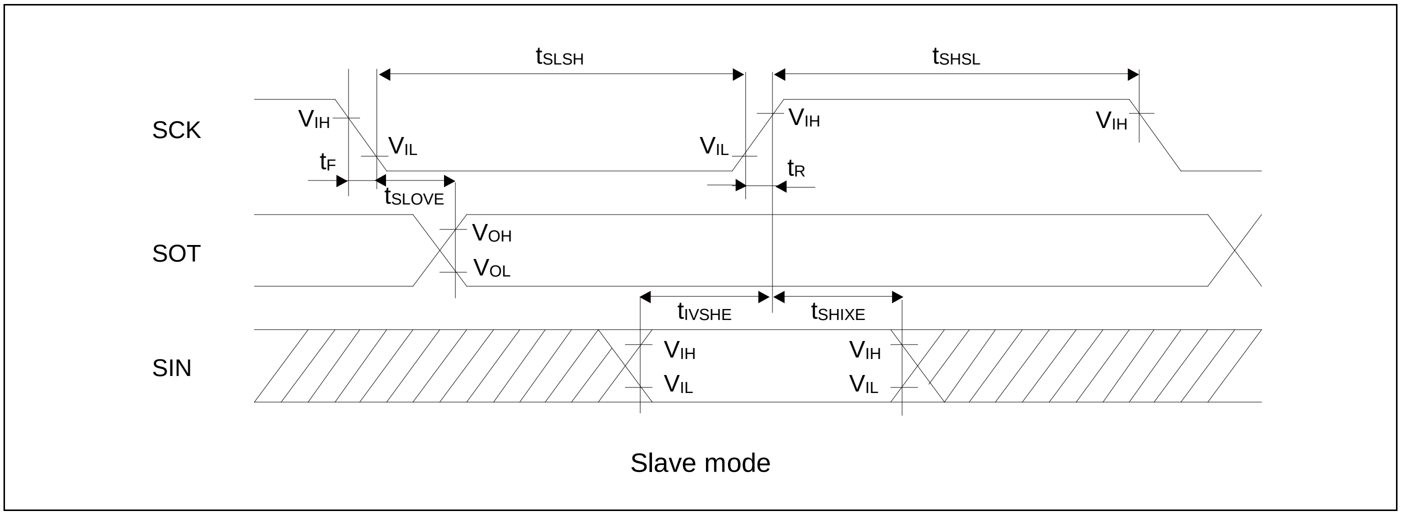
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
Master mode


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tF
tR
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
Slave mode

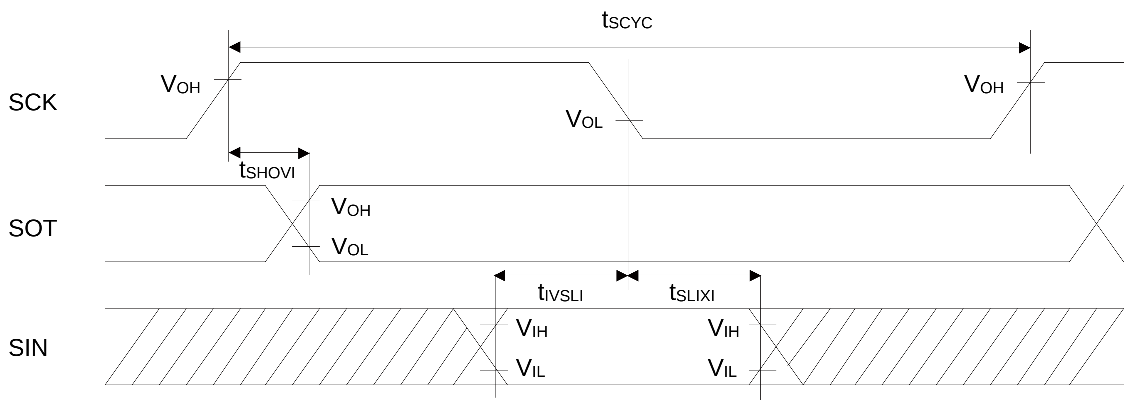
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

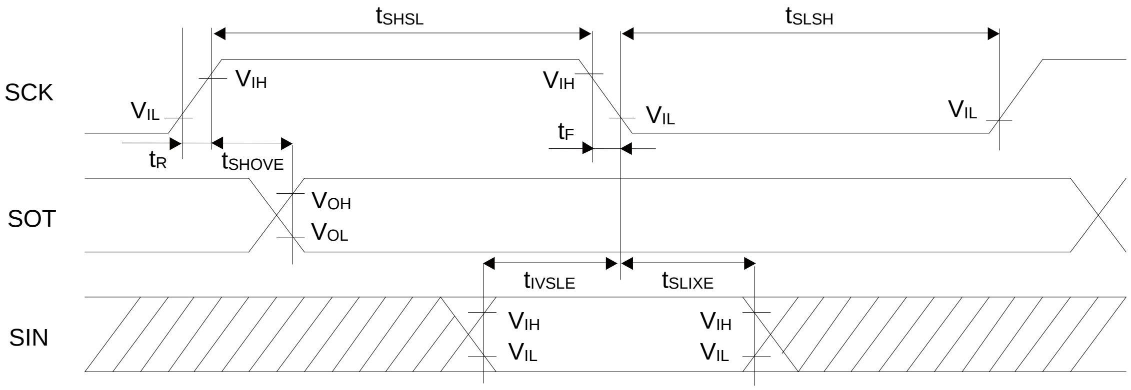
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		$V_{CC} \geq$ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

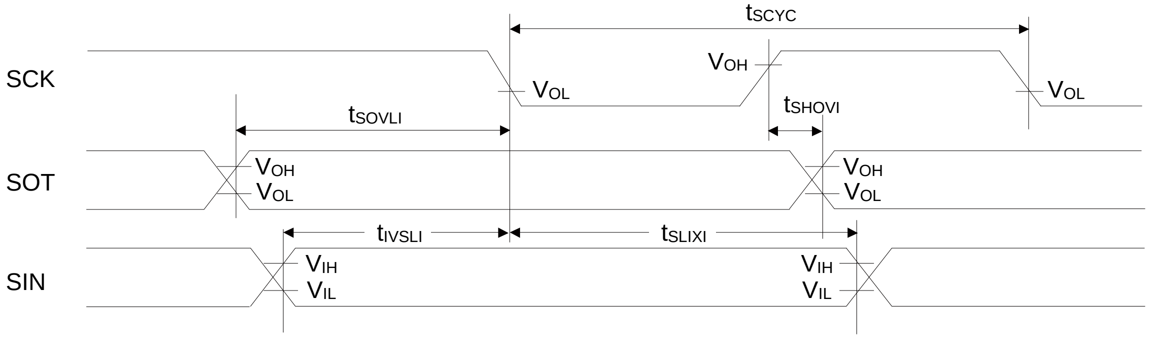
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

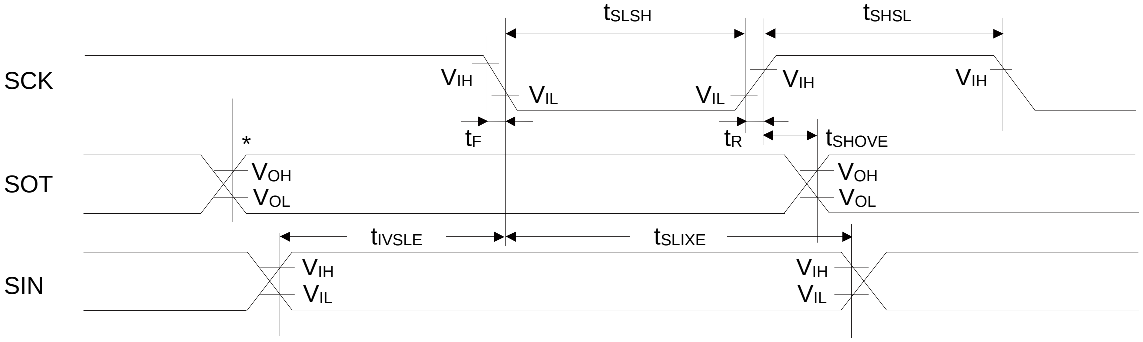
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see “Block Diagram” in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

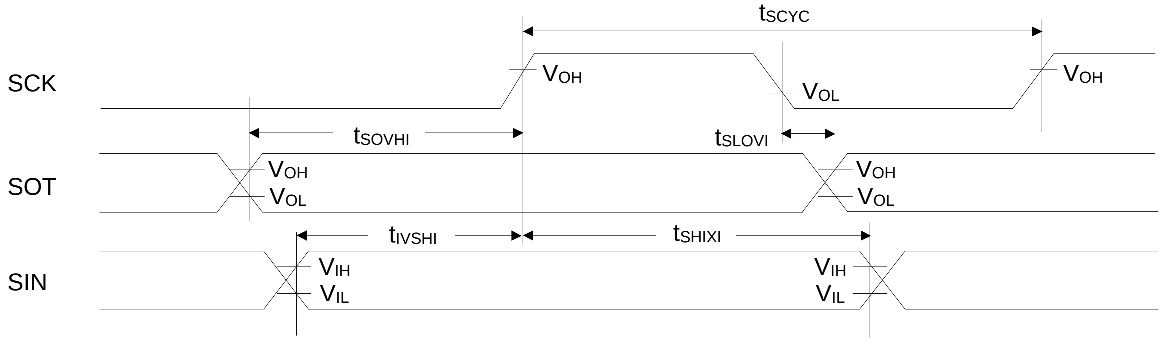
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

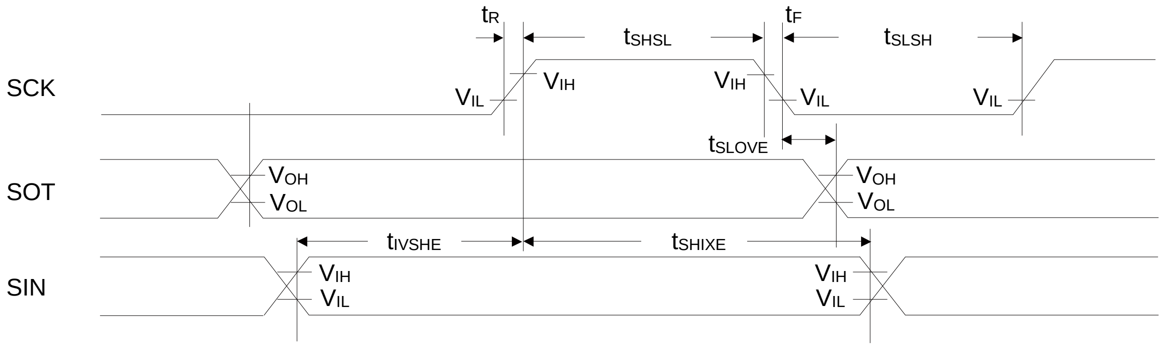
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		$V_{CC} \geq$ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- t_{CYCP} *indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance* C_L *= 30 pF.*



Master mode

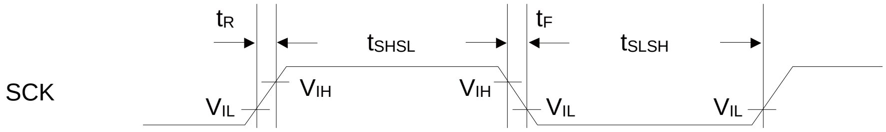


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.4.10 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx,	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt
		NMIX	*3	500	-	ns	NMI
		WKUPx	*4	500	-	ns	Deep standby wake up

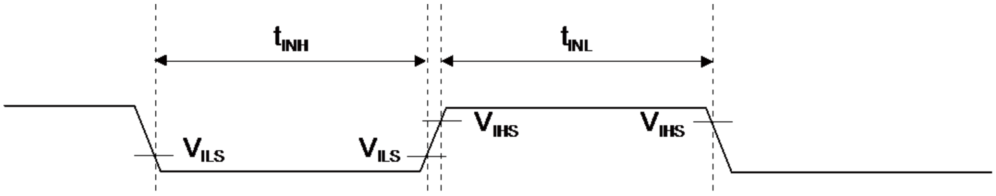
*1: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "Block Diagram" in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in Stop mode, in RTL mode, in Timer mode.

*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.



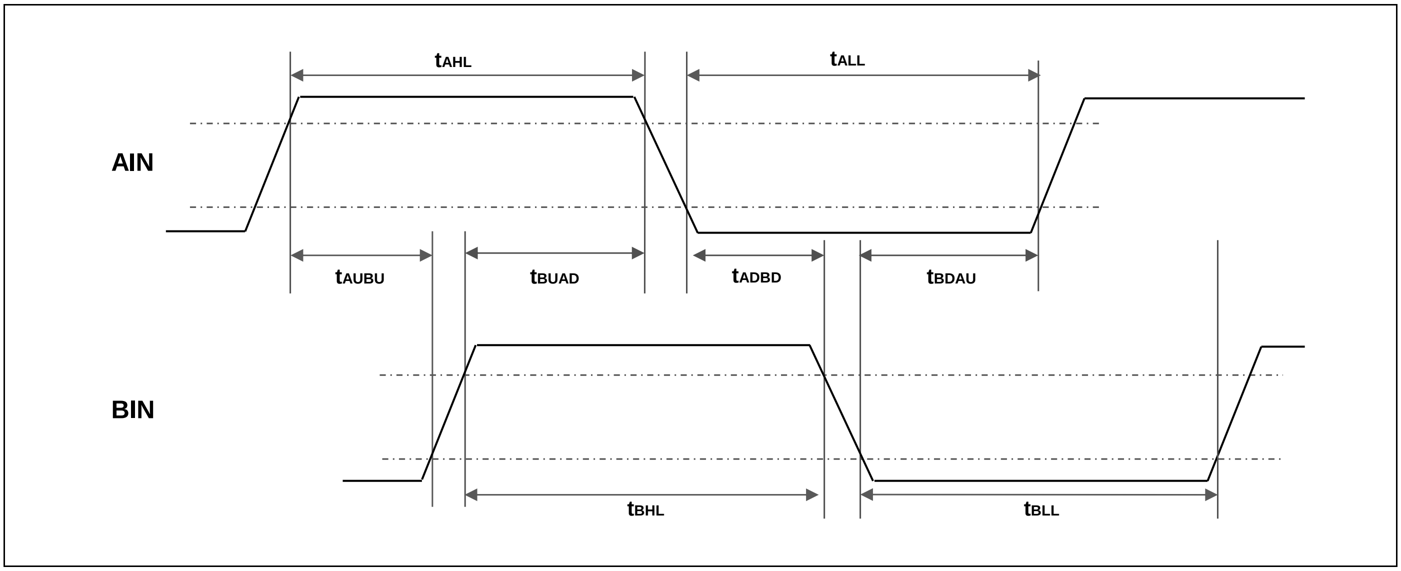
12.4.11 Quadrature Position/Revolution Counter timing

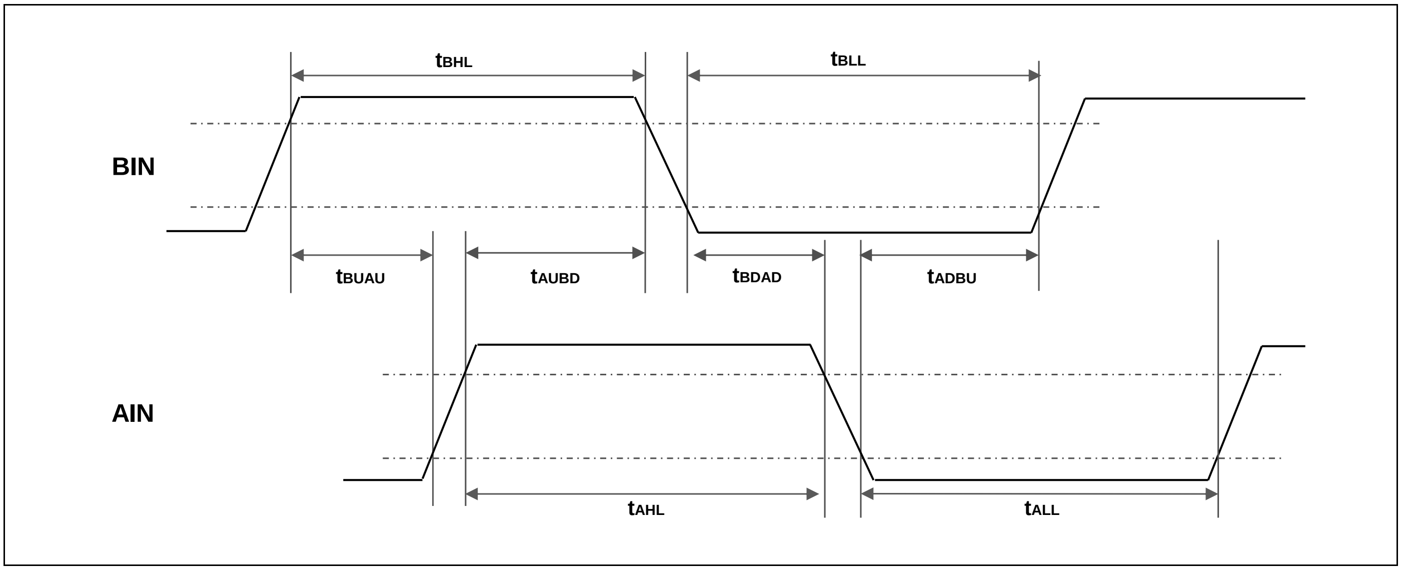
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

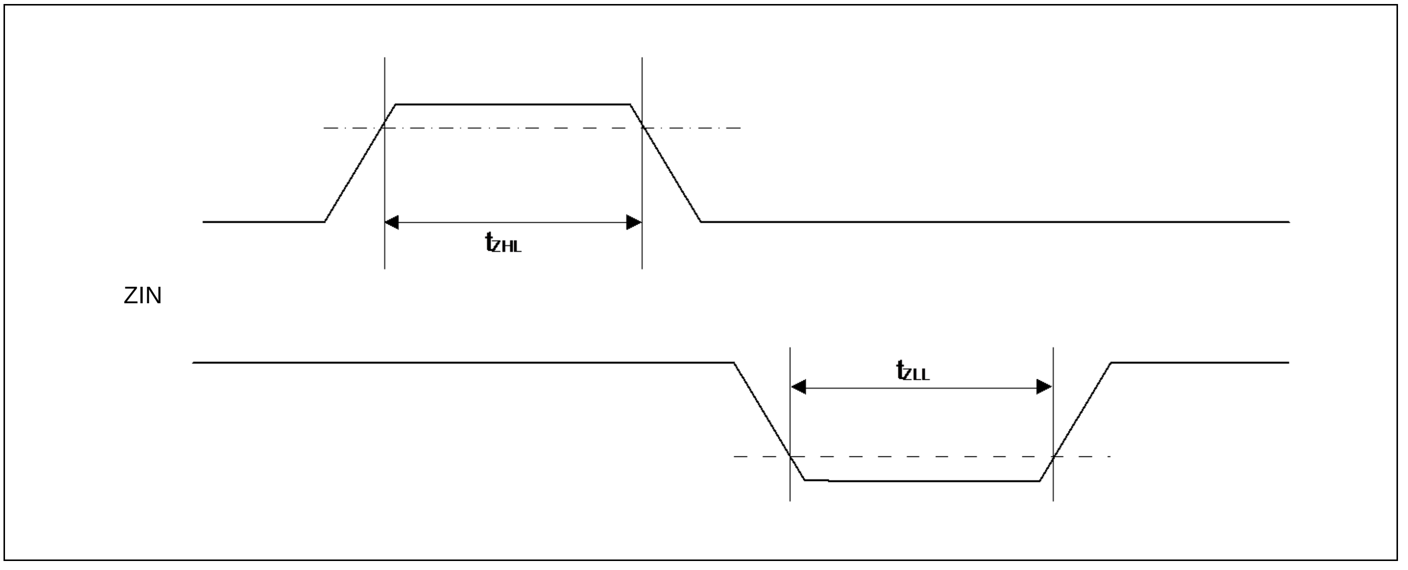
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

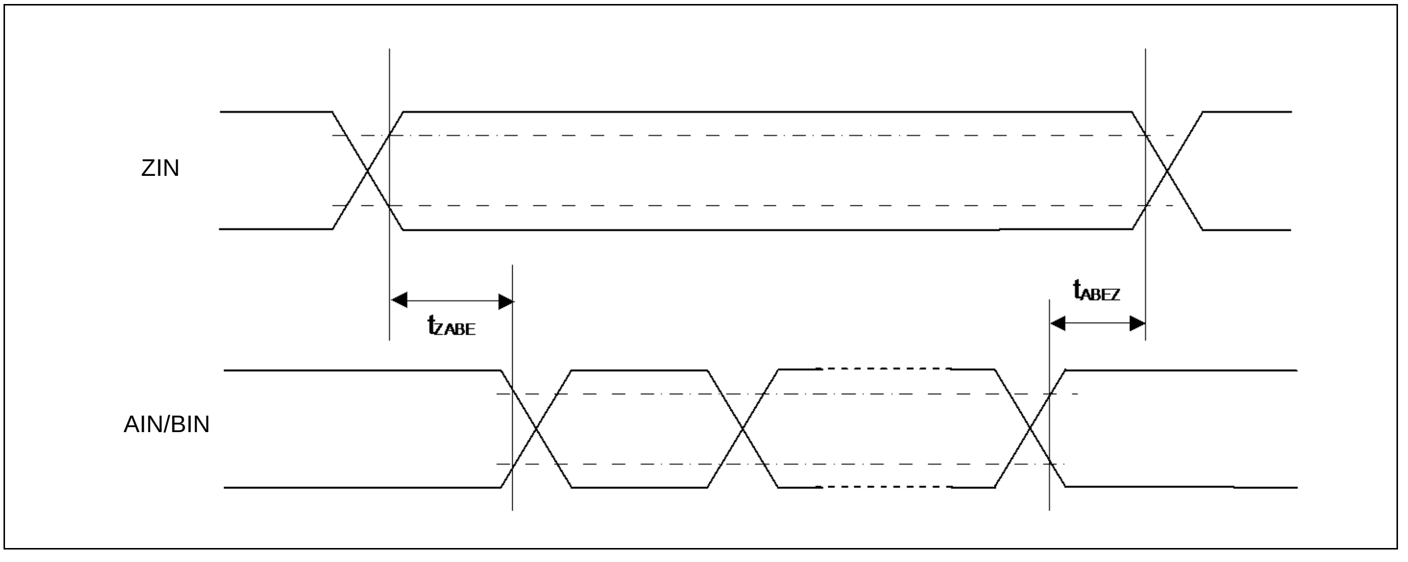
*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see "Block Diagram" in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.12 I^2C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_P/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	μs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	μs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	μs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	μs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	μs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

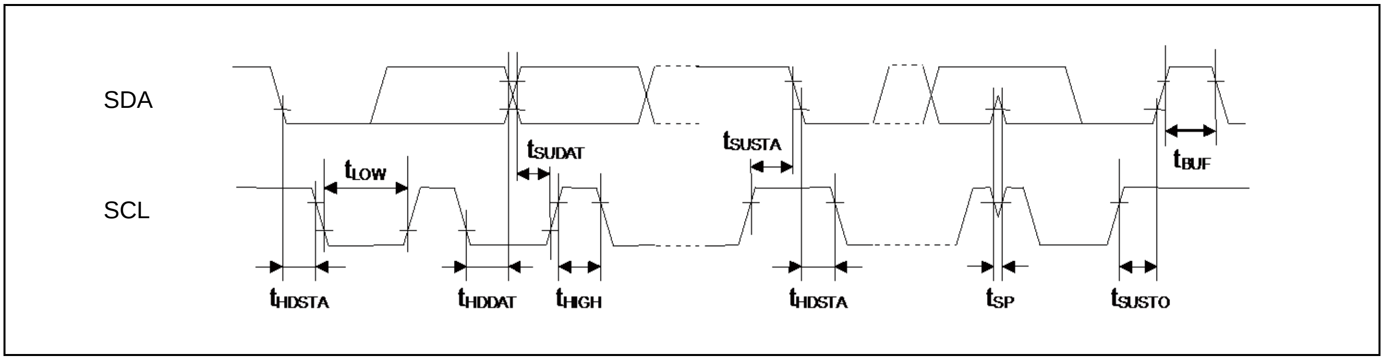
*1: R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.
V_P indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I^2C bus device can be used on a Standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "Block Diagram" in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more

To use Fast-mode, set the APB bus clock at 8 MHz or more.



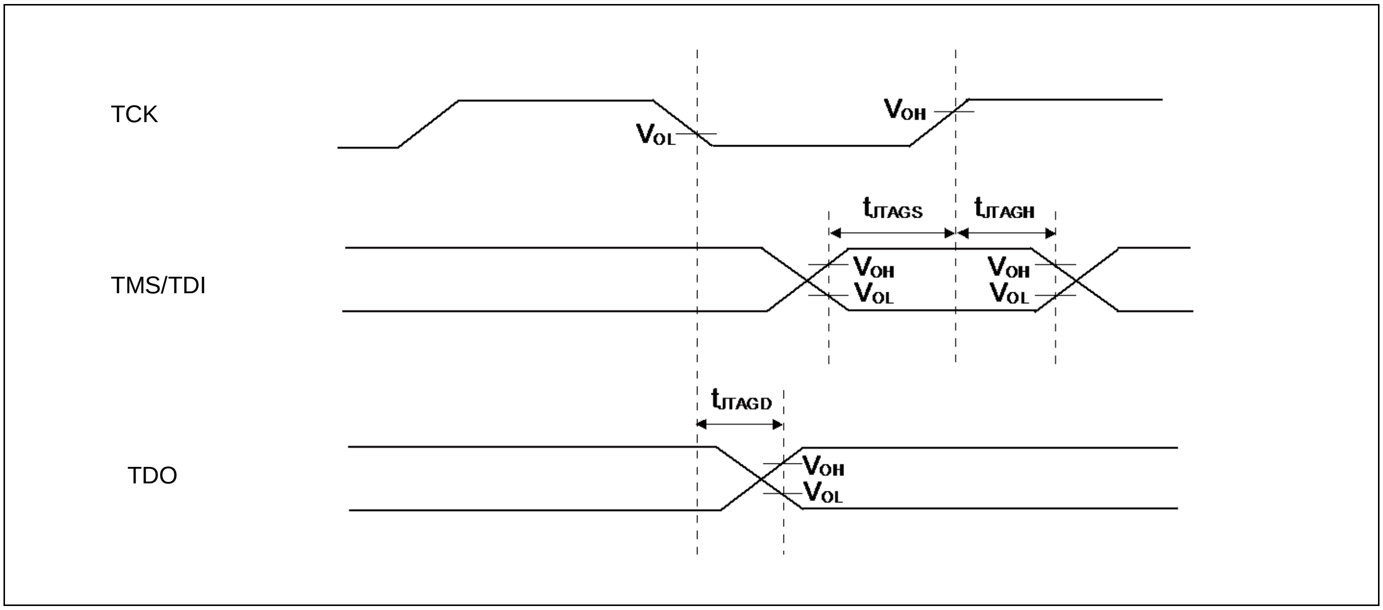
12.4.13 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V $V_{CC} < 4.5$ V	15	-	ns	
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V $V_{CC} < 4.5$ V	15	-	ns	
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

– *When the external load capacitance C_L = 30 pF.*



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.5	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 1.7	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 5	AVRH ± 15	mV	
Conversion time	-	-	0.8*1	-	-	μs	AV_{CC} ≧ 4.5 V
			1.0*1	-	-		AV_{CC} < 4.5 V
Sampling time*2	t_S	-	0.24	-	10	μs	AV_{CC} ≧ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	40	-	1000	ns	AV_{CC} ≧ 4.5 V
			50	-			AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	μs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistor	R_{AIN}	-	-	-	1.7	kΩ	AV_{CC} ≥ 4.5 V
					2.4		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AVSS	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

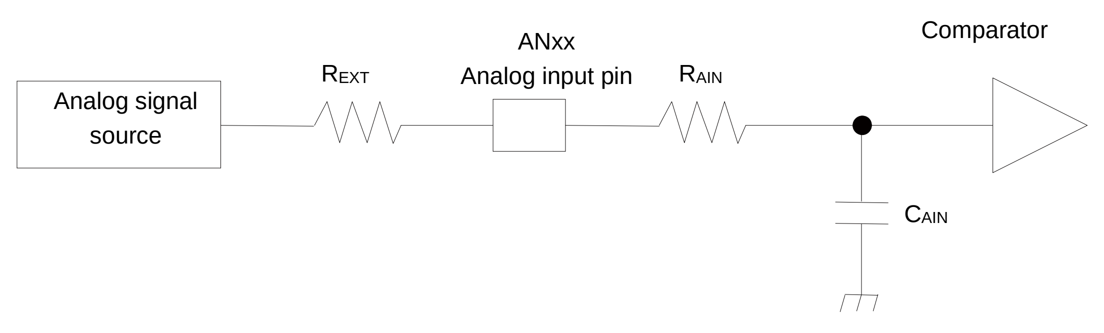
The condition of the minimum conversion time is the following.
AV_{CC} ≥ 4.5 V, HCLK=50 MHz sampling time: 240 ns, compare time: 560 ns.
AV_{CC} < 4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns
Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of the sampling time and compare clock cycle, see “Chapter 1-1: A/D Converter” in “FM3 Family Peripheral Manual Analog Macro Part”.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see “Block Diagram”.
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistor of A/D = 1.5 kΩ at $4.5\ V \leq AV_{CC} \leq 5.5\ V$ ch.0 to ch.7
Input resistor of A/D = 1.6 kΩ at $4.5\ V \leq AV_{CC} \leq 5.5\ V$ ch.8 to ch.15
Input resistor of A/D = 1.7 kΩ at $4.5\ V \leq AV_{CC} \leq 5.5\ V$ ch.16 to ch.26
Input resistor of A/D = 2.2 kΩ at $2.7\ V \leq AV_{CC} < 4.5\ V$ ch.0 to ch.7
Input resistor of A/D = 2.3 kΩ at $2.7\ V \leq AV_{CC} < 4.5\ V$ ch.8 to ch.15
Input resistor of A/D = 2.4 kΩ at $2.7\ V \leq AV_{CC} < 4.5\ V$ ch.16 to ch.26

C_{AIN}: Input capacity of A/D = 9.7 pF at $2.7\ V \leq AV_{CC} \leq 5.5\ V$

R_{EXT}: Output impedance of external circuit

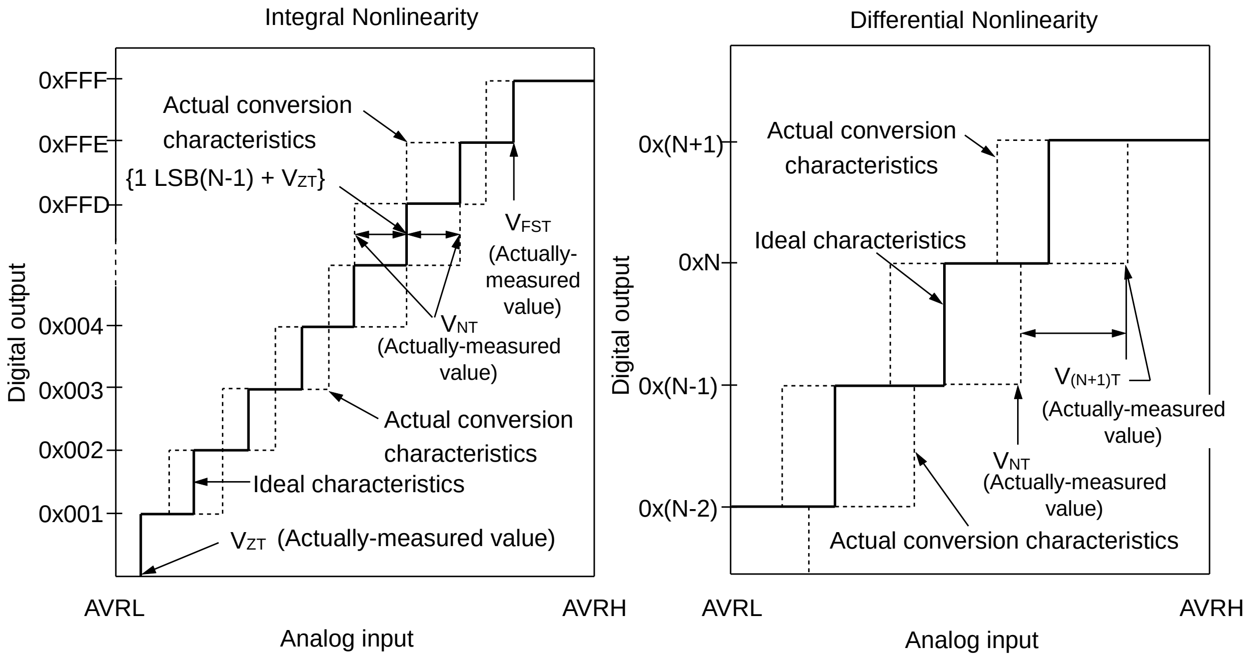
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

■Resolution:	Analog variation that is recognized by an A/D converter.
■Integral Nonlinearity:	Deviation of the line between the zero-transition point (0b000000000000 ←→ 0b000000000001) and the full-scale transition point (0b111111111110 ←→ 0b111111111111) from the actual conversion characteristics.
■Differential Nonlinearity:	Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{ZT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 10-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	t_{C20}		0.47	0.58	0.69	μs	Load 20 pF
	t_{C100}		2.37	2.90	3.43	μs	Load 100 pF
Integral Nonlinearity*1	INL		- 4.0	-	+ 4.0	LSB	
Differential Nonlinearity*1,*2	DNL		- 0.9	-	+ 0.9	LSB	
Output Voltage offset	V_{OFF}		-	-	10.0	mV	Code is 0x000
			- 20.0	-	+ 5.4	mV	Code is 0x3FF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	D/A stop
Output undefined period	t_R		-	-	70	ns	

*1: No-load

*2: Generates the max current by the CODE about 0x200

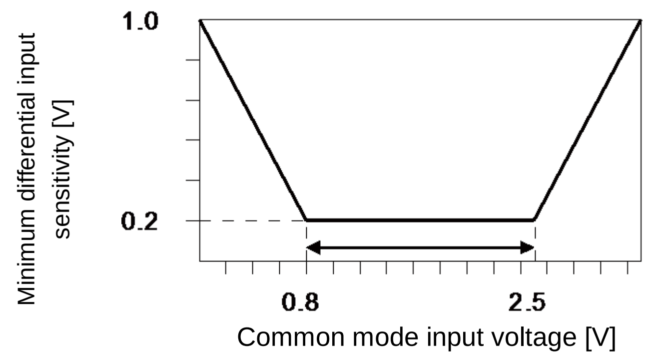
12.7 USB Characteristics

(V_{CC} = 2.7V to 5.5V, $USBV_{CC}$ = 3.0V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input charact-eristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output charact-eristics	Output H level voltage	V_{OH}		External pull-down resistor = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistor = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/ falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/ falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

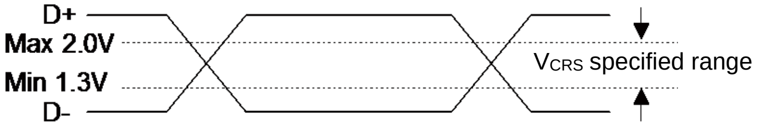
*1: The switching threshold voltage of the Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2: Use the differential-Receiver to receive the USB differential data signal.
The Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
The voltage range above is said to be the common mode input voltage range.

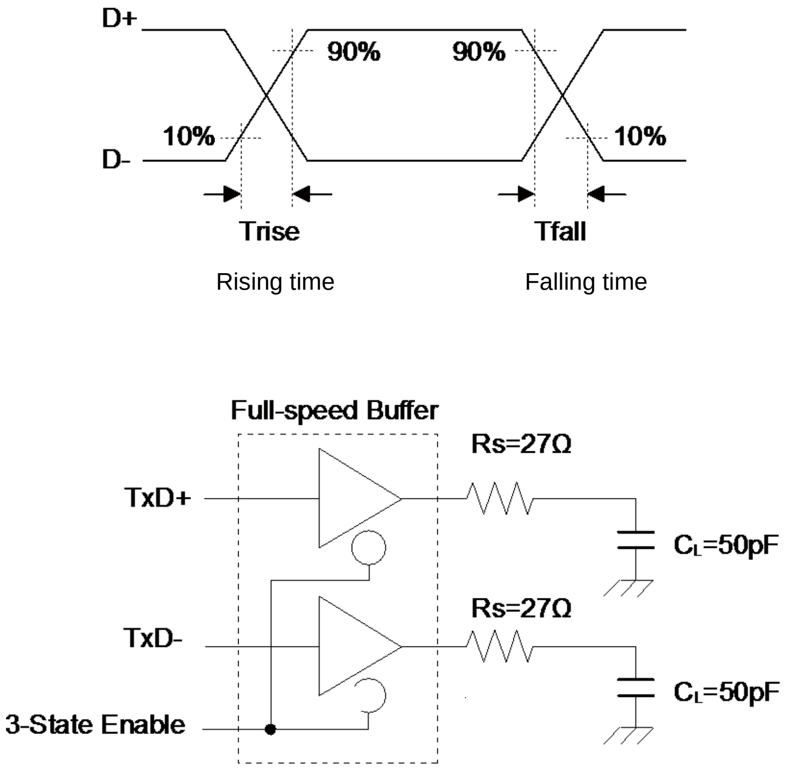


*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to ground and 15 kΩ load) at High-State (V_{OH}).

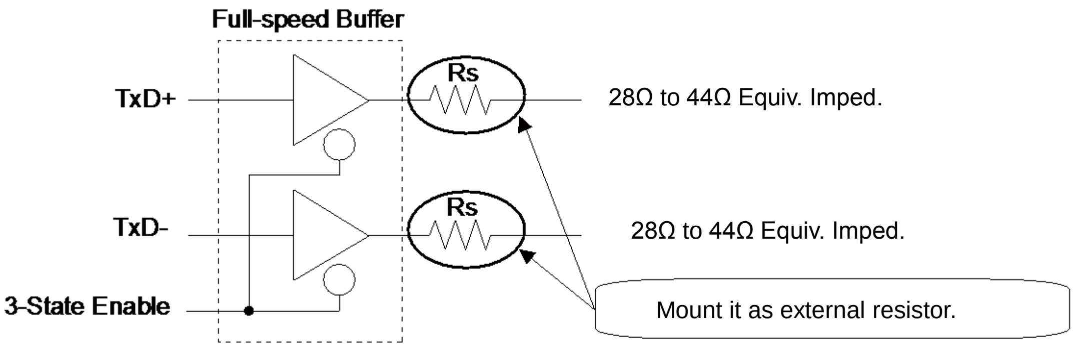
*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



*5: They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.

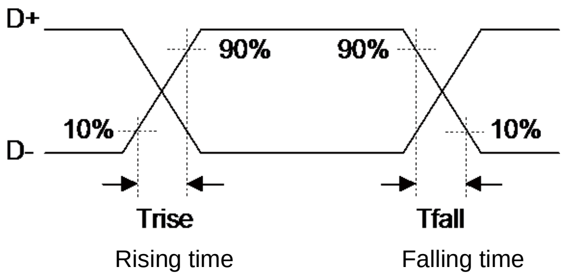


*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.



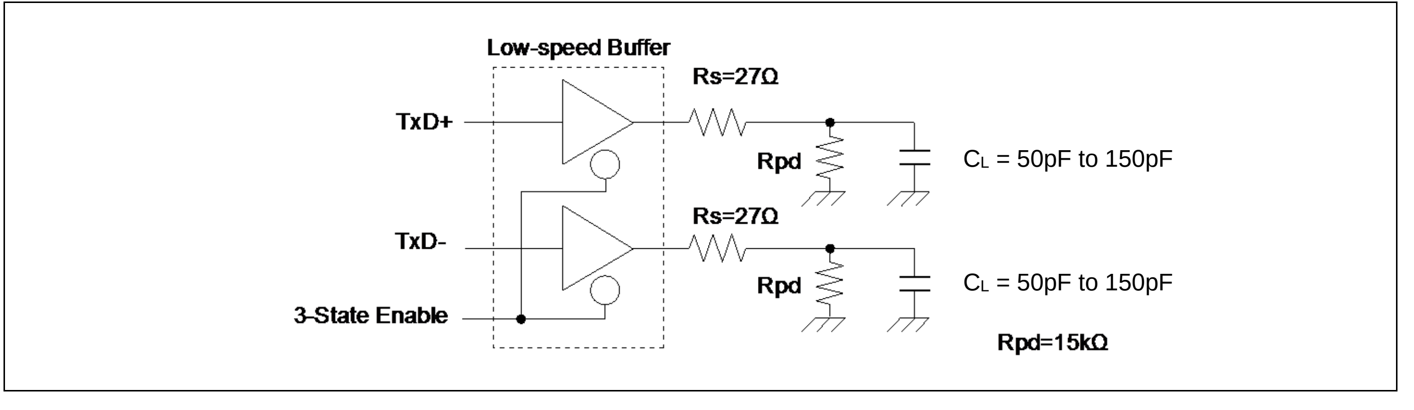
Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence".

*7: They indicate rising time (Trise) and falling time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.

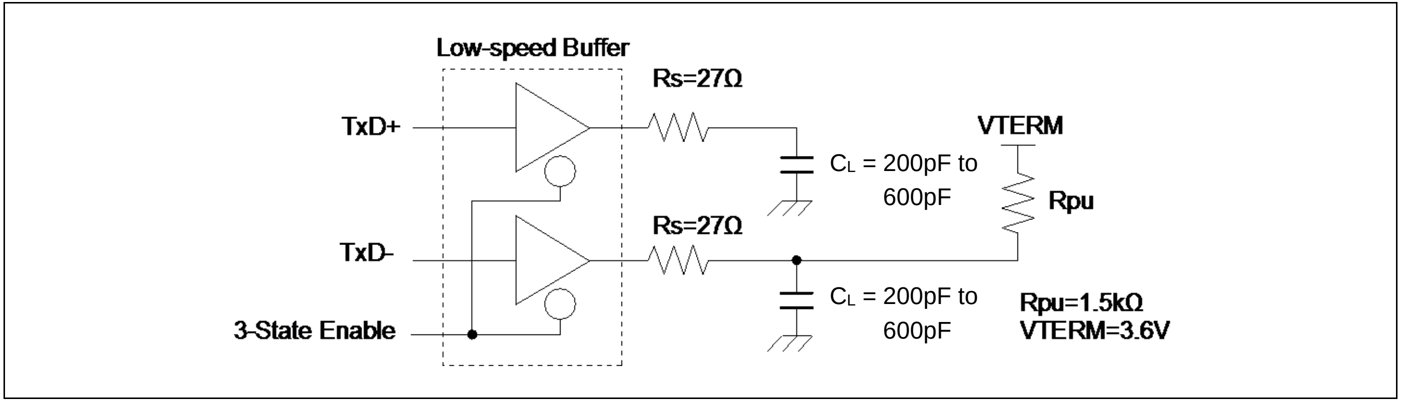


See “Low-Speed Load (Compliance Load)” for conditions of the external load.

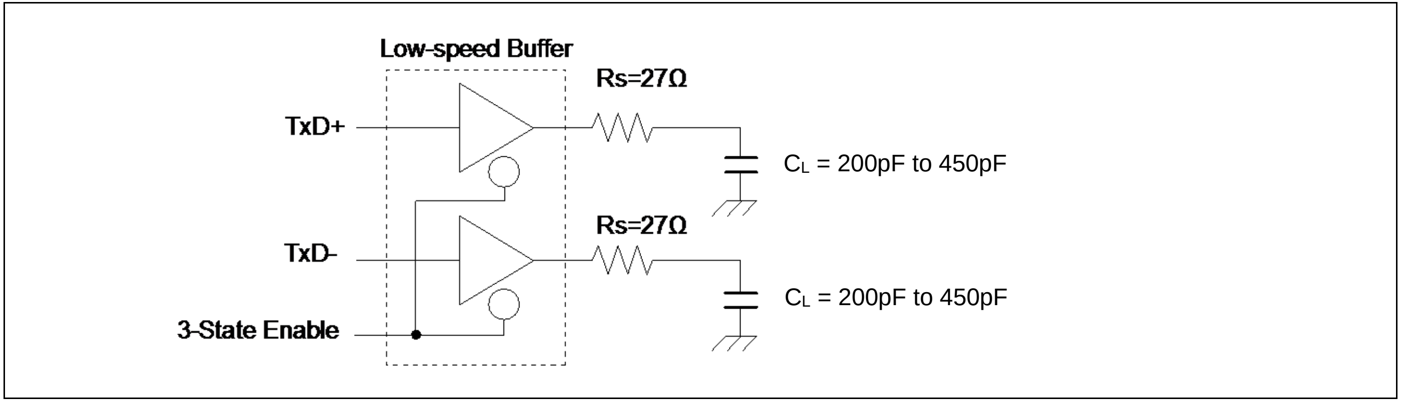
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1= 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1= 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*2	μs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	μs	

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to "00000" by Low-Voltage Detection Reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	μs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	μs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.9 Flash Memory Write/Erase Characteristics

12.9.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ	Max		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		16	310	μs	Not including system-level overhead time
Chip erase time		6.8	18	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.9.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.10Return Time from Low-Power Consumption Mode

12.10.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

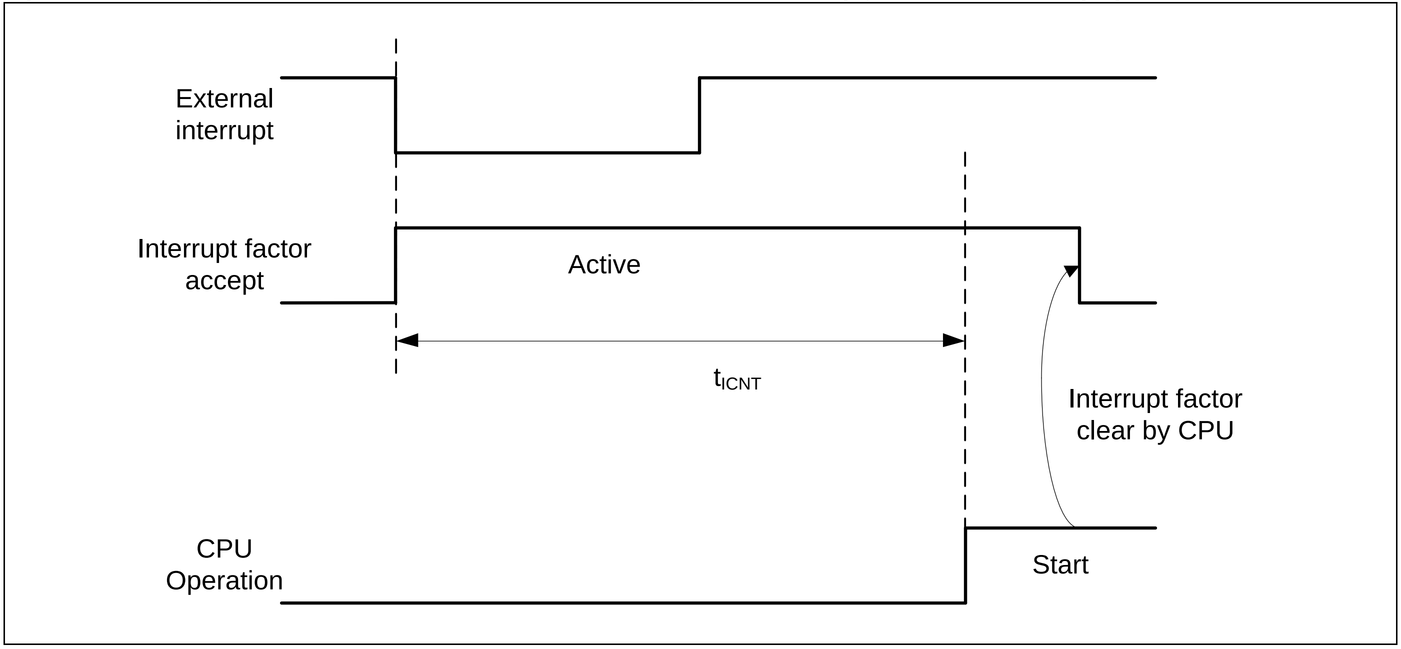
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	t_{CYCC}		μs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	μs	
Low-speed CR Timer mode		340	680	μs	
Sub Timer mode		680	860	μs	
RTC mode, Stop mode		268	503	μs	
Deep Standby RTC mode Deep Standby Stop mode		308	583	μs	When RAM is off
		268	503	μs	When RAM is on

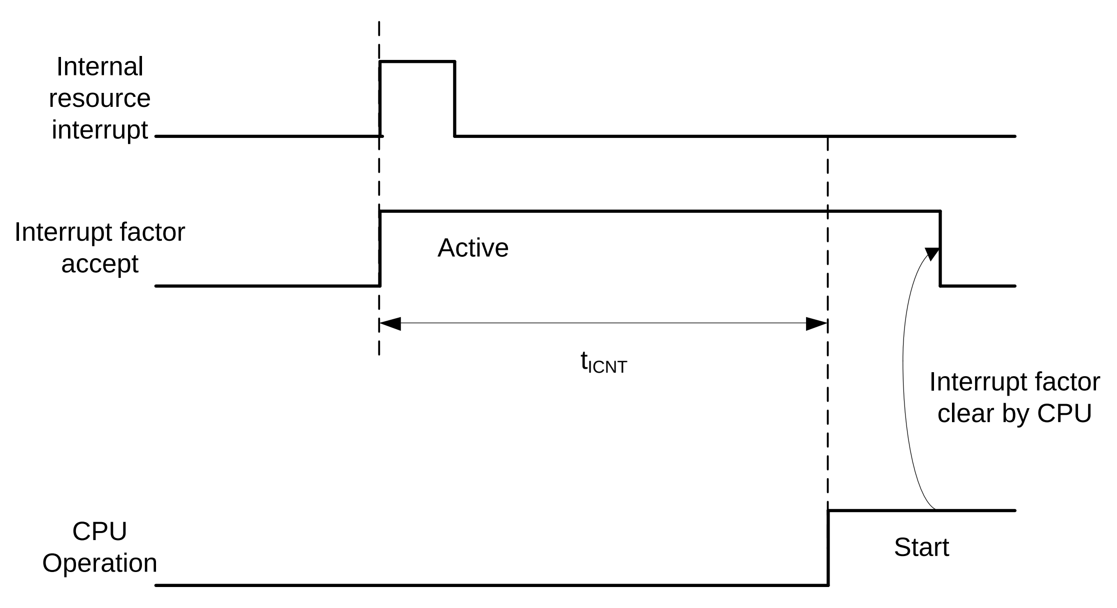
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
- *See “Chapter 6: Low Power Consumption Mode” and “Operations of Standby Modes” in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See “Chapter 6: Low Power Consumption Mode” in “FM3 Family Peripheral Manual”.*

12.10.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

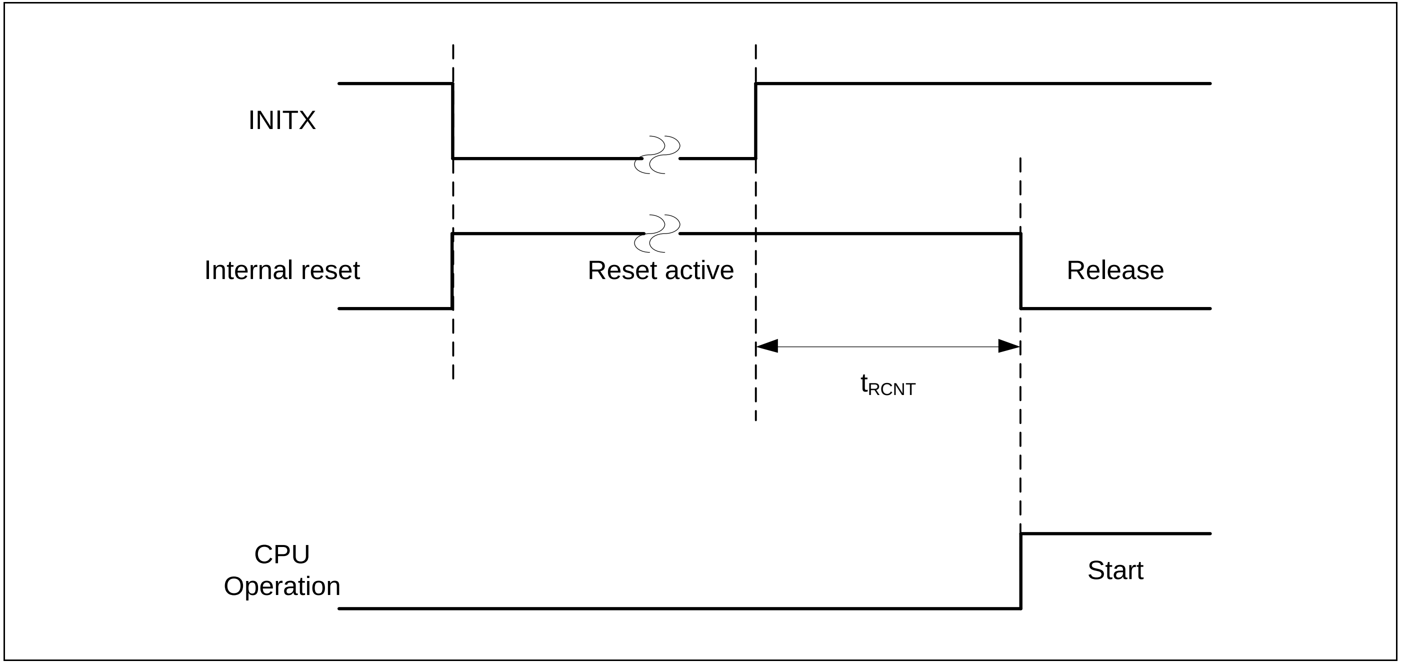
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

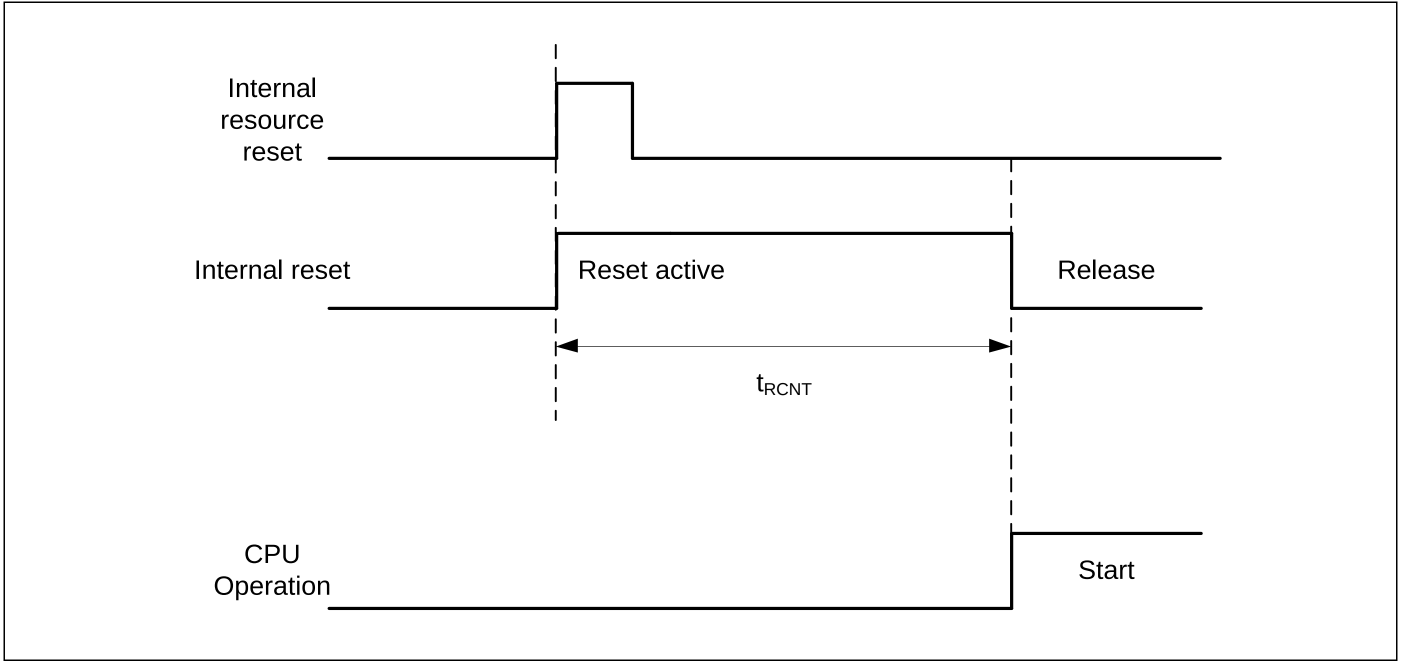
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	148	263	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		148	263	µs	
Low-speed CR Timer mode		248	463	µs	
Sub Timer mode		312	496	µs	
RTC mode, Stop mode		268	503	µs	
Deep Standby RTC mode Deep Standby Stop mode		308	583	µs	When RAM is off
		268	503	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

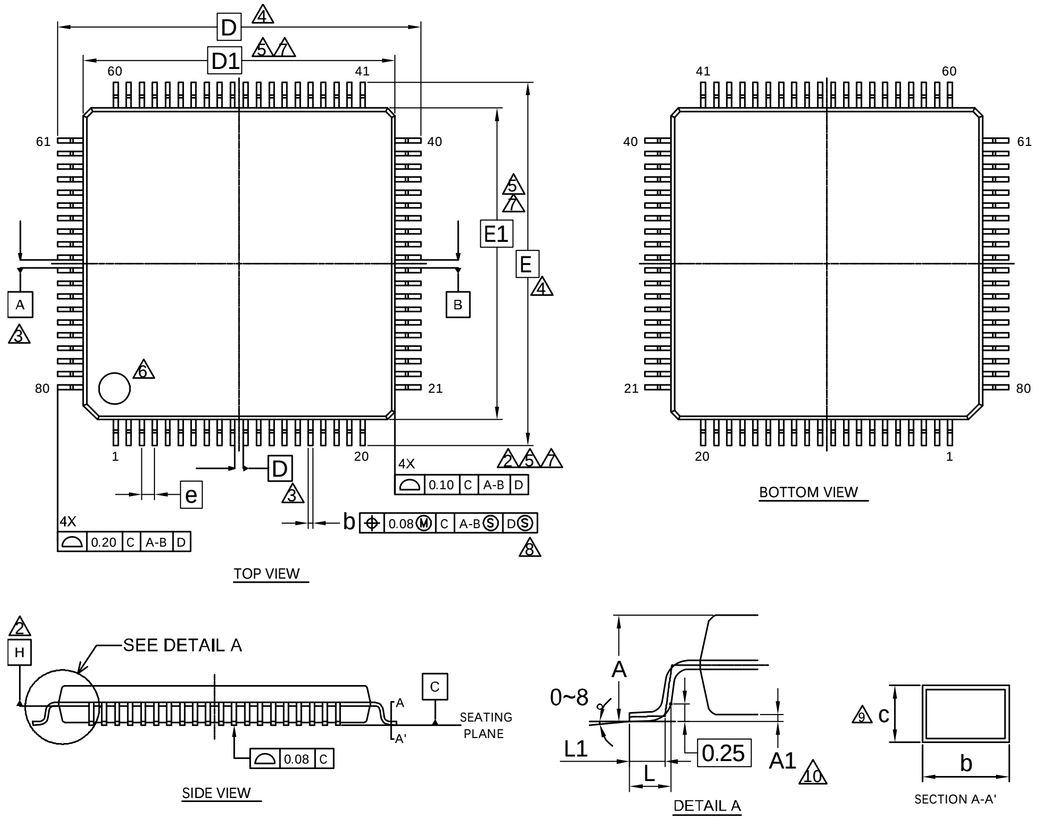
- *The return factor is different in each Low-Power consumption modes.*
- *See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7. Power-on Reset Timing in 12.4. AC Characteristics in 12.Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9BF321KQN-G-AVE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・QFN (0.5 mm pitch), 48-pin (VNA048)	Tray
MB9BF322KQN-G-AVE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324KQN-G-AVE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321KPMC-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP (0.5 mm pitch), 48-pin (LQA048)	
MB9BF322KPMC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324KPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321LQN-G-AVE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・QFN (0.5 mm pitch), 64-pin (VNC064)	
MB9BF322LQN-G-AVE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324LQN-G-AVE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321LPMC1-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP (0.5 mm pitch), 64-pin (LQD064)	
MB9BF322LPMC1-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324LPMC1-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321LPMC-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP (0.65 mm pitch), 64-pin (LQG064)	
MB9BF322LPMC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324LPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321MPMC-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP (0.5 mm pitch), 80-pin (LQH080)	
MB9BF322MPMC-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324MPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321MPMC1-G-JNE2	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・LQFP (0.65 mm pitch), 80-pin (LQJ080)	
MB9BF322MPMC1-G-JNE2	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324MPMC1-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		
MB9BF321MBGL-GE1	Main: 64 Kbyte Work: 32 Kbyte	16 Kbyte	Plastic・PFBGA (0.5 mm pitch), 96-pin (FDG096)	Tray
MB9BF322MBGL-GE1	Main: 128 Kbyte Work: 32 Kbyte	16 Kbyte		
MB9BF324MBGL-GE1	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte		

14. Package Dimensions

Package Type	Package Code
LQFP 80	LQH080



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)

△2 DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△3 DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△4 TO BE DETERMINED AT SEATING PLANE C.

△5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△6 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△7 REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△8 DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

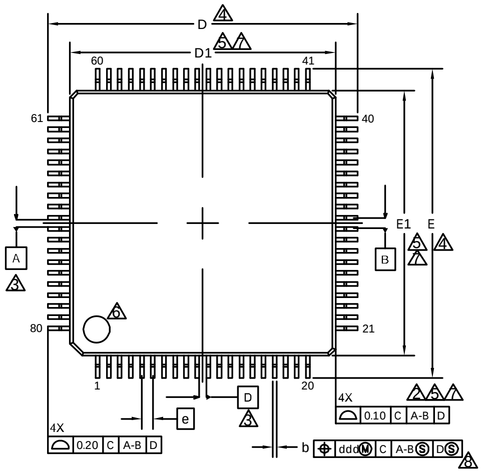
△9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△10 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

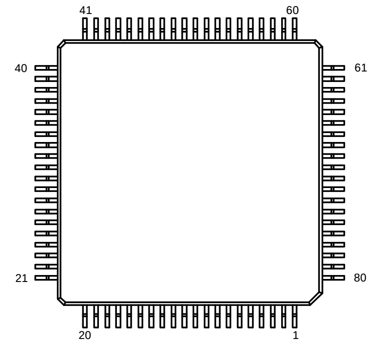
PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

002-11501 **

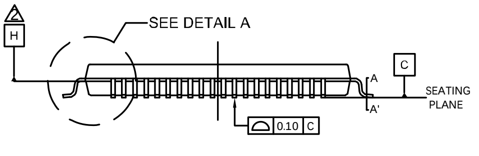
Package Type	Package Code
LQFP 80	LQJ080



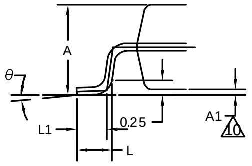
TOP VIEW



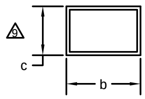
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.16	0.32	0.38
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△2 DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△3 DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△4 TO BE DETERMINED AT SEATING PLANE C.

△5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△6 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△7 REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△8 DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

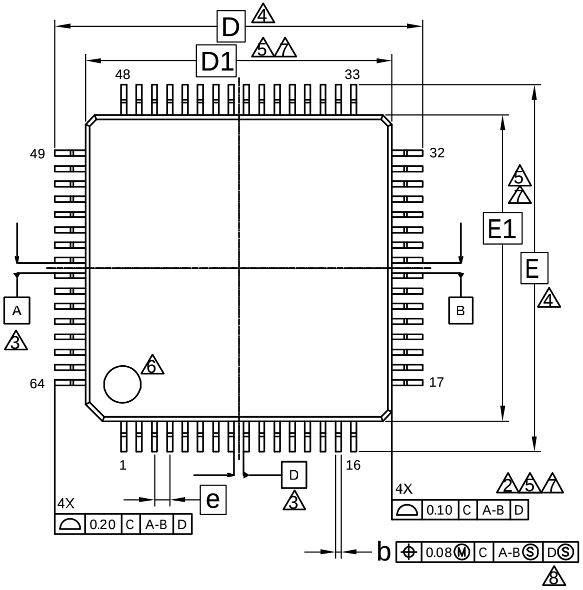
△9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△10 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

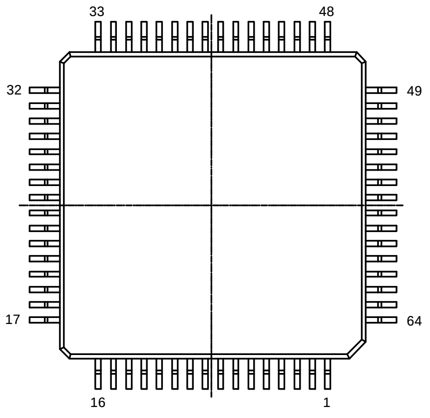
002-14043 **

PACKAGE OUTLINE, 80 LEAD LQFP
14.0X14.0X1.7 MM LQJ080 REV**

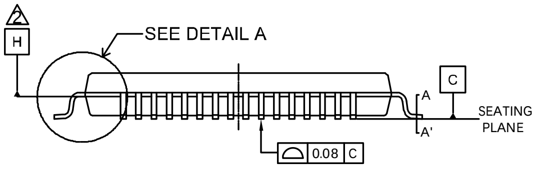
Package Type	Package Code
LQFP 64	LQD064



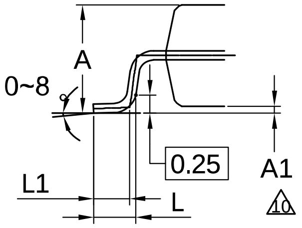
TOP VIEW



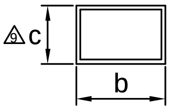
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△2 DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△3 DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△4 TO BE DETERMINED AT SEATING PLANE C.

△5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△6 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△7 REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△8 DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

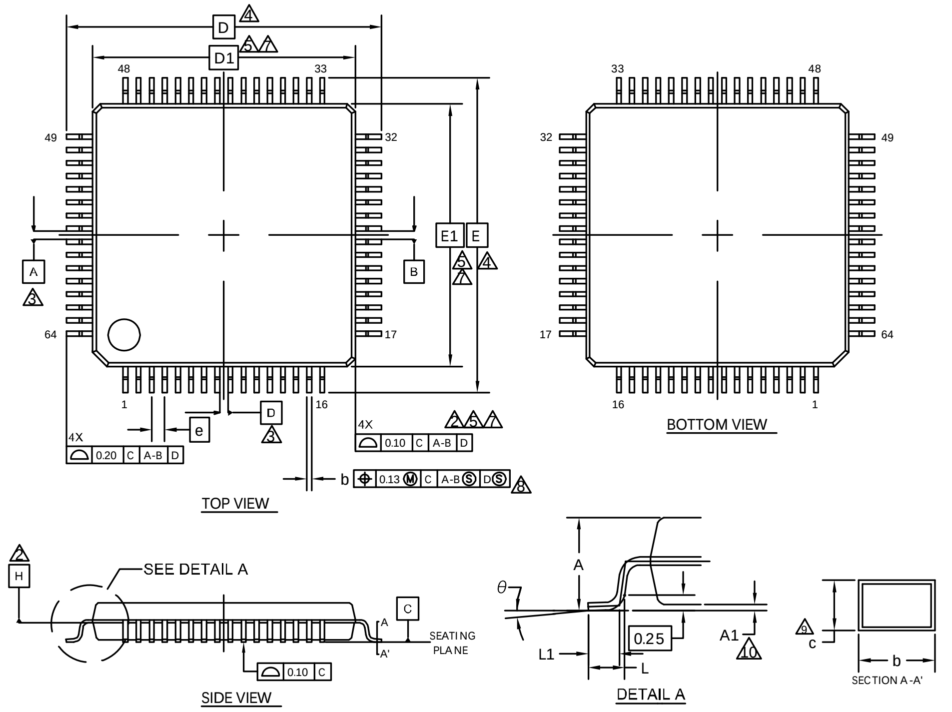
△9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△10 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Package Type	Package Code
LQFP 64	LQG064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△2 DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△3 DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△4 TO BE DETERMINED AT SEATING PLANE C.

△5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△6 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△7 REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△8 DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

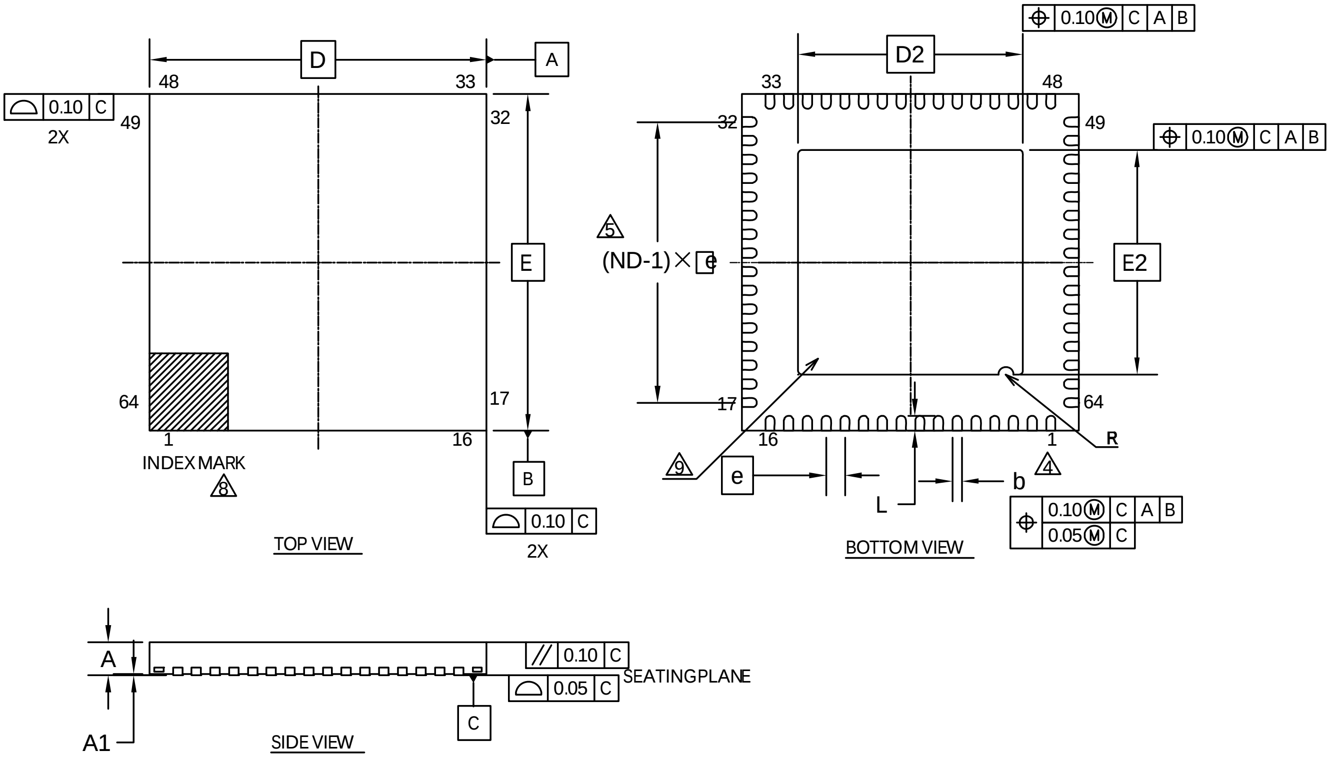
△9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△10 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

Package Type	Package Code
QFN 64	VNC064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	0.00	—	0.05
D	9.00 BSC		
E	9.00 BSC		
b	0.20	0.25	0.30
D2	6.00 BSC		
E2	6.00 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45
N	64		
ND	16		

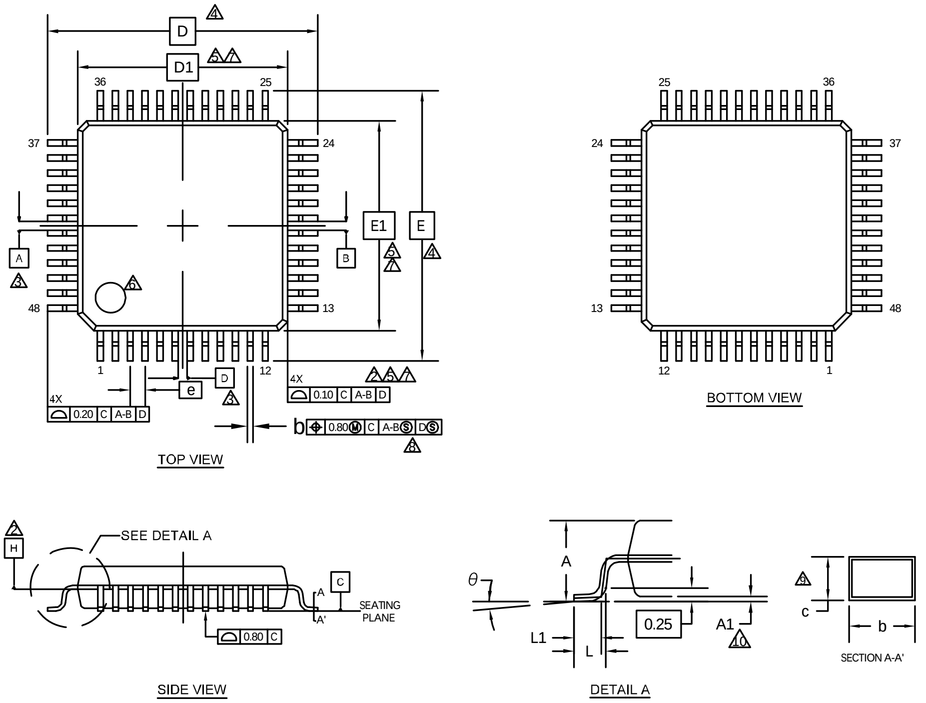
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

002-13234 **

PACKAGE OUTLINE, 64 LEAD QFN
9.0X9.0X0.9 MM VNC064 6.0X6.0 MM EPAD (SAWN) Rev*.*

Package Type	Package Code
LQFP 48	LQA048



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△2 DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△3 DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△4 TO BE DETERMINED AT SEATING PLANE C.

△5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△6 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△7 REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△8 DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

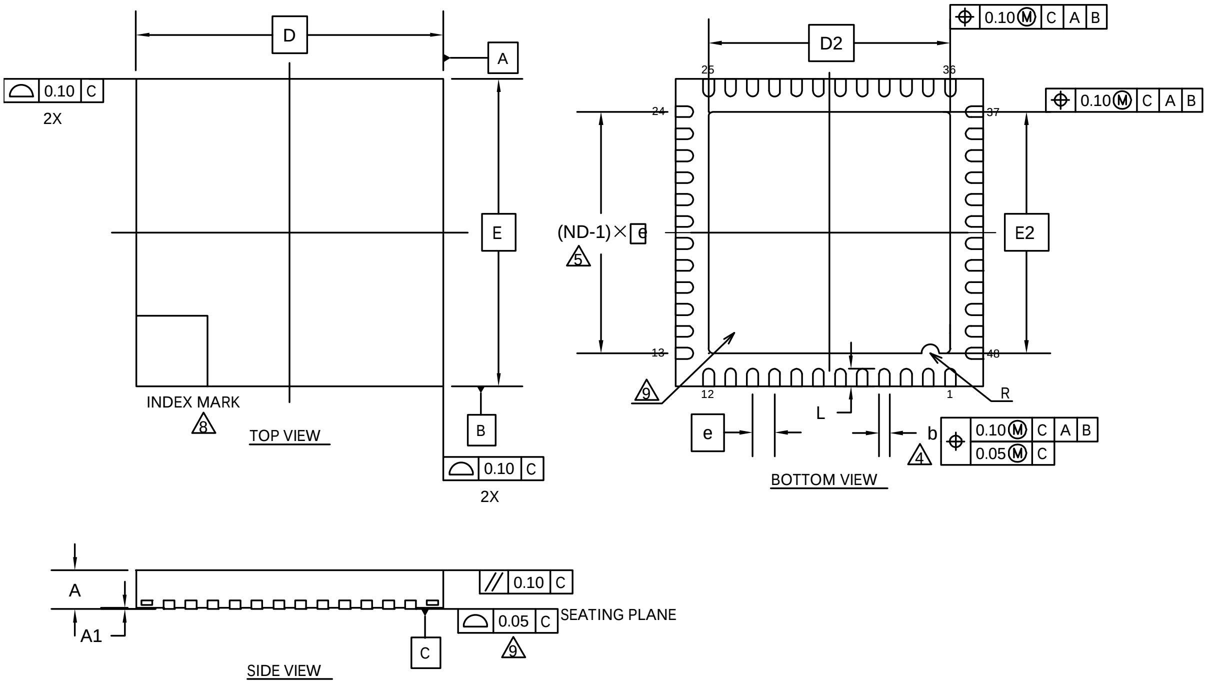
△9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△10 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Package Type	Package Code
QFN 48	VNA048



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	0.00	—	0.05
D	7.00 BSC		
E	7.00 BSC		
b	0.20	0.25	0.30
D2	5.50 BSC		
E2	5.50 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45

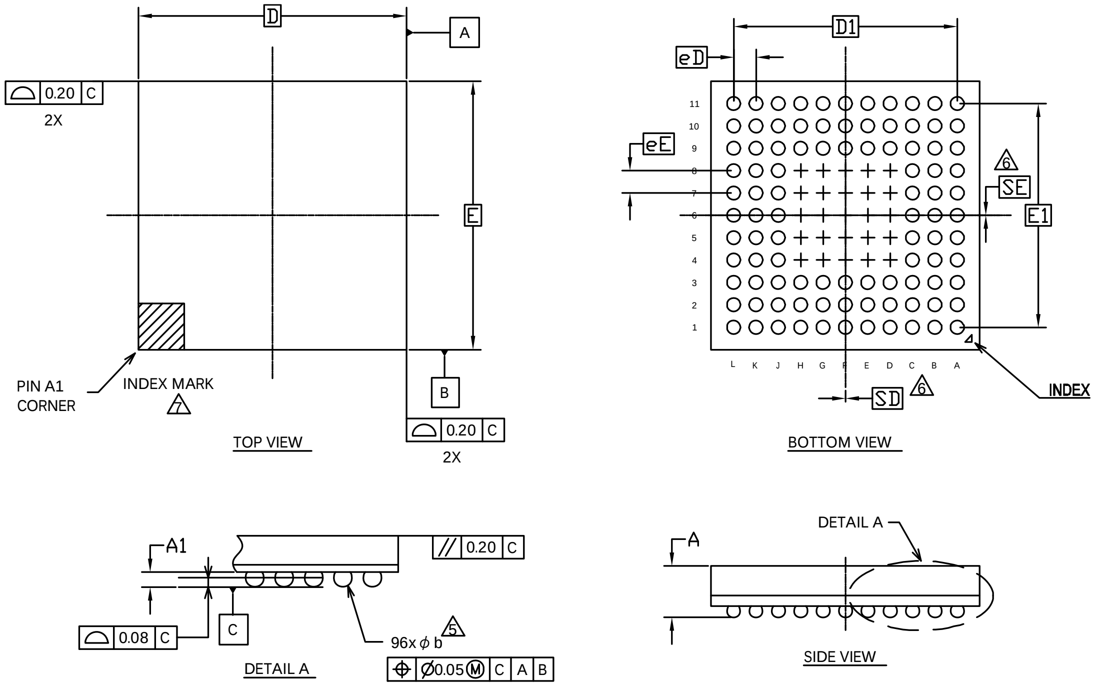
NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPEC IFICATIONNO . REF : N/A

002-15528 **

PACKAGE OUTLINE, 48 LEAD QFN
7.0X7.0X0.9 MMVNA048 5.5X5.5 MMEPAD(SAWN) REV**

Package Type	Package Code
FBGA 96	FDG096



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.30
A1	0.15	0.25	0.35
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	96		
∅ b	0.20	0.30	0.40
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13224 **

PACKAGE OUTLINE, 96 BALL FBGA
6.0X6.0X1.3 MM FDG096 REV**

15. Major Changes

Spansion Publication Number: DS706-00049

Page	Section	Change Results
Revision 1.0		
-	-	Preliminary → Data Sheet
3	Features A/D Converter (Max 26channels)	Revised the conversion time: 1.0μs → 0.8μs
6	Uniqueid	Added the "Unique ID".
7	Product Lineup Function	Added the "Unique ID".
16 to 18	List Of Pin Functions List Of Pin Numbers	Corrected the I/O circuit type. Corrected the Pin state type.
33	List Of Pin Functions	Corrected the Pin function.
39	I/O Circuit Type	Added the "Type: L".
46	Block Diagram	Corrected the figure. - TIOA: input → input/output - TIOB: output → input
55	Electrical Characteristics 1. Absolute Maximum Ratings	Revised the value of "TBD".
57	2. Recommended Operating Conditions	Revised the Condition of "Operating temperature".
58, 59	3. Dc Characteristics (1) Current Rating	Revised the value of "TBD". Added "Flash memory write/erase current".
62	4. Ac Characteristics (3) Built-In Cr Oscillation Characteristics	Revised the Condition. Revised the footnote.
63	(4-2) Operating Conditions Of Main PLL (In The Case Of Using Built-In High-Speed CR For Input Clock Of Main PLL)	Revised the value of "TBD".
79	5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	Deleted "(Preliminary value)". Revised the conversion time. Min: 1.0μs → 0.8μs Revised the value of "Compare clock cycle ($AV_{CC} \geq 4.5V$)". Min: 50ns → 40ns Revised the footnote.
82	6. 10-Bit D/A Converter	Deleted "(Preliminary value)".
87	8. Low-Voltage Detection Characteristics	Revised the value of "TBD".
88	9. Mainflash Memory Write/Erase Characteristics	Revised the value of "TBD". Revised the value of "Sector erase time". - Large Sector Typ: 1.065s → 1.1s - Small Sector Typ: 0.606s → 0.3s Revised the value of "Chip erase time". Typ: 9.11s → 6.8s Deleted "(targeted value)".
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	Features On-Chip Memories [Flash Memory]	Revised the features of Dual operation Flash memory
	USB Interface [USB Function]	Added the size of each endpoint.
3	Multi-Function Serial Interface [I^2C]	Corrected the mode. High speed mode → Fast mode
4	General-Purpose I/O Port	Revised the features of 5V tolerant I/O.
	Multi-Function Timer	Corrected the number of A/D activating compare channels. 3ch. → 2ch.

Page	Section	Change Results
7	Product Lineup Function	Corrected the number of A/D activating compare channels. 3ch. → 2ch. Revised Built-in CR . High-speed: 4MHz(± 2%) → 4MHz Low-speed: 100kHz(Typ) → 100kHz
8		Revised the footnote.
21	List Of Pin Functions List Of Pin Numbers	Corrected the pin number of ZIN1_1.
24	List Of Pin Functions	Corrected the pin number of ADTG_2.
29		Corrected pin numbers of SIN0_1 and SOT0_1.
31		Corrected the pin number of DTTI0X_2.
37	I/O Circuit Type	Corrected the I/O circuit figure. TYPE H : GPIO Digital input → GPIO Digital output
44	Handling Devices Sub Crystal Oscillator	Added the descriptions.
47	Block Diagram	Corrected the figure. -A/D Activation Compare: 3ch → 2ch
49	Memory Map Memory Map (2)	Added the explanatory note.
54	Pin Status In Each Cpu State List Of Pin Status	Added the pin function of selected Analog output about type L.
55		Corrected the footnote. Sub CR timer→ Low-speed CR tim
58	Electrical Characteristics 2. Recommended Operating Conditions	Added the note and footnote. Corrected the value of Analog reference voltage “AVRH”. Min.: AVss → 2.7
59	3. Dc Characteristics (1) Current Rating	Added notes and footnotes. Added the remarks of Icc. Added the frequency of main clock crystal oscillator in remarks
63	4. Ac Characteristics (2) Sub Clock Input Characteristics	Added the footnote.
64	(3) Built-In CR Oscillation Characteristics Built-In High-Speed CR	Added "Frequency stabilization time" Added notes and footnotes.
66	(6) Power-On Reset Timing	Added "Timing until releasing Power-on reset" Added the timing chart
68	(8) Csio Timing	Corrected the title. UART Timing → CSIO Timing Corrected the notefoot. UART → Multi-function serial
70,72,74		Corrected the notefoot. UART → Multi-function serial
79	(11) I^{2}c Timing	Revised the Condition. Revised the footnote.
81	5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	Changed the name of parameter. •Non Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity Changed the Symbol. Of Zero transition voltage. V_{0T} → V_{ZT} Changed the pin name. AN00 to AN26 → ANxx Corrected the value of $V_{0T,}$ $V_{FST,}$ Ts, Tstt, and reference voltage. Revises footnotes.
82		Change the figure. AN00 to AN26 → ANxx
83	Difinition Of 12-Bit A/D Converter Terms	•Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity V_{0T} → V_{ZT}
84	6. 10-Bit D/A Converter Electrical Characteristics For The D/A Converter	•Revised the remark of IDDA. D/A operation → D/A 1unit operation Changed the name of parameter. •Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity

Page	Section	Change Results
89	8. Low-Voltage Detection Characteristics (1) Low-Voltage Detection Reset	Corrected the condition and the value. Added the note and the footnote. Added “LVD detection delay time”.
90	(2) Interrupt Of Low-Voltage Detection	Corrected the condition and the value. Added “LVD detection delay time”.
91	9. Flash Memory Write/Erase Characteristics	Changed the title of Chapter. Main Flash Memory Write/Erase Characteristics → Flash Memory Write/Erase Characteristics
92	10. Return Time Low-Power Consumption Mode	Added the Chapter “Return Time from Low-Power Consumption mode”.
Revision 3.0		
2	Features □Usb Interface	Added the description of Pll For USB
36, 37	I/O Circuit Type	Added about +B Input
49	Memory Map · Memory Map(2)	Added the summary of Flash Memory Sector and the note
54	PIN STATUS IN EACH CPU STAE · List Of Pin Status	Changed the Pin Status of I-type
56, 57	Electrical Characteristics 1. Absolute Maximum Ratings	· Added the clamp maximum current · Added about +B Input
59-61	Electrical Characteristics 3. DC Characteristics (1) Current Rating	· Changed the table format · Added Main TIMER mode current · Moved A/D converter current · Moved D/A converter current
66	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions Of Main And USB PLL (4-2) Operating Conditions Of Main PLL	· Added the figure of Main PLL connection and USB PLL connection
69-76	Electrical Characteristics 4. Ac Characteristics (7) Csio/Uart Timing	· Modified from UART timing to Csio/UART timing · Changed from Internal Shift Clock Operation to Master mode · Changed from External Shift Clock Operation to Slave mode
77	Electrical Characteristics 4. Ac Characteristics (9) External Input Timing	Added Input Pulse Width of Wkupx Pin
82	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral nonlinearity, Differential nonlinearity, Zero transition voltage and Full-scale transition voltage · Added conversion time at Avcc < 4.5V
97, 98	Ordering Information	Change to full part number

Note: Please see “Document History” about later revised information.

Document History

Document Title: MB9B320M Series 32-bit Arm® Cortex®-M3, FM3 Microcontroller
Document Number: 002-05652

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TOYO	09/13/2012	Migrated to Cypress and assigned document number 002-05652. No change to document contents or format.
*A	5166569	TOYO	03/08/2016	Updated to Cypress format.
*B	5653470	HTER	03/09/2017	・ Modified RTC description in “Features, Real-Time Clock(RTC)”. Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function. (Page 3) ・ Updated Package code and dimensions as follows (Page 8-14, 95-103) - FPT-48P-M49 -> LQA048 - LCC-48P-M73 -> VNA048 - FPT-64P-M38 -> LQD064 - FPT-64P-M39 -> LQG064 - LCC-64P-M24 -> VNC064 - FPT-80P-M37 -> LQH080 - FPT-80P-M40 -> LQJ080 - BGA-96P-M07 -> FDG096 ・ Added Notes for JTAG. (Page 32) ・ Updated “12.4.7 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(Tr) [ms]” to “Power ramp rate(dV/dt) [mV/us]” and add some comments. (Page 65) ・ Added the Baud rate spec in “12.4.9 CSIO/UART Timing”.(Page 67-73) ・ Corrected the erroneous descriptions as follows. - “USB Function” -> “USB Device” (Page 1, 7, 31, 44) - “J-TAG” -> “JTAG” (Page 24) “Analog port input current” -> “Analog port input leak current” (Page 80)
*C	5787206	YSAT	06/28/2017	Adapted new Cypress logo
*D	6064687	HUAL	02/09/2018	Updated the Sales information and legal

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