CY7C135
CY7C135A
CY7C1342

4K x 8 Dual-Port Static RAM and 4K x 8 Dual-Port SRAM with Semaphores

Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 4K x 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power: I_{CC} = 160 mA (max)
- Fully asynchronous operation
- Automatic power down
- Semaphores included on the 7C1342 to permit software handshaking between ports
- Available in 52-pin plastic leaded chip carrier (PLCC)
- Pb-free packages available

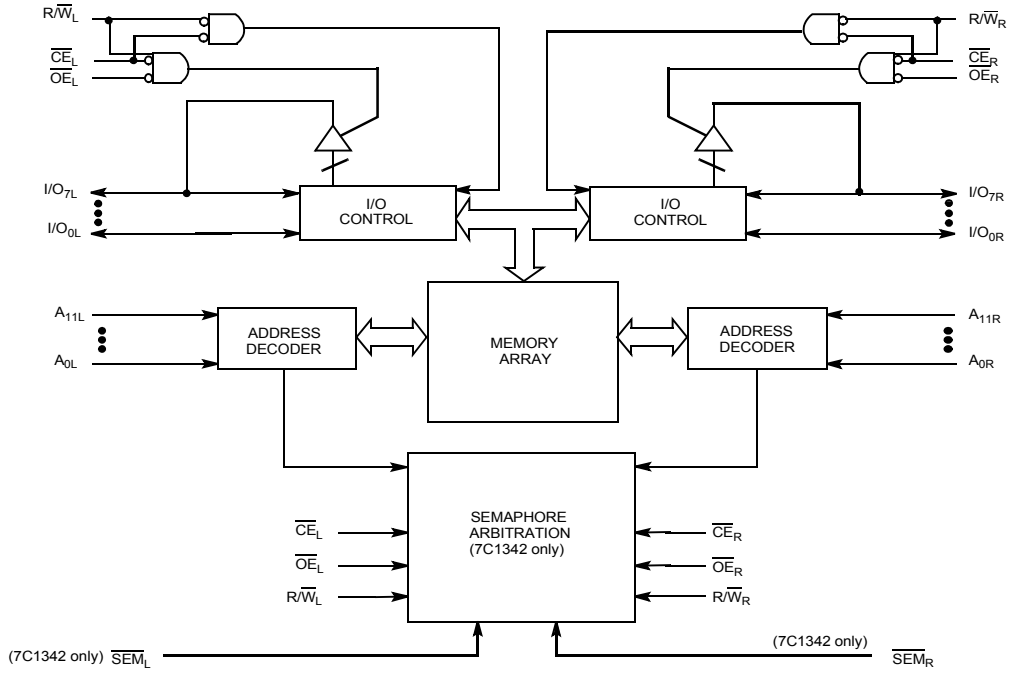
Functional Description

The CY7C135/135A[1] and CY7C1342 are high speed CMOS 4K x 8 dual-port static RAMs. The CY7C1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). The CY7C135/135A is suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7C1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7C1342 only).

The CY7C135/135A and CY7C1342 are available in 52-pin PLCC.

Logic Block Diagram



Note
1. CY7C135 and CY7C135A are functionally identical

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Selection Guide

Parameter		7C135-15 7C1342-15	7C135-20 7C1342-20	7C135/135A-25 7C1342-25	7C135-35 7C1342-35	7C135-55 7C1342-55	Unit
Maximum access time		15	20	25	35	55	ns
Maximum operating current	Commercial	220	190	180	160	160	mA
Maximum standby current for I_{SB1}	Commercial	60	50	40	30	30	mA

Pin Configurations

Figure 1. Pin Diagram - CY7C135/135A (Top View)

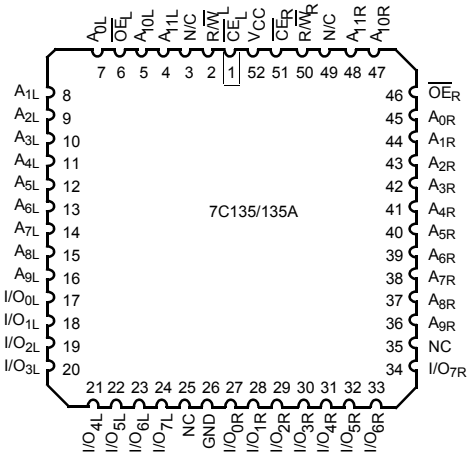
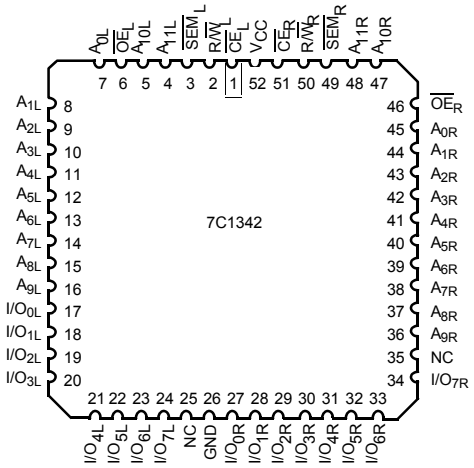


Figure 2. Pin Diagram - CY7C1342 (Top View)



Pin Definitions

Left Port	Right Port	Description
A_{0L-11L}	A_{0R-11R}	Address lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7C1342 only)	$\overline{SEM}_R$ (CY7C1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines determines which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

[+] Feedback

Maximum Ratings[2]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential (Pin 48 to Pin 24) ..... –0.5 V to +7.0 V

DC voltage applied to outputs in High Z state ..... –0.5 V to +7.0 V

DC input voltage[3] ..... –3.0 V to +7.0 V

Static discharge voltage ..... > 2001 V (per MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C135-15 7C1342-15		7C135-20 7C1342-20		7C135-25 7C135A-25 7C1342-25		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	–	2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min., I_{OL} = 4.0 mA		–	0.4	–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage			2.2	–	2.2	–	2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	–	0.8	–	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output leakage current	Outputs disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l	–	220	–	190	–	180	mA
			Ind.	–	–	–	–	–	190	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l	–	60	–	50	–	40	mA
			Ind.	–	–	–	–	–	50	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l	–	130	–	120	–	110	mA
			Ind.	–	–	–		–	120	
I_{SB3}	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l	–	15	–	15	–	15	mA
			Ind.	–	–	–	–	–	30	
I_{SB4}	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active port outputs, f = f_{MAX}[4]	Com'l	–	125		115		100	mA
			Ind.	–	–	–	–	–	115	

Notes
2. The voltage on any input or I/O pin cannot exceed the power pin during power up.
3. Pulse width < 20 ns.
4. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

[+] Feedback

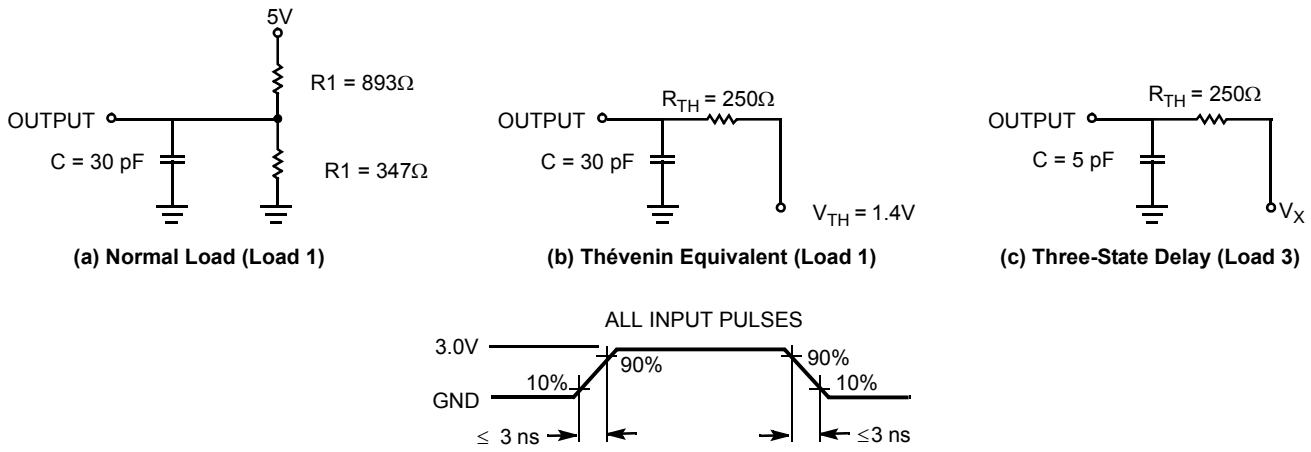
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C135-35 7C1342-35 Min	7C135-35 7C1342-35 Max	7C135-55 7C1342-55 Min	7C135-55 7C1342-55 Max	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min., I_{OL} = 4.0 mA		–	0.4	–	0.4	V
V_{IH}				2.2	–	2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	–	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output leakage current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	µA
I_{CC}	Operating current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l	–	160	–	160	mA
		V_{CC} = Max., I_{OUT} = 0 mA	Ind.	–	180	–	180	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l	–	30	–	30	mA
			Ind.	–	40	–	40	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l	–	100	–	100	mA
			Ind.	–	110	–	110	
I_{SB3}	Standby current (Both ports CMOS levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Com'l	–	15	–	15	mA
			Ind.	–	30	–	30	
I_{SB4}	Standby current (One port CMOS level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active port outputs, f = f_{MAX}[5]	Com'l	–	90	–	90	mA
			Ind.	–	100	–	100	

Capacitance[6]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load 1) (b) Thévenin Equivalent (Load 1) (c) Three-State Delay (Load 3)

Notes
5. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
6. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C135-15 7C1342-15		7C135-20 7C1342-20		7C135-25 7C135A-25 7C1342-25		7C135-35 7C1342-35		7C135-55 7C1342-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle												
t_{RC}	Read cycle time	15	–	20	–	25	–	35	–	55	–	ns
t_{AA}	Address to data valid	–	15	–	20	–	25	–	35	–	55	ns
t_{OHA}	Output hold from address change	3	–	3	–	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	–	20	–	25	–	35	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	13	–	15	–	20	–	25	ns
t_{LZOE}[8,9,10]	$\overline{OE}$ Low to Low Z	3	–	3	–	3	–	3	–	3	–	ns
t_{HZOE}[8,9,10]	$\overline{OE}$ HIGH to High Z	–	10	–	13	–	15	–	20	–	25	ns
t_{LZCE}[8,9,10]	$\overline{CE}$ LOW to Low Z	3	–	3	–	3	–	3	–	3	–	ns
t_{HZCE}[8,9,10]	$\overline{CE}$ HIGH to High Z	–	10	–	13	–	15	–	20	–	25	ns
t_{PU}[10]	$\overline{CE}$ LOW to Power-up	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}[10]	$\overline{CE}$ HIGH to Power-down	–	15	–	20	–	25	–	35	–	55	ns
Write Cycle												
t_{WC}	Write cycle time	15	–	20	–	25	–	35	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12	–	15	–	20	–	30	–	50	–	ns
t_{AW}	Address setup to Write End	12	–	15	–	20	–	30	–	50	–	ns
t_{HA}	Address hold from Write End	2	–	2	–	2	–	2	–	2	–	ns
t_{SA}	Address setup to Write Start	0	–	0	–	0	–	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	15	–	20	–	25	–	50	–	ns
t_{SD}	Data setup to Write End	10	–	13	–	15	–	15	–	25	–	ns
t_{HD}	Data hold from Write End	0	–	0	–	0	–	0	–	0	–	ns
t_{HZWE}[9,10]	R/$\overline{W}$ LOW to High Z	–	10	–	13	–	15	–	20	–	25	ns
t_{LZWE}[9,10]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	3	–	3	–	3	–	ns
t_{WDD}[11]	Write pulse to data delay	–	30	–	40	–	50	–	60	–	70	ns
t_{DDD}[11]	Write data valid to read data valid	–	25	–	30	–	30	–	35	–	40	ns
Semaphore Timing[12]												
t_{SOP}	SEM flag update pulse ($\overline{OE}$ or SEM)	10	–	10	–	10	–	15	–	15	–	ns
t_{SWRD}	SEM flag write to read time	5	–	5	–	5	–	5	–	5	–	ns
t_{SPS}	SEM flag contention window	5	–	5	–	5	–	5	–	5	–	ns

Notes
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.
10. This parameter is guaranteed but not tested.
11. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 6.
12. Semaphore timing applies only to CY7C1342.

[+] Feedback

Switching Waveforms

Figure 4. Read Cycle No. 1[13,14]

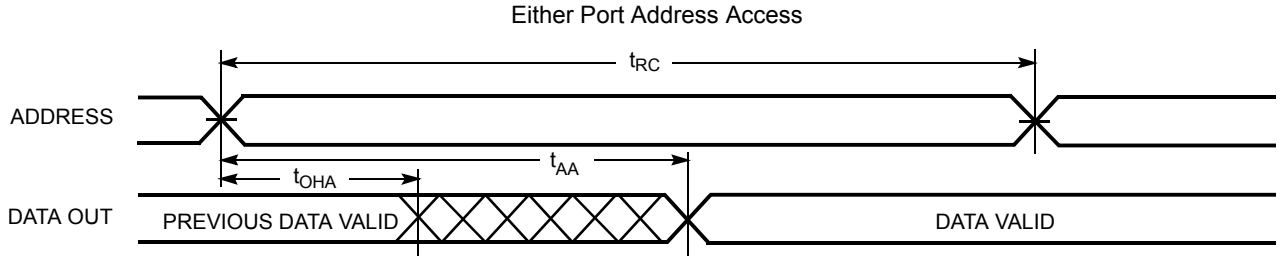


Figure 5. Read Cycle No. 2[13,15]

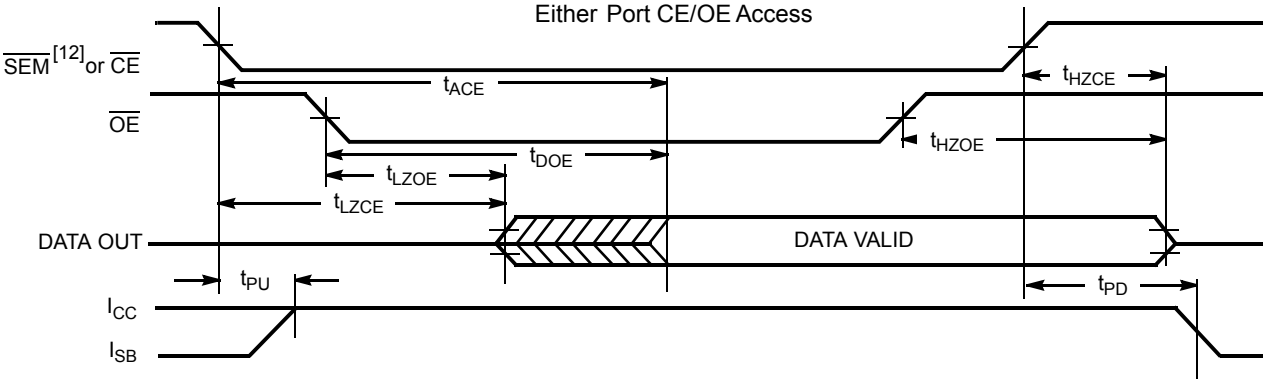
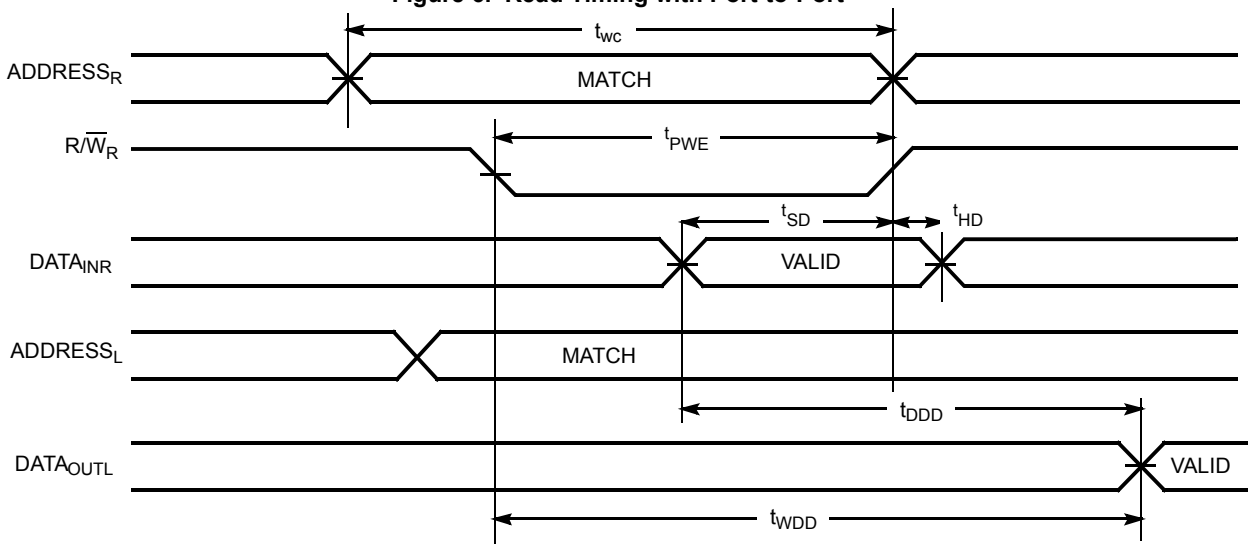


Figure 6. Read Timing with Port-to-Port[16]



Notes
13. R/W is HIGH for read cycle.
14. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
15. Address valid prior to or coincident with CE transition LOW.
16. CE_L = CE_R =LOW; R/W_L = HIGH

[+] Feedback

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1: OE Three-States Data I/Os (Either Port)[17, 18, 19]

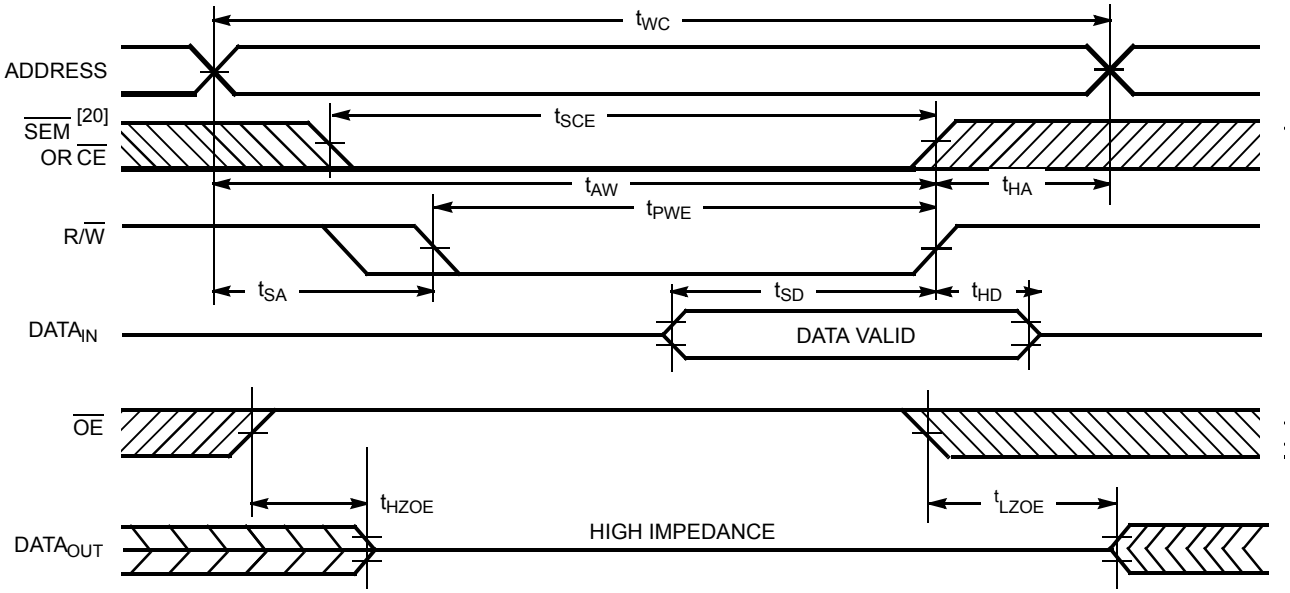
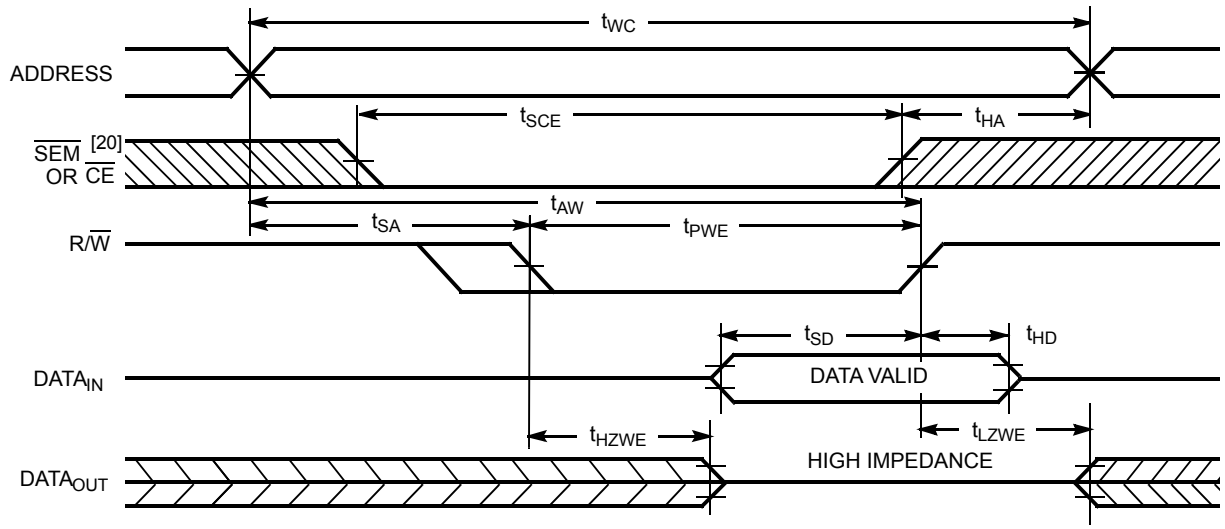


Figure 8. Write Cycle No. 2: R/W Three-States Data I/Os (Either Port)[18, 21]



Notes

17. The internal write time of the memory is defined by the overlap of CE or SEM LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. R/W must be HIGH during all address transactions.
19. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If OE is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
20. Semaphore timing applies only to CY7C1342.
21. Data I/O pins enter high impedance when OE is held LOW during write.

[+] Feedback

Switching Waveforms (continued)

Figure 9. Semaphore Read After Write Timing, Either Side (CY7C1342 only)[22]

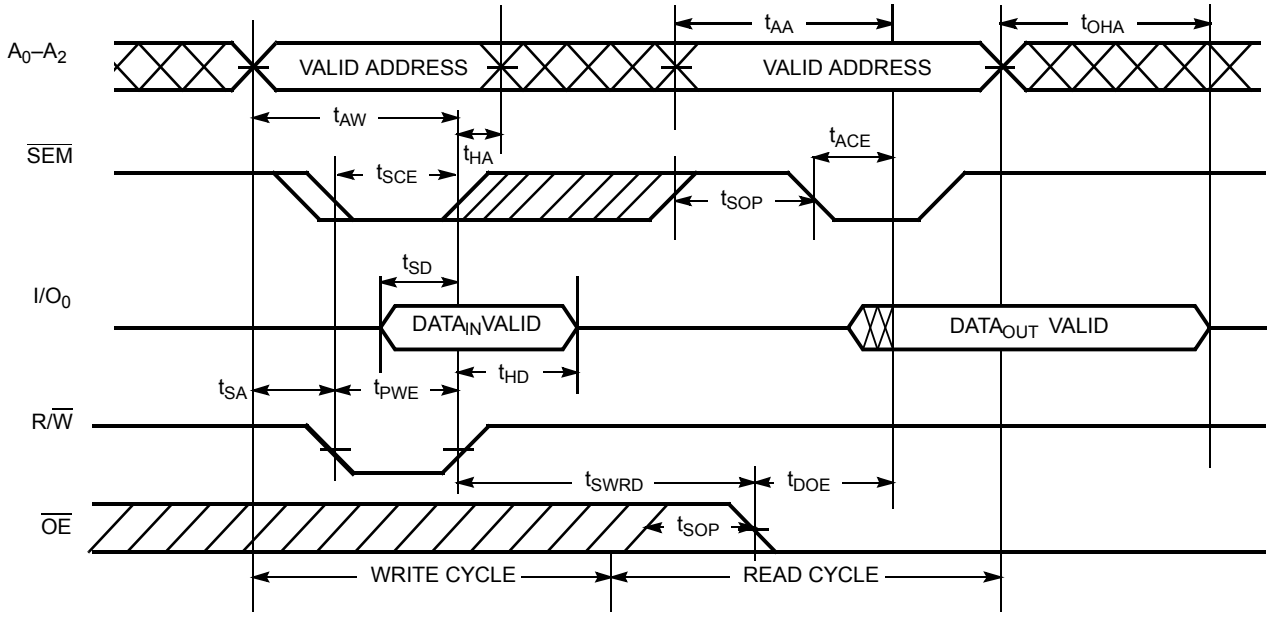
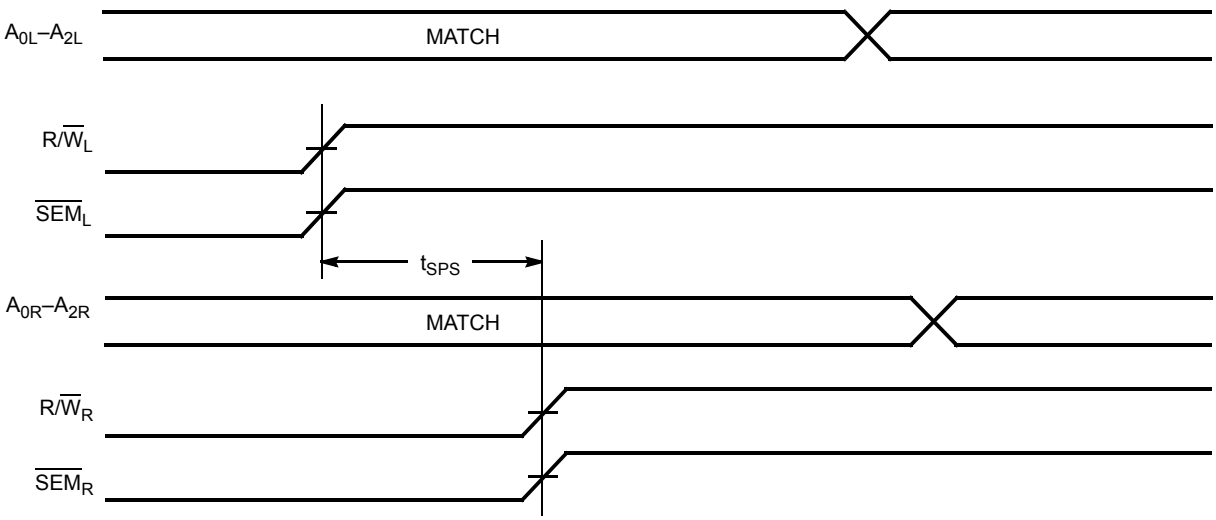


Figure 10. Timing Diagram of Semaphore Contention (CY7C1342 Only)[23, 24, 25]



Notes
22. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
23. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
24. Semaphores are reset (available to both ports) at cycle start.
25. If t_{SPS} is violated, it is guaranteed that only one side gains access to the semaphore.

[+] Feedback

Architecture

The CY7C135/135A consists of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). Two semaphore control pins exist for the CY7C1342 ($SEM_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to guarantee a valid write. Because there is no on-chip arbitration, the user must be sure that a specific location is not accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the OE pin (see Figure 7) or the R/W pin (see Figure 8). Data can be written t_{HZOE} after the OE is deasserted or t_{HZWE} after the falling edge of R/W. Required inputs for write operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data is valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data is available t_{ACE} after CE or t_{DOE} after OE are asserted. If the user of the CY7C1342 wishes to access a semaphore, the SEM pin must be asserted instead of the CE pin. Required inputs for read operations are summarized in Table 1.

Semaphore Operation

The CY7C1342 provides eight semaphore latches, which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip enable for the semaphore latches. CE must remain HIGH during SEM LOW. A_{0-2} represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. Table 2 shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side gains access to the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program during power up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they are free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	Operation
CE	R/W	OE	SEM	$I/O_0 – I/O_7$	
H	X	X	H	High Z	Power-down
H	H	L	L	Data out	Read semaphore
X	X	H	X	High Z	I/O Lines disabled
H	L	X	L	Data in	Write to Semaphore
L	H	L	H	Data out	Read
L	L	X	H	Data in	Write
L	X	X	L		Illegal condition

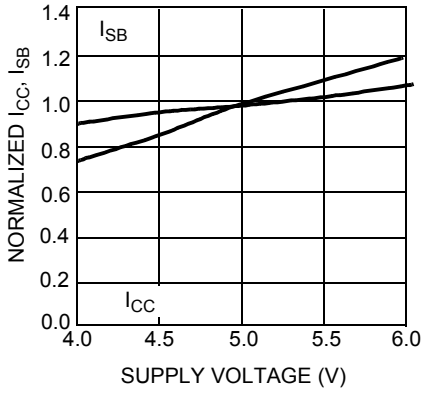
Table 2. Semaphore Operation Example

Function	I/O_{0-7} Left	I/O_{0-7} Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

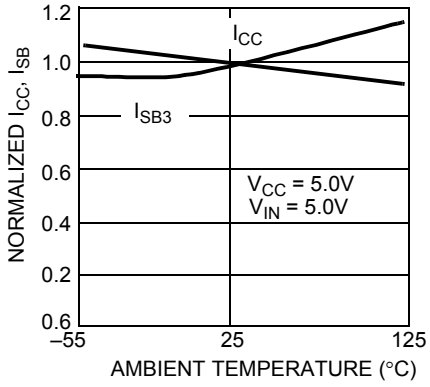
[+] Feedback

Typical DC and AC Characteristics

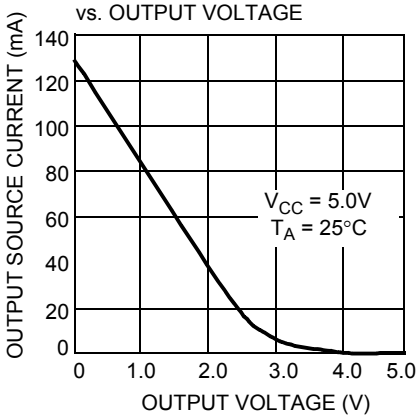
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



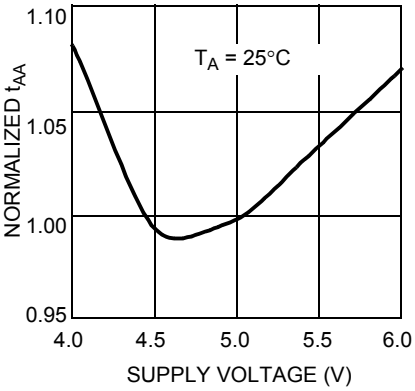
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



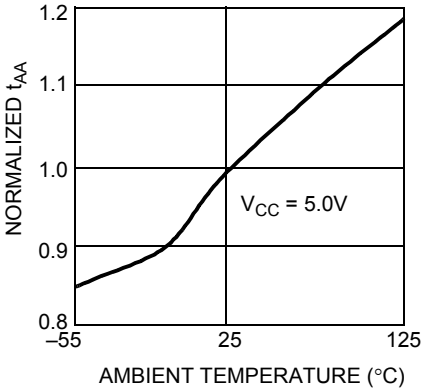
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



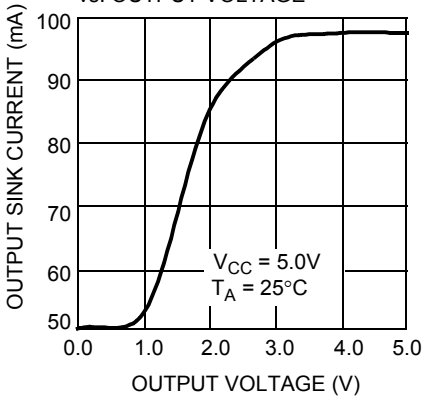
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



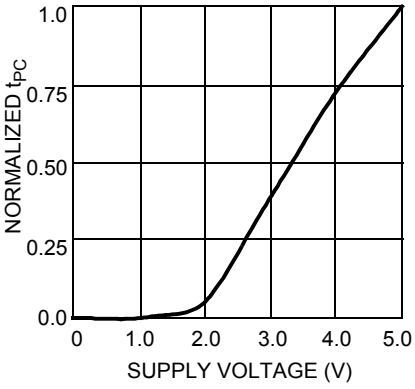
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



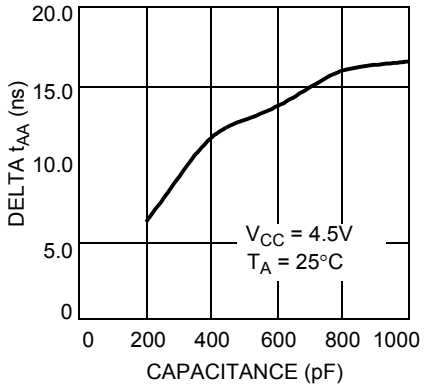
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



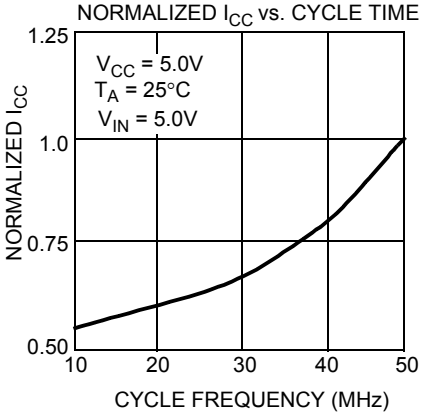
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



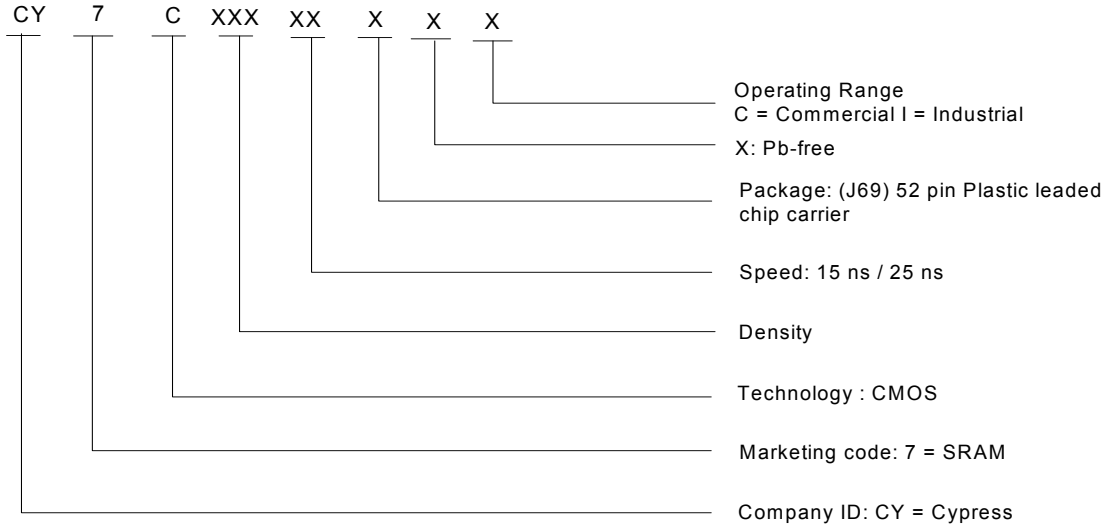
[+] Feedback

Ordering Information

4K x8 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C135-15JXC	J69	52-Pin Pb-free Plastic Leaded Chip Carrier	Commercial
25	CY7C135–25JXI	J69	52-Pin Pb-free Plastic Leaded Chip Carrier	Industrial

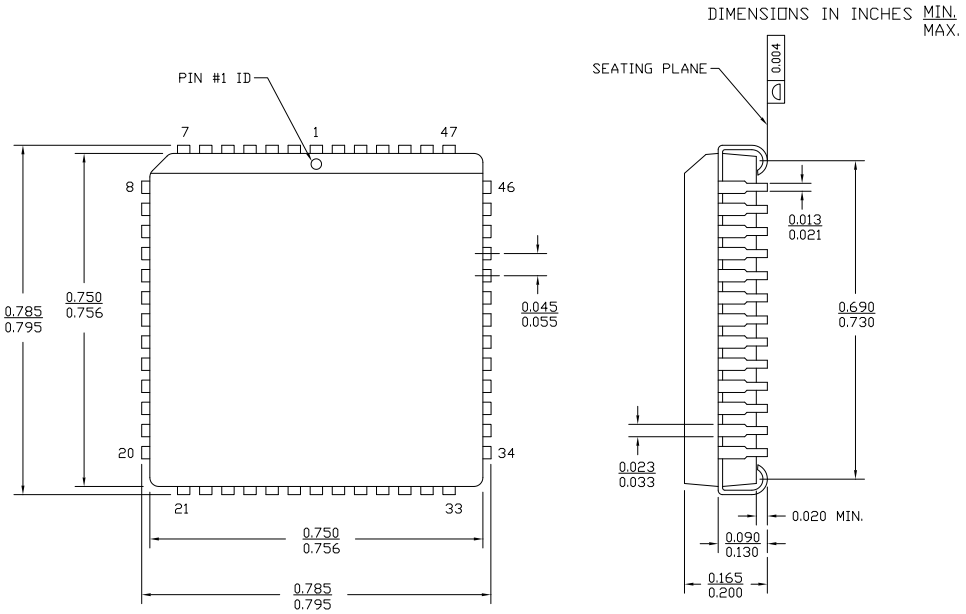
Ordering Code Definition



[+] Feedback

Package Diagram

Figure 11. 52-Pin Pb-free Plastic Leaded Chip Carrier J69



51-85004 *B

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
TQFP	thin quad plastic flatpack
I/O	input/output
SRAM	static random access memory
PLCC	plastic leaded chip carrier

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
Ω	Ohms
mV	milli Volts
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

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Document History Page

Document Title: CY7C135, CY7C135A, CY7C1342 4K x 8 Dual-Port Static RAM and 4K x 8 Dual-Port SRAM with Semaphores Document Number: 38-06038				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110181	SZV	10/21/01	Change from Spec number: 38-00541 to 38-06038
*A	122288	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	236763	YDT	SEE ECN	Removed cross information from features section
*C	393413	YIM	See ECN	Added Pb-free Logo Added Pb-free parts to ordering information: CY7C135-15JXC, CY7C135-25JXC
*D	2623540	VKN/PYRS	12/17/08	Added CY7C135A parts Removed CY7C1342 from the ordering information table
*E	2897217	RAME	03/22/2010	Updated Ordering Information Updated Package Diagram
*F	3081925	ADMU	11/10/2010	Added Ordering Code Definition details Added Acronyms and Units of Measure table. Updated all the footnotes Updated the datasheet as per new template

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