



THIS SPEC IS OBSOLETE

Spec No: 38-05256

Spec Title: CY7C1061AV33, 16-MBIT (1M X 16) STATIC  
RAM

Replaced by: None

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 990 mW (max)
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free and non Pb-free 54-pin TSOP II package and non Pb-free 60-ball fine-pitch ball grid array (FBGA) package

## Functional Description

The CY7C1061AV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

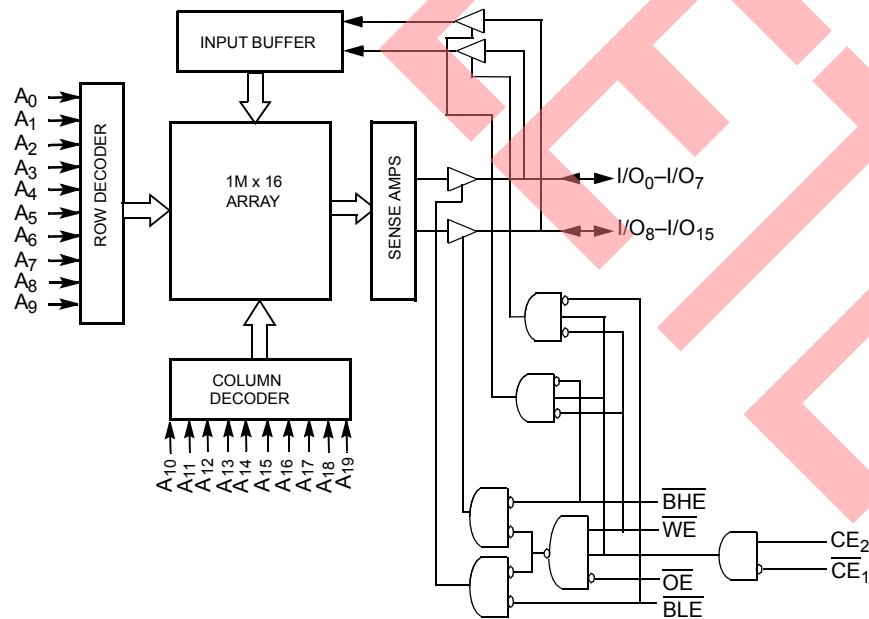
To write to the device, enable the chip ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) while forcing the Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, enable the chip by taking  $\overline{CE}_1$  LOW and  $CE_2$  HIGH while forcing the Output Enable ( $\overline{OE}$ ) LOW and the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See Truth Table on page 11 for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or a Write operation is in progress ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

For a complete list of related documentation, click [here](#).

## Logic Block Diagram



## Contents

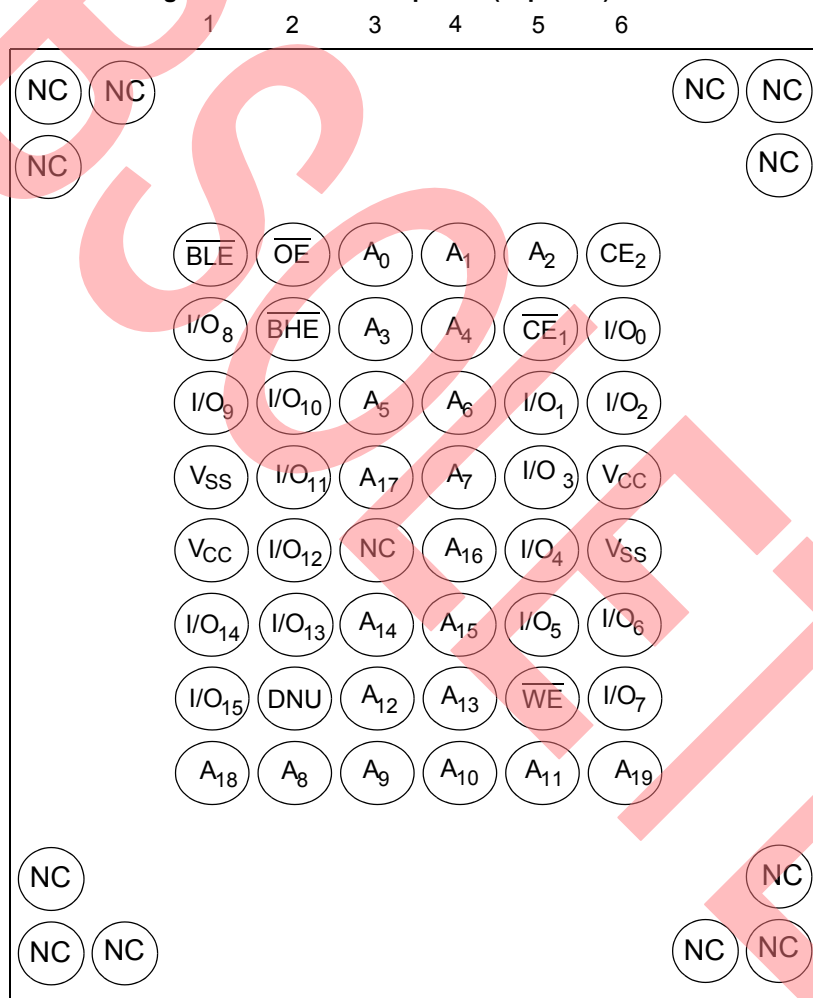
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### Selection Guide

Description		-10	Unit
Maximum Access Time		10	ns
Maximum Operating Current	Commercial	275	mA
	Industrial	275	
Maximum CMOS Standby Current	Commercial / Industrial	50	mA

### Pin Configurations

Figure 1. 60-ball FBGA pinout (Top View) [1, 2]



**Notes**

1. NC pins are not connected on the die.
2. DNU (Do Not Use) pins have to be left floating or tied to VSS to ensure proper operation.

Pin Configurations (continued)

Figure 2. 54-pin TSOP II pinout (Top View) [3, 4]

I/O <sub>12</sub>	1	54	I/O <sub>11</sub>
V <sub>CC</sub>	2	53	V <sub>SS</sub>
I/O <sub>13</sub>	3	52	I/O <sub>10</sub>
I/O <sub>14</sub>	4	51	I/O <sub>9</sub>
V <sub>SS</sub>	5	50	V <sub>CC</sub>
I/O <sub>15</sub>	6	49	I/O <sub>8</sub>
A <sub>4</sub>	7	48	A <sub>5</sub>
A <sub>3</sub>	8	47	A <sub>6</sub>
A <sub>2</sub>	9	46	A <sub>7</sub>
A <sub>1</sub>	10	45	A <sub>8</sub>
A <sub>0</sub>	11	44	A <sub>9</sub>
<u>BHE</u>	12	43	NC
CE <sub>1</sub>	13	42	OE
V <sub>CC</sub>	14	41	V <sub>SS</sub>
<u>WE</u>	15	40	DNU
CE <sub>2</sub>	16	39	BLE
A <sub>19</sub>	17	38	A <sub>10</sub>
A <sub>18</sub>	18	37	A <sub>11</sub>
A <sub>17</sub>	19	36	A <sub>12</sub>
A <sub>16</sub>	20	35	A <sub>13</sub>
A <sub>15</sub>	21	34	A <sub>14</sub>
I/O <sub>1</sub>	22	33	I/O <sub>7</sub>
V <sub>CC</sub>	23	32	V <sub>SS</sub>
I/O <sub>1</sub>	24	31	I/O <sub>6</sub>
I/O <sub>2</sub>	25	30	I/O <sub>5</sub>
V <sub>SS</sub>	26	29	V <sub>CC</sub>
I/O <sub>3</sub>	27	28	I/O <sub>4</sub>

Notes

3. NC pins are not connected on the die.
4. DNU (Do Not Use) pins have to be left floating or tied to VSS to ensure proper operation.

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on  $V_{CC}$  to Relative GND [5] ..... -0.5 V to +4.6 V  
 DC Voltage Applied to Outputs in High Z State [5] ..... -0.5 V to  $V_{CC} + 0.5$  V

DC Input Voltage [5] ..... -0.5 V to  $V_{CC} + 0.5$  V  
 Current into Outputs (LOW) ..... 20 mA

### Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0 °C to +70 °C	3.3 V ± 0.3 V
Industrial	-40 °C to +85 °C	

### DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -4.0$ mA	2.4	-	V	
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8.0$ mA	-	0.4	V	
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	V	
$V_{IL}$	Input LOW Voltage [5]		-0.3	0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA	
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1	+1	μA	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \max$ , $f = f_{max} = 1/t_{RC}$	Commercial	-	275	mA
			Industrial	-	275	mA
$I_{SB1}$	Automatic CE Power-down Current – TTL Inputs	$CE_2 \leq V_{IL}$ , Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{max}$	-	70	mA	
$I_{SB2}$	Automatic CE Power-down Current – CMOS Inputs	$CE_2 \leq 0.3$ V, Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$	-	50	mA	

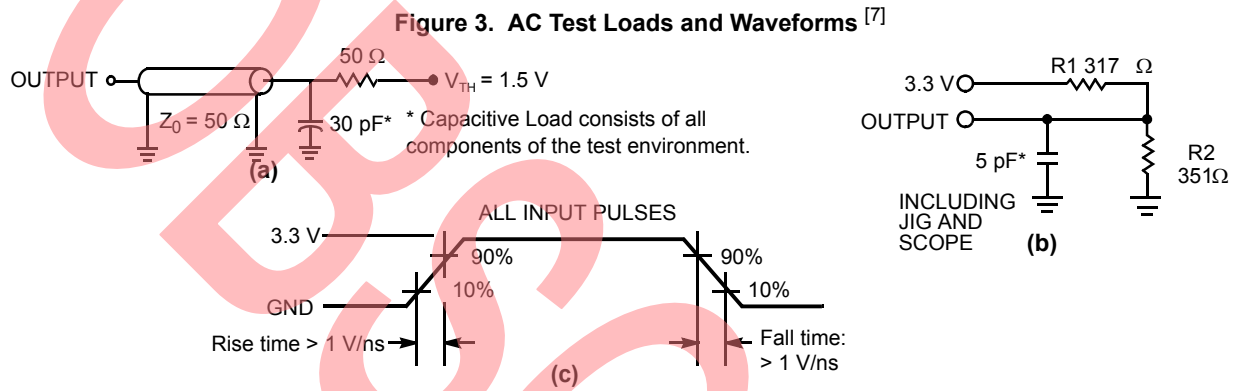
**Note**

5.  $V_{IL}(\min) = -2.0$  V for pulse durations of less than 20 ns.

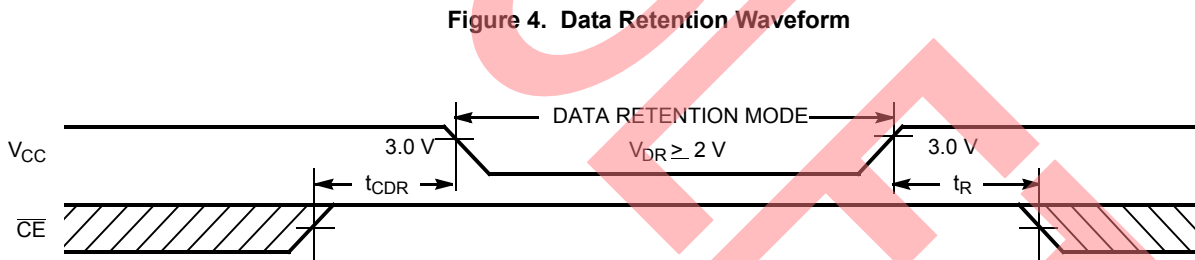
### Capacitance

Parameter [6]	Description	Test Conditions	TSOP II	FBGA	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	6	8	pF
$C_{OUT}$	I/O capacitance		8	10	pF

### AC Test Loads and Waveforms



### Data Retention Waveform



**Notes**

- 6. Tested initially and after any design or process changes that may affect these parameters.
- 7. Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0 V). As soon as 1 ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0 V) voltage.

## AC Switching Characteristics

Over the Operating Range

Parameter [8]	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}$ (typical) to the first access [9]	1	–	ms
$t_{RC}$	Read Cycle Time	10	–	ns
$t_{AA}$	Address to Data Valid	–	10	ns
$t_{OHA}$	Data Hold from Address Change	3	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Data Valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	1	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z [10]	–	5	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Low Z [10]	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to High Z [10]	–	5	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Power Up [11]	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to Power Down [11]	–	10	ns
$t_{DBE}$	Byte Enable to Data Valid	–	5	ns
$t_{LZBE}$	Byte Enable to Low Z	1	–	ns
$t_{HZBE}$	Byte Disable to High Z	–	5	ns
<b>Write Cycle [12, 13]</b>				
$t_{WC}$	Write Cycle Time	10	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to Write End	7	–	ns
$t_{AW}$	Address Setup to Write End	7	–	ns
$t_{HA}$	Address Hold from Write End	0	–	ns
$t_{SA}$	Address Setup to Write Start	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7	–	ns
$t_{SD}$	Data Setup to Write End	5.5	–	ns
$t_{HD}$	Data Hold from Write End	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z [10]	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z [10]	–	5	ns
$t_{BW}$	Byte Enable to End of Write	7	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and specified transmission line loads. Test conditions for the Read cycle use output loading shown in (a) of the Figure 3 on page 6, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3 V to 2 V internally.  $t_{power}$  time must be provided initially before a Read/Write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 6. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW ( $CE_2$  HIGH) and  $\overline{WE}$  LOW. Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .



### Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

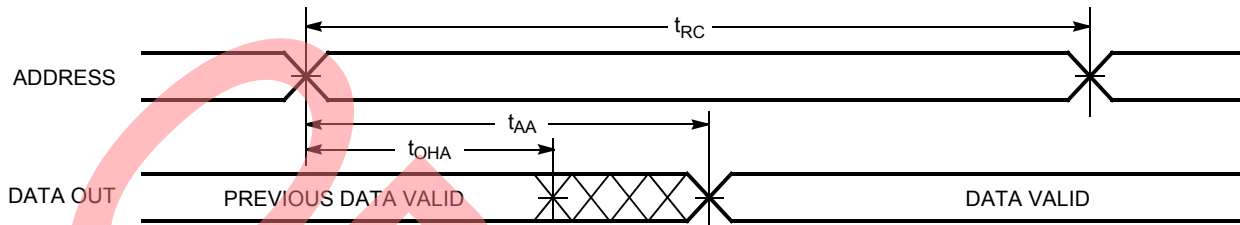
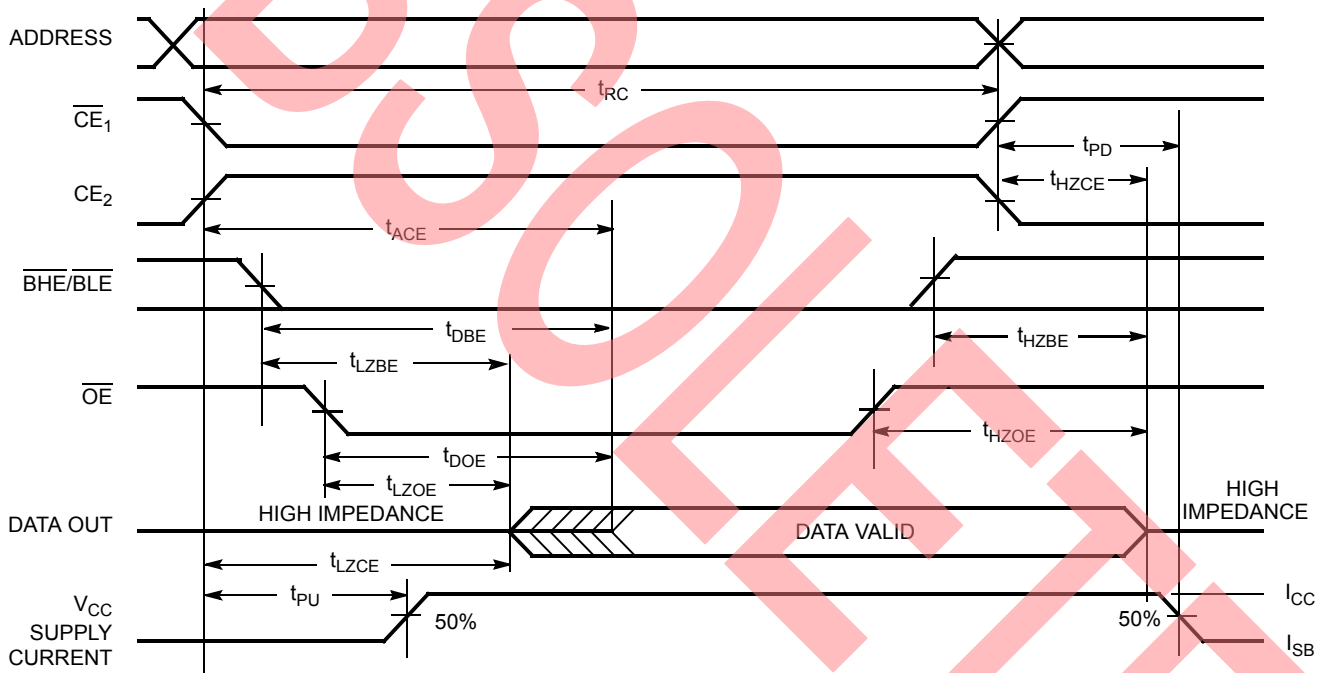


Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [15, 16]



**Notes**

- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  or  $\overline{BHE}$ , or both =  $V_{IL}$ .  $CE_2 = V_{IH}$ .
- 15.  $\overline{WE}$  is HIGH for Read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [17, 18]

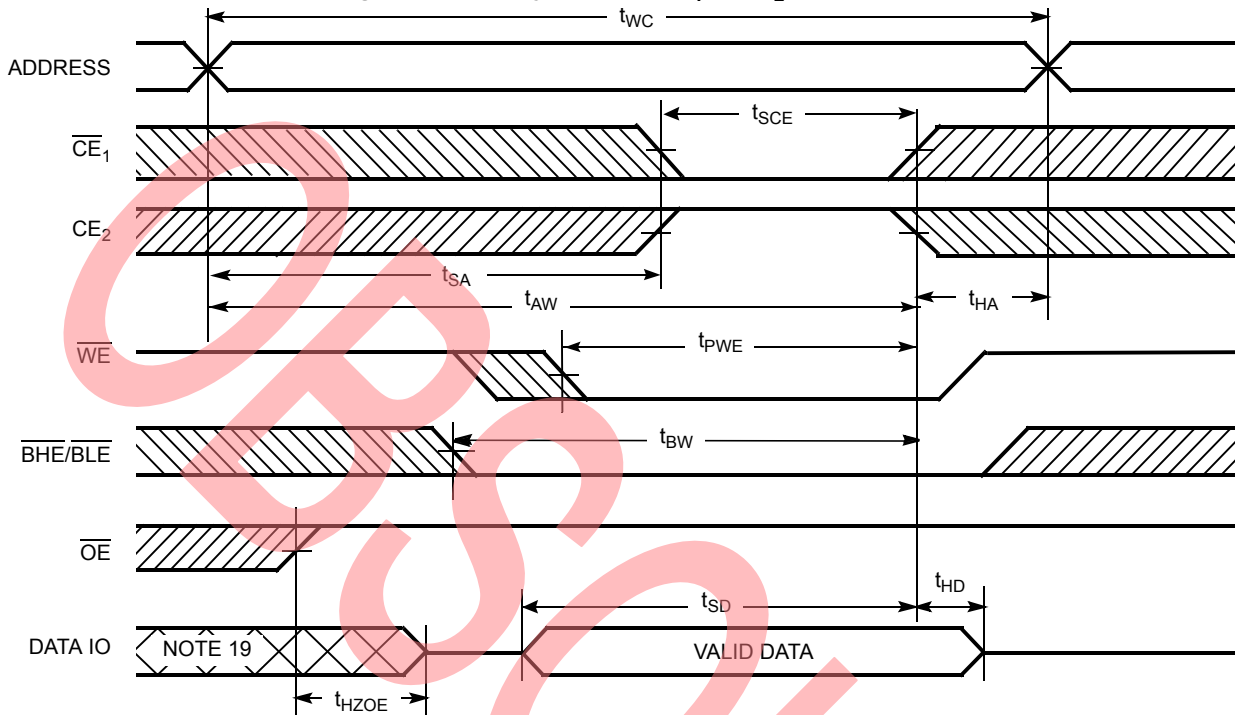
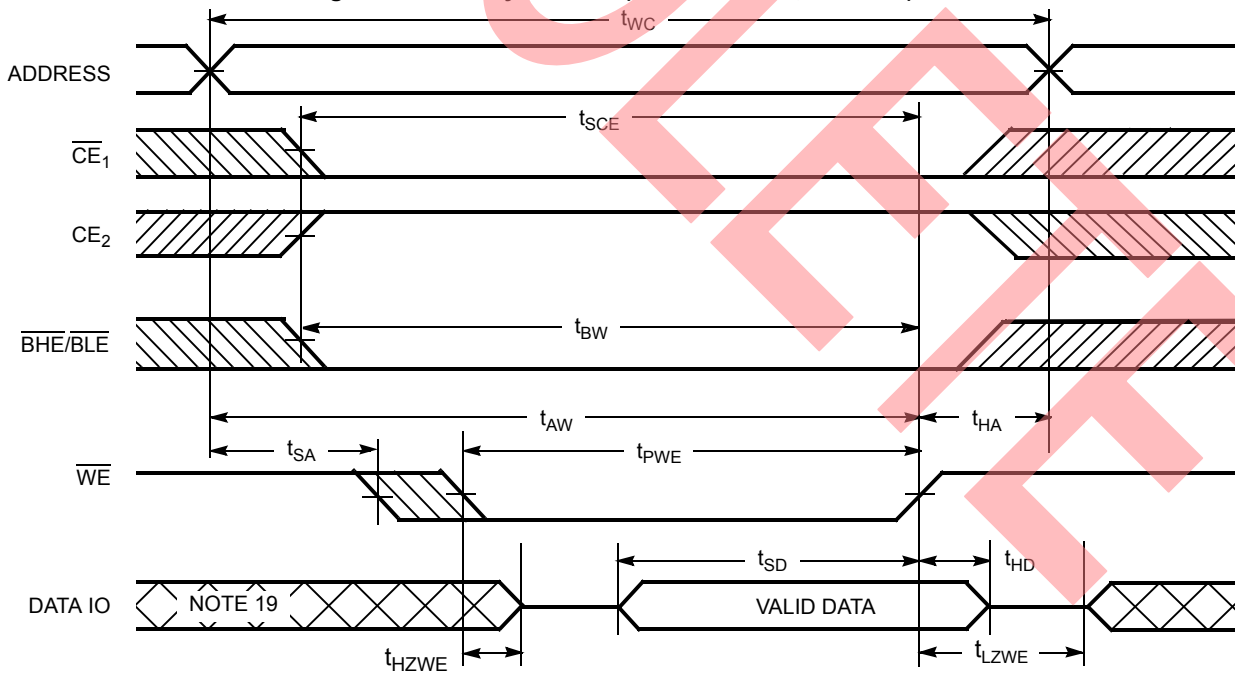


Figure 8. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [17, 18, 20]

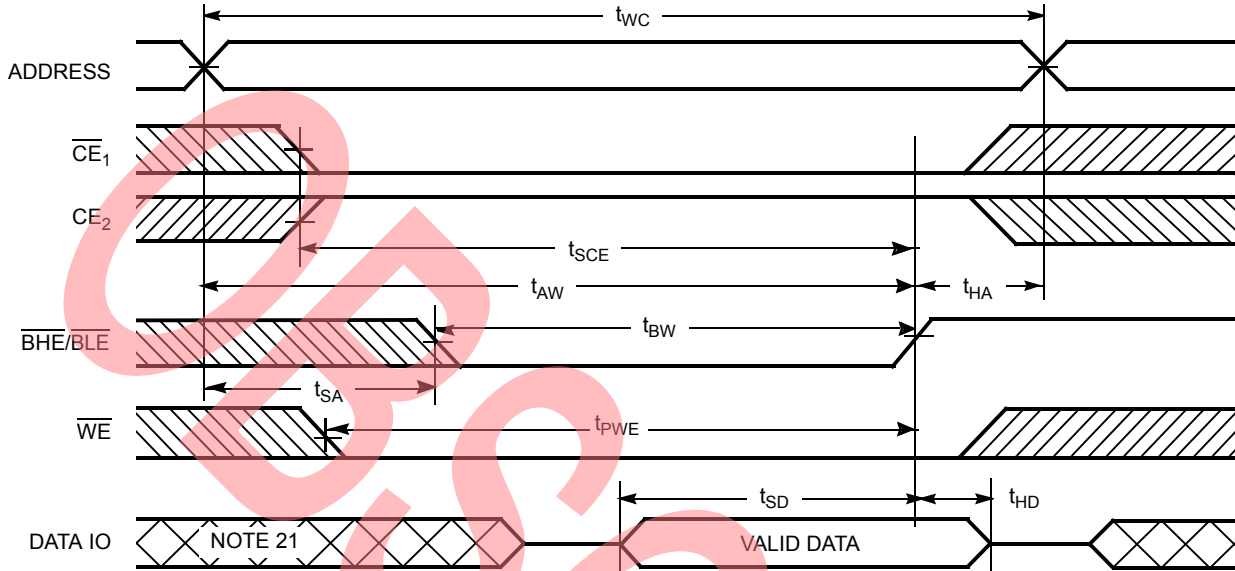


Notes

- 17. Data IO is high impedance if  $\overline{OE}$ , or  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IH}$ .
- 18. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high impedance state.
- 19. During this period, the IOs are in output state and input signals should not be applied.
- 20. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled)



**Note**  
21. During this period, the IOs are in output state and input signals should not be applied.

**Truth Table**

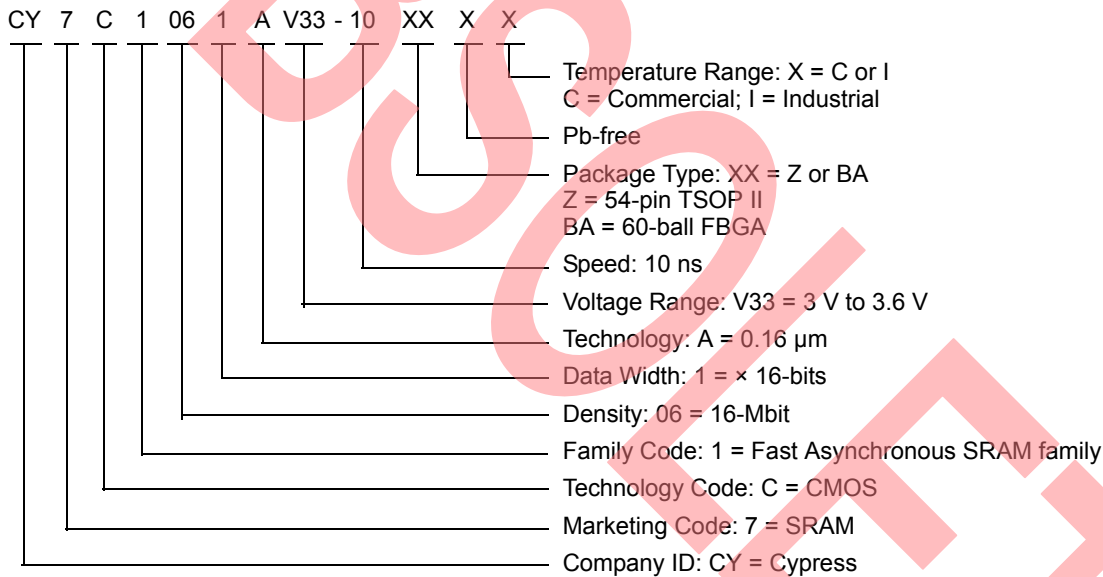
$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

### Ordering Information

The following table lists the CY7C1061AV33 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061AV33-10ZXC	51-85160	54-pin TSOP II (Pb-free)	Commercial
	CY7C1061AV33-10ZXI	51-85160	54-pin TSOP II (Pb-free)	Industrial
	CY7C1061AV33-10BAXI	51-85162	60-ball FBGA (Pb-free)	

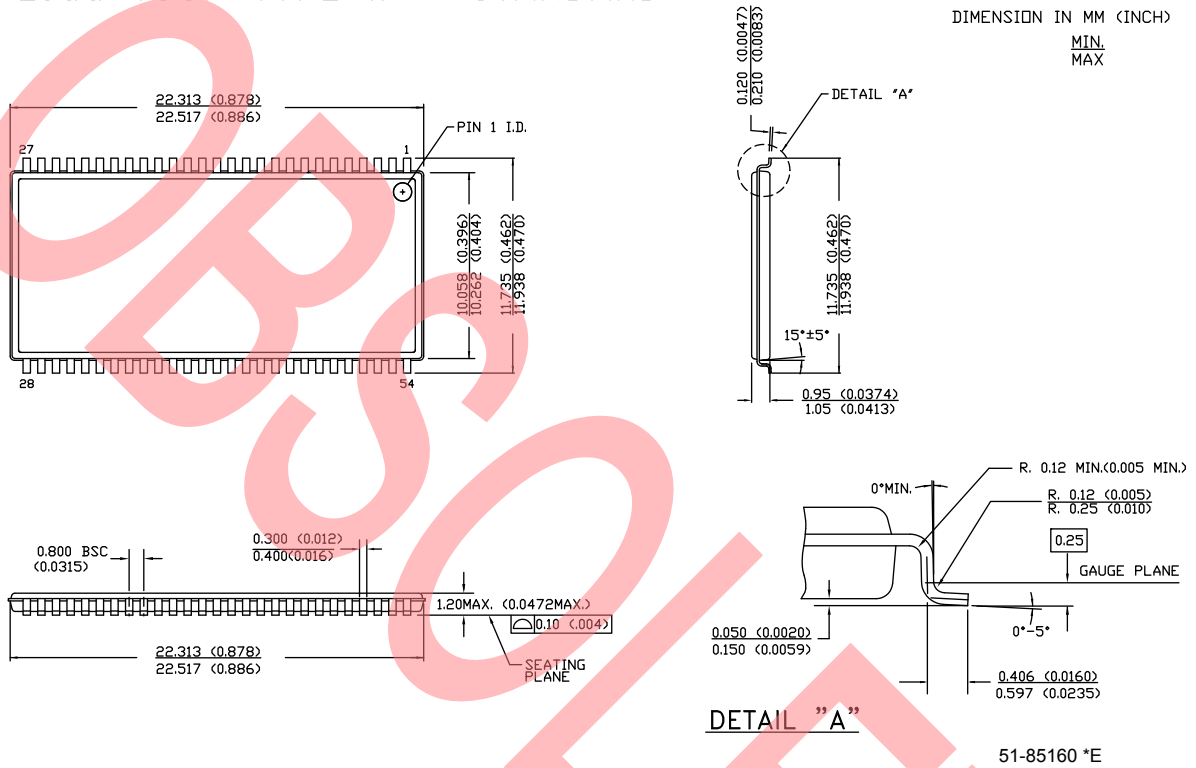
### Ordering Code Definitions



Package Diagrams

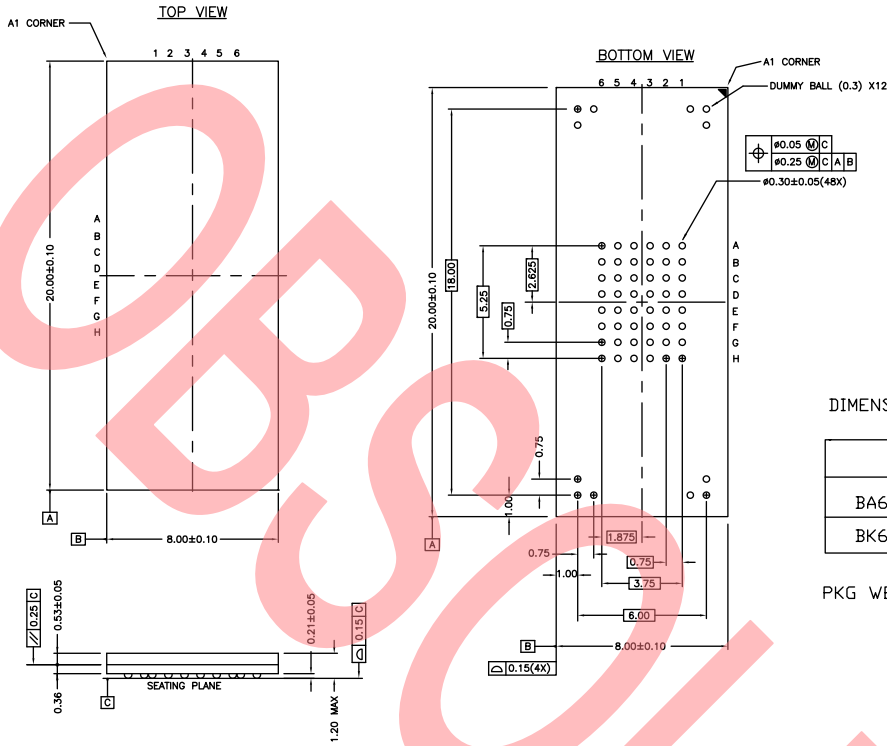
Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160

54 Lead TSOP TYPE II – STANDARD



Package Diagrams (continued)

Figure 11. 60-ball FBGA (8 × 20 × 1.2 mm) Package Outline, 51-85162



**Acronyms**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



Document History Page

Document Title: CY7C1061AV33, 16-Mbit (1M × 16) Static RAM				
Document Number: 38-05256				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	113725	03/28/02	NSL	New data sheet
*A	117058	07/31/02	DFP	Removed 15-ns bin
*B	117989	08/30/02	DFP	Added 8-ns bin Changed I <sub>cc</sub> for 8, 10, 12 bins t <sub>power</sub> changed from 1 μs to 1 ms. Load Cap Comment changed (for Tx line load) t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin numbers (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> ) Removed hz<lz comments from data sheet
*C	120383	11/06/02	DFP	Final data sheet Added note 3 to “AC Test Loads and Waveforms” and note 7 to t <sub>pu</sub> and t <sub>pd</sub> Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF
*D	124439	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded FBGA production ordering information
*E	492137	See ECN	NXR	Corrected Block Diagram on page #1 Removed 8 ns speed bin Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Included Note #1 and 2 on page #2 Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*F	508117	See ECN	NXR	Updated FBGA Pin Configuration Updated Ordering Information table
*G	877322	See ECN	VKN	Updated Ordering Information table
*H	2897049	03/22/10	KAO	Removed inactive parts from the ordering information table. Updated package diagrams. Updated links in Sales, Solutions and Legal Information.
*I	3109147	12/13/2010	KAO	Added Ordering Code Definitions under Ordering Information.
*J	3160428	02/02/11	PRAS	Updated Ordering Information: Updated part numbers. Updated to new template.
*K	3222127	04/11/2011	PRAS	Added Acronyms and Units of Measure.
*L	4363272	04/28/2014	MEMJ	Updated Switching Waveforms: Added Note 20 and referred in Figure 8. Updated Package Diagrams: spec 51-85160 – Changed revision from *A to *D. spec 51-85162 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*M	4578447	01/16/2015	MEMJ	Updated Functional Description: Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end. Updated Package Diagrams: spec 51-85160 – Changed revision from *D to *E.
*N	5738556	05/16/2017	VINI	Obsolete document. Completing Sunset Review.

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