

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex™-M0+ CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. PSoC 4100S Plus is a member of the PSoC 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CapSense) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC 4100S Plus products will be upward compatible with members of the PSoC 4 platform for new applications and design needs.

Features

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0+ CPU
- Up to 128 KB of flash with Read Accelerator
- Up to 16 KB of SRAM
- 8-channel DMA engine

Programmable Analog

- Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode.
- 12-bit 1-Msps SAR ADC with differential and single-ended modes, and Channel Sequencer with signal averaging
- Single-slope 10-bit ADC function provided by a capacitance sensing block
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep low-power mode

Programmable Digital

- Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs

Low-Power 1.71-V to 5.5-V Operation

- Deep Sleep mode with operational analog and 2.5-μA digital system current

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

LCD Drive Capability

- LCD segment drive capability on GPIOs

Serial Communication

- Five independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I²C, SPI, or UART functionality

Timing and Pulse-Width Modulation

- Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications
- Quadrature decoder

Clock Sources

- 4 to 33 MHz external crystal oscillator (ECO)
- PLL to generate 48-MHz frequency
- 32-kHz Watch Crystal Oscillator (WCO)
- ±2% Internal Main Oscillator (IMO)
- 32-kHz Internal Low-power Oscillator (ILO)

True Random Number Generator (TRNG)

- TRNG generates truly random number for secure key generation for Cryptography applications

CAN Block

- CAN 2.0B block with support for Time-Triggered CAN (TTCAN)

Up to 54 Programmable GPIO Pins

- 44-pin TQFP (0.8-mm pitch) and 64-pin TQFP normal (0.8 mm) and Fine Pitch (0.5 mm) packages
- Any GPIO pin can be CapSense, analog, or digital
- Drive modes, strengths, and slew rates are programmable

PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API) component for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with Arm-based industry-standard development tools

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): Arm Cortex Code Optimization
 - [AN85951](#): PSoC® 4 and PSoC Analog Coprocessor CapSense® Design Guide
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - [CY8CKIT-041-41XX](#) PSoC 4100S CapSense Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
 - [CY8CKIT-149](#) PSoC® 4100S Plus Prototyping Kit enables you to evaluate and develop with Cypress' fourth-generation, low-power CapSense solution using the PSoC 4100S Plus devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.
- [Software User Guide](#):
 - A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.
- Component Datasheets:
 - The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.
- Online:
 - In addition to print documentation, the [Cypress PSoC forums](#) connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

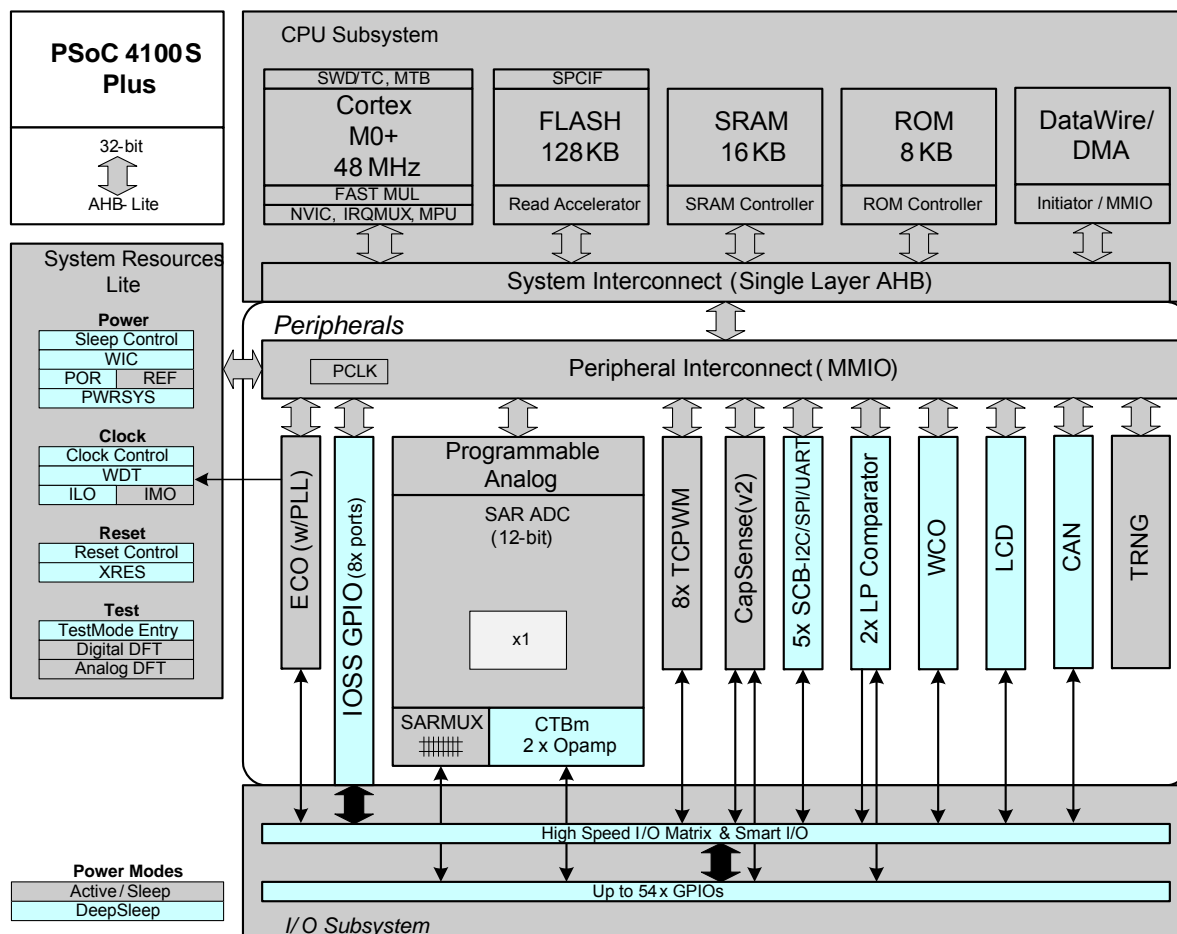
PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

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Contents

| | | | |
|--|-----------|--|-----------|
| Functional Definition | 6 | Ordering Information..... | 33 |
| CPU and Memory Subsystem | 6 | Packaging..... | 35 |
| System Resources | 6 | Package Diagrams | 36 |
| Analog Blocks..... | 7 | Acronyms | 38 |
| Programmable Digital Blocks | 8 | Document Conventions | 40 |
| Fixed Function Digital Blocks | 8 | Units of Measure | 40 |
| GPIO | 8 | Revision History | 41 |
| Special Function Peripherals..... | 9 | Sales, Solutions, and Legal Information | 42 |
| Pinouts | 10 | Worldwide Sales and Design Support..... | 42 |
| Alternate Pin Functions | 12 | Products | 42 |
| Power | 14 | PSoC® Solutions | 42 |
| Mode 1: 1.8 V to 5.5 V External Supply | 14 | Cypress Developer Community..... | 42 |
| Mode 2: 1.8 V ±5% External Supply..... | 14 | Technical Support | 42 |
| Electrical Specifications | 15 | | |
| Absolute Maximum Ratings..... | 15 | | |
| Device Level Specifications..... | 15 | | |
| Analog Peripherals | 19 | | |
| Digital Peripherals | 26 | | |
| Memory | 29 | | |
| System Resources | 29 | | |

Figure 2. Block Diagram


PSoC 4100S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S Plus devices. The SWD interface is fully compatible with industry-standard third-party tools. PSoC 4100S Plus provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S Plus, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S Plus allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU subsystem includes an 8-channel DMA engine and also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S Plus has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S Plus device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

16 KB of SRAM are provided with zero wait-state access at 48 MHz.

SRAM

An 8-KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). PSoC 4100S Plus operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC 4100S Plus provides Active, Sleep, and Deep Sleep low-power modes.

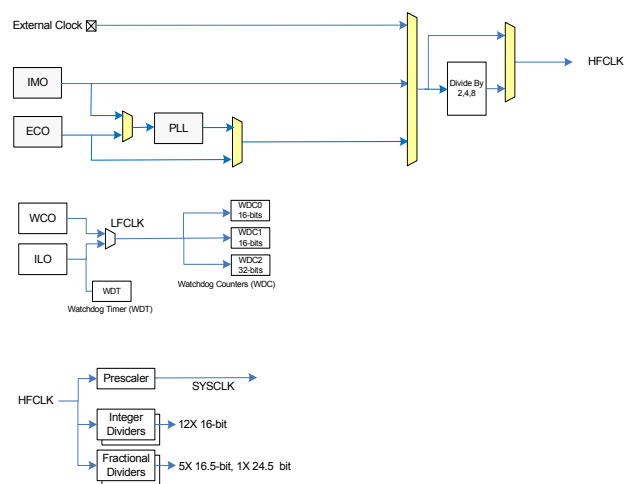
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC 4100S Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S Plus consists of the IMO, ILO, a 32-kHz Watch Crystal Oscillator (WCO), MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

Figure 3. PSoC 4100S Plus MCU Clocking Architecture



The HFCLK signal can be divided down as shown to generate synchronous clocks for the Analog and Digital peripherals. There are 18 clock dividers for the PSoC 4100S Plus (six with fractional divide capability, twelve with integer divide only). The twelve 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S Plus. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2% over the entire voltage and temperature range.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

External Crystal Oscillators (ECO)

The PSoC 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

Watchdog Timer and Counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

Reset

PSoC 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

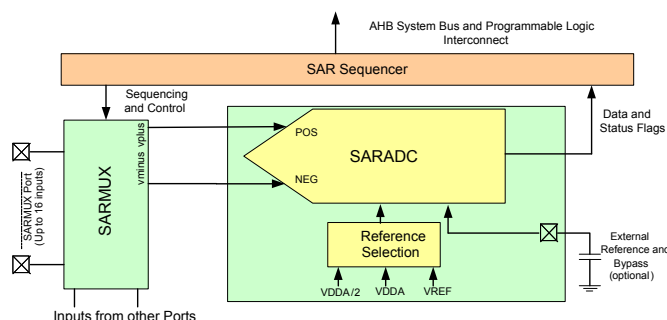
The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range

values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

PSoC 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

PSoC 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

PSoC 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

PSoC 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

Smart I/O Block

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital Blocks

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a Quadrature decoder. There are eight TCPWM blocks in PSoC 4100S Plus.

Serial Communication Block (SCB)

PSoC 4100S Plus has five serial communication blocks, which can be programmed to have SPI, I²C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of PSoC 4100S Plus and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

PSoC 4100S Plus is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

CAN

There is a CAN 2.0B block with support for TT-CAN.

GPIO

PSoC 4100S Plus has up to 54 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-up
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S Plus through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

PSoC 4100S Plus has an LCD controller, which can drive up to 4 commons and up to 50 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

Pinouts

The following table provides the pin list for PSoC 4100S Plus for the 44-pin TQFP and 64-pin TQFP Normal and Fine Pitch packages.

| 64-TQFP | | 44-TQFP | |
|---------|-----------------|---------|------|
| Pin | Name | Pin | Name |
| 39 | P0.0 | 24 | P0.0 |
| 40 | P0.1 | 25 | P0.1 |
| 41 | P0.2 | 26 | P0.2 |
| 42 | P0.3 | 27 | P0.3 |
| 43 | P0.4 | 28 | P0.4 |
| 44 | P0.5 | 29 | P0.5 |
| 45 | P0.6 | 30 | P0.6 |
| 46 | P0.7 | 31 | P0.7 |
| 47 | XRES | 32 | XRES |
| 48 | VCCD | 33 | VCCD |
| 49 | VSSD | | |
| 50 | VDDD | 34 | VDDD |
| 51 | P5.0 | | |
| 52 | P5.1 | | |
| 53 | P5.2 | | |
| 54 | P5.3 | | |
| 55 | P5.5 | | |
| 56 | VDDA | 35 | VDDA |
| 57 | VSSA | 36 | VSSA |
| 58 | P1.0 | 37 | P1.0 |
| 59 | P1.1 | 38 | P1.1 |
| 60 | P1.2 | 39 | P1.2 |
| 61 | P1.3 | 40 | P1.3 |
| 62 | P1.4 | 41 | P1.4 |
| 63 | P1.5 | 42 | P1.5 |
| 64 | P1.6 | 43 | P1.6 |
| 1 | P1.7 | 44 | P1.7 |
| | | 1 | VSSD |
| 2 | P2.0 | 2 | P2.0 |
| 3 | P2.1 | 3 | P2.1 |
| 4 | P2.2 | 4 | P2.2 |
| 5 | P2.3 | 5 | P2.3 |
| 6 | P2.4 | 6 | P2.4 |
| 7 | P2.5 | 7 | P2.5 |
| 8 | P2.6 | 8 | P2.6 |
| 9 | P2.7 | 9 | P2.7 |
| 10 | VSSD | 10 | P6.0 |
| 11 | No Connect (NC) | | |
| 12 | P6.0 | | |
| 13 | P6.1 | | |

| 64-TQFP | | 44-TQFP | |
|---------|------|---------|------|
| Pin | Name | Pin | Name |
| 14 | P6.2 | | |
| 15 | P6.4 | | |
| 16 | P6.5 | | |
| 17 | VSSD | | |
| 17 | VSSD | | |
| 18 | P3.0 | 11 | P3.0 |
| 19 | P3.1 | 12 | P3.1 |
| 20 | P3.2 | 13 | P3.2 |
| 21 | P3.3 | 14 | P3.3 |
| 22 | P3.4 | 15 | P3.4 |
| 23 | P3.5 | 16 | P3.5 |
| 24 | P3.6 | 17 | P3.6 |
| 25 | P3.7 | 18 | P3.7 |
| 26 | VDDD | 19 | VDDD |
| 27 | P4.0 | 20 | P4.0 |
| 28 | P4.1 | 21 | P4.1 |
| 29 | P4.2 | 22 | P4.2 |
| 30 | P4.3 | 23 | P4.3 |
| 31 | P4.4 | | |
| 32 | P4.5 | | |
| 33 | P4.6 | | |
| 34 | P4.7 | | |
| 35 | P5.6 | | |
| 36 | P5.7 | | |
| 37 | P7.0 | | |
| 38 | P7.1 | | |

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V $\pm 5\%$)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

GPIOs by package:

| | 64 TQFP | 44 TQFP |
|--------|---------|---------|
| Number | 54 | 37 |

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for example, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

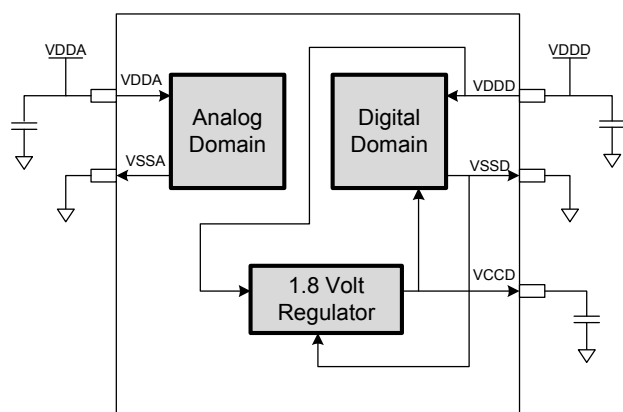
| Port/Pin | Analog | Smart I/O | ACT #0 | ACT #1 | ACT #3 | DS #2 | DS #3 |
|----------|---|------------------|-----------------------|-------------------|-------------------|------------------|----------------------|
| P0.0 | lpcomp.in_p[0] | | | tcpwm.tr_in[0] | scb[2].uart_cts:0 | scb[2].i2c_scl:0 | scb[0].spi_select1:0 |
| P0.1 | lpcomp.in_n[0] | | | tcpwm.tr_in[1] | scb[2].uart_rts:0 | scb[2].i2c_sda:0 | scb[0].spi_select2:0 |
| P0.2 | lpcomp.in_p[1] | | | | | | scb[0].spi_select3:0 |
| P0.3 | lpcomp.in_n[1] | | | | | | scb[2].spi_select0:1 |
| P0.4 | wco.wco_in | | | scb[1].uart_rx:0 | scb[2].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:1 |
| P0.5 | wco.wco_out | | | scb[1].uart_tx:0 | scb[2].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:1 |
| P0.6 | exco.eco_in | | srss.ext_clk:0 | scb[1].uart_cts:0 | scb[2].uart_tx:1 | | scb[1].spi_clk:1 |
| P0.7 | exco.eco_out | | tcpwm.line[0]:3 | scb[1].uart_rts:0 | | | scb[1].spi_select0:1 |
| P5.0 | | | tcpwm.line[4]:2 | | scb[2].uart_rx:1 | scb[2].i2c_scl:1 | scb[2].spi_mosi:0 |
| P5.1 | | | tcpwm.line_compl[4]:2 | | scb[2].uart_tx:2 | scb[2].i2c_sda:1 | scb[2].spi_miso:0 |
| P5.2 | | | tcpwm.line[5]:2 | | scb[2].uart_cts:1 | lpcomp.comp[0]:2 | scb[2].spi_clk:0 |
| P5.3 | | | tcpwm.line_compl[5]:2 | | scb[2].uart_rts:1 | lpcomp.comp[1]:0 | scb[2].spi_select0:0 |
| P5.4 | | | tcpwm.line[6]:2 | | | | scb[2].spi_select1:0 |
| P5.5 | | | tcpwm.line_compl[6]:2 | | | | scb[2].spi_select2:0 |
| P1.0 | ctb0_oa0+ | Smartlo[2].io[0] | tcpwm.line[2]:1 | scb[0].uart_rx:1 | | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | ctb0_oa0- | Smartlo[2].io[1] | tcpwm.line_compl[2]:1 | scb[0].uart_tx:1 | | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | ctb0_oa0_out | Smartlo[2].io[2] | tcpwm.line[3]:1 | scb[0].uart_cts:1 | tcpwm.tr_in[2] | scb[2].i2c_scl:2 | scb[0].spi_clk:1 |
| P1.3 | ctb0_oa1_out | Smartlo[2].io[3] | tcpwm.line_compl[3]:1 | scb[0].uart_rts:1 | tcpwm.tr_in[3] | scb[2].i2c_sda:2 | scb[0].spi_select0:1 |
| P1.4 | ctb0_oa1- | Smartlo[2].io[4] | tcpwm.line[6]:1 | | | scb[3].i2c_scl:0 | scb[0].spi_select1:1 |
| P1.5 | ctb0_oa1+ | Smartlo[2].io[5] | tcpwm.line_compl[6]:1 | | | scb[3].i2c_sda:0 | scb[0].spi_select2:1 |
| P1.6 | ctb0_oa0+ | Smartlo[2].io[6] | tcpwm.line[7]:1 | | | | scb[0].spi_select3:1 |
| P1.7 | ctb0_oa1+ sar_ext_vref0 sar_ext_vref1 | Smartlo[2].io[7] | tcpwm.line_compl[7]:1 | | | | scb[2].spi_clk:1 |
| P2.0 | sarmux[0] | Smartlo[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | sarmux[1] | Smartlo[0].io[1] | tcpwm.line_compl[4]:0 | | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | sarmux[2] | Smartlo[0].io[2] | tcpwm.line[5]:1 | | | | scb[1].spi_clk:2 |
| P2.3 | sarmux[3] | Smartlo[0].io[3] | tcpwm.line_compl[5]:1 | | | | scb[1].spi_select0:2 |

| Port/Pin | Analog | Smart I/O | ACT #0 | ACT #1 | ACT #3 | DS #2 | DS #3 |
|----------|--------------|------------------|-----------------------|-------------------|--------------------|--------------------|----------------------|
| P2.4 | sarmux[4] | Smartlo[0].io[4] | tcpwm.line[0]:1 | scb[3].uart_rx:1 | | | scb[1].spi_select1:1 |
| P2.5 | sarmux[5] | Smartlo[0].io[5] | tcpwm.line_compl[0]:1 | scb[3].uart_tx:1 | | | scb[1].spi_select2:1 |
| P2.6 | sarmux[6] | Smartlo[0].io[6] | tcpwm.line[1]:1 | scb[3].uart_cts:1 | | | scb[1].spi_select3:1 |
| P2.7 | sarmux[7] | Smartlo[0].io[7] | tcpwm.line_compl[1]:1 | scb[3].uart_rts:1 | | lpcomp.comp[0]:0 | scb[2].spi_mosi:1 |
| P6.0 | | | tcpwm.line[4]:1 | scb[3].uart_rx:0 | can.can_tx_enb_n:0 | scb[3].i2c_scl:1 | scb[3].spi_mosi:0 |
| P6.1 | | | tcpwm.line_compl[4]:1 | scb[3].uart_tx:0 | can.can_rx:0 | scb[3].i2c_sda:1 | scb[3].spi_miso:0 |
| P6.2 | | | tcpwm.line[5]:0 | scb[3].uart_cts:0 | can.can_tx:0 | | scb[3].spi_clk:0 |
| P6.3 | | | tcpwm.line_compl[5]:0 | scb[3].uart_rts:0 | | | scb[3].spi_select0:0 |
| P6.4 | | | tcpwm.line[6]:0 | | | scb[4].i2c_scl | scb[3].spi_select1:0 |
| P6.5 | | | tcpwm.line_compl[6]:0 | | | scb[4].i2c_sda | scb[3].spi_select2:0 |
| P3.0 | | Smartlo[1].io[0] | tcpwm.line[0]:0 | scb[1].uart_rx:1 | | scb[1].i2c_scl:2 | scb[1].spi_mosi:0 |
| P3.1 | | Smartlo[1].io[1] | tcpwm.line_compl[0]:0 | scb[1].uart_tx:1 | | scb[1].i2c_sda:2 | scb[1].spi_miso:0 |
| P3.2 | | Smartlo[1].io[2] | tcpwm.line[1]:0 | scb[1].uart_cts:1 | | cpuss.swd_data | scb[1].spi_clk:0 |
| P3.3 | | Smartlo[1].io[3] | tcpwm.line_compl[1]:0 | scb[1].uart_rts:1 | | cpuss.swd_clk | scb[1].spi_select0:0 |
| P3.4 | | Smartlo[1].io[4] | tcpwm.line[2]:0 | | tcpwm.tr_in[6] | | scb[1].spi_select1:0 |
| P3.5 | | Smartlo[1].io[5] | tcpwm.line_compl[2]:0 | | | | scb[1].spi_select2:0 |
| P3.6 | | Smartlo[1].io[6] | tcpwm.line[3]:0 | | | scb[4].spi_select3 | scb[1].spi_select3:0 |
| P3.7 | | Smartlo[1].io[7] | tcpwm.line_compl[3]:0 | | | lpcomp.comp[1]:1 | scb[2].spi_miso:1 |
| P4.0 | csd.vref_ext | | | scb[0].uart_rx:0 | can.can_rx:1 | scb[0].i2c_scl:1 | scb[0].spi_mosi:0 |
| P4.1 | csd.cshield | | | scb[0].uart_tx:0 | can.can_tx:1 | scb[0].i2c_sda:1 | scb[0].spi_miso:0 |
| P4.2 | csd.cmod | | | scb[0].uart_cts:0 | can.can_tx_enb_n:1 | lpcomp.comp[0]:1 | scb[0].spi_clk:0 |
| P4.3 | csd.csh_tank | | | scb[0].uart_rts:0 | | lpcomp.comp[1]:2 | scb[0].spi_select0:0 |
| P4.4 | | | | scb[4].uart_rx | | scb[4].spi_mosi | scb[0].spi_select1:2 |
| P4.5 | | | | scb[4].uart_tx | | scb[4].spi_miso | scb[0].spi_select2:2 |
| P4.6 | | | | scb[4].uart_cts | | scb[4].spi_clk | scb[0].spi_select3:2 |
| P4.7 | | | | scb[4].uart_rts | | scb[4].spi_select0 | |
| P5.6 | | | tcpwm.line[7]:0 | | | scb[4].spi_select1 | scb[2].spi_select3:0 |
| P5.7 | | | tcpwm.line_compl[7]:0 | | | scb[4].spi_select2 | |
| P7.0 | | | tcpwm.line[0]:2 | scb[3].uart_rx:2 | | scb[3].i2c_scl:2 | scb[3].spi_mosi:1 |
| P7.1 | | | tcpwm.line_compl[0]:2 | scb[3].uart_tx:2 | | scb[3].i2c_sda:2 | scb[3].spi_miso:1 |
| P7.2 | | | tcpwm.line[1]:2 | scb[3].uart_cts:2 | | | scb[3].spi_clk:1 |

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S Plus. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 5. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is $1.8 \text{ V} \pm 5\%$ (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, PSoC 4100S Plus is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100S Plus supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μF ; X5R ceramic or better) and must not be connected to anything else.

Mode 2: 1.8 V $\pm 5\%$ External Supply

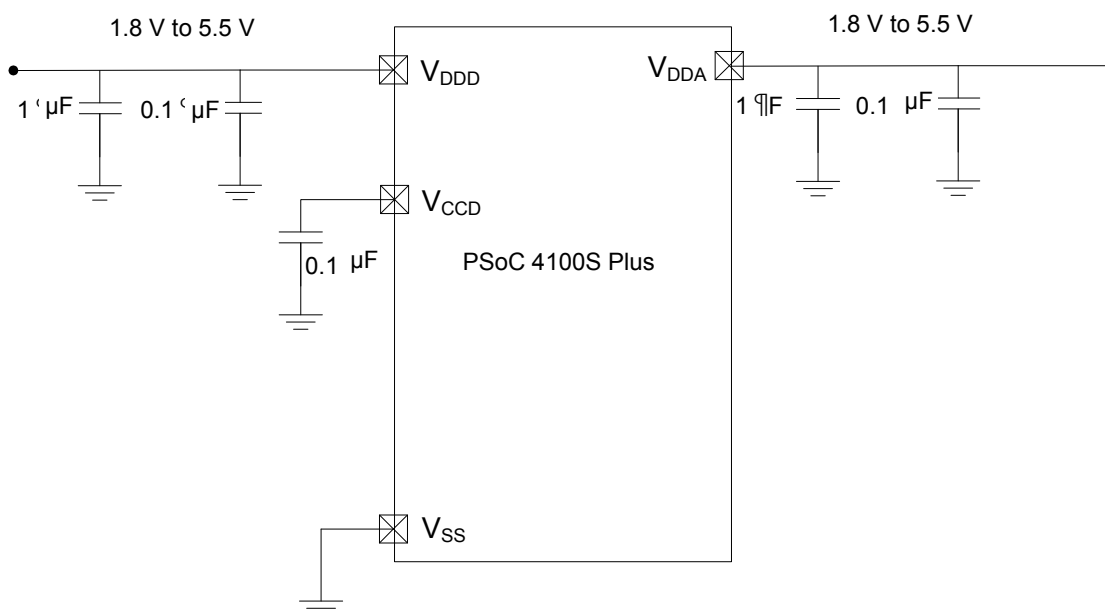
In this mode, PSoC 4100S Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μF range, in parallel with a smaller capacitor (0.1 μF , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 6. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active

Power supply bypass connections example



Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------------------------|--|------|-----|----------------------|-------|--------------------------|
| SID1 | V _{DDD_ABS} | Digital supply relative to V _{SS} | −0.5 | − | 6 | V | − |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SS} | −0.5 | − | 1.95 | | − |
| SID3 | V _{GPIO_ABS} | GPIO voltage | −0.5 | − | V _{DD} +0.5 | | − |
| SID4 | I _{GPIO_ABS} | Maximum current per GPIO | −25 | − | 25 | mA | − |
| SID5 | I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS} | −0.5 | − | 0.5 | | Current injected per pin |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | − | − | V | − |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | − | − | | − |
| BID46 | LU | Pin current for latch-up | −140 | − | 140 | mA | − |

Device Level Specifications

All specifications are valid for −40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|------------------|--|------|-----|------|-------|-------------------------------|
| SID53 | V _{DD} | Power supply input voltage | 1.8 | − | 5.5 | V | Internally regulated supply |
| SID255 | V _{DD} | Power supply input voltage (V _{CCD} = V _{DDD} = V _{DDA}) | 1.71 | − | 1.89 | | Internally unregulated supply |
| SID54 | V _{CCD} | Output voltage (for core logic) | − | 1.8 | − | | − |
| SID55 | C _{EFC} | External regulator voltage bypass | − | 0.1 | − | μF | X5R ceramic or better |
| SID56 | C _{EXC} | Power supply bypass capacitor | − | 1 | − | | X5R ceramic or better |

Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25 °C.

| | | | | | | | |
|-------|-------------------|-----------------------------------|---|-----|-----|----|---------------------------|
| SID10 | I _{DD5} | Execute from flash; CPU at 6 MHz | − | 1.8 | 2.4 | mA | Max is at 85 °C and 5.5 V |
| SID16 | I _{DD8} | Execute from flash; CPU at 24 MHz | − | 3.0 | 4.6 | | Max is at 85 °C and 5.5 V |
| SID19 | I _{DD11} | Execute from flash; CPU at 48 MHz | − | 5.4 | 7.1 | | Max is at 85 °C and 5.5 V |

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications (continued)

 Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|--------------------|---|-----|-----|-----|-------|------------------------------------|
| Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on) | | | | | | | |
| SID22 | I _{DD17} | I ² C wakeup WDT, and Comparators on | – | 1.1 | 1.8 | mA | 6 MHZ. Max is at 85 °C and 5.5 V |
| SID25 | I _{DD20} | I ² C wakeup, WDT, and Comparators on | – | 1.5 | 2.1 | | 12 MHZ. Max is at 85 °C and 5.5 V |
| Sleep Mode, V _{DDD} = 1.71 V to 1.89 V (Regulator bypassed) | | | | | | | |
| SID28 | I _{DD23} | I ² C wakeup, WDT, and Comparators on | – | 1.1 | 1.8 | mA | 6 MHZ. Max is at 85 °C and 1.89 V |
| SID28A | I _{DD23A} | I ² C wakeup, WDT, and Comparators on | – | 1.5 | 2.1 | mA | 12 MHZ. Max is at 85 °C and 1.89 V |
| Deep Sleep Mode, V _{DD} = 1.8 V to 3.6 V (Regulator on) | | | | | | | |
| SID30 | I _{DD25} | I ² C wakeup and WDT on; T = –40 °C to 60 °C | – | 2.5 | 40 | μA | T = –40 °C to 60 °C |
| SID31 | I _{DD26} | I ² C wakeup and WDT on | – | 2.5 | 125 | μA | Max is at 3.6 V and 85 °C |
| Deep Sleep Mode, V _{DD} = 3.6 V to 5.5 V (Regulator on) | | | | | | | |
| SID33 | I _{DD28} | I ² C wakeup and WDT on; T = –40 °C to 60 °C | – | 2.5 | 40 | μA | T = –40 °C to 60 °C |
| SID34 | I _{DD29} | I ² C wakeup and WDT on | – | 2.5 | 125 | μA | Max is at 5.5 V and 85 °C |
| Deep Sleep Mode, V _{DD} = V _{CCD} = 1.71 V to 1.89 V (Regulator bypassed) | | | | | | | |
| SID36 | I _{DD31} | I ² C wakeup and WDT on; T = –40 °C to 60 °C | – | 2.5 | 60 | μA | T = –40 °C to 60 °C |
| SID37 | I _{DD32} | I ² C wakeup and WDT on | – | 2.5 | 180 | μA | Max is at 1.89 V and 85 °C |
| XRES Current | | | | | | | |
| SID307 | I _{DD XR} | Supply current while XRES asserted | – | 2 | 5 | mA | – |

Table 3. AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------|-----------------|-----------------------------|-----|-----|-----|---------------|-----------------------------|
| SID48 | F_{CPU} | CPU frequency | DC | – | 48 | MHz | $1.71 \leq V_{DD} \leq 5.5$ |
| SID49 ^[2] | T_{SLEEP} | Wakeup from Sleep mode | – | 0 | – | μs | |
| SID50 ^[2] | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | | |

Note

2. Guaranteed by characterization.

GPIO
Table 4. GPIO DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------------------|------------------|---|----------------------|-----|---------------------|------------|-----------------------------------|
| SID57 | $V_{IH}^{[3]}$ | Input voltage high threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS Input |
| SID58 | V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DD}$ | | CMOS Input |
| SID241 | $V_{IH}^{[3]}$ | LVTTL input, $V_{DD} < 2.7$ V | $0.7 \times V_{DD}$ | – | – | | – |
| SID242 | V_{IL} | LVTTL input, $V_{DD} < 2.7$ V | – | – | $0.3 \times V_{DD}$ | | – |
| SID243 | $V_{IH}^{[3]}$ | LVTTL input, $V_{DD} \geq 2.7$ V | 2.0 | – | – | | – |
| SID244 | V_{IL} | LVTTL input, $V_{DD} \geq 2.7$ V | – | – | 0.8 | | – |
| SID59 | V_{OH} | Output voltage high level | $V_{DD} - 0.6$ | – | – | | $I_{OH} = 4$ mA at 3 V V_{DD} |
| SID60 | V_{OH} | Output voltage high level | $V_{DD} - 0.5$ | – | – | | $I_{OH} = 1$ mA at 1.8 V V_{DD} |
| SID61 | V_{OL} | Output voltage low level | – | – | 0.6 | | $I_{OL} = 4$ mA at 1.8 V V_{DD} |
| SID62 | V_{OL} | Output voltage low level | – | – | 0.6 | | $I_{OL} = 10$ mA at 3 V V_{DD} |
| SID62A | V_{OL} | Output voltage low level | – | – | 0.4 | | $I_{OL} = 3$ mA at 3 V V_{DD} |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | | – |
| SID65 | I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DD} = 3.0$ V |
| SID66 | C_{IN} | Input capacitance | – | – | 7 | pF | – |
| SID67 ^[4] | V_{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DD} \geq 2.7$ V |
| SID68 ^[4] | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DD}$ | – | – | | $V_{DD} < 4.5$ V |
| SID68A ^[4] | $V_{HYSCMOS5V5}$ | Input hysteresis CMOS | 200 | – | – | | $V_{DD} > 4.5$ V |
| SID69 ^[4] | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μ A | – |
| SID69A ^[4] | I_{TOT_GPIO} | Maximum total source or sink chip current | – | – | 200 | mA | – |

Table 5. GPIO AC Specifications
 (Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-------------|-------------------------------|-----|-----|-----|-------|-------------------------------|
| SID70 | T_{RISEF} | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V V_{DD} , Load = 25 pF |
| SID71 | T_{FALLF} | Fall time in fast strong mode | 2 | – | 12 | | 3.3 V V_{DD} , Load = 25 pF |
| SID72 | T_{RISES} | Rise time in slow strong mode | 10 | – | 60 | – | 3.3 V V_{DD} , Load = 25 pF |

Notes

3. V_{IH} must not exceed $V_{DD} + 0.2$ V.
4. Guaranteed by characterization.

Table 5. GPIO AC Specifications (continued)
 (Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|----------------|---|-----|-----|------|-------|---|
| SID73 | T_{FALLS} | Fall time in slow strong mode | 10 | – | 60 | – | 3.3 V V_{DD} , $C_{load} = 25$ pF |
| SID74 | $F_{GPIOOUT1}$ | GPIO F_{OUT} ; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Fast strong mode | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOOUT2}$ | GPIO F_{OUT} ; $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ Fast strong mode | – | – | 16.7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOOUT3}$ | GPIO F_{OUT} ; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Slow strong mode | – | – | 7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOOUT4}$ | GPIO F_{OUT} ; $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ Slow strong mode. | – | – | 3.5 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | F_{GPIOIN} | GPIO input operating frequency; $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 48 | | 90/10% V_{IO} |

XRES
Table 6. XRES DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------|---------------|--|---------------------|-----|---------------------|------------|---|
| SID77 | V_{IH} | Input voltage high threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS Input |
| SID78 | V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DD}$ | | |
| SID79 | R_{PULLUP} | Pull-up resistor | – | 60 | – | k Ω | – |
| SID80 | C_{IN} | Input capacitance | – | – | 7 | pF | – |
| SID81 ^[5] | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Typical hysteresis is 200 mV for $V_{DD} > 4.5\text{ V}$ |
| SID82 | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μ A | |

Table 7. XRES AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------------------|------------------|---------------------------------|-----|-----|-----|---------|------------------------|
| SID83 ^[5] | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | μ s | – |
| BID194 ^[5] | $T_{RESETWAKE}$ | Wake-up time from reset release | – | – | 2.7 | ms | – |

Note

5. Guaranteed by characterization.

Analog Peripherals
CTBm Opamp
Table 8. CTBm Opamp Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|--------------------------|--|-------|------|-----------------------|-------|---|
| | I _{DD} | Opamp block current, External load | | | | | |
| SID269 | I _{DD_HI} | power=hi | – | 1100 | 1850 | μA | – |
| SID270 | I _{DD_MED} | power=med | – | 550 | 950 | | – |
| SID271 | I _{DD_LOW} | power=lo | – | 150 | 350 | | – |
| | G _{BW} | Load = 20 pF, 0.1 mA V _{DDA} = 2.7 V | | | | | |
| SID272 | G _{BW_HI} | power=hi | 6 | – | – | MHz | Input and output are 0.2 V to V _{DDA} -0.2 V |
| SID273 | G _{BW_MED} | power=med | 3 | – | – | | Input and output are 0.2 V to V _{DDA} -0.2 V |
| SID274 | G _{BW_LO} | power=lo | – | 1 | – | | Input and output are 0.2 V to V _{DDA} -0.2 V |
| | I _{OUT_MAX} | V _{DDA} = 2.7 V, 500 mV from rail | | | | | |
| SID275 | I _{OUT_MAX_HI} | power=hi | 10 | – | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID276 | I _{OUT_MAX_MID} | power=mid | 10 | – | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| SID277 | I _{OUT_MAX_LO} | power=lo | – | 5 | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| | I _{OUT} | V _{DDA} = 1.71 V, 500 mV from rail | | | | | |
| SID278 | I _{OUT_MAX_HI} | power=hi | 4 | – | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID279 | I _{OUT_MAX_MID} | power=mid | 4 | – | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| SID280 | I _{OUT_MAX_LO} | power=lo | – | 2 | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| | I _{DD_Int} | Opamp block current Internal Load | | | | | |
| SID269_I | I _{DD_HI_Int} | power=hi | – | 1500 | 1700 | μA | – |
| SID270_I | I _{DD_MED_Int} | power=med | – | 700 | 900 | | – |
| SID271_I | I _{DD_LOW_Int} | power=lo | – | – | – | | – |
| | G _{BW} | V _{DDA} = 2.7 V | – | – | – | | – |
| SID272_I | G _{BW_HI_Int} | power=hi | 8 | – | – | MHz | Output is 0.25 V to V _{DDA} -0.25 V |
| | | General opamp specs for both internal and external modes | | | | | |
| SID281 | V _{IN} | Charge-pump on, V _{DDA} = 2.7 V | –0.05 | – | V _{DDA} -0.2 | V | – |
| SID282 | V _{CM} | Charge-pump on, V _{DDA} = 2.7 V | –0.05 | – | V _{DDA} -0.2 | | – |
| | V _{OUT} | V _{DDA} = 2.7 V | | | | | |

Table 8. CTBm Opamp Specifications *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------------------|--|------|------|-----------------------|--------|--|
| SID283 | V _{OUT_1} | power=hi, Iload=10 mA | 0.5 | – | V _{DDA} -0.5 | V | – |
| SID284 | V _{OUT_2} | power=hi, Iload=1 mA | 0.2 | – | V _{DDA} -0.2 | | – |
| SID285 | V _{OUT_3} | power=med, Iload=1 mA | 0.2 | – | V _{DDA} -0.2 | | – |
| SID286 | V _{OUT_4} | power=lo, Iload=0.1 mA | 0.2 | – | V _{DDA} -0.2 | | – |
| SID288 | V _{OS_TR} | Offset voltage, trimmed | –1.0 | ±0.5 | 1.0 | mV | High mode, input 0 V to V _{DDA} -0.2 V |
| SID288A | V _{OS_TR} | Offset voltage, trimmed | – | ±1 | – | | Medium mode, input 0 V to V _{DDA} -0.2 V |
| SID288B | V _{OS_TR} | Offset voltage, trimmed | – | ±2 | – | | Low mode, input 0 V to V _{DDA} -0.2 V |
| SID290 | V _{OS_DR_TR} | Offset voltage drift, trimmed | –10 | ±3 | 10 | µV/°C | High mode |
| SID290A | V _{OS_DR_TR} | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Medium mode |
| SID290B | V _{OS_DR_TR} | Offset voltage drift, trimmed | – | ±10 | – | | Low mode |
| SID291 | CMRR | DC | 70 | 80 | – | dB | Input is 0 V to V _{DDA} -0.2 V, Output is 0.2 V to V _{DDA} -0.2 V |
| SID292 | PSRR | At 1 kHz, 10-mV ripple | 70 | 85 | – | | V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} -0.2 V |
| | Noise | | | | | | |
| SID294 | VN2 | Input-referred, 1 kHz, power = Hi | – | 72 | – | nV/rHz | Input and output are at 0.2 V to V _{DDA} -0.2 V |
| SID295 | VN3 | Input-referred, 10 kHz, power = Hi | – | 28 | – | | Input and output are at 0.2 V to V _{DDA} -0.2 V |
| SID296 | VN4 | Input-referred, 100 kHz, power = Hi | – | 15 | – | | Input and output are at 0.2 V to V _{DDA} -0.2 V |
| SID297 | C _{LOAD} | Stable up to max. load. Performance specs at 50 pF. | – | – | 125 | pF | – |
| SID298 | SLEW_RATE | Cload = 50 pF, Power = High, V _{DDA} = 2.7 V | 6 | – | – | V/µs | – |
| SID299 | T _{OP_WAKE} | From disable to enable, no external RC dominating | – | – | 25 | µs | – |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | |
| | COMP_MODE | Comparator mode; 50 mV drive, T _{rise} =T _{fall} (approx.) | | | | | |

Table 8. CTBm Opamp Specifications *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------|------------------------|--|-----|------|-----|-------|--|
| SID300 | TPD1 | Response time; power=hi | – | 150 | – | ns | Input is 0.2 V to $V_{DDA}-0.2$ V |
| SID301 | TPD2 | Response time; power=med | – | 500 | – | | Input is 0.2 V to $V_{DDA}-0.2$ V |
| SID302 | TPD3 | Response time; power=lo | – | 2500 | – | | Input is 0.2 V to $V_{DDA}-0.2$ V |
| SID303 | VHYST_OP | Hysteresis | – | 10 | – | mV | – |
| SID304 | WUP_CTB | Wake-up time from Enabled to Usable | – | – | 25 | µs | – |
| | Deep Sleep Mode | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | |
| SID_DS_1 | I _{DD_HI_M1} | Mode 1, High current | – | 1400 | – | µA | 25 °C |
| SID_DS_2 | I _{DD_MED_M1} | Mode 1, Medium current | – | 700 | – | | 25 °C |
| SID_DS_3 | I _{DD_LOW_M1} | Mode 1, Low current | – | 200 | – | | 25 °C |
| SID_DS_4 | I _{DD_HI_M2} | Mode 2, High current | – | 120 | – | | 25 °C |
| SID_DS_5 | I _{DD_MED_M2} | Mode 2, Medium current | – | 60 | – | | 25 °C |
| SID_DS_6 | I _{DD_LOW_M2} | Mode 2, Low current | – | 15 | – | | 25 °C |
| SID_DS_7 | G _{BW_HI_M1} | Mode 1, High current | – | 4 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_8 | G _{BW_MED_M1} | Mode 1, Medium current | – | 2 | – | | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_9 | G _{BW_LOW_M1} | Mode 1, Low current | – | 0.5 | – | | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_10 | G _{BW_HI_M2} | Mode 2, High current | – | 0.5 | – | | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_11 | G _{BW_MED_M2} | Mode 2, Medium current | – | 0.2 | – | | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_12 | G _{BW_Low_M2} | Mode 2, Low current | – | 0.1 | – | | 20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_13 | V _{OS_HI_M1} | Mode 1, High current | – | 5 | – | mV | With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_14 | V _{OS_MED_M1} | Mode 1, Medium current | – | 5 | – | | With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_15 | V _{OS_LOW_M2} | Mode 1, Low current | – | 5 | – | | With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_16 | V _{OS_HI_M2} | Mode 2, High current | – | 5 | – | | With trim 25 °C, 0.2V to $V_{DDA}-0.2$ V |
| SID_DS_17 | V _{OS_MED_M2} | Mode 2, Medium current | – | 5 | – | | With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V |
| SID_DS_18 | V _{OS_LOW_M2} | Mode 2, Low current | – | 5 | – | | With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V |

Table 8. CTBm Opamp Specifications *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|-----------|-------------------------|------------------------|-----|-----|-----|-------|--|
| SID_DS_19 | I _{OUT_HI_M1} | Mode 1, High current | – | 10 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_20 | I _{OUT_MED_M1} | Mode 1, Medium current | – | 10 | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_21 | I _{OUT_LOW_M1} | Mode 1, Low current | – | 4 | – | | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_22 | I _{OUT_HI_M2} | Mode 2, High current | – | 1 | – | | |
| SID_DS_23 | I _{OUT_MED_M2} | Mode 2, Medium current | – | 1 | – | | |
| SID_DS_24 | I _{OUT_LOW_M2} | Mode 2, Low current | – | 0.5 | – | | |

Comparator

Table 9. Comparator DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|----------------------|---|-----|-----|------------------------|-------|------------------------------------|
| SID84 | V _{OFFSET1} | Input offset voltage, Factory trim | – | – | ±10 | mV | |
| SID85 | V _{OFFSET2} | Input offset voltage, Custom trim | – | – | ±4 | | |
| SID86 | V _{HYST} | Hysteresis when enabled | – | 10 | 35 | | |
| SID87 | V _{ICM1} | Input common mode voltage in normal mode | 0 | – | V _{DDD} -0.1 | V | Modes 1 and 2 |
| SID247 | V _{ICM2} | Input common mode voltage in low power mode | 0 | – | V _{DDD} | | |
| SID247A | V _{ICM3} | Input common mode voltage in ultra low power mode | 0 | – | V _{DDD} -1.15 | | V _{DDD} ≥ 2.2 V at –40 °C |
| SID88 | C _{MRR} | Common mode rejection ratio | 50 | – | – | dB | V _{DDD} ≥ 2.7V |
| SID88A | C _{MRR} | Common mode rejection ratio | 42 | – | – | | V _{DDD} ≤ 2.7V |
| SID89 | I _{CMP1} | Block current, normal mode | – | – | 400 | μA | |
| SID248 | I _{CMP2} | Block current, low power mode | – | – | 100 | | |
| SID259 | I _{CMP3} | Block current in ultra low-power mode | – | – | 6 | | V _{DDD} ≥ 2.2 V at –40 °C |
| SID90 | Z _{CMP} | DC Input impedance of comparator | 35 | – | – | MΩ | |

Table 10. Comparator AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------|---|-----|-----|-----|-------|------------------------------------|
| SID91 | TRESP1 | Response time, normal mode, 50 mV overdrive | – | 38 | 110 | ns | |
| SID258 | TRESP2 | Response time, low power mode, 50 mV overdrive | – | 70 | 200 | | |
| SID92 | TRESP3 | Response time, ultra-low power mode, 200 mV overdrive | – | 2.3 | 15 | μs | V _{DDD} ≥ 2.2 V at –40 °C |

Note

6. Guaranteed by characterization.

Temperature Sensor

Table 11. Temperature Sensor Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------|-----------------------------|-----|-----|-----|-------|----------------------|
| SID93 | TSENSACC | Temperature sensor accuracy | -5 | ±1 | 5 | °C | -40 to +85 °C |

SAR ADC

Table 12. SAR ADC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------------------|------------|--|-----------------|-----|----------------------|-------|--|
| SAR ADC DC Specifications | | | | | | | |
| SID94 | A_RES | Resolution | – | – | 12 | bits | |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 4 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | | Yes |
| SID98 | A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR | Current consumption | – | – | 1 | mA | |
| SID101 | A_VINS | Input voltage range - single ended | V _{SS} | – | V _{DDA} | V | |
| SID102 | A_VIND | Input voltage range - differential | V _{SS} | – | V _{DDA} | V | |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | KΩ | |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | |
| SID260 | VREFSAR | Trimmed internal reference to SAR | – | – | TBD | V | |
| SAR ADC AC Specifications | | | | | | | |
| SID106 | A_PSRR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| SID108 | A_SAMP | Sample rate | – | – | 1 | Msp/s | |
| SID109 | A_SNR | Signal-to-noise and distortion ratio (SINAD) | 65 | – | – | dB | F _{IN} = 10 kHz |
| SID110 | A_BW | Input bandwidth without aliasing | – | – | A _{samp} /2 | kHz | |
| SID111 | A_INL | Integral non linearity. V _{DD} = 1.71 to 5.5, 1 Msp/s | -1.7 | – | 2 | LSB | V _{REF} = 1 to V _{DD} |
| SID111A | A_INL | Integral non linearity. V _{DD} = 1.71 to 3.6, 1 Msp/s | -1.5 | – | 1.7 | LSB | V _{REF} = 1.71 to V _{DD} |
| SID111B | A_INL | Integral non linearity. V _{DD} = 1.71 to 5.5, 500 ksp/s | -1.5 | – | 1.7 | LSB | V _{REF} = 1 to V _{DD} |
| SID112 | A_DNL | Differential non linearity. V _{DD} = 1.71 to 5.5, 1 Msp/s | -1 | – | 2.2 | LSB | V _{REF} = 1 to V _{DD} |
| SID112A | A_DNL | Differential non linearity. V _{DD} = 1.71 to 3.6, 1 Msp/s | -1 | – | 2 | LSB | V _{REF} = 1.71 to V _{DD} |
| SID112B | A_DNL | Differential non linearity. V _{DD} = 1.71 to 5.5, 500 ksp/s | -1 | – | 2.2 | LSB | V _{REF} = 1 to V _{DD} |
| SID113 | A_THD | Total harmonic distortion | – | – | -65 | dB | F _{IN} = 10 kHz |
| SID261 | FSARINTREF | SAR operating speed without external reference bypass | – | – | 100 | ksp/s | 12-bit resolution |

CSD and IDAC

Table 13. CSD and IDAC Specifications

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|-------------|----------------|--|------|-----|-----------------|-------|---|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD} > 2\text{ V}$ (with ripple), 25°C T_A , Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD} > 1.75\text{V}$ (with ripple), 25°C T_A , Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | μA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator |
| SID.CSD#15 | V_{REF} | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.06$ or 4.4, whichever is lower |
| SID.CSD#15A | VREF_EXT | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.06$ or 4.4, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | μA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | μA | |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.06$ or 4.4, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$ |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$ |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | μA | LSB = 37.5-nA typ |
| SID314A | IDAC1CRT2 | Output current of IDAC1(7 bits) in medium range | 34 | – | 41 | μA | LSB = 300-nA typ |
| SID314B | IDAC1CRT3 | Output current of IDAC1(7 bits) in high range | 275 | – | 330 | μA | LSB = 2.4-μA typ |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | μA | LSB = 75-nA typ |
| SID314D | IDAC1CRT22 | Output current of IDAC1(7 bits) in medium range, 2X mode | 69 | – | 82 | μA | LSB = 600-nA typ. |
| SID314E | IDAC1CRT32 | Output current of IDAC1(7 bits) in high range, 2X mode | 540 | – | 660 | μA | LSB = 4.8-μA typ |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | μA | LSB = 37.5-nA typ |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | μA | LSB = 300-nA typ |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | μA | LSB = 2.4-μA typ |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | μA | LSB = 75-nA typ |
| SID315D | IDAC2CRT22 | Output current of IDAC2(7 bits) in medium range, 2X mode | 69 | – | 82 | μA | LSB = 600-nA typ |
| SID315E | IDAC2CRT32 | Output current of IDAC2(7 bits) in high range, 2X mode | 540 | – | 660 | μA | LSB = 4.8-μA typ |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | μA | LSB = 37.5-nA typ |

Table 13. CSD and IDAC Specifications (continued)

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|---------------|--|-----|-----|-----|-------|---|
| SID315G | IDAC3CRT23 | Output current of IDAC in 8-bit mode in medium range | 69 | – | 82 | µA | LSB = 300-nA typ |
| SID315H | IDAC3CRT33 | Output current of IDAC in 8-bit mode in high range | 540 | – | 660 | µA | LSB = 2.4-µA typ |
| SID320 | IDACOFFSET | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode |
| SID321 | IDACGAIN | Full-scale error less offset | – | – | ±10 | % | |
| SID322 | IDACMISMATCH1 | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ |
| SID322A | IDACMISMATCH2 | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 5.6 | LSB | LSB = 300-nA typ |
| SID322B | IDACMISMATCH3 | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 6.8 | LSB | LSB = 2.4-µA typ |
| SID323 | IDACSET8 | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 5 | µs | Full-scale transition. No external load |
| SID324 | IDACSET7 | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 5 | µs | Full-scale transition. No external load |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap |

10-bit CapSense ADC

Table 14. 10-bit CapSense ADC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------|--|------------------|-----|------------------|-------|---|
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SIDA95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | Defined by AMUX Bus |
| SIDA97 | A-MONO | Monotonicity | – | – | – | Yes | |
| SIDA98 | A_GAINERR | Gain error | – | – | ±3 | % | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF |
| SIDA99 | A_OFFSET | Input offset voltage | – | – | ±18 | mV | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF |
| SIDA100 | A_ISAR | Current consumption | – | – | 0.25 | mA | |
| SIDA101 | A_VINS | Input voltage range - single ended | V _{SSA} | – | V _{DDA} | V | |
| SIDA103 | A_INRES | Input resistance | – | 2.2 | – | KΩ | |
| SIDA104 | A_INCAP | Input capacitance | – | 20 | – | pF | |
| SIDA106 | A_PSR | Power supply rejection ratio | – | 60 | – | dB | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 µF |
| SIDA107 | A_TACQ | Sample acquisition time | – | 1 | – | µs | |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = F _{hclk} /(2 ^{N+2}). Clock frequency = 48 MHz. | – | – | 21.3 | µs | Does not include acquisition time. Equivalent to 44.8 ksp/s including acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = F _{hclk} /(2 ^{N+2}). Clock frequency = 48 MHz. | – | – | 85.3 | µs | Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time. |

Table 14. 10-bit CapSense ADC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-----------|--|-----|-----|------|-------|---|
| SIDA109 | A_SND | Signal-to-noise and Distortion ratio (SINAD) | – | 61 | – | dB | With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode |
| SIDA110 | A_BW | Input bandwidth without aliasing | – | – | 22.4 | KHz | 8-bit resolution |
| SIDA111 | A_INL | Integral Non Linearity. 1 ksp | – | – | 2 | LSB | V _{REF} = 2.4 V or greater |
| SIDA112 | A_DNL | Differential Non Linearity. 1 ksp | – | – | 1 | LSB | |

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 15. TCPWM Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------------------|-------------------------------------|------------------|-----|----------------|-------|--|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | μA | All modes (TCPWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | – | – | 155 | | All modes (TCPWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | – | – | 650 | | All modes (TCPWM) |
| SID.TCPWM.3 | TCPWM _{FREQ} | Operating frequency | – | – | F _c | MHz | F _c max = CLK_SYS Maximum = 48 MHz |
| SID.TCPWM.4 | TPWM _{ENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events ^[7] |
| SID.TCPWM.5 | TPWM _{EXT} | Output trigger pulse widths | 2/F _c | – | – | | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | TC _{RES} | Resolution of counter | 1/F _c | – | – | | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | | Minimum pulse width between Quadrature phase inputs |

²C

Table 16. Fixed I²C DC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---|-----|-----|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 50 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | 1 | – | | |

Table 17. Fixed I²C AC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Msp | – |

Note

7. Guaranteed by characterization.

SPI

Table 18. SPI DC Specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID163 | ISPI1 | Block current consumption at 1 Mbps | – | – | 360 | μA | – |
| SID164 | ISPI2 | Block current consumption at 4 Mbps | – | – | 560 | | – |
| SID165 | ISPI3 | Block current consumption at 8 Mbps | – | – | 600 | | – |

Table 19. SPI AC Specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------|--|-----|-----|-------------|-------|---------------------------------------|
| SID166 | FSPI | SPI Operating frequency (Master; 6X Oversampling) | – | – | 8 | MHz | |
| Fixed SPI Master Mode AC Specifications | | | | | | | |
| SID167 | TDMO | MOSI Valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | TDSI | MISO Valid before SClock capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | THMO | Previous MOSI data hold time | 0 | – | – | | Referred to Slave capturing edge |
| Fixed SPI Slave Mode AC Specifications | | | | | | | |
| SID170 | TDMI | MOSI Valid before Scklock Capturing edge | 40 | – | – | ns | – |
| SID171 | TDSO | MISO Valid after Scklock driving edge | – | – | 42 + 3*Tcpu | | T _{CPU} = 1/F _{CPU} |
| SID171A | TDSO_EXT | MISO Valid after Scklock driving edge in Ext. Clk mode | – | – | 48 | | – |
| SID172 | THSO | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | TSSELSSCK | SSEL Valid to first SCK Valid edge | – | – | 100 | ns | – |

UART

Table 20. UART DC Specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|--|-----|-----|-----|-------|--------------------|
| SID160 | I _{UART1} | Block current consumption at 100 Kbps | – | – | 55 | μA | – |
| SID161 | I _{UART2} | Block current consumption at 1000 Kbps | – | – | 312 | μA | – |

Table 21. UART AC Specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | – |

Note

8. Guaranteed by characterization.

LCD Direct Drive

Table 22. LCD Direct Drive DC Specifications^[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------|---|-----|-----|------|---------|-------------------------------------|
| SID154 | I_{LCDLOW} | Operating current in low power mode | – | 5 | – | μA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | C_{LCDCAP} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | LCD_{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | I_{LCDOP1} | LCD system operating current V_{bias} = 5 V | – | 2 | – | mA | 32 × 4 segments at 50 Hz 25 °C |
| SID158 | I_{LCDOP2} | LCD system operating current V_{bias} = 3.3 V | – | 2 | – | | 32 × 4 segments at 50 Hz 25 °C |

Table 23. LCD Direct Drive AC Specifications^[9]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|----------------|-----|-----|-----|-------|--------------------|
| SID159 | F_{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Note

9. Guaranteed by characterization.

Memory

Table 24. Flash DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------|------|-----|-----|-------|--------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | – |

Table 25. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|---|---|-------|-----|-----|---------|--------------------------|
| SID174 | T _{ROWWRITE} ^[10] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 256 bytes |
| SID175 | T _{ROWERASE} ^[10] | Row erase time | – | – | 16 | | – |
| SID176 | T _{ROWPROGRAM} ^[10] | Row program time after erase | – | – | 4 | | – |
| SID178 | T _{BULKERASE} ^[10] | Bulk erase time (64 KB) | – | – | 35 | | – |
| SID180 ^[11] | T _{DEVPROG} ^[10] | Total device program time | – | – | 7 | Seconds | – |
| SID181 ^[11] | F _{END} | Flash endurance | 100 K | – | – | Cycles | – |
| SID182 ^[11] | F _{RET} | Flash retention. T _A ≤ 55 °C, 100 K P/E cycles | 20 | – | – | Years | – |
| SID182A ^[11] | – | Flash retention. T _A ≤ 85 °C, 10 K P/E cycles | 10 | – | – | | – |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |

System Resources

Power-on Reset (POR)

Table 26. Power On Reset (PRES)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|-----------------------|------------------------|------|-----|-----|-------|--------------------|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185 ^[11] | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186 ^[11] | V _{FALLIPOR} | Falling trip voltage | 0.70 | – | 1.4 | | – |

Table 27. Brown-out Detect (BOD) for V_{CCD}

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|--|------|-----|------|-------|--------------------|
| SID190 ^[11] | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192 ^[11] | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

11. Guaranteed by characterization.

SWD Interface

Table 28. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|--------------|---|----------------|-----|---------------|-------|---------------------------------------|
| SID213 | F_SWCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | | SWDCLK \leq 1/3 CPU clock frequency |
| SID215 ^[12] | T_SWDI_SETUP | $T = 1/f_{\text{SWDCLK}}$ | $0.25 \cdot T$ | – | – | ns | – |
| SID216 ^[12] | T_SWDI_HOLD | $T = 1/f_{\text{SWDCLK}}$ | $0.25 \cdot T$ | – | – | | – |
| SID217 ^[12] | T_SWDO_VALID | $T = 1/f_{\text{SWDCLK}}$ | – | – | $0.5 \cdot T$ | | – |
| SID217A ^[12] | T_SWDO_HOLD | $T = 1/f_{\text{SWDCLK}}$ | 1 | – | – | | – |

Internal Main Oscillator

Table 29. IMO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|-----|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | – | – | 250 | μA | – |
| SID219 | I _{IMO2} | IMO operating current at 24 MHz | – | – | 180 | μA | – |

Table 30. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|---|-----|-----|-----|-------|--------------------|
| SID223 | F _{IMOTOL1} | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2 | % | |
| SID226 | T _{STARTIMO} | IMO startup time | – | – | 7 | μs | – |
| SID228 | T _{JITRMSIMO2} | RMS jitter at 24 MHz | – | 145 | – | ps | – |

Internal Low-Speed Oscillator

Table 31. ILO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-----------------------|-----|-----|------|-------|--------------------|
| SID231 | I _{ILO1} | ILO operating current | – | 0.3 | 1.05 | μA | – |

Table 32. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|---------------------|-----|-----|-----|-------|--------------------|
| SID234 ^[12] | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | – |
| SID236 ^[12] | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | F _{ILOTRIM1} | ILO frequency range | 20 | 40 | 80 | kHz | – |

Note

12. Guaranteed by design.

Watch Crystal Oscillator (WCO)

Table 33. WCO Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------|-------------------------------------|-----|--------|------|-------|----------------------|
| SID398 | FWCO | Crystal frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | μW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal Load Capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal Shunt Capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating Current (high power mode) | – | – | 8 | uA | |

External Clock

Table 34. External Clock Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------|--|-----|-----|-----|-------|--------------------|
| SID305 ^[13] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306 ^[13] | ExtClkDuty | Duty cycle; measured at V _{DD} /2 | 45 | – | 55 | % | – |

External Crystal Oscillator and PLL

Table 35. External Crystal Oscillator (ECO) Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|-----------|--------------------------------|-----|-----|-----|-------|--------------------|
| SID316 ^[13] | IECO1 | External clock input frequency | – | – | 1.5 | mA | – |
| SID317 ^[13] | FECO | Crystal frequency range | 4 | – | 33 | MHz | – |

Table 36. PLL Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|------------|--|------|-----|-----|-------|----------------------|
| SID410 | IDD_PLL_48 | In = 3 MHz, Out = 48 MHz | – | 530 | 610 | uA | |
| SID411 | IDD_PLL_24 | In = 3 MHz, Out = 24 MHz | – | 300 | 405 | uA | |
| SID412 | Fp1lin | PLL input frequency | 1 | – | 48 | MHz | |
| SID413 | Fp1int | PLL intermediate frequency; prescaler out | 1 | – | 3 | MHz | |
| SID414 | Fp1vco | VCO output frequency before post-divide | 22.5 | – | 104 | MHz | |
| SID415 | Divvco | VCO Output post-divider range; PLL output frequency is Fp1vco/Divvco | 1 | – | 8 | | |
| SID416 | P1locktime | Lock time at startup | – | – | 250 | μs | |
| SID417 | Jperiod_1 | Period jitter for VCO ≥ 67 MHz | – | – | 150 | ps | Guaranteed by design |
| SID416A | Jperiod_2 | Period jitter for VCO ≤ 67 MHz | – | – | 200 | ps | Guaranteed by design |

System Clock

Table 37. Block Specs

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|------------------------------------|-----|-----|-----|---------|--------------------|
| SID262 ^[13] | T _{CLKSWITCH} | System clock source switching time | 3 | – | 4 | Periods | – |

Note

13. Guaranteed by characterization.

Smart I/O

Table 38. Smart I/O Pass-through Time (Delay in Bypass Mode)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|------------|---|-----|-----|-----|-------|----------------------|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

CAN

Table 39. CAN Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|---------------------------|-----|-----|-----|-------|--------------------|
| SID420 | IDD_CAN | Block current consumption | – | – | 200 | μA | |
| SID421 | CAN_bits | CAN Bit rate | – | – | 1 | Mbps | Min 8-MHZ clock |

Ordering Information

The marketing part numbers for the PSoC 4100S Plus devices are listed in the following table.

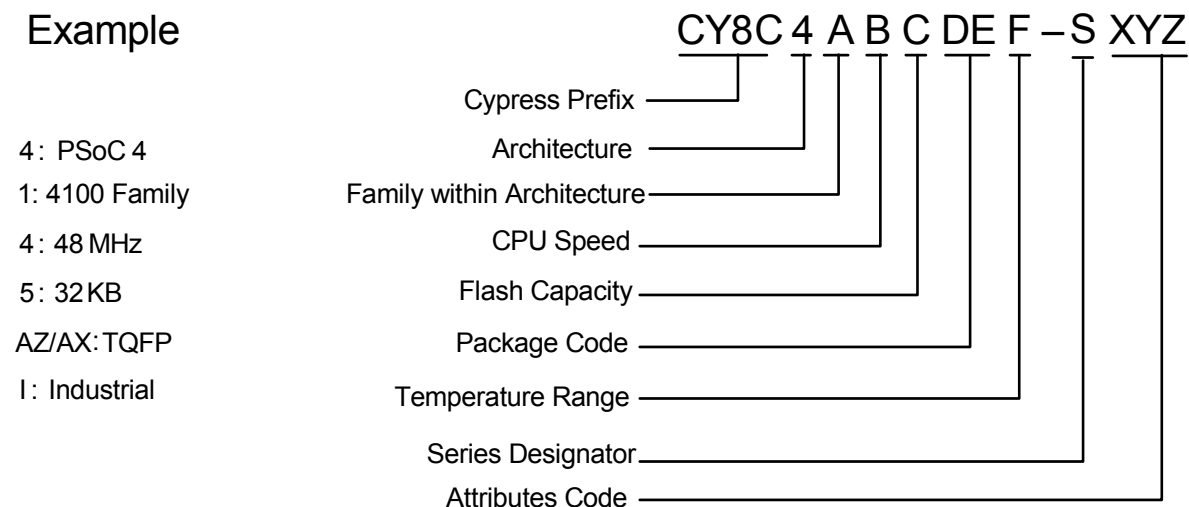
| Category | MPN | Features | | | | | | | | | | | | | | | Packages | | |
|----------|------------------|---------------------|------------|-----------|---------------|-----|----------------|----------------|---------------------|----------------|--------------|------------|-----|----------------|------------|------|------------------------|------------------------|------------------------|
| | | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | Op-amp (CTBm) | CSD | 10-bit CSD ADC | 12-bit SAR ADC | SAR ADC Sample Rate | LP Comparators | TCPWM Blocks | SCB Blocks | ECO | CAN Controller | Smart I/Os | GPIO | 44-TQFP (0.8-mm pitch) | 64-TQFP (0.5-mm pitch) | 64-TQFP (0.8-mm pitch) |
| 4126 | CY8C4126AXI-S443 | 24 | 64 | 8 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4126AZI-S445 | 24 | 64 | 8 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4126AXI-S445 | 24 | 64 | 8 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| | CY8C4126AZI-S455 | 24 | 64 | 8 | 2 | 1 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4126AXI-S455 | 24 | 64 | 8 | 2 | 1 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| 4146 | CY8C4146AXI-S443 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4146AZI-S445 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4146AXI-S445 | 48 | 64 | 8 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| | CY8C4146AXI-S453 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4146AZI-S455 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4146AXI-S455 | 48 | 64 | 8 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| 4127 | CY8C4127AXI-S443 | 24 | 128 | 16 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4127AZI-S445 | 24 | 128 | 16 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4127AXI-S445 | 24 | 128 | 16 | 2 | 0 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| | CY8C4127AXI-S453 | 24 | 128 | 16 | 2 | 1 | 1 | 1 | 806 ksp/s | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4127AZI-S455 | 24 | 128 | 16 | 2 | 1 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4127AXI-S455 | 24 | 128 | 16 | 2 | 1 | 1 | 1 | 806 ksp/s | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| 4147 | CY8C4147AXI-S443 | 48 | 128 | 16 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4147AZI-S445 | 48 | 128 | 16 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4147AXI-S445 | 48 | 128 | 16 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| | CY8C4147AXI-S453 | 48 | 128 | 16 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 4 | ✓ | 0 | 24 | 36 | ✓ | – | – |
| | CY8C4147AZI-S455 | 48 | 128 | 16 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | ✓ | – |
| | CY8C4147AXI-S455 | 48 | 128 | 16 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 0 | 24 | 54 | – | – | ✓ |
| | CY8C4147AZI-S465 | 48 | 128 | 16 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 1 | 24 | 54 | – | ✓ | – |
| | CY8C4147AXI-S465 | 48 | 128 | 16 | 2 | 0 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 1 | 24 | 54 | – | – | ✓ |
| | CY8C4147AZI-S475 | 48 | 128 | 16 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 1 | 24 | 54 | – | ✓ | – |
| | CY8C4147AXI-S475 | 48 | 128 | 16 | 2 | 1 | 1 | 1 | 1 Msps | 2 | 8 | 5 | ✓ | 1 | 24 | 54 | – | – | ✓ |

The nomenclature used in the preceding table is based on the following part numbering convention:

| Field | Description | Values | Meaning |
|-------|-------------------|---------|--|
| CY8C | Cypress Prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family | 1 | 4100 Family |
| B | CPU Speed | 2 | 24 MHz |
| | | 4 | 48 MHz |
| C | Flash Capacity | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package Code | AX | TQFP (0.8-mm pitch) |
| | | AZ | TQFP (0.5-mm pitch) |
| | | LQ | QFN |
| | | PV | SSOP |
| | | FN | CSP |
| F | Temperature Range | I | Industrial |
| S | Series Designator | S | PSoC 4 S-Series |
| | | M | PSoC 4 M-Series |
| | | L | PSoC 4 L-Series |
| | | BL | PSoC 4 BLE-Series |
| XYZ | Attributes Code | 000-999 | Code of feature set in the specific family |

The following is an example of a part number:

Example



Packaging

The PSoC 4100S Plus will be offered in 44 TQFP, 64 TQFP Normal pitch, and 64 TQFP Fine Pitch packages.

Package dimensions and Cypress drawing numbers are in the following table.

Table 40. Package List

| Spec ID# | Package | Description | Package Dwg |
|----------|-------------|---|-------------|
| BID20 | 64-pin TQFP | 14 × 14 × 1.4-mm height with 0.8-mm pitch | 51-85046 |
| BID27 | 64-pin TQFP | 10 × 10 × 1.6-mm height with 0.5-mm pitch | 51-85051 |
| BID34A | 44-pin TQFP | 10 × 10 × 1.4-mm height with 0.8-mm pitch | 51-85064 |

Table 41. Package Thermal Characteristics

| Parameter | Description | Package | Min | Typ | Max | Units |
|-----------------|--------------------------------|----------------------------|-----|------|-----|---------|
| T _A | Operating ambient temperature | | −40 | 25 | 85 | °C |
| T _J | Operating junction temperature | | −40 | – | 100 | °C |
| T _{JA} | Package θ _{JA} | 44-pin TQFP | – | 55.6 | – | °C/Watt |
| T _{JC} | Package θ _{JC} | 44-pin TQFP | – | 14.4 | – | °C/Watt |
| T _{JA} | Package θ _{JA} | 64-pin TQFP (0.5-mm pitch) | – | 46 | – | °C/Watt |
| T _{JC} | Package θ _{JC} | 64-pin TQFP (0.5-mm pitch) | – | 10 | – | °C/Watt |
| T _{JA} | Package θ _{JA} | 64-pin TQFP (0.8-mm pitch) | – | 36.8 | – | °C/Watt |
| T _{JC} | Package θ _{JC} | 64-pin TQFP (0.8-mm pitch) | – | 9.4 | – | °C/Watt |

Table 42. Solder Reflow Peak Temperature

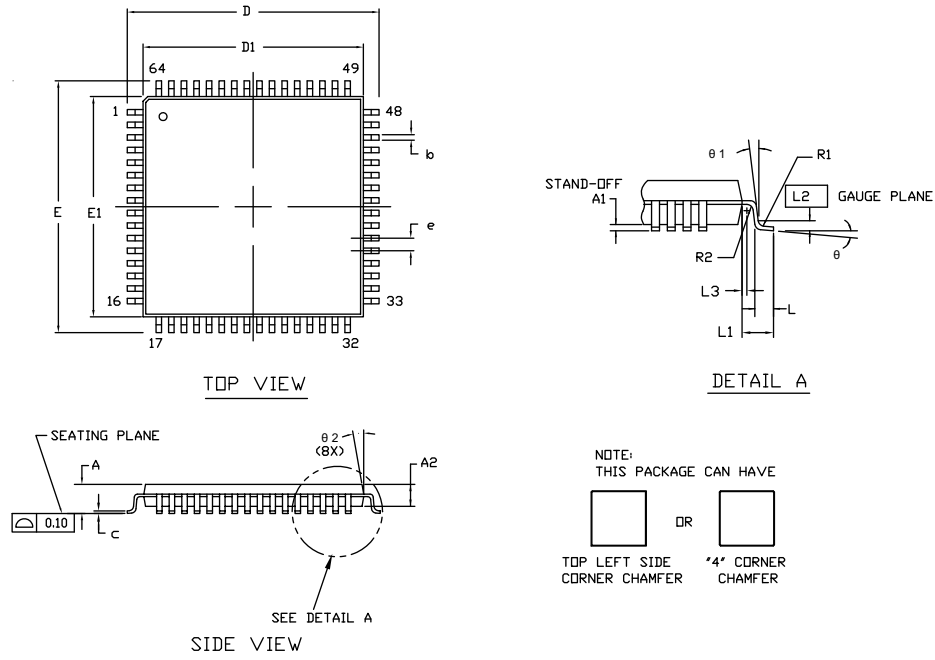
| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------|--------------------------|----------------------------------|
| All | 260 °C | 30 seconds |

Table 43. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

| Package | MSL |
|---------|-------|
| All | MSL 3 |

Package Diagrams

Figure 7. 64-pin TQFP Package (0.8-mm Pitch) Outline

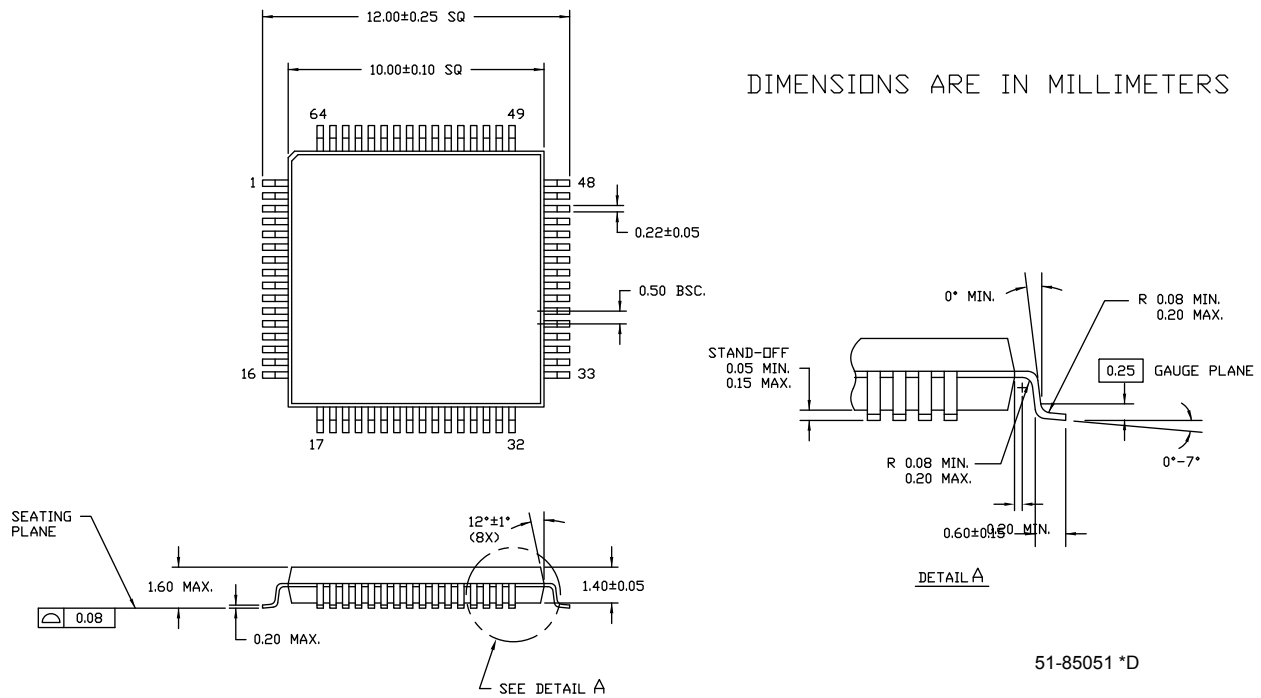
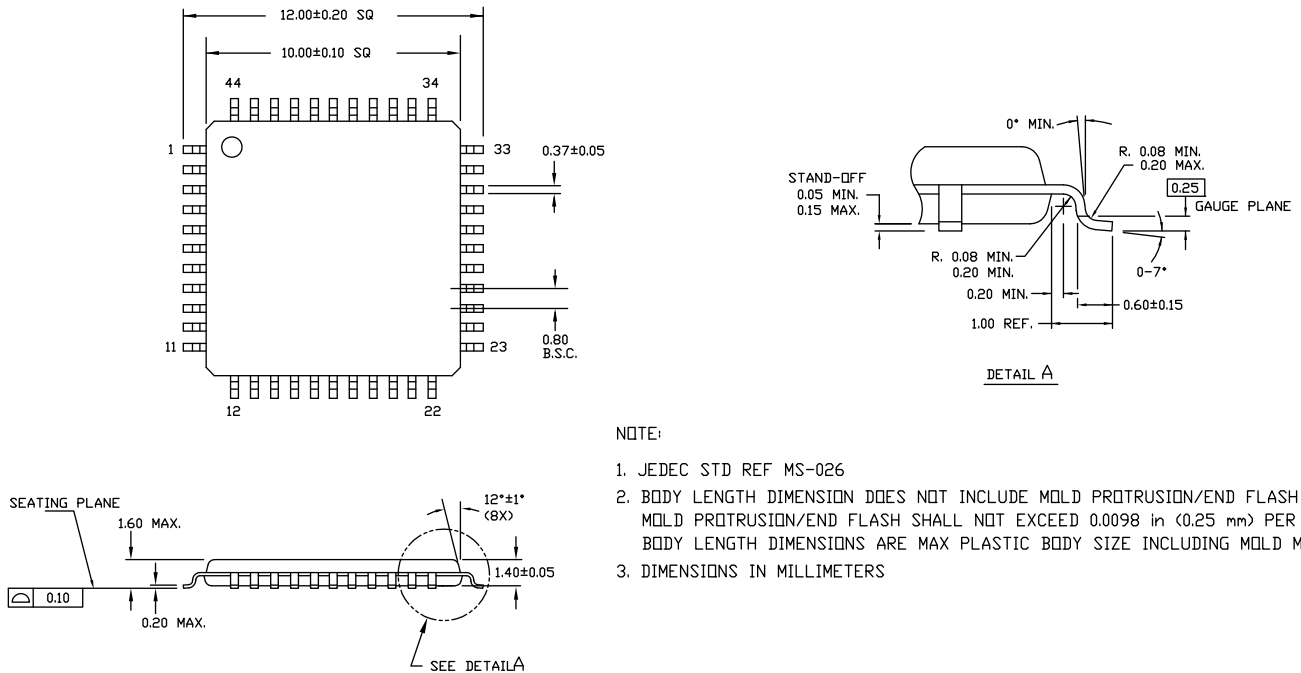


| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 15.75 | 16.00 | 16.25 |
| D1 | 13.95 | 14.00 | 14.05 |
| E | 15.75 | 16.00 | 16.25 |
| E1 | 13.95 | 14.00 | 14.05 |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | — | 7° |
| θ1 | 0° | — | — |
| θ2 | 11° | 12° | 13° |
| c | — | — | 0.20 |
| b | 0.30 | 0.35 | 0.40 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| L3 | 0.20 | — | — |
| e | 0.80 TYP | | |

NOTE:

- JEDEC STD REF MS-026
- BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
- DIMENSIONS IN MILLIMETERS

51-85046 *H

Figure 8. 64-pin TQFP Package (0.5-mm Pitch) Outline

Figure 9. 44-Pin TQFP Package Outline


51-85064 *G

Acronyms

Table 44. Acronyms Used in this Document

| Acronym | Description |
|---------|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

Table 44. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|--------------------------|--|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

Table 44. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

Table 44. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

Document Conventions

Units of Measure

Table 45. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Revision History

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|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *E | 5995731 | WKA | 12/15/2017 | New release |
| *F | 6069640 | JIAO | 02/13/2018 | Updated Pinouts and DC Specifications . |
| *G | 6169676 | WKA | 05/09/2018 | Updated Clock Diagram to show Watchdog details and clock divider information. Removed preliminary statement in Pinouts . |

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