4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5 μA
  - Maximum standby current: 8.7 μA
- Embedded ECC for single-bit error correction[1]
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

CY62146G/CY62146GE and CY62146GSL/CY62146GESL are high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62146GE/CY62146GESL device includes an ERR pin that signals an error-detection and correction event during a read cycle. The CY62146GSL/CY62146GESL[1] device supports a wide voltage range of 2.2 V–3.6 V and 4.5 V–5.5 V.

Devices with a single chip enable input are accessed by asserting the chip enable ($\overline{CE}$) input LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – $\overline{CE}_1$ as low and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on I/O_0 through I/O_{15} and address on A_0 through A_{17} pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control write operations to the upper and lower bytes of the specified memory location. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH/CE_2 LOW for a dual chip enable device), or control signals are deasserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

On the CY62146GE/CY62146GESL devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)[2]. See the Truth Table – CY62146G/CY62146GE/CY62146GSL/CY62146GESL on page 17 for a complete description of read and write modes.

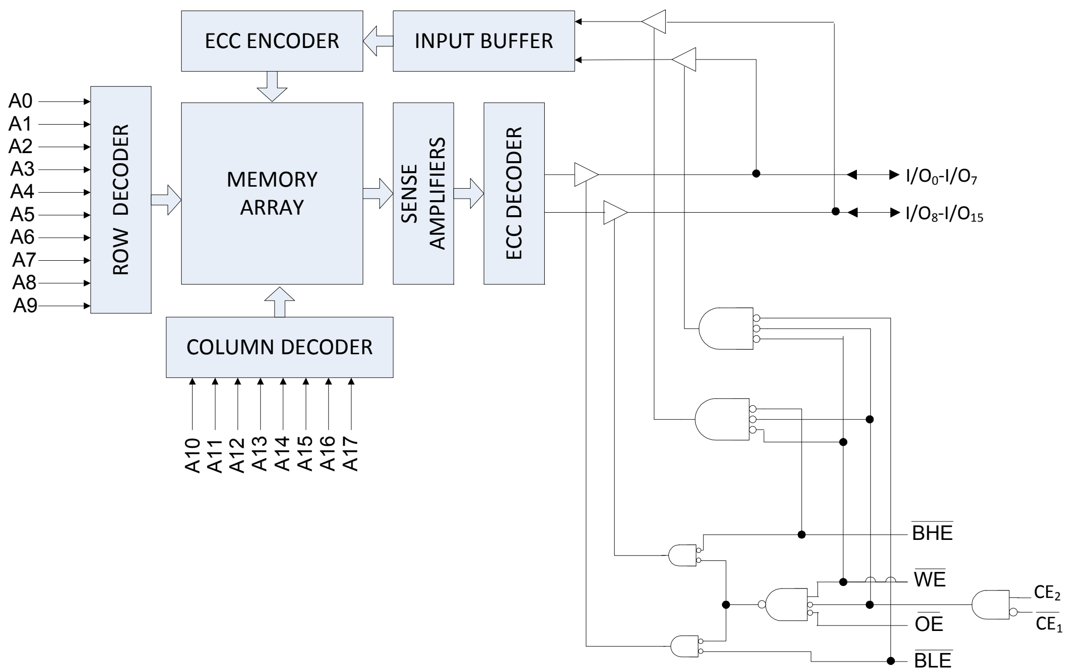
The logic block diagrams are on page 2.

Product Portfolio

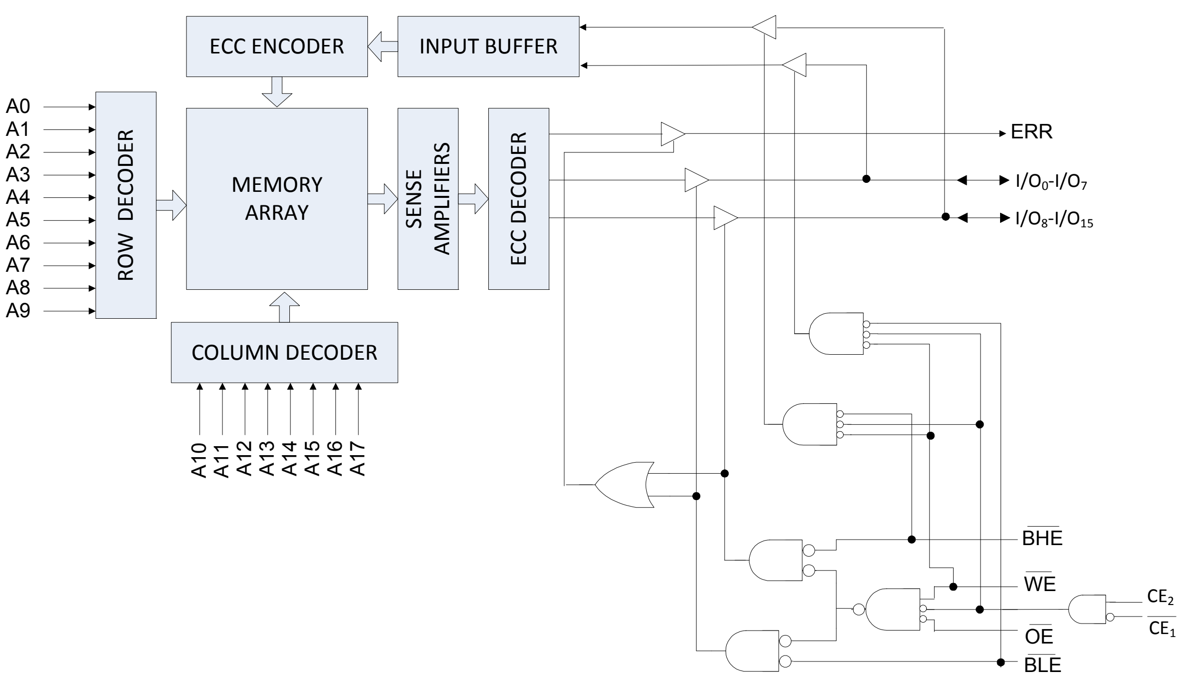
Product[3]	Features and Options (see the Pin Configurations section)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA) $f = f_{max}$		Standby, I_{SB2} (μA)	
					Typ[4]	Max	Typ[4]	Max
CY62146G(E)18	Single or dual Chip Enables	Industrial	1.65 V–2.2 V	55	15	20	3.5	10
CY62146G(E)30			2.2 V–3.6 V	45	15	20	3.5	8.7
CY62146G(E)	Optional ERR pin		4.5 V–5.5 V					
CY62146G(E)SL[5]			2.2 V–3.6 V and 4.5 V–5.5 V					

Notes
1. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
2. This device does not support automatic write-back on error detection.
3. The ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer Ordering Information for details.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
5. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.

Logic Block Diagram – CY62146G/CY62146GSL



Logic Block Diagram – CY62146GE/CY62146GESL



Contents

Pin Configuration – CY62146G/CY62146GSL

Figure 1. 48-ball VFBGA pinout (Dual Chip Enable without ERR) – CY62146G/CY62146GSL [6]

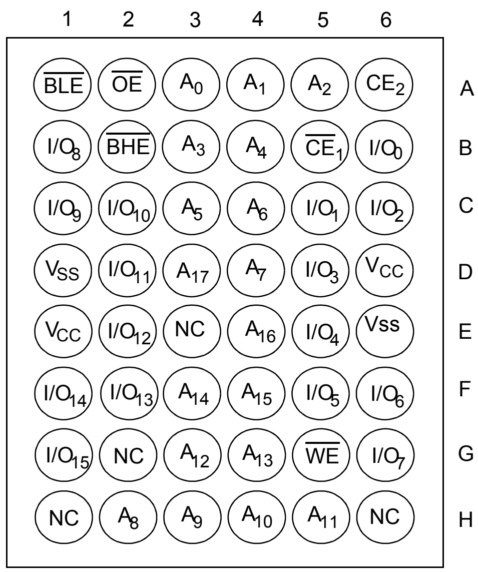
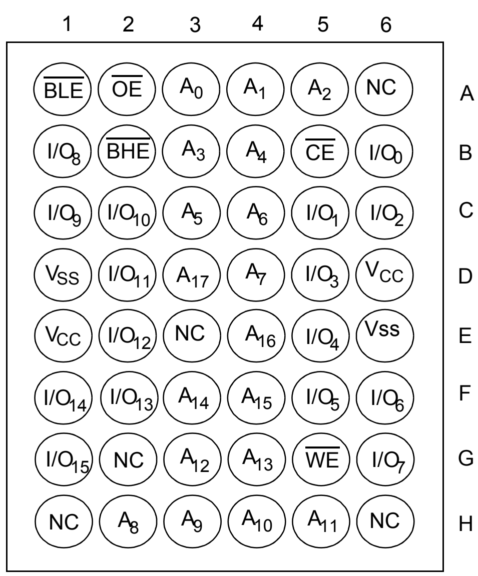


Figure 2. 48-ball VFBGA pinout (Single Chip Enable without ERR) – CY62146G/CY62146GSL [6]

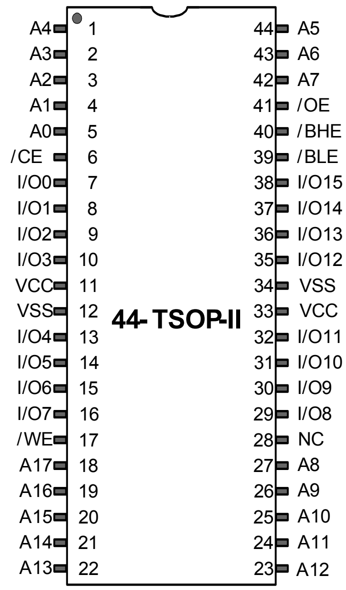


Note

6. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY62146G/CY62146GSL (continued)

Figure 3. 44-pin TSOP II pinout (Single Chip Enable without ERR) – CY62146G/CY62146GSL [7]



Note

7. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY62146GE

Figure 4. 48-ball VFBGA pinout (Single Chip Enable with ERR) – CY62146GE [8, 9]

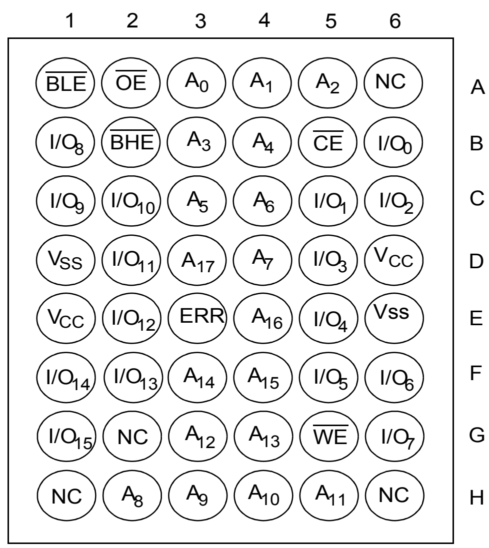
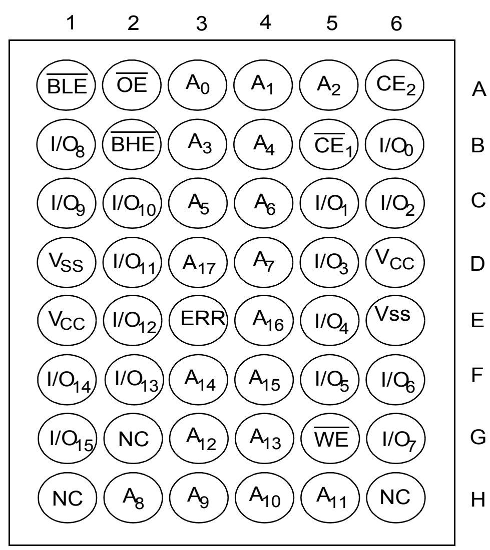


Figure 5. 48-ball VFBGA pinout (Dual Chip Enable with ERR) – CY62146GE [8, 9]



Notes

8. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
9. ERR is an output pin.

Pin Configuration – CY62146GE (continued)

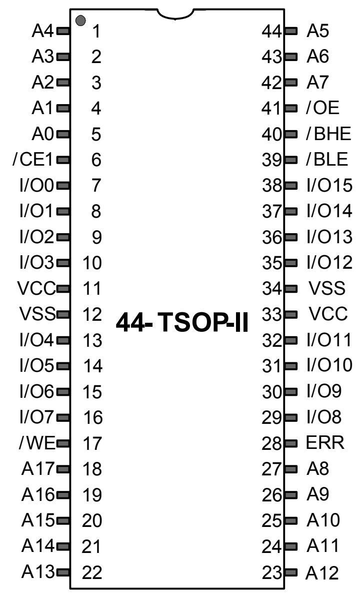


Figure 6. 44-pin TSOP II pinout (Single Chip Enable with ERR) – CY62146GE /CY62146GESL[10, 11]

Notes

10. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
11. ERR is an output pin.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature
with power applied .... –55 °C to + 125 °C

Supply voltage
to ground potential[12] .... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs
in HI-Z state[12] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage[12] .... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (in low state) .... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial[13]	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions	45/55 ns Min	45/55 ns Typ	45/55 ns Max	Unit
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA	1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA	2	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA	V_{CC} – 0.5[14]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA	–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–	1.4	–	V_{CC} + 0.2[12]	V
		2.2 V to 2.7 V	–	1.8	–	V_{CC} + 0.3[12]	
		2.7 V to 3.6 V	–	2	–	V_{CC} + 0.3[12]	
		4.5 V to 5.5 V	–	2.2	–	V_{CC} + 0.5[12]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–	–0.2[12]	–	0.4	V
		2.2 V to 2.7 V	–	–0.3[12]	–	0.6	
		2.7 V to 3.6 V	–	–0.3[12]	–	0.8	
		4.5 V to 5.5 V	–	–0.5[12]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}	–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels; f = 22.22 MHz (45 ns)	–	15	20	mA
			f = 18.18 MHz (55 ns)	–	15	20	mA
			f = 1 MHz	–	–	6	mA

Notes
12. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
13. Wide voltage range part supports V_{CC} range of 2.2 V–3.6 V and 4.5 V–5.5 V. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V–4.5 V.
14. This parameter is guaranteed by design and not tested.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns Min	45/55 ns Typ	45/55 ns Max	Unit
I_{SB1}[15]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), Max V_{CC}		–	3.5	8.7	µA
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V			–	–	10	
I_{SB2}[15]	Automatic power down current – CMOS inputs V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	25 °C [16]	–	3.5	3.7	µA
			40 °C [16]	–	–	4.8	
			70 °C [16]	–	–	7	
			85 °C	–	–	8.7	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	25 °C [16]	–	3.5	4.3	
			40 °C [16]	–	–	5	
			70 °C [16]	–	–	7.5	
			85 °C	–	–	10	

Notes
15. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
16. The I_{SB2} limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

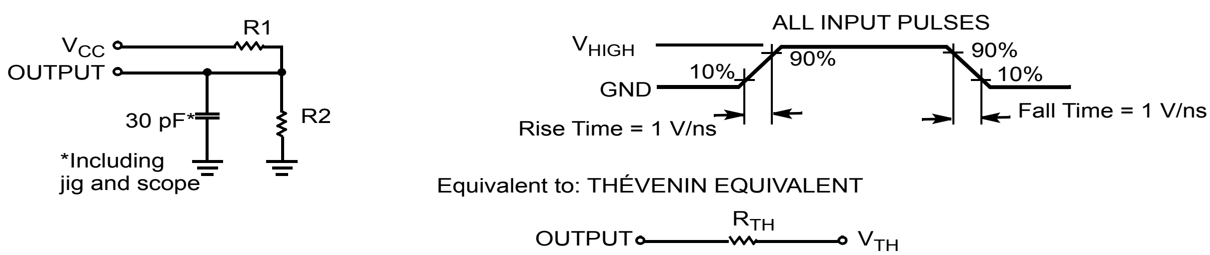
Parameter [17]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [17]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.35	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.74	15.97	°C/W

AC Test Loads and Waveforms

Figure 7. AC Test Loads and Waveforms [18]



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Notes
17. Tested initially and after any design or process changes that may affect these parameters.
18. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu s$ or stable at $V_{CC(min)} \geq 100\ \mu s$.

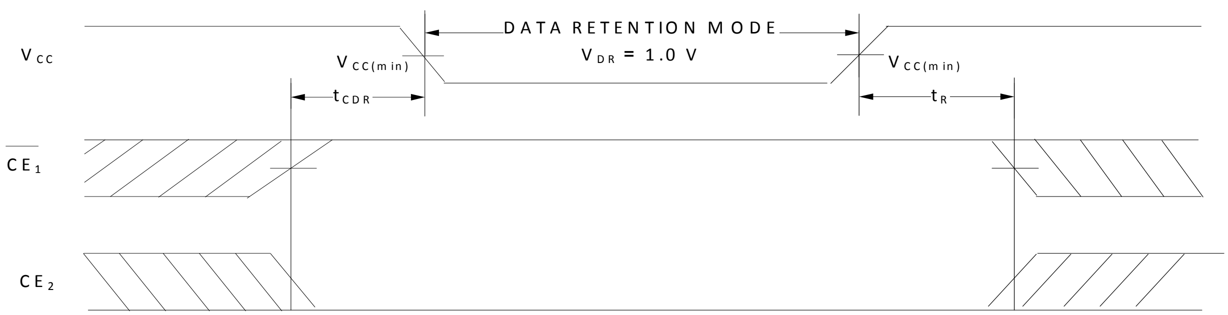
Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions	Min	Typy [19]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR}[20, 21]	Data retention current	V_{CC} = 1.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–		13	µA
t_{CDR}[22, 23]	Chip deselect to data retention time		0	–	–	ns
t_R[23]	Operation recovery time		45/55	–	–	ns

Data Retention Waveform

Figure 8. Data Retention Waveform



Notes
19. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
20. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
21. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
22. These parameters are guaranteed by design.
23. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

AC Switching Characteristics

Parameter [24]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid / Address to ERR valid	–	45	–	55	ns
t_{OHA}	Data hold from address change / ERR hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low impedance [25, 26]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z [25, 26, 27]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low impedance [25, 26]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to HI-Z [25, 26, 27]	–	18	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up [26]	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down [26]	–	45	–	55	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	–	25	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to low impedance [25, 26]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z [25, 26, 27]	–	18	–	18	ns
Write Cycle [28, 29]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	45	–	ns
t_{AW}	Address setup to write end	35	–	45	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	45	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z [25, 26, 27]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low impedance [25, 26]	10	–	10	–	ns

Notes

24. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
25. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
26. These parameters are guaranteed by design.
27. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
28. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$, or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 9. Read Cycle No. 1 of CY62146G (Address Transition Controlled) [30, 31]

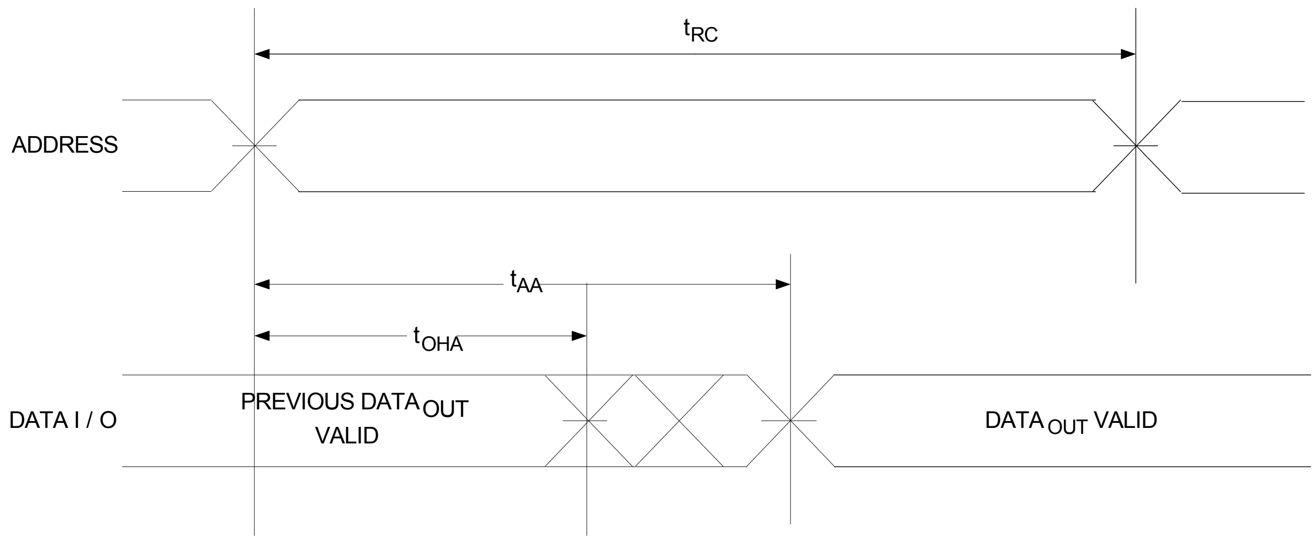
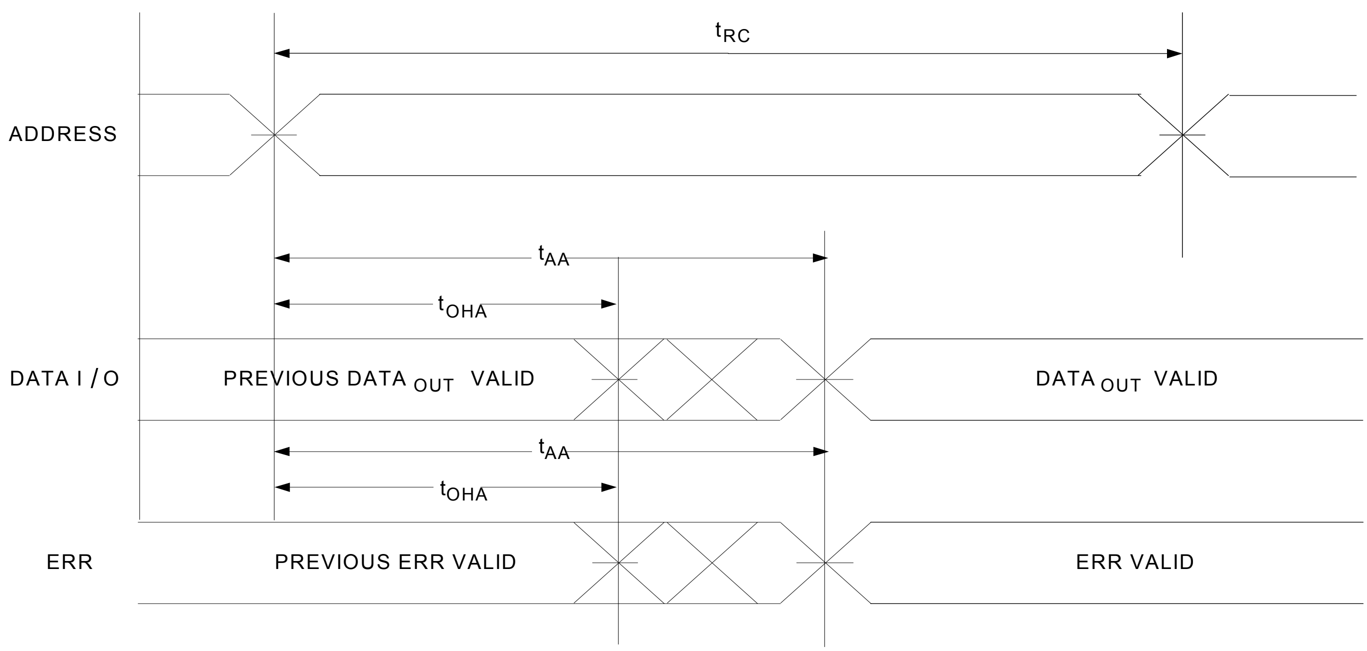


Figure 10. Read Cycle No. 1 of CY62146GE (Address Transition Controlled) [30, 31]



Notes
30. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
31. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 11. Read Cycle No. 2 ($\overline{OE}$ Controlled) [32, 33, 34]

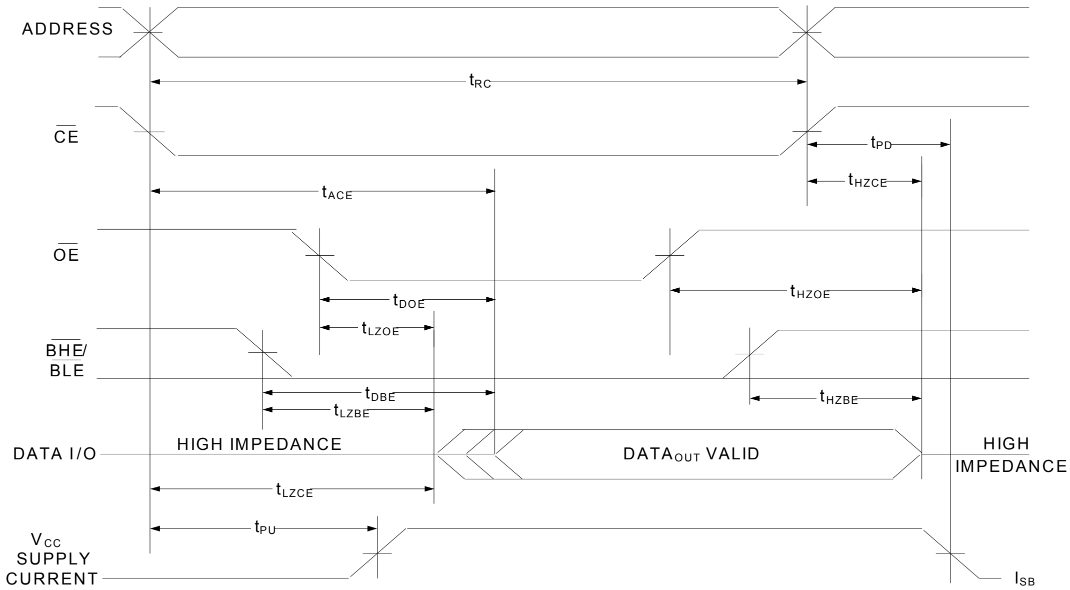
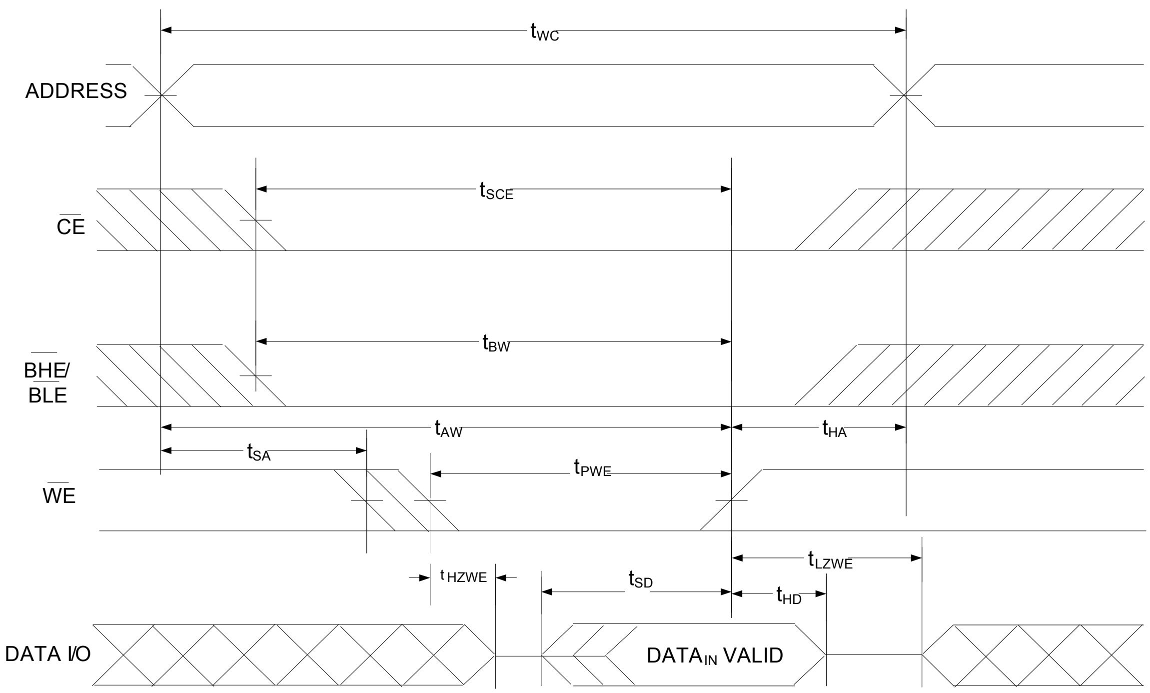


Figure 12. Write Cycle No. 1 ($\overline{WE}$ Controlled) [33, 35, 36]



Notes

32. $\overline{WE}$ is HIGH for Read cycle.
33. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
34. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
35. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
36. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 2 ($\overline{CE}$ Controlled) [37, 38, 39]

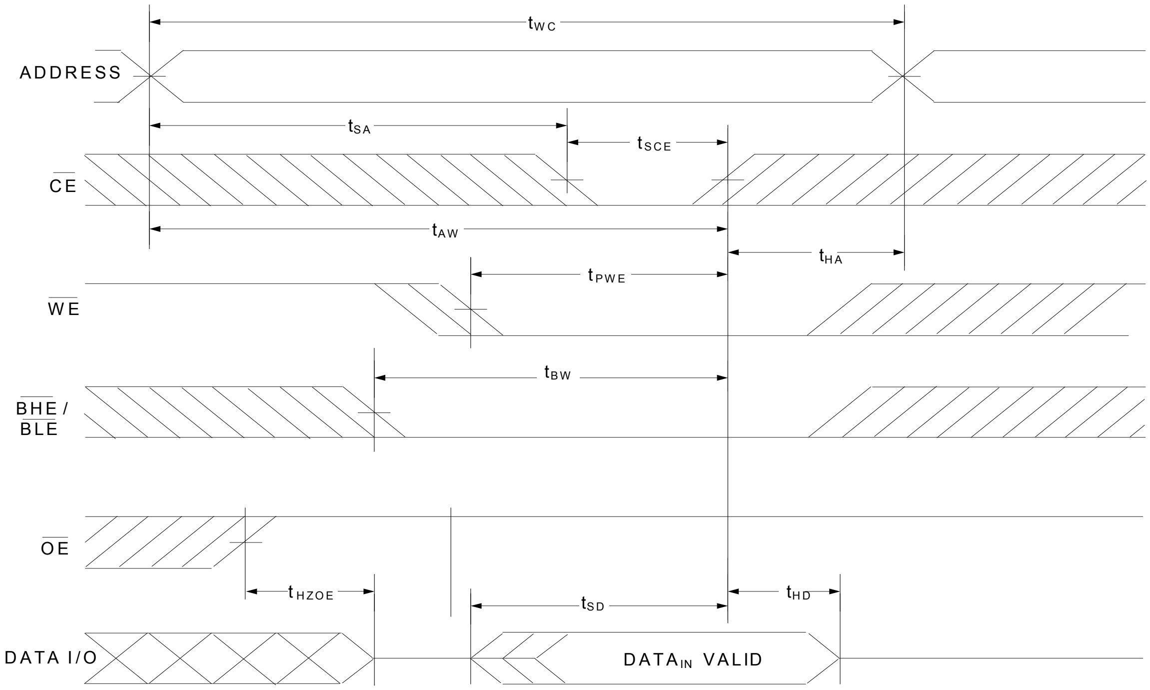
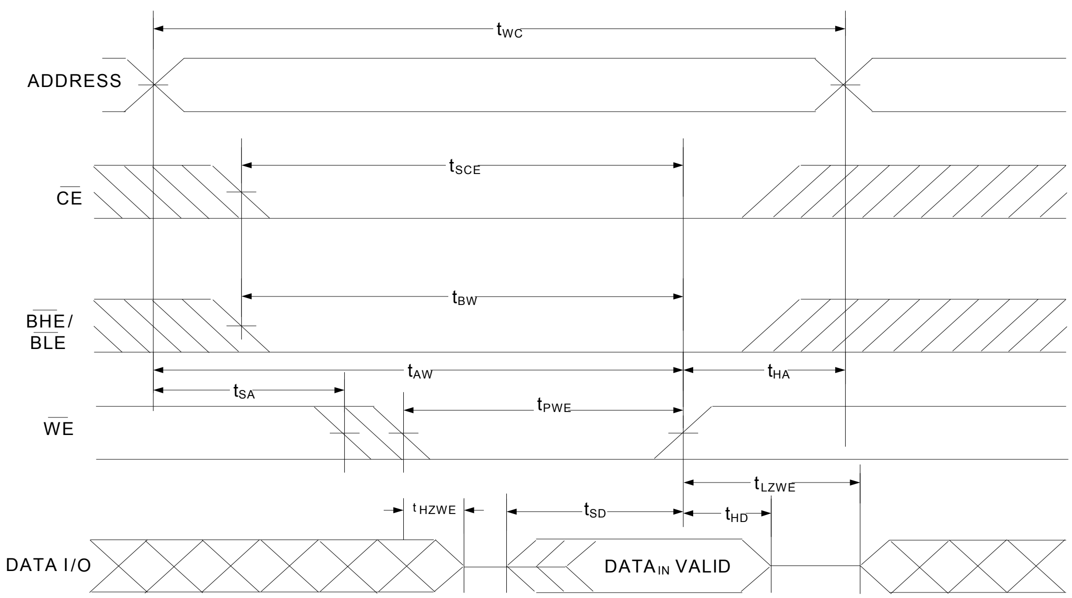


Figure 14. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [37, 38, 39, 40]

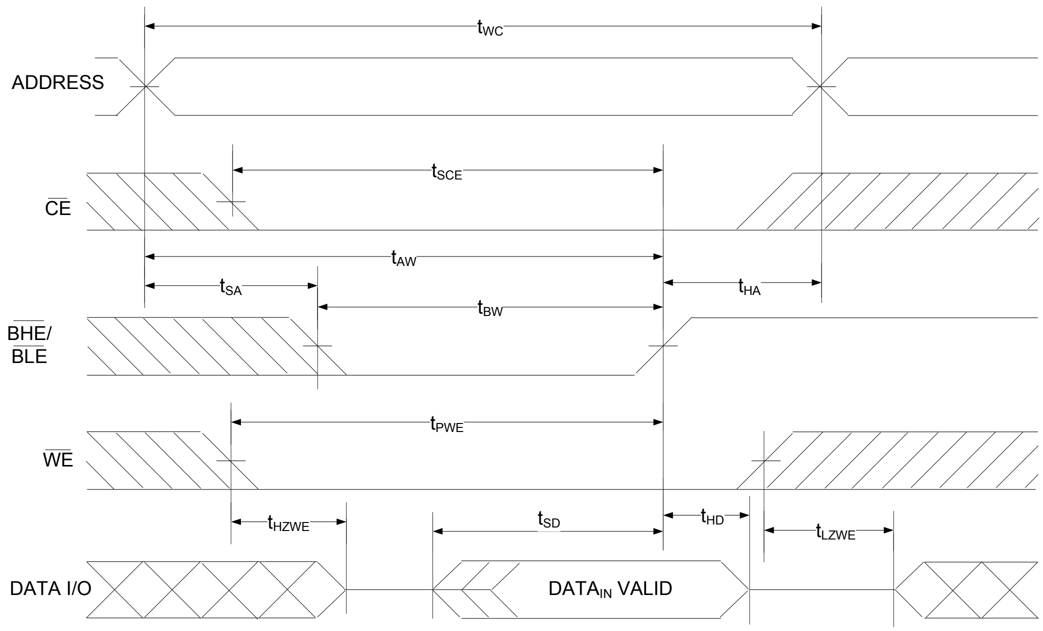


Notes

37. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
38. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
39. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
40. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 15. Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled) [41, 42, 43]



Notes

41. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
42. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
43. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

Truth Table – CY62146G/CY62146GE/CY62146GSL/CY62146GESL

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[44]	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[44]	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	HI-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	X	X	HI-Z	Output disabled	Active (I_{CC})
L	H	H	X	H	H	HI-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	HI-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

ERR Output – CY62146GE/CY62146GESL

Output[45]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected/outputs disabled/Write operation

Notes

44. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.
45. ERR is an output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62146G30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable without ERR	Industrial
		CY62146G30-45BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable without ERR, Tape and Reel	
		CY62146GE30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable with ERR	
		CY62146GE30-45BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable with ERR, Tape and Reel	
		CY62146GE30-45ZSXI	51-85087	44-pin TSOP II with ERR	
		CY62146GE30-45ZSX	51-85087	44-pin TSOP II with ERR, Tape and Reel	
		CY62146G30-45ZSXI	51-85087	44-pin TSOP II without ERR	
		CY62146G30-45ZSXIT	51-85087	44-pin TSOP II without ERR, Tape and Reel	
	4.5 V–5.5 V	CY62146GE-45ZSXI	51-85087	44-pin TSOP II with ERR	
		CY62146GE-45ZSXIT	51-85087	44-pin TSOP II with ERR, Tape and Reel	
		CY62146G-45ZSXI	51-85087	44-pin TSOP II without ERR	
		CY62146G-45ZSXIT	51-85087	44-pin TSOP II without ERR, Tape and Reel	

Ordering Code Definitions

CY 621 4 6 G X XX - 45 XX X X

- Temperature Grade: X = I
  I = Industrial
- Pb-free
- Package Type: XX = BV or ZS
  BV = 48-ball VFBGA (Single Chip enable)
  ZS = 44-pin TSOP II
- Speed Grade: 45 ns
- Voltage Range: XX = 30 or blank
  30 = 3 V typ; no character = 5 V typ
- X = blank or E
  blank = without ERR output;
  E = with ERR output, Single-bit error correction indicator
- Process Technology: G = 65 nm
- Bus width: 6 = × 16
- Density: 4 = 4-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

Package Diagrams

Figure 16. 44-pin TSOP Z44-II Package Outline, 51-85087

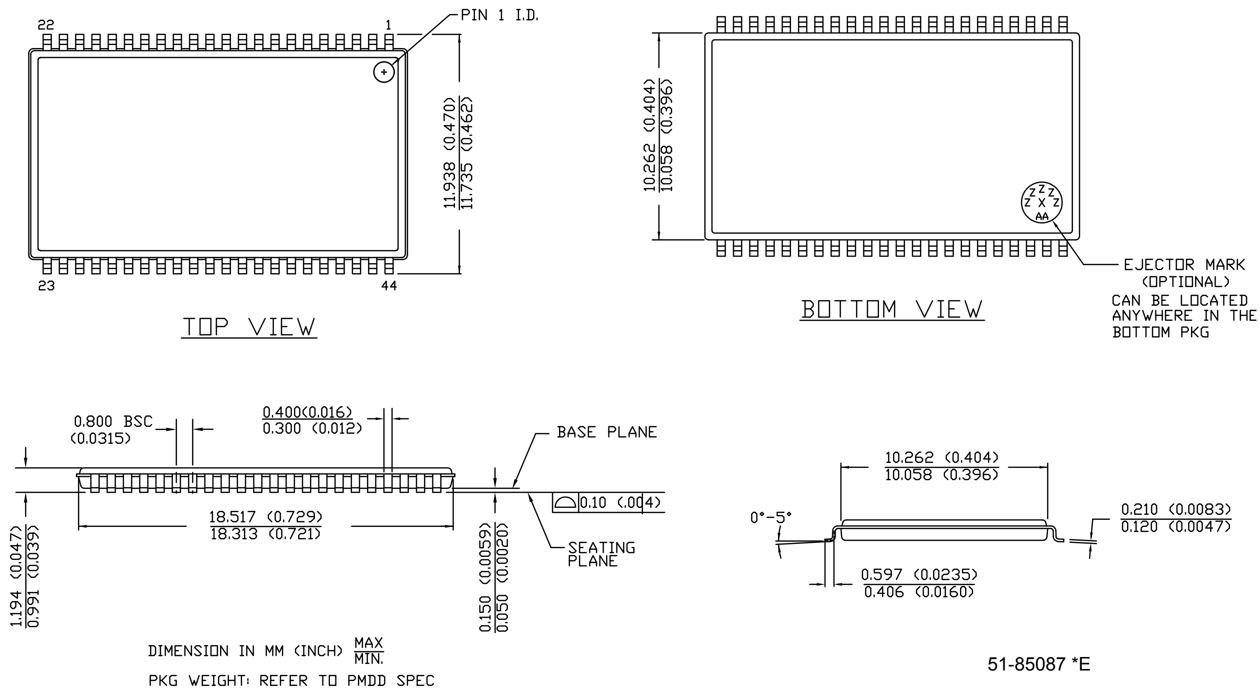
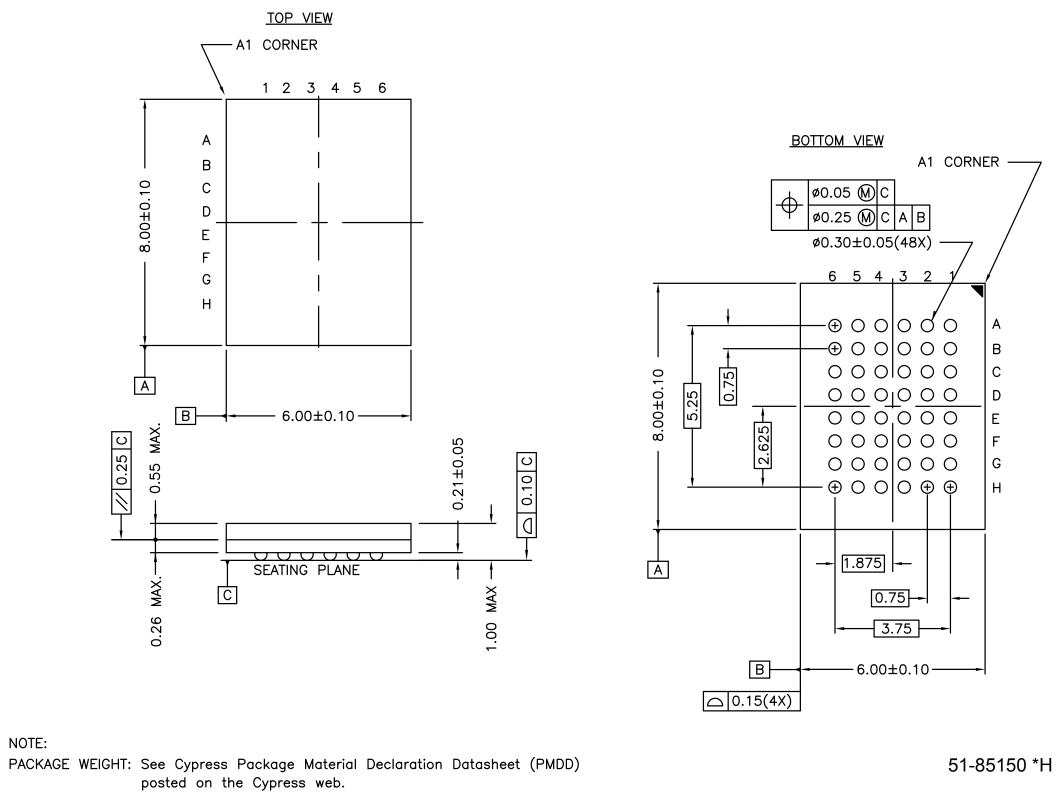


Figure 17. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
Document Title: CY62146G/CY62146GE/CY62146GSL/CY62146GESL MoBL®, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC) **Document Number: 001-95420**				
*B	5023868	VINI	11/25/2015	Changed status from Preliminary to Final.
*C	5080447	NILE	01/11/2016	Updated Ordering Information: Updated part numbers. Completing Sunset Review.
*D	5430481	NILE	09/08/2016	Updated Maximum Ratings: Updated Note 12 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –1.0 mA”. Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Ordering Information: Updated part numbers. Updated to new template.
*E	5708694	AESATMP8	04/26/2017	Updated logo and Copyright.

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