CY22801

Universal Programmable Clock Generator (UPCG)

Features

- Integrated phase-locked loop (PLL)
- Field-Programmable
- Input frequency range:
  - Crystal: 8 MHz to 30 MHz
  - CLKIN: 1 MHz to 133 MHz
- Low-voltage complementary metal oxide semiconductor (LVCMOS) output frequency:
  - Up to 200 MHz (commercial grade)
  - Up to 166.6 MHz (industrial grade)
- Special Features:
  - Spread Spectrum
  - VCXO
  - Inputs: PD or OE, FS
- Low-jitter, high-accuracy outputs
- 3.3 V operation
- Commercial and industrial temperature ranges
- 8-pin small-outline integrated circuit (SOIC) package
- Serial interface for device configuration

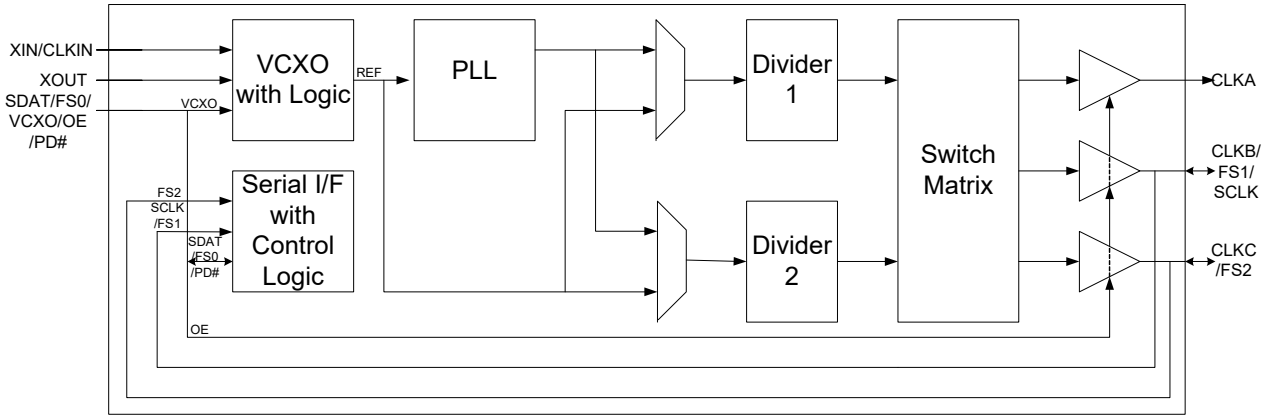
Functional Description

The CY22801 is a flash-programmable clock generator that supports various applications in consumer and communications markets. The device uses the Cypress-proprietary PLL along with Spread Spectrum and VCXO technology to make it one of the most versatile clock synthesizers in the market. The device uses a Cypress-proprietary PLL to drive up to three configurable outputs in an 8-pin SOIC.

The CY22801 is programmed with an easy-to-use programmer dongle, the CY36800, in conjunction with the CyClocksRT™ software. This enables fast sample generation of prototype builds for user-defined frequencies. Cypress's value-added distribution partners and third-party programming systems from BP Microsystems, HiLo Systems, and others, can also be contacted for large production quantities. A JEDEC file needs to be configured to program CY22801, which can be generated using the CyClocksRT™ software.

For a complete list of related documentation, click here.

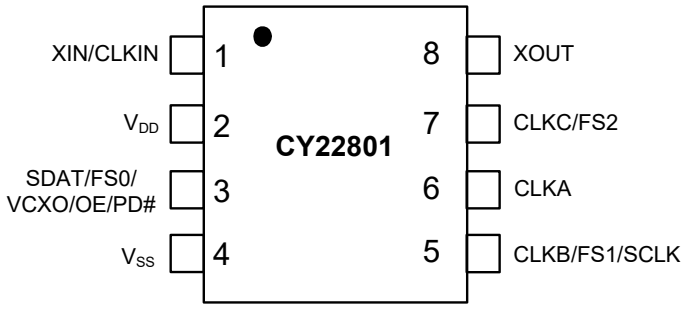
Logic Block Diagram



Contents

Pin Configurations

Figure 1. CY22801 8-pin SOIC pinout



Pin Definitions

Name	Pin Number	Description
CLKIN / XIN	1	External reference crystal input / external reference clock input
V_{DD}	2	3.3 V voltage supply
SDAT / FS0 / VCXO / OE / PD#	3	Serial interface data line / frequency select 0 / VCXO analog control voltage / Output Enable / Power-down
V_{SS}	4	Ground
CLKB / FS1 / SCLK	5	Clock output B / frequency select 1 / serial interface clock line
CLKA	6	Clock output A
CLKC / FS2	7	Clock output C / frequency select 3 / V_{SS}
XOUT	8	External reference crystal output: Connect to external crystal. When the reference is an external clock signal (applied to pin 1), this pin is not used and must be left floating.

External Reference Crystal/Clock Input

CY22801 can accept external reference clock input as well as crystal input. External reference clock input frequency range is from 1 MHz to 133 MHz.

The input crystal oscillator of the CY22801 is an important feature because of the flexibility it provides in selecting a crystal as a reference clock source. The oscillator inverter has programmable gain, enabling maximum compatibility with a reference crystal, based on manufacturer, process, performance, and quality.

Input load capacitors are placed on the CY22801 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when non-linear load capacitance is affected by load, bias, supply, and temperature changes.

The value of the input load capacitors is determined by eight bits in a programmable register. Total load capacitance is determined by the formula:

$$CapLoad = (C_L - C_{BRD} - C_{CHIP}) / 0.09375\ pF$$

In CyClocksRT, enter the crystal capacitance (C_L). The value of CapLoad is determined automatically and programmed into the CY22801.

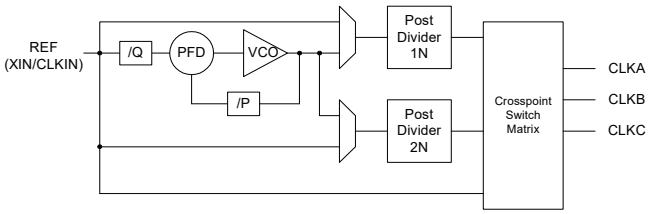
Output Clock Frequencies

The CY22801 is a very flexible clock generator with up to three individual outputs, generated from an integrated PLL. See Figure 2 for details.

The output of the PLL runs at high frequency and is divided down to generate the output clocks. Two programmable dividers are available for this purpose. Therefore, although the output clocks may have different frequencies, they must be related, based on the PLL frequency.

It is also possible to direct the reference clock input to any of the outputs, thereby bypassing the PLL. Lastly, the reference clock may be passed through either divider.

Figure 2. Basic PLL Block Diagram



VCXO

One of the key components of the CY22801 device is the VCXO. The VCXO is used to 'pull' the reference crystal higher or lower to lock the system frequency to an external source. This is ideal for applications where the output frequency needs to track along with an external reference frequency that is constantly shifting.

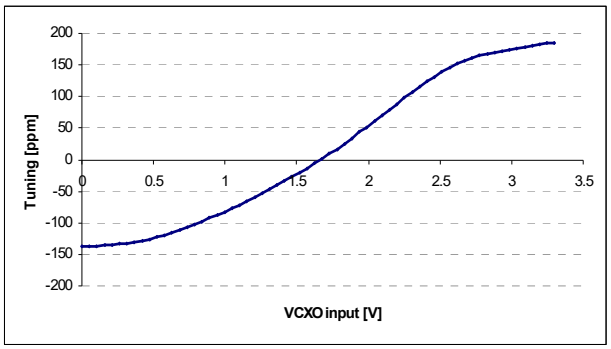
A special pullable crystal must be used to have adequate VCXO pull range. Pullable crystal specifications are included in this data sheet.

VCXO is not compatible with Spread spectrum and Serial Interface.

VCXO Profile

Figure 3 shows an example of a VCXO profile. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This moves the PPM from a negative to positive offset.

Figure 3. VCXO Profile



Spread Spectrum Clock Generation (SSCG)

Spread spectrum clock generation (SSCG) in CY22801 helps to reduce EMI found in today's high-speed digital electronic systems.

The device uses the proprietary spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the input clock. By modulating the frequency of the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with the regulatory agency electromagnetic compatibility (EMC) requirements and improve time to market without degrading system performance.

Programmed spread spectrum modulation will appear same on all three clock outputs as they come from same PLL even if operating at different frequencies. Spread spectrum is not compatible with VCXO feature.

Spread Percentage

The percentage of spread can be programmed from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% for down spread. The granularity is 0.25%.

Modulation Frequency

The default modulation frequency is 31.5 kHz. Other modulation frequencies available through configuration software are 30.1 kHz and 32.9 kHz.

SSON Pin

SSON pin functionality can be used to turn Spread ON and OFF in clock output. Any one of the Multifunction pins can be configured as SSON pin.

Multifunction Pins

There are three pins [1] with multiple functions either as control pins or as output pins. The following are the acronyms used for the different control function pins:

- Output enable (OE): If OE = 1, all outputs are enabled
- Frequency select (FS0, 1, 2): These pins can be used to select one of the programmed clock frequencies for clock output. All of three multifunction pins support this functionality. Any of these pins can also be configured as Spread spectrum ON (SSON) pin. If SSON = 1, clock output has programmed spread; if SSON = 0, clock output does not have spread.
- Power-down: active low (PD#): If PD# = 0, all outputs are tristated and the device enters in the low-power state
- Voltage controlled crystal oscillator (VCXO): Analog voltage on this pin controls the output frequency of oscillator
- Serial interface clock line (SCLK) and serial interface data line (SDAT): These pins are for serial interface and are compatible with I^2C.

Each of these three multi-function pins supports selected functions mentioned in Table 1. One of the supported functions can be programmed on the pin at a time.

Table 1. Multi Function Pin Options

Pin#	Pin Name	OE	PD#	VCXO	FS	CLK OUTPUT	I^2C
3	SDAT / FS0 / VCXO / OE / PD#	Y	Y	Y[2]	Y[3]	N[4]	SDAT[2]
5	CLKB / FS1 / SCLK	N	N	N	Y	Y	SCLK
7	CLKC / FS2	N	N	N	Y	Y[5]	N

Table 2. Possible Combinations for Multifunction Pins

Possible Combinations	Pin#3	Pin#5	Pin#7
A	FS0	CLKB	CLKC
B	FS0	CLKB	FS2
C	FS0	FS1	FS2
D	OE / PD#	CLKB	CLKC
E	OE / PD#	FS1	CLKC
F	OE / PD#	FS1	FS2
G	SDAT	SCLK	CLKC
H	VCXO	CLKB	CLKC

Frequency Calculation and Register Definitions

The CY22801 is an extremely flexible clock generator with four basic variables that are used to determine the final output frequency. They are the input reference frequency (REF), the internally calculated P and Q dividers, and the post divider, which can be a fixed or calculated value. There are three formulas to determine the final output frequency of a CY22801 based design:

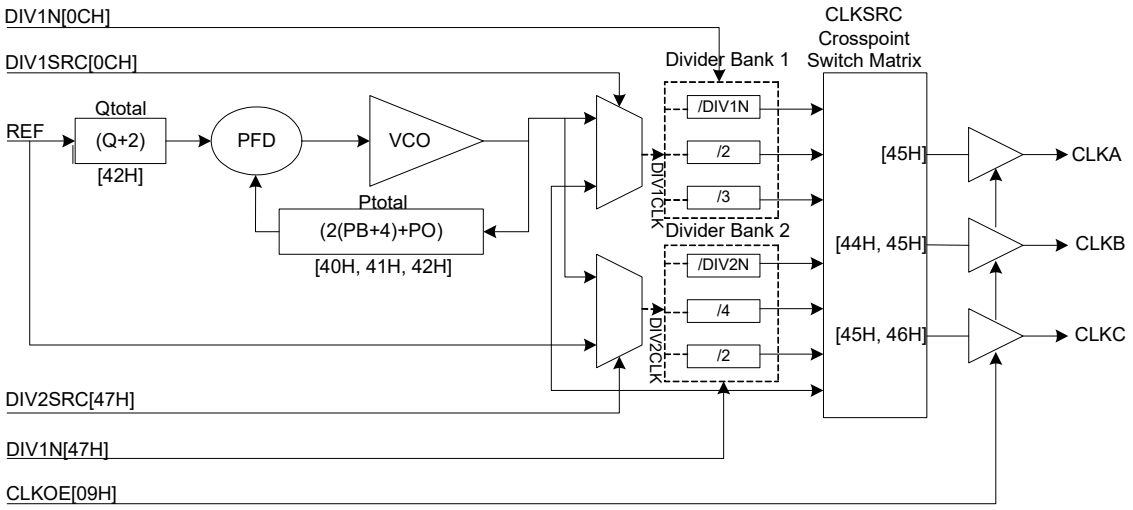
- CLK = ((REF × P) / Q) / Post divider
- CLK = REF / Post divider
- CLK = REF

The basic PLL block diagram is shown in Figure 4 on page 6. Each of the three clock outputs on the CY22801 has a total of seven output options available to it. There are six post divider options available: /2 (two of these), /3, /4, /DIV1N and /DIV2N. DIV1N and DIV2N are independently calculated and are applied to individual output groups. The post divider options can be applied to the calculated VCO frequency ((REF × P) / Q) or to the REF directly.

In addition to the six post divider output options, the seventh option bypasses the PLL and passes the REF directly to the crosspoint switch matrix.

Notes
1. There are Weak Pull up resistors (approximately 100 kΩ) on all Multifunctional pins.
2. VCXO and SSON functions as well as VCXO and Serial Interface functions are not compatible.
3. 'Y' means pin supports this function.
4. 'N' means pin does not support this function.
5. Do not use this pin as Reference Clock Output.

Figure 4. Basic Block Diagram of CY22801 PLL



Default Startup Condition for the CY22801

The default (programmed) condition of the device is generally set by the distributor who programs the device using a customer specific JEDEC file produced by CyClocksRT™. Parts shipped from the factory are blank and unprogrammed. In this condition, all bits are set to 0, all outputs are three-stated, and the crystal oscillator circuit is active.

While you can develop your own subroutine to program any or all of the individual registers described in the following pages, it may be easier to use CyClocksRT to produce the required register setting file [6].

The serial interface address of the CY22801 is 69H. If there is a conflict with any other devices in your system, then this can also be changed [7, 8].

Frequency Calculations and Register Definitions using the Serial (I^2C) Interface

The CY22801 provides an industry standard serial interface for volatile, in-system programming of unique frequencies and options. Serial programming and re-programming allows for quick design changes and product enhancements, eliminates inventory of old design parts, and simplifies manufacturing.

The I^2C Interface provides volatile programming. This means when the target system is powered down, the CY22801 reverts to its pre-I^2C state, as defined above (programmed or unprogrammed). When the system is powered back up again, the I^2C registers must be reconfigured again.

All programmable registers in the CY22801 are addressed with eight bits and contain eight bits of data. The CY22801 is a slave device with an address of 1101001 (69H).

Table 3 on page 7 lists the I^2C registers and their definitions. Specific register definitions and their allowable values are listed as follows.

Reference Frequency

The REF can be a crystal or a driven frequency (CLKIN). For crystals, the frequency range must be between 8 MHz and 30 MHz. For a driven frequency, the frequency range must be between 1 MHz and 133 MHz.

Programmable Crystal Input Oscillator Gain Settings

The Input crystal oscillator gain (XDRV) is controlled by two bits in register 12H and are set according to Table 4 on page 8. The parameters controlling the gain are the crystal frequency, the internal crystal parasitic resistance (ESR, available from the manufacturer), and the CapLoad setting during crystal startup.

Bits 3 and 4 of register 12H control the input crystal oscillator gain setting. Bit 4 is the MSB of the setting, and bit 3 is the LSB. The setting is programmed according to Table 4 on page 8. All other bits in the register are reserved and should be programmed as shown in Table 5 on page 8.

FTAAddrSrc[1:0] bits set Frequency tuning array address source. This will be set by CyClockRT software based on selected configuration.

Notes
6. Advanced features like VCXO, SCL, SDA, FS, OE, SSON are not supported by CyClocksRT. Contact your local Cypress field application engineer for functional feasibility and custom configuration with these advanced features.
7. Please Contact your local Cypress FAE, if you need serial interface address other than 69H.
8. while configuring Jedec through CyClocksRT software, if Pin3 (SDAT) and Pin5 (SCLK) is not configured for any functionality, the jedec file automatically gets configured with I2C Enable Functionality with default I2C address as 69 H.

Using an External Clock as the Reference Input

The CY22801 also accepts an external clock as reference, with speeds up to 133 MHz. With an external clock, the XDRV (register 12H) bits must be set according to Table 6 on page 8.

Table 3. Summary Table – CY22801 Programmable Registers

Register	Description	D7	D6	D5	D4	D3	D2	D1	D0
09H	CLKOE control	0	0	CLKC	CLKA	0	CLKB	0	0
OCH	DIV1SRC mux and DIV1N divider	DIV1SRC	DIV1N (6)	DIV1N (5)	DIV1N (4)	DIV1N (3)	DIV1N (2)	DIV1N (1)	DIV1N (0)
12H	Input crystal oscillator drive control	FTAAddrSrc[1]	FTAAddrSrc[0]	XCapSrc	XDRV (1)	XDRV (0)	0	0	0
13H	Input load capacitor control	CapLoad (7)	CapLoad (6)	CapLoad (5)	CapLoad (4)	CapLoad (3)	CapLoad (2)	CapLoad (1)	CapLoad (0)
40H	Charge pump and PB counter	1	1	0	Pump (2)	Pump (1)	Pump (0)	PB (9)	PB (8)
41H		PB (7)	PB (6)	PB (5)	PB (4)	PB (3)	PB (2)	PB (1)	PB (0)
42H	PO counter, Q counter	PO	Q (6)	Q (5)	Q (4)	Q (3)	Q (2)	Q (1)	Q (0)
44H	Crosspoint switch matrix control	1	1	1	1	1	1	CLKSRC2 for CLKB	CLKSRC1 for CLKB
45H		CLKSRC0 for CLKB	1	1	1	CLKSRC2 for CLKA	CLKSRC1 for CLKA	CLKSRC0 for CLKA	CLKSRC2 for CLKC
46H		CLKSRC1 for CLKC	CLKSRC0 for CLKC	1	1	1	1	1	1
47H	DIV2SRC mux and DIV2N divider	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV2N(1)	DIV2N(0)

Table 4. Programmable Crystal Input Oscillator Gain Settings

	Cap Register Settings	00H–80H		80H–C0H		C0H–FFH	
	Effective Load Capacitance (CapLoad)	6 pF to 12 pF		12 pF to 18 pF		18 pF to 30 pF	
	Crystal ESR	30 Ω	60 Ω	30 Ω	60 Ω	30 Ω	60 Ω
Crystal input frequency	8 to 15 MHz	00	01	01	10	01	10
	15 to 20 MHz	01	10	01	10	10	10
	20 to 25 MHz	01	10	10	10	10	11
	25 to 30 MHz	10	10	10	11	11	N/A

Table 5. Crystal Oscillator Gain Bit Locations and Values

Address	D7	D6	D5	D4	D3	D2	D1	D0
12H	0	0	1	XDRV(1)	XDRV(0)	0	0	0

Table 6. Programmable External Reference Input Oscillator Drive Settings

Reference Frequency	1 to 25 MHz	25 to 50 MHz	50 to 90 MHz	90 to 133 MHz
Drive Setting	00	01	10	11

Input Load Capacitors

XCapSrc bit in 12H register selects the source of Input load capacitance. This will be set by CyClockRT software based on selected configuration.

Input load capacitors allow you to set the load capacitance of the CY22801 to match the input load capacitance from a crystal. The value of the input load capacitors is determined by 8 bits in a programmable register [13H]. Total load capacitance is determined by the formula:

CapLoad = (C_L – C_{BRD} – C_{CHIP}) / 0.09375 pF

where:

- C_L = specified load capacitance of your crystal.
- C_{BRD} = the total board capacitance, due to external capacitors and board trace capacitance. In CyClocksRT, this value defaults to 2 pF.
- C_{CHIP} = 6 pF.
- 0.09375 pF = the step resolution available due to the 8-bit register.

In CyclocksRT, only the crystal capacitance (C_L) is specified. C_{CHIP} is set to 6 pF and C_{BRD} defaults to 2 pF. If your board capacitance is higher or lower than 2 pF, the formula given earlier is used to calculate a new CapLoad value and programmed into register 13H.

In CyClocksRT, enter the crystal capacitance (C_L). The value of CapLoad is determined automatically and programmed into the CY22801. Through the SDAT and SCLK pins, the value can be adjusted up or down if your board capacitance is greater or less than 2 pF. For an external clock source, CapLoad defaults to 0. See Table 7 on page 9 for CapLoad bit locations and values.

The input load capacitors are placed on the CY22801 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when nonlinear load capacitance is affected by load, bias, supply, and temperature changes.

PLL Frequency, Q Counter [42H(6..0)]

The first counter is known as the Q counter. The Q counter divides REF by its calculated value. Q is a 7 bit divider with a maximum value of 127 and minimum value of 0. The primary value of Q is determined by 7 bits in register 42H (6..0), but 2 is added to this register value to achieve the total Q, or Q_{total}. Q_{total} is defined by the formula:

Q_{total} = Q + 2

The minimum value of Q_{total} is 2. The maximum value of Q_{total} is 129. Register 42H is defined in the table.

Stable operation of the CY22801 cannot be guaranteed if REF/Q_{total} falls below 250 kHz. Q_{total} bit locations and values are defined in Table 8 on page 9.

PLL Frequency, P Counter [40H(1..0)], [41H(7..0)], [42H(7)]

The next counter definition is the P (product) counter. The P counter is multiplied with the (REF/Q_{total}) value to achieve the VCO frequency. The product counter, defined as P_{total}, is made up of two internal variables, PB and PO. The formula for calculating P_{total} is:

$P_{total} = (2(PB + 4) + PO)$

PB is a 10-bit variable, defined by registers 40H(1:0) and 41H(7:0). The 2 LSBs of register 40H are the two MSBs of variable PB. Bits 4..2 of register 40H are used to determine the charge pump settings. The three MSBs of register 40H are preset and reserved and cannot be changed. PO is a single bit variable, defined in register 42H(7). This allows for odd numbers in P_{total}.

The remaining seven bits of 42H are used to define the Q counter, as shown in Table 8.

The minimum value of P_{total} is 8. The maximum value of P_{total} is 2055. To achieve the minimum value of P_{total}, PB and PO should both be programmed to 0. To achieve the maximum value of P_{total}, PB should be programmed to 1023, and PO should be programmed to 1.

Stable operation of the CY22801 cannot be guaranteed if the value of (P_{total} × (REF/Q_{total})) is above 400 MHz or below 100 MHz.

PLL Post Divider Options [0CH(7..0)], [47H(7..0)]

The output of the VCO is routed through two independent muxes, then to two divider banks to determine the final clock output frequency. The mux determines if the clock signal feeding into the divider banks is the calculated VCO frequency or REF. There are two select muxes (DIV1SRC and DIV2SRC) and two divider banks (Divider Bank 1 and Divider Bank 2) used to determine this clock signal. The clock signal passing through DIV1SRC and DIV2SRC is referred to as DIV1CLK and DIV2CLK, respectively.

The divider banks have four unique divider options available: /2, /3, /4, and /DIVxN. DIVxN is a variable that can be independently programmed (DIV1N and DIV2N) for each of the two divider banks. The minimum value of DIVxN is 4. The maximum value of DIVxN is 127. A value of DIVxN below 4 is not guaranteed to work properly.

DIV1SRC is a single bit variable, controlled by register 0CH. The remaining seven bits of register 0CH determine the value of post divider DIV1N.

DIV2SRC is a single bit variable, controlled by register 47H. The remaining seven bits of register 47H determine the value of post divider DIV2N.

Register 0CH and 47H are defined in Table 9.

Charge Pump Settings [40H(2..0)]

The correct pump setting is important for PLL stability. Charge pump settings are controlled by bits (4..2) of register 40H, and are dependent on internal variable PB (see "*PLL Frequency, P Counter[40H(1..0)], [41H(7..0)], [42H(7)]*"). Table 10 on page 10 summarizes the proper charge pump settings, based on Ptotal.

See Table 11 on page 10 for register 40H bit locations and values.

Table 7. Input Load Capacitor Register Bit Settings

Address	D7	D6	D5	D4	D3	D2	D1	D0
13H	CapLoad(7)	CapLoad(6)	CapLoad(5)	CapLoad(4)	CapLoad(3)	CapLoad(2)	CapLoad(1)	CapLoad(0)

Table 8. P Counter and Q Counter Register Definition

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	**PB(9)**	**PB(8)**
41H	**PB(7)**	**PB(6)**	**PB(5)**	**PB(4)**	**PB(3)**	**PB(2)**	**PB(1)**	**PB(0)**
42H	**PO**	Q(6)	Q(5)	Q(4)	Q(3)	Q(2)	Q(1)	Q(0)

Table 9. PLL Post Divider Options

Address	D7	D6	D5	D4	D3	D2	D1	D0
0CH	DIV1SRC	DIV1N(6)	DIV1N(5)	DIV1N(4)	DIV1N(3)	DIV1N(2)	DIV1N(1)	DIV1N(0)
47H	DIV2SRC	DIV2N(6)	DIV2N(5)	DIV2N(4)	DIV2N(3)	DIV2N(2)	DIV2N(1)	DIV2N(0)

Table 10. Charge Pump Settings

Charge Pump Setting – Pump(2..0)	Calculated P_{total}
000	16–44
001	45–479
010	480–639
011	640–799
100	800–1023
101, 110, 111	Do not use – device will be unstable

Table 11. Register 40H Change Pump Bit Settings

Address	D7	D6	D5	D4	D3	D2	D1	D0
40H	1	1	0	Pump(2)	Pump(1)	Pump(0)	PB(9)	PB(8)

Although using the above table guarantees stability, it is recommended to use the Print preview function in CyClocksRT to determine the correct charge pump settings for optimal jitter performance.

PLL stability cannot be guaranteed for values below 16 and above 1023. If values above 1023 are needed, use CyClocksRT to determine the best charge pump setting. To configure device using serial interface, please refer CyClocksRT.

Clock Output Settings: CLKSRC – Clock Output Crosspoint Switch Matrix [44H(7..0)], [45H(7..0)], [46H(7..6)]

Every clock output can be defined to come from one of seven unique frequency sources. The CLKSRC(2..0) crosspoint switch matrix defines which source is attached to each individual clock output. CLKSRC(2..0) is set in Registers 44H, 45H, and 46H. The remainder of register 46H(5:0) must be written with the values stated in the register table when writing register values 46H(7:6).

When DIV1N is divisible by four, then CLKSRC(0,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1). When DIV1N is six, then CLKSRC(0,1,1) is guaranteed to be rising edge phase-aligned with CLKSRC(0,0,1).

When DIV2N is divisible by four, then CLKSRC(1,0,1) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0). When DIV2N is divisible by eight, then CLKSRC(1,1,0) is guaranteed to be rising edge phase-aligned with CLKSRC(1,0,0).

CLKOE – Clock Output Enable Control [09H(5..0)]

Each clock output has its own output enable, controlled by register 09H(5..0). To enable an output, set the corresponding CLKOE bit to 1. CLKOE settings are in Table 14 on page 11.

Test, Reserved, and Blank Registers

Writing to any of the following registers causes the part to exhibit abnormal behavior, as follows.

[00H to 08H] – Reserved
[0AH to 0BH] – Reserved
[0DH to 11H] – Reserved
[14H to 3FH] – Reserved
[43H] – Reserved
[48H to FFH] – Reserved.

Table 12. Clock Output Setting

CLKSRC2	CLKSRC1	CLKSRC0	Definition and Notes
0	0	0	Reference input.
0	0	1	DIV1CLK/DIV1N. DIV1N is defined by register [OCH]. Allowable values for DIV1N are 4 to 127. If Divider Bank 1 is not being used, set DIV1N to 8.
0	1	0	DIV1CLK/2. Fixed /2 divider option. If this option is used, DIV1N must be divisible by 4.
0	1	1	DIV1CLK/3. Fixed /3 divider option. If this option is used, set DIV1N to 6.
1	0	0	DIV2CLK/DIV2N. DIV2N is defined by Register [47H]. Allowable values for DIV2N are 4 to 127. If Divider Bank 2 is not being used, set DIV2N to 8.
1	0	1	DIV2CLK/2. Fixed /2 divider option. If this option is used, DIV2N must be divisible by 4.
1	1	0	DIV2CLK/4. Fixed /4 divider option. If this option is used, DIV2N must be divisible by 8.
1	1	1	Reserved – do not use.

Table 13. Clock Output Register Setting

Address	D7	D6	D5	D4	D3	D2	D1	D0
44H	1	1	1	1	1	1	CLKSRC2 for CLKB	CLKSRC1 for CLKB
45H	CLKSRC0 for CLKB	1	1	1	CLKSRC2 for CLKA	CLKSRC1 for CLKA	CLKSRC0 for CLKA	CLKSRC2 for CLKC
46H	CLKSRC1 for CLKC	CLKSRC0 for CLKC	1	1	1	1	1	1

Table 14. CLKOE Bit Setting

Address	D7	D6	D5	D4	D3	D2	D1	D0
09H	0	0	CLKC	CLKA	0	CLKB	0	0

Application Guideline

Best Practices for Best Jitter Performance

Jitter can be specified in different terminologies:

Time Domain:

- Cycle-to-cycle jitter
- Period jitter
- Long-term jitter

Frequency domain:

- Deterministic jitter
- Random jitter
- Phase noise

These jitter terms are usually given in terms of root mean square (RMS), peak-to-peak, or in the case of phase noise, dBC/Hz with respect to fundamental frequency. Cycle-to-cycle and period jitter are generally used terminologies. Jitter depends on many factors and few of the them can be controlled in application:

- Input reference jitter
- Number of active clock outputs
- Operating temperature
- Clock output load
- PLL frequencies
- Termination and layout
- Supply voltage accuracy

Jitter is directly proportional to the input reference jitter, number of active clock outputs, operating temperature and clock output load, but inversely proportional to the PLL frequency. Best practices for termination, layout and supply voltage filtering are discussed in application note “Layout and Termination Techniques For Cypress Clock Generators – AN1111”.

Field Programming the CY22801

The CY22801 is programmed using the CY36800 USB programmer dongle. The CY22801 is flash-technology based, so the parts are reprogrammed up to 100 times. This enables fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities are programmed using the CY36800 programmer. Cypress’s value-added distribution partners and third-party programming systems from BP Microsystems, HiLo Systems, and others, can also be contacted for large production quantities. Third-Party Programmer List can be found at below link http://www.cypress.com/?rID=14364.

CyClocksRT Software

CyClocksRT is an easy-to-use software application that enables the user to custom-configure the CY22801. Users can specify the XIN/CLKIN frequency, crystal load capacitance, and output frequencies. CyClocksRT then creates an industry-standard JEDEC file that is used to program the CY22801[6].

When needed, an advanced mode is available that enables users to override the automatically generated voltage controlled oscillator (VCO) frequency and output divider values.

CyClocksRT is a component of the CyberClocks™ software that you can download free of charge from the Cypress website at http://www.cypress.com.

CY36800 InstaClock™ Kit

The Cypress CY36800 InstaClock kit comes with everything needed to design the CY22801 and program samples and small prototype quantities. The CyClocksRT software is used to quickly create a JEDEC programming file, which is then downloaded directly to the portable programmer that is included in the CY36800 InstaClock kit. The JEDEC file can also be saved for use in a production programming system for larger volumes.

The CY36800 also comes with five samples of the CY22801, which are programmed with preconfigured JEDEC files using the InstaClock software.

Possible Configuration Examples

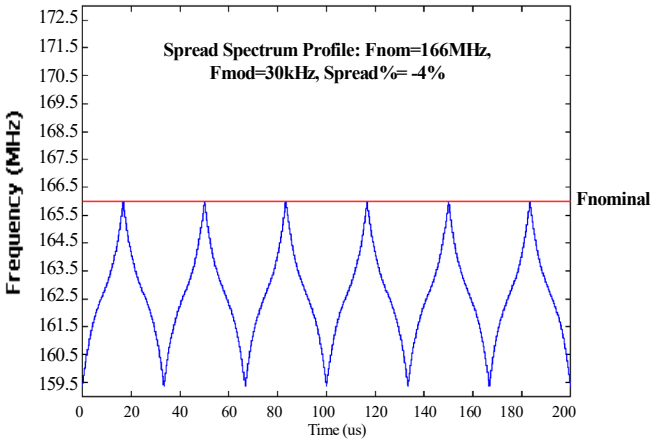
Table 15. Possible Configuration

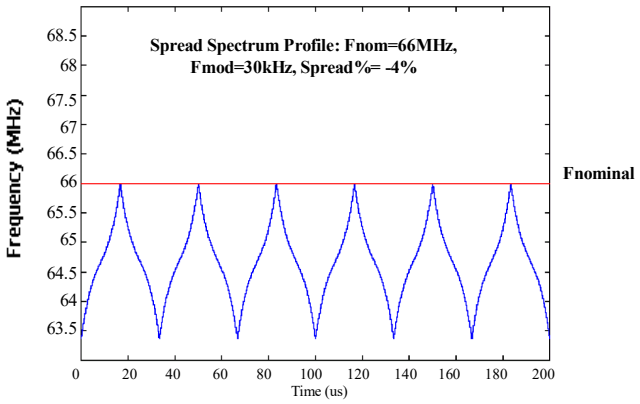
Possible Configurations	Pin#1	Pin#3	Pin#5	Pin#6	Pin#7	Pin#8
A	CLKIN: 33 MHz	OE	CLKB: 33 MHz	CLKA: 100 MHz with +/-1% Spread	SSON	NC
B	XIN: 27 MHz crystal	VCXO	PD#	CLKA: 74.25 / 74.175824 MHz	FS2	XOUT: 27 MHz crystal
C	CLKIN: 10 MHz	OE	FS1	CLKA: 25 / 40 / 33.3333 / 50 MHz	FS2	NC
D	CLKIN: 10 MHz	SDAT	SCLK	CLKA	CLKB	NC

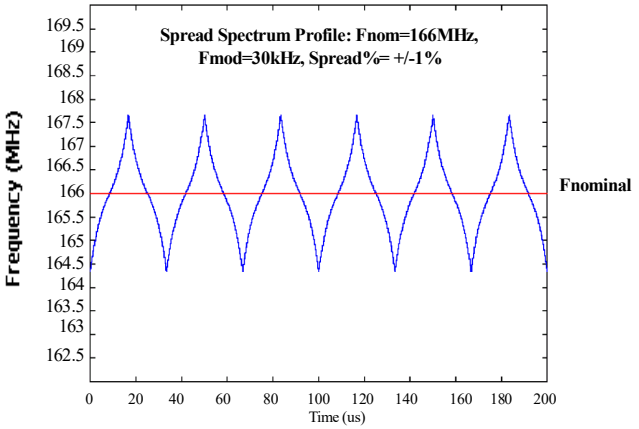
Contact your local Cypress field application engineer for functional feasibility and custom configuration with these advanced features.

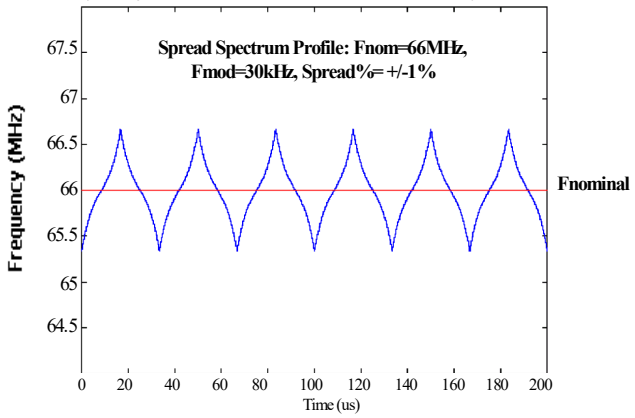
Informational Graphs

The informational graphs are meant to convey the typical performance levels. No performance specifications is implied or guaranteed.









Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	–0.5	4.6	V
T_S	Storage temperature	–65	150	°C
T_J	Junction temperature	–	125	°C
V_{IO}	Input and output voltage	V_{SS} – 0.5	V_{DD} + 0.5	V
ESD	Electrostatic discharge voltage per MIL-STD-833, Method 3015	2000	–	V

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating voltage	3.14	3.3	3.47	V
T_A	Ambient temperature, commercial grade	0	–	70	°C
	Ambient temperature, industrial grade	–40	--	85	°C
C_{LOAD}	Maximum load capacitance on the CLK output	–	–	15	pF
t_{PU}	Power-up time for V_{DD} to reach the minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Recommended Crystal Specifications for non-VCXO Applications

Parameter	Name	Description	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, and AT cut	8	–	30	MHz
C_{LNOM}	Nominal load capacitance		6	–	30	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	35	50	Ω
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW

Pullable Crystal Specifications for VCXO Application only

Parameter [9]	Name	Min	Typ	Max	Unit
C_{LNOM}	Crystal load capacitance	–	14	–	pF
R_1	Equivalent series resistance	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR. Ratio is used because typical R_1 values are much less than the maximum spec.	3	–	–	–
DL	Crystal drive level. No external series resistor assumed	–	0.5	2	mW
F_{3SEPHI}	Third overtone separation from 3 × F_{NOM} (high side)	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3 × F_{NOM} (low side)	–	–	–150	ppm
C0	Crystal shunt capacitance			7	pF
C0/C1	Ratio of shunt to motional capacitance	180	–	250	
C_1	Crystal motional capacitance	14.4	18	21.6	fF

Note
9. Crystals that meet this specification include Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, and PDI HA13500XFSA14XC.

DC Electrical Specifications

Parameter [10]	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output high current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V (source)	12	24	–	mA
I_{OL}	Output low current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V (sink)	12	24	–	mA
C_{IN1}	Input capacitance	All input pins except XIN and XOUT	–	–	7	pF
C_{IN2}	Input capacitance	XIN and XOUT pins for non-VCXO applications	–	24	–	pF
I_{IH}	Input high current	$V_{IH} = V_{DD}$	–	5	10	µA
I_{IL}	Input low current	$V_{IL} = 0$ V	–	–	50	µA
$f_{\Delta XO}$	VCXO pullability range	Using crystal in this data sheet	±150	–		ppm
V_{VCXO}	VCXO input range		0	–	V_{DD}	V
V_{IH}	Input high voltage	CMOS levels, 70% of V_{DD}	0.7 × V_{DD}	–	–	V
V_{IL}	Input low voltage	CMOS levels, 30% of V_{DD}	–	–	0.3 × V_{DD}	V
I_{DD}[11]	V_{DD} supply current	All three clock outputs are at 100 MHz	–	30	–	mA

Notes
10. Not 100% tested, guaranteed by design.
11. Power supply current is configuration dependent. Use CyClocksRT to calculate actual I_{DD} for specific output frequency configurations.

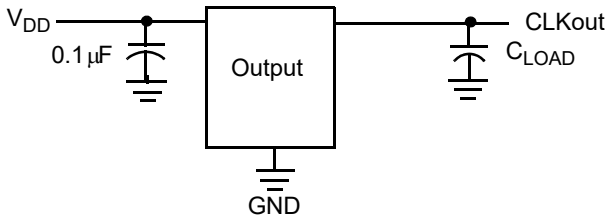
AC Electrical Characteristics

Parameter [12]	Name	Description	Min	Typ	Max	Unit
f_{REFC}	Reference frequency - crystal		8	–	30	MHz
f_{REFD}	Reference frequency - driven		1	–	133	MHz
f_{OUT}	Output frequency, commercial grade		–	–	200	MHz
	Output frequency, industrial grade		–	–	166.6	MHz
DC	Output duty cycle	50% of V_{DD}, see Figure 6	45	50	55	%
t_3	Rising edge slew rate	Output clock rise time, 20%–80% of V_{DD}, see Figure 7	0.8	1.4	–	V/ns
t_4	Falling edge slew rate	Output clock fall time, 80%–20% of V_{DD}, see Figure 7	0.8	1.4	–	V/ns
t_5[13]	Skew	Output-output skew between related outputs, see Figure 9	–	–	250	ps
t_6[14]	Clock jitter	Peak-to-peak period jitter, see Figure 8	–	250	–	ps
t_{CCJ}[14]	Cycle-to-cycle jitter CLKA/B/C	XIN = CLKA/B/C = 166 MHz, ±2% spread and No REFOUT, V_{DD} = 3.3 V, see Figure 10	–	–	110	ps
		XIN = CLKA/B/C = 66.66 MHz, ±2% spread and No REFOUT, V_{DD} = 3.3 V, see Figure 10	–	–	170	ps
		XIN = CLKA/B/C = 33.33 MHz, ±2% spread and No REFOUT, V_{DD} = 3.3 V, see Figure 10	–	–	140	ps
		XIN = CLKA/B/C = 14.318 MHz, ±2% spread and No REFOUT, V_{DD} = 3.3 V, see Figure 10	–	–	290	ps
t_{PD}	Power-down time	Time from falling edge on PD# pin to tristated outputs (asynchronous), see Figure 11	–	150	300	ns
t_{OE1}	Output disable time	Time from falling edge on OE pin to tristated outputs (asynchronous), see Figure 12	–	150	300	ns
t_{OE2}	Output enable time	Time from rising edge on OE pin to valid clock outputs (asynchronous), see Figure 12	–	150	300	ns
F_{MOD}	Spread spectrum modulation frequency		30.1	31.5	32.9	kHz
t_{10}	PLL lock time		–	–	3	ms

Notes
12. Not 100% tested, guaranteed by design.
13. Skew value guaranteed when outputs are generated from the same divider bank.
14. Jitter measurement may vary. Actual jitter is dependent on input jitter and edge rate, number of active outputs, input and output frequencies, supply voltage, temperature, and output load.

Test Circuit

Figure 5. Test Circuit Diagram



Timing Definitions

Figure 6. Duty Cycle Definition; DC = t2/t1

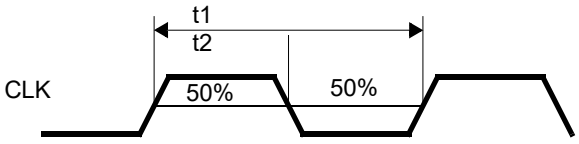


Figure 7. Rise and Fall Time Definitions

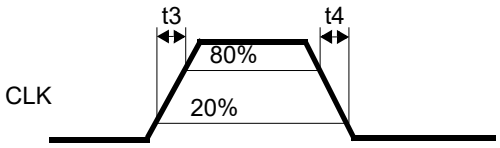


Figure 8. Period Jitter Definition

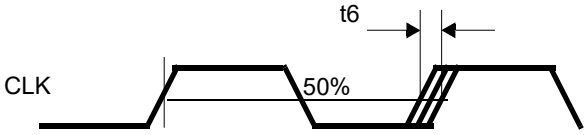


Figure 9. Skew Definition

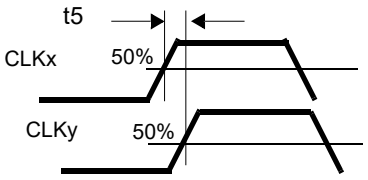


Figure 10. Cycle to Cycle Jitter Definition (CCJ)

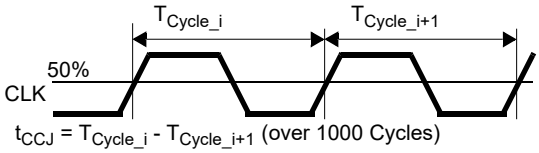


Figure 11. Power-Down and Power-Up Timing

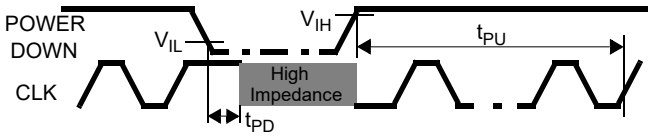
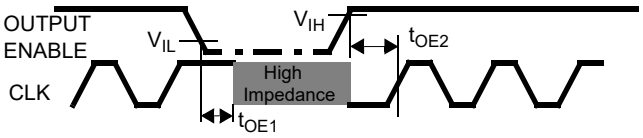


Figure 12. Output Enable and Disable Timing



2-wire Serial (I^2C) Interface Timing

When using I^2C interface, the CY22801 should be programmed as I^2C-capable prior to using this interface.

The CY22801 uses a 2-wire serial-interface SDAT and SCLK that operates up to 400 kbits/second in read or write mode. The basic write serial format is as follows.

Start Bit; seven-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); eight-bit Memory Address (MA); ACK; eight-bit data; ACK; eight-bit data in MA + 1 if desired; ACK; eight-bit data in MA+2; ACK; and so on, until STOP bit. The basic serial format is illustrated in Figure 14.

Data Valid

Data is valid when the Clock is HIGH, and may only be transitional when the clock is LOW, as illustrated in Figure 13.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 15.

Start Sequence – Start frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a Start signal is given, the next eight-bit data must be the device address (seven bits) and a R/W bit, followed by the register address (eight bits) and register data (eight bits).

Stop Sequence – Stop frame is indicated by SDAT going HIGH when SCLK is HIGH. A Stop frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During Write mode, the CY22801 responds with an ACK pulse after every eight bits. This is accomplished by pulling the SDAT line LOW during the N × 9th clock cycle, as illustrated in Figure 16. (N = the number of eight-bit segments transmitted.) During Read mode, the ACK pulse, after the data packet is sent, is generated by the master.

Figure 13. Data Valid and Data Transition Periods

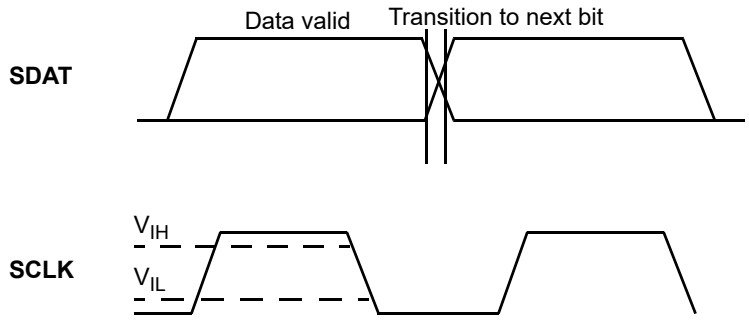


Figure 14. Data Frame Architecture

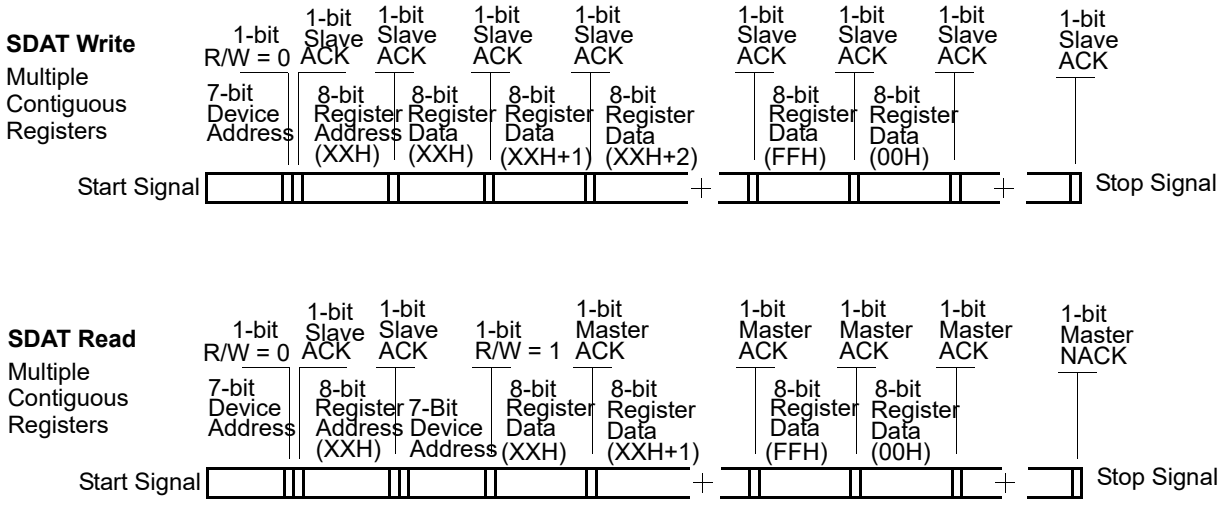


Figure 15. Start and Stop Frame

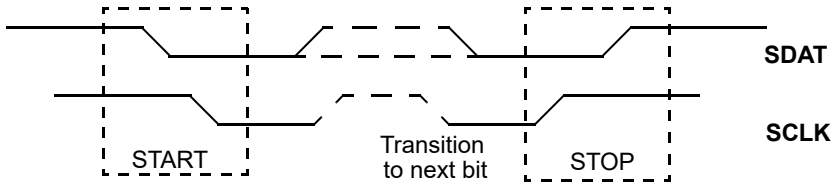


Figure 16. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data

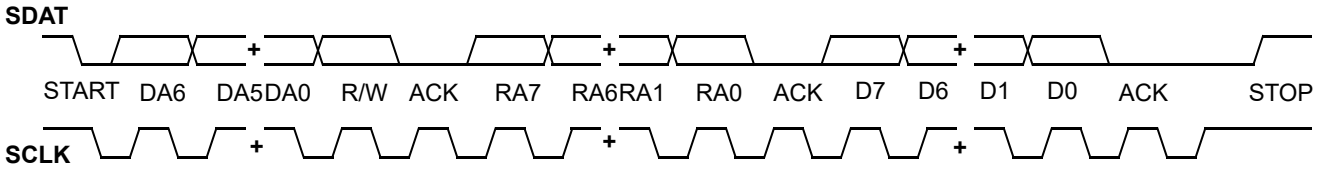


Figure 17. Definition for Timing on the Serial BUS

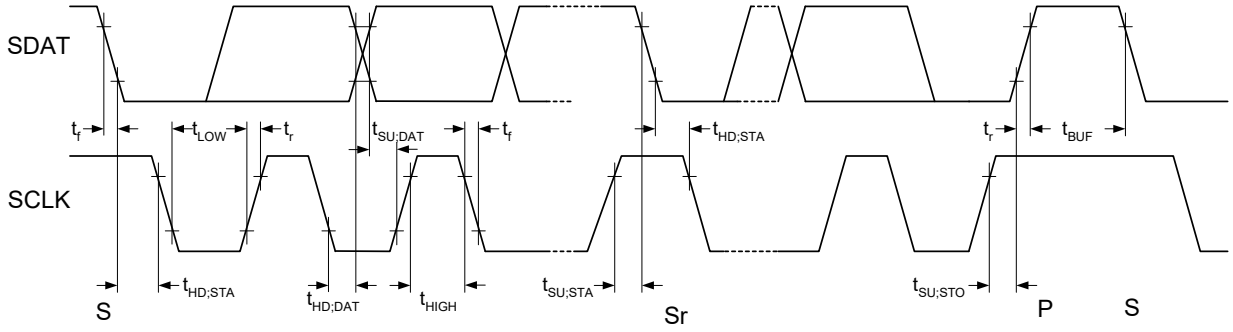


Table 16. Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	µs
t_{LOW}	Low period of the SCLK clock	1.3	–	µs
t_{HIGH}	High period of the SCLK clock	0.6	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	µs
$t_{HD:DAT}$	Data hold time	100	–	ns
$t_{SU:DAT}$	Data setup time	100	–	ns
t_R	Rise time	–	300	ns
t_F	Fall time	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	µs

Ordering Information

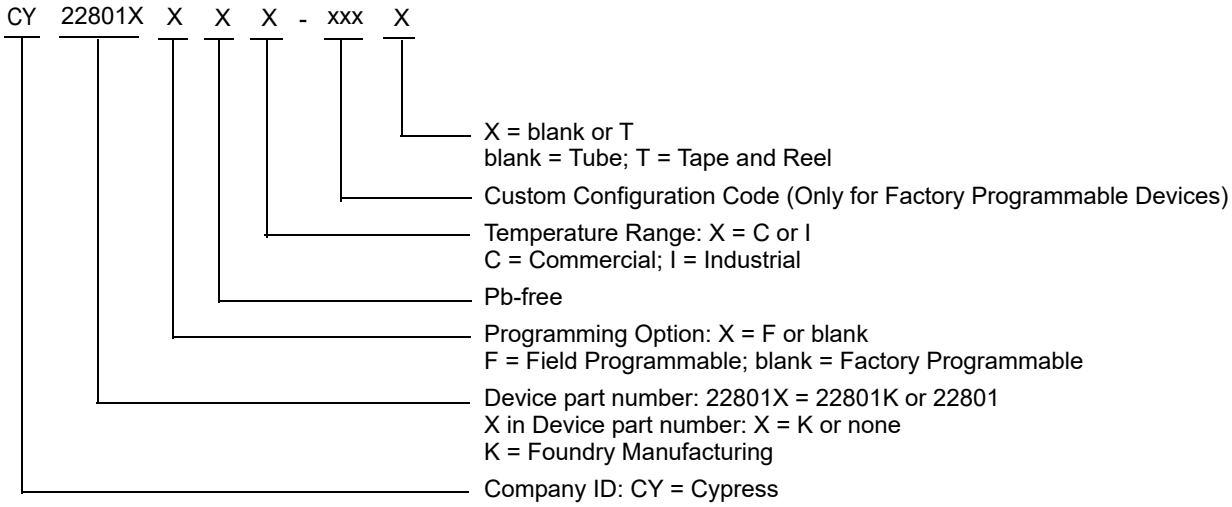
Ordering Code	Package Type	Operating Range	Operating Voltage
CY22801KFXC	8-pin SOIC	Commercial, 0 °C to 70 °C	3.3 V
CY22801KFXCT	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C	3.3 V
CY22801KFXI	8-pin SOIC	Industrial, –40 °C to 85 °C	3.3 V
CY22801KFXIT	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C	3.3 V

Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

Ordering Code	Package Type	Operating Range	Operating Voltage
CY22801SXC-xxx [15]	8-pin SOIC	Commercial, 0 °C to 70 °C	3.3 V
CY22801SXC-xxxT [15]	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C	3.3 V
CY22801SXI-xxx [15]	8-pin SOIC	Industrial, –40 °C to 85 °C	3.3 V
CY22801SXI-xxxT [15]	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C	3.3 V
CY22801KSXC-xxx [15]	8-pin SOIC	Commercial, 0 °C to 70 °C	3.3 V
CY22801KSXC-xxxT [15]	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C	3.3 V
CY22801KSXI-xxx [15]	8-pin SOIC	Industrial, –40 °C to 85 °C	3.3 V
CY22801KSXI-xxxT [15]	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C	3.3 V

Ordering Code Definitions

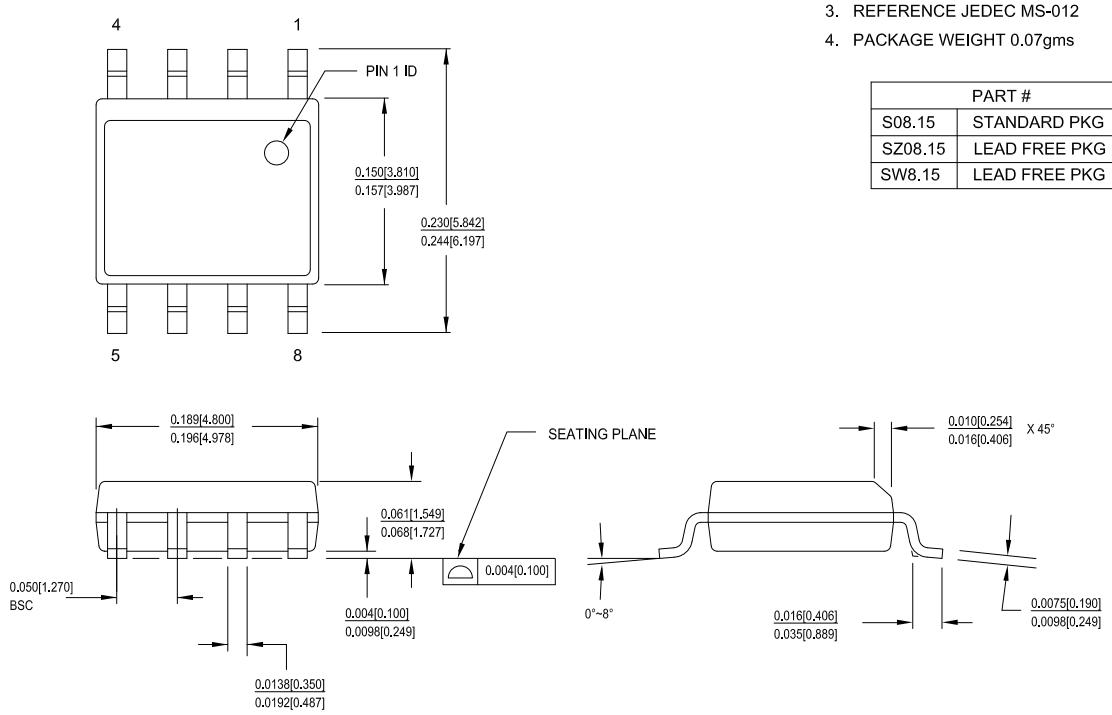


Note

15. Ordering codes with “xxx” are factory-programmed configurations. Factory programming is available for high volume orders. For more details, contact your local Cypress field application engineer or Cypress sales representative.

Package Diagram

Figure 18. 8-pin SOIC (150 Mils) S08.15/SZ08.15 Package Outline, 51-85066



Acronyms

Table 17. Acronyms Used in this Document

Acronym	Description
ACK	Acknowledge
CLKIN	Clock Input
CMOS	Complementary Metal-Oxide Semiconductor
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
EMC	Electromagnetic Compatibility
ESR	Equivalent Series Resistance
FS	Frequency Select
I^2C	Inter Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LSB	Least Significant Bit
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
MSB	Most Significant Bit
OE	Output Enable
PD	Power Down
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
SSON	Spread Spectrum ON
SCLK	Serial Interface Clock
SDAT	Serial Interface Data
SOIC	Small-Outline Integrated Circuit
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generation
UPCG	Universal Programmable Clock Generator
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator

Document Conventions

Units of Measure

Table 18. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc/Hz	decibels relative to the carrier per Hertz
fF	femtofarad
Hz	hertz
kbit	1024 bits
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY22801, Universal Programmable Clock Generator (UPCG) Document Number: 001-15571				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1058080	KVM / KKVTMP	05/10/07	New data sheet.
*A	2440787	AESA	05/16/08	Updated Ordering Information (Added existing part numbers CY22801FXCT, CY22801FXI, CY22801FXIT, CY22801SXC-xxx and CY22801SXC-xxxT and added new part numbers CY22801KFXC, CY22801KFXCT, CY22801KFXI, CY22801KFXIT, CY22801KSXC-xxx and CY22801KSXC-xxxT, added Note “Not recommended for new designs.” and referred the same note for some ordering codes, Added Note 15 and referred the same note for some ordering codes). Updated to new template.
*B	2724806	KVM / AESA	6/26/09	Updated Recommended Operating Conditions (Added T_A parameter (Industrial Grade Ambient Temperature) and details). Updated AC Electrical Characteristics (Added f_{OUT} parameter (Industrial Grade Output Frequency) and details). Updated Ordering Information (Removed CY22801FXCT and CY22801FXIT, added CY22801KSXI-xxx and CY22801KSXI-xxxT, added temperature ranges in the Operating Range column in the Ordering Information Table). Updated Package Diagram (Corrected package reference from S8 to SZ08 for the spec 51-85066).
*C	2897775	KVM	03/23/10	Updated Ordering Information: Updated part numbers (Removed inactive parts). Added Possible Configurations and moved xxx parts under the same. Updated Package Diagram: spec 51-85066 – Changed revision from *C to *D.
*D	2981862	BASH	07/15/2010	Updated Features (Added Special Features). Removed the section Benefits. Updated Logic Block Diagram. Updated Pin Configurations. Updated Pin Definitions. Added VCXO. Added Spread Spectrum Clock Generation (SSCG). Added Multifunction Pins. Added Frequency Calculation and Register Definitions Added Default Startup Condition for the CY22801. Added Frequency Calculations and Register Definitions using the Serial (I2C) Interface. Added Application Guideline. Added Possible Configuration Examples. Added Informational Graphs. Added Pullable Crystal Specifications for VCXO Application only. Updated DC Electrical Specifications (Added I_{IH}, I_{IL}, $f_{\Delta XO}$, V_{VCXO} parameters and their details). Updated AC Electrical Characteristics (Added t_{CCJ}, t_{PD}, t_{OE1}, t_{OE2}, F_{MOD} parameters and their details). Updated Timing Definitions (Added Figure 8, Figure 9, Figure 10, Figure 11, Figure 12). Added 2-wire Serial (I2C) Interface Timing. Updated Ordering Information: Updated Possible Configurations: Updated details in “Ordering Code” column. Added Ordering Code Definitions. Added Acronyms and Units of Measure.

Document History Page (continued)

Document Title: CY22801, Universal Programmable Clock Generator (UPCG) Document Number: 001-15571				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	3207656	CXQ	03/28/2011	Updated 2-wire Serial (I2C) Interface Timing: Updated Table 16 (Changed minimum value of t_{DH} parameter from 0 ns to 100 ns).
*F	3455237	BASH / PURU	12/05/2011	Updated Multifunction Pins (Added Note 1 and referred the same note in the first paragraph in the section). Updated Package Diagram: spec 51-85066 – Changed revision from *D to *E. Updated to new template.
*G	3580417	PURU	04/12/2012	Updated Features (Removed Field-programmable). Updated Functional Description (Replaced “programming using CY36800” with “programmed using Factory Specific Configurations”). Updated Default Startup Condition for the CY22801 (Added Note 6 and referred the same note at the end of 2nd paragraph in the section, added Note 7 and referred the same note at the end of 3rd paragraph in the section). Updated Frequency Calculations and Register Definitions using the Serial (I2C) Interface (Updated PLL Frequency, P Counter [40H(1..0)], [41H(7..0)], [42H(7)] (“Replaced CY22150 with CY22801”)). Updated Field Programming the CY22801 (Replaced “programming using CY36800” with “programmed using Factory Specific Configurations”). Removed the section “CY36800 InstaClock™ Kit”.
*H	3686409	PURU	07/20/2012	Updated Features (Added Field-programmable). Updated Functional Description (Replaced “programmed using Factory Specific Configurations” with “programming using CY36800”). Updated Field Programming the CY22801 (Replaced “programmed using Factory Specific Configurations” with “programming using CY36800”). Added the section “CY36800 InstaClock™ Kit”. Updated Default Startup Condition for the CY22801 (Added Note 8 and referred the same note at the end of 3nd paragraph in the section) Updated to new template.
*I	4576237	AJU	11/21/2014	Updated Features: Updated details under “Low-voltage complementary metal oxide semiconductor (LVCMOS) output frequency”. Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated AC Electrical Characteristics: Removed minimum values corresponding to f_{REFD} and f_{OUT} parameters. Updated 2-wire Serial (I2C) Interface Timing: Updated Figure 14 (Updated the last ACK in SDAT Read (Multiple Contiguous Registers) to “NACK”. Updated Package Diagram: spec 51-85066 – Changed revision from *E to *F.
*J	4632360	TAVA	01/20/2015	Updated Ordering Information: Updated Possible Configurations: Updated details in “Ordering Code” column. Updated to new template.
*K	4643649	TAVA	01/28/2015	Updated Ordering Information: Updated Possible Configurations: Updated details in “Ordering Code” column. Updated Package Diagram: spec 51-85066 – Changed revision from *F to *G.

Document History Page (continued)

Document Title: CY22801, Universal Programmable Clock Generator (UPCG) Document Number: 001-15571				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	4805790	TAVA	06/26/2015	Updated 2-wire Serial (I2C) Interface Timing: Updated Figure 13. Added Figure 17. Updated Table 16: Updated entire table. Updated to new template. Completing Sunset Review.
*M	6012075	PAWK	01/03/2018	Updated Package Diagram: spec 51-85066 – Changed revision from *G to *I. Updated to new template.

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