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DATA SHEET

PMC-1991437                    ISSUE 9

PM8316 TEMUX 84

HIGH DENSITY T1/E1 FRAMER  WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

**PMC-SIERRA**

# PM8316

# TEMUX 84

# HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MULTIPLEXER

# DATA SHEET

## PROPRIETARY AND CONFIDENTIAL

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## ISSUE 9: JANUARY 2006

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PMC-1991437 (R9), ref PMC-1991191 (R10)

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## Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,640,398   Canadian patent 2,161,921

Relevant patent applications and other patents may also exist.

# REVISION HISTORY

| Issue No. | Issue Date | Details of Change |
|---|---|---|
| 1 | Oct 27, 1999 | Original Document. Advance version. |
| 2 | Jan 24, 2000 | Upgrade document from Preview to Advance |
| 3 | Oct 19, 2000 | Preliminary version released in conjunction with Rev. A tapeout |
| 4 | May 4, 2001 | Datasheet updated to reflect Issue 5 of PMC-1991191. |
| 5 | Oct 22, 2001 | Datasheet updated to reflect Issue 6 of PMC-1991191. Go to the sections noted below to see the marked corrections in the text.<br><br>Change to Section 1: HDLC interface with 127 bytes of buffering for terminating the facility data link.<br><br>Change to Section 1: Seamlessly interfaces with 77.76 MHz Drop and 77.76 MHz Add buses.<br><br>New: Figure 1   Fractional DS3 Application<br><br>New: Figure 2   TEMUX 84 Block Diagram<br><br>Change to Section 6: In this configuration the T1 and E1 transmit framers are disabled and either the ingress or egress T1 or E1 signals are routed to the T1 or E1 framers for performance monitoring purposes, which include error event accumulation, alarm monitoring and HDLC termination.<br><br>Changes in pin table:<br><br>**Framer Recovered Clock (RSCLK[3:1])…**  When a DS3 is demapped from SONET/SDH (i.e. LINEOPT_SPEx = 01), RSCLK is a gapped version of CLK52M.<br><br>**The Ingress Flexible Bandwidth Enables (IFBWEN[3:1])…** The IFBWEN[3:1] inputs are constrained such that the maximum data rate of each of IFBWDAT[3:1] is less than 48.96 Mbit/s.<br><br>**System Reference Clock (SREFCLK)…** This clock must be phase locked to LREFCLK and can be external connected to LREFCLK.  When passing transparent virtual tributaries between the telecom bus and the SBI bus, SREFCLK must be the same frequency as LREFCLK (i.e. S77 = L77).<br><br>Change in second note to pin table:<br><br>The outputs TCLK[3:1], TPOS/TDAT[3:1], TNEG/TMFP[3:1], RGAPCLK/RSCLK[3:1], RDATO[3:1], RFPO/RMFPO[3:1], ROVRHD[3:1], TFPO/TMFPO/TGAPCLK[3:1], SBIACT, LAOE/LATPL, RECVCLK1, RECVCLK2, RECVCLK3, CASID[21:1], CCSID, TS0ID, TDO and INTB have 4 mA drive capability… The bidirectional SBI signal SDC1FP has 8mA drive capability.  MVID[21:1] have 8mA drive capability.<br><br>Changes to section 9.1<br><br>New: Section 9.2<br><br>Change to Section 9.3: For ESF, out-of-frame declaration is based strictly on Frame Alignment Signal (F1-F6) bit errors; a new frame search is never initiated upon |

excessive CRC-6 errors.

Change to Section 9.6: Received data is placed into a 127-byte FIFO buffer.

Changes to Section 9.14

Changes to Section 9.21: Add E3

New: Table 1 Path Signal Label Mismatch State

New: Section 19.37.1

Change to end of Section 9.40 The CCS H-MVIP interface, CCSID[1:3], is not multiplexed
    with any other pins.   The CCSID[1:3] outputs is always available provided
    CMV8MCLK, CMVFPB and CMVFPC are active.

Change to Section 9.43: SPE (48.96 Mbit/s).

New: Section 9.43.1 Burst Lengths on Ingress Flexible Bandwidth Port

Change to Section 9.44: The TEMUX 84 identification code is 183160CD hexadecimal.

Changes to Table 2 Register Memory Map:

| 0x0157 | SIGX Configuration |
|---|---|
| 0x01E9 | INSBI T1 Thresholds Register |
| 0x01EA | INSBI E1 Thresholds Register |
| 0x0F20 + 0x40*N | RTTB TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt |

Change to bullet in Section 12.2.1: The SAC1FP pulse must be 3n +/ 1 (where n =
    0,1,2…) SREFCLK cycles before the LAC1 pulse.

Change to Section 12.2.2: When TVTs are supported an additional constraint exists
    between SAC1FP and LAC1.  Table 16 gives the permissible combinations.

New: Table 3 TVT Constraints for 77.76MHz

Change to Section 12.2.3: TVTs are not supported for this bus configuration.

Change to Section 12.3.2: The T1 framer will determine frame alignment within 13ms

Change to Step 10 in 12.8: If PBS[2:0] = 1XX, discard the data byte read in step 5,
    decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors
    before deciding whether or not to keep the packet.

Changes to Section 12.14 and Fig 27: Add E3

Change to text just before Table 32: The signaling contained within the robbed bit
    positions of the DS0s will also have an arbitrary alignment relative to the $P_1P_0$ bits.

Change to text just after Table 38: When carrying framed E3, only the ITU-T Rec. G.751
    format is supported.  Unframed E3 is carried clear channel.

Changes to Table 39 E3 Frame Stuffing Format

Just before Figure 61: The LAC1J1V1 signal is high when the LAPL signal is high to mark
    every J1 byte of each of the three STS-1 SPEs. The LAV5 signal pulses high to mark
    the V5 bytes of each tributary.  LATPL, multiplexed with LAOE shown separately in [x-

| | | |
|---|---|---|
| | | ref], indicates valid tributary payload when high. During the V3 location LATPL indicates a negative pointer justification when high and during the byte after the V3 location LATPL low indicates a positive pointer justification. The three STS-1 SPEs have an alignment determined by the SONET/SDH Transmit Pointer Configuration registers.  A pointer of 522 decimal is illustrated in [x-ref].

Changes to Table 51

Changes to Table 54

Changes to Table 56

Changes to Table 58

Changes to Table 62 |
| 6 | Apr '02 | Change bars relative to Issue 5.

⁰  [Errata Item] The SBI Alarms description now describes the necessary conditions for setting the ALM bit for T1, E1, DS3 and E3.

⁰  [Errata Item] In the Functional Timing section there is a new description of the LADDOE register bit settings. Also, the 77.76MHz tPtel parameter has been changed.

⁰  The pin description for LAPL now clearly indicates that it will be driven only for payload bytes as configured in the TTMP, and optionally in the J1, V1, and overhead bytes.  The description of the 77MHz telecom add bus makes it clear that LATOHEN must be set on all 4 devices so that the combined telecom bus will have a valid LAPL signal.

⁰  Some A.C. parameters were added to TICLK and RCLK.

⁰  More information about whether the TEMUX 84 supports DS3 LIU interfaces simultaneously with SPEs over the telecom bus interface. Text added to Functional Description section explaining what can/ cannot be done dependent on config bits.

⁰  [Errata Item] In order for the TEMUX 84 to work along with TBS/TSE and Spectra devices in an ADM the TEMUX 84 must place a constant value in the H1/H2 fields that equals a valid pointer corresponding to the chosen, fixed SPE offset. Added text to the VTPP portion of the functional description.

⁰  All references to receive alarms affecting bit 4 of V5 removed. This behaviour is appropriate according to G.707-2000.

⁰  [Errata Item] The DS3 mapper/demapper in TEMUX 84 operates in AU3 mode only. Note added that a mix of T1/E1s mapped into SDH AU4 SPEs with DS3 Mapper/Demapper SPEs is not allowed.

⁰  The "Egress H-MVIP System Interface" section now includes text about avoiding controlled frame slips.

⁰  [Errata Item] For each reference to the DS3 linkrate, a comment has been added explaining that the ClkRate[1:0] information is not valid when the DS3 has been demapped from SONET/SDH by the D3MD function.

⁰  LAOE/LATPL has the same pad as all other Combus Add outputs, and an 8mA drive.

⁰  Functional timing diagrams for the Ingress and Egress Flexible Bandwidth ports now |

| | | |
|---|---|---|
| | | included. |
| | | º In the "T1 Bit Oriented Code Generation" section, more explanation about what happens if the code is overwritten before transmission is finished. |
| | | º In the "H-MVIP Data Format" section, some text has been added describing what happens in applications where the F-bit value is not overwritten by the transmitter. |
| | | º Flexible bandwidth now spec'd for a load of 50pf on all outputs. |
| | | º The description for MFSDC1FP has been changed. |
| | | º [Errata Item] New comments in "Clock and Frame Synchronization Constraints". |
| | | º Changes to the formula for calculating the SBI index value: <br> =4*(MVED index – 7*(SPE-1) – 1) + DS1 <br> =4*(MVED index – 7*(SPE-1) – 1) + E1 |
| | | º There is a new section outlining the PRGD blocks, mentioning how to program TAP & LENGTH registers to generate specific PRBS patterns and Repetitive patterns. |
| 7 | April 2002 | º Updated table in Operation section (Table 16: TVT Constraints for 77.76MHz) |
| | | º Changed Vt- from 0.8V to 0.6V for Schmitt trigger pads. |
| | | º Noted that L77 and S77_MVED_3 (S77 and MVED[3] pin D10) are Schmitt trigger inputs. |
| | | º Changed tSsbiadd @ 77MHz to 2.7ns from 3ns. |
| | | º Some minor changes to "Notes on Pin Desciptions" Item #2, Output drive capabilities. |
| | | º Section 15: DC Characteristics, VOH VOL, minor corrections: <br> 1) CASID[7:0] changed to CASID[21:1] <br> 2) MVID[7:0] changed to MVID[21:1] |
| 8 | January 2003 | º Documented Line Side SBI operation throughout the document including the block diagram |
| | | º Added 3 more block diagrams showing Transmux mode, Mapper/Mux mode and the placement of the T1/E1 framer and transmitter in High Density Framer mode. |
| | | º Updated the RCLK pin description to limit the tolerance on the input clock to maintain a DS1 demultiplexed clock within the standard's requirements. |
| | | º Updated the RGAPCLK/RSCLK pin description to note that an external jitter attenuator is required when connected the output clock to the PM73122 AAL1gator32 device. |
| | | º Updated the TFPI/TMFPI pin description to correct the location of the TDATIFALL bit. |
| | | º Updated the LAOE/LATPL pin description changing its output type to a tristate output. |
| | | º Updated the CLK52M pin description stating that when demapping a DS3 from SONET its frequency must be 44.928 MHz. |

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º   Updated the SREFCLK pin description adding that it can tolerate a +/-50 ppm accurate clock source when operating in serial DS3 mode.

º   Updated the SDC1FP pin description noting that the input must be held low when the SBI and H-MVIP buses are both not being used.

º   Updated the MVID[21:1] output pins' current drive strength to 4 mA.

º   Updated section 9.2 Transmultiplexing to state that section 12.2.3 of the datasheet must be followed when operating in transmux mode. Also that the initialization sequence of the TEMUX 84 Programmer's Guide for transmux mode must be followed to operate correctly.

º   Updated section 9.11, E1 Transmitter, with details on the operation of inserting National Use, Sa, bits.

º   Updated an input to a multiplexer in Figure 17 DS3/E3 Configuration Options.

º   Updated a register bit setting in section 9.20 Receive Tributary Byte Synchronous Demapper and section 9.25 Transmit Tributary Byte Synchronous Mapper.

º   Updated 9.21.3 DS3 Desynchronizer to note that the demapped clock must pass through an external jitter attenuator before connecting it to the PM73122 AAL1gator32 device. Also removed the 51.84 MHz option for CLK52M.

º   Added the following registers to Table 9 Register Memory Map: 0x01C4 DLL Configuration (SBI Bus), 0x01C6 DLL Delay Tap Status (SBI Bus), 0x01C7 DLL Control Status (SBI Bus), 0x073C DLL Configuration (TelecomBus), 0x073E DLL Delay Tap Status (TelecomBus) and 0x073F DLL Control Status (TelecomBus).

º   Updated the Version Number and Device Identification values of Table 11 Identification Register in section 11.1 JTAG Test Port.

º   Updated the Id bit for OEB_RECVCLK_1 in Table 12 Boundary Scan Register of 11.1 JTAG Test Port.

º   Updated section 12.2.2 SBI and Telecom Buses Both 19.44 MHz with TVT constraints when the IVTPP or EVTPP are bypassed.

º   Updated section 12.2.3 SBI and Telecom Buses Both 77.76 MHz stating that the constraints must be followed for transmux mode.

º   Updated section 12.3 SLC®96, removing all references to using the H-MVIP bus.

º   Updated section 12.10 Using the Internal T1/E1 Data Link Transmitter noting that the minimum packet size for THDL is 2 bytes.

º   Updated section 12.14 DS3 and E3 Loopback Modes removing the sentence that states a DS3 AIS can be transmitted when a DS3 digital diagnostic loopback is enabled.

º   Added section 12.20 Configuring the Line Side SBI.

º   Updated the Lead Temperature Maximum rating to 225°C from 230°C in Table 47

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| | | | |
|---|---|---|---|
| | | | Absolute Maximum Ratings.<br><br>º   Corrected the maximum RCLK[3:1] frequency for E3 mode in Table 53: DS3/E3 Receive Interface Timing. |
| 9 | January 2006 | º | Updated ordering information including RoHS-compliant device details. |

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# 1    <u>FEATURES</u>

- Integrates 84 T1/E1 framers, three SONET/SDH VT1.5/VT2/TU11/TU12 bit asynchronous or byte synchronous mappers, three full featured M13 multiplexers with DS3 framers, three E3 framers, and three SONET/SDH DS3 mappers in a single monolithic device for terminating DS3 multiplexed T1 streams, SONET/SDH mapped T1 streams or SONET/SDH mapped E1 streams.

- Each SPE/DS3 independently programmable to allow the following modes of operation:

- Eight T1 modes of operation:

  - Up to 84 T1 streams mapped as bit asynchronous VT1.5 virtual tributaries into three STS-1 SPEs or TU-11 tributary units into three STM-1/VC3 or TUG3 from a STM-1/VC4.

  - Up to 84 T1 streams mapped as byte synchronous VT1.5 virtual tributaries into three STS-1 SPEs or TU-11 tributary units into three STM-1/VC3 or TUG3 from a STM-1/VC4.

  - Three STS-1, AU3 or TUG3 Bit Asynchronous VT1.5 or TU-11 Mappers with ingress or egress per tributary link monitoring.

  - Up to 84 T1 streams M13 multiplexed into three serial DS3 streams.

  - Up to 84 T1 streams M13 multiplexed into three DS3s, the DS3s are asynchronously mapped into three STS-1/STM-0 SPEs.

  - DS3 M13 Multiplexer with ingress or egress per link monitoring.

  - Up to 84 DS3 multiplexed T1 streams are mapped as bit asynchronous VT1.5 virtual tributaries or TU-11 tributary units, providing a transmultiplexing ("transmux") function between DS3 and SONET/SDH.

  - Up to 63 T1 streams mapped as bit asynchronous TU-12 tributary units into three STM-1/VC3 or TUG3 from a STM-1/VC4.

- Four E1 modes of operation:

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- Up to 63 E1 streams mapped as bit asynchronous VT2 virtual tributaries into three STS-1 SPE or TU-12 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4.

- Up to 63 E1 streams mapped as byte synchronous VT2 virtual tributaries into three STS-1 SPE or TU-12 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4.

- Three STS-1, AU3 or TUG3 Bit Asynchronous VT2 or TU-12 Mappers with ingress or egress per tributary link monitoring.

- Up to 63 E1 streams multiplexed into three DS3s following the ITU-T G.747 recommendation.

- Two unchannelized DS3 modes of operation:

  - Standalone unchannelized DS3 framer mode for access to the entire DS3 payload.

  - Up to three DS3 streams are mapped bit asynchronously into VC-3s. The VC-3s are aligned within AU-3s.

- Standalone unchannelized E3 framer mode (ITU-T Rec. G.751) for access to the entire E3 payload.

- Up to 84 VT1.5/TU11 or 63 VT2/TU12 tributaries can be passed between the line SONET/SDH bus and the system SBI bus as transparent virtual tributaries with pointer processing.

- Supports 8 Mbit/s H-MVIP on the system interface for all T1 or E1 links, a separate 8 Mbit/s H-MVIP system interface for all T1 or E1 CAS channels and a separate 8 Mbit/s H-MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.

- Supports a byte serial Scaleable Bandwidth Interconnect (SBI) bus interface for high density system side device interconnection of up to 84 T1 streams, 63 E1 streams, 3 DS3 streams or 3 E3 streams. This interface also supports transparent virtual tributaries when used with the SONET/SDH mapper.

- Supports insertion and extraction of arbitrary rate (eg. fractional DS3) data streams to and from the SBI bus interface.

- Provides jitter attenuation in the T1 or E1 receive and transmit directions.

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- Provides three independent de-jittered T1 or E1 recovered clocks for system timing and redundancy.

- Provides per link diagnostic and line loopbacks.

- Provides an on-board programmable binary sequence generator and detector for error testing at DS3 and E3 rates. Includes support for patterns recommended in ITU-T O.151.

- Also provides PRBS generators and detectors on each tributary for error testing at DS1, E1 and NxDS0 rates as recommended in ITU-T O.151 and O.152.

- Supports the M23 and C-bit parity DS3 formats.

- When configured to operate as a DS3 or E3 Framer, gapped transmit and receive clocks can be optionally generated for interface to link layer devices which only need access to payload data bits.

- DS3 or E3 Transmit clock source can be selected from either an external oscillator or from the receive side clock (loop-timed).

- Provides a SONET/SDH Add/Drop bus interface with integrated VT1.5, TU-11, VT2 and TU-12 mapper for T1 and E1 streams. Also provides a DS3 mapper.

- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.

- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

- Low power 1.8V/3.3V CMOS technology.  All pins are 5V tolerant.

- 324-pin fine pitch PBGA package (23mm x 23mm). Supports industrial temperature range (-40$^o$C to 85$^o$C) operation.

**Each one of 84 T1 receiver sections:**

- Frames to DS-1 signals in SF, SLC®96 and ESF formats.

- Frames to TTC JT-G.704 multiframe formatted J1 signals.  Supports the alternate CRC-6 calculation for Japanese applications.

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- Provides Red, Yellow, and AIS alarm integration.

- Supports RAI-CI and AIS-CI alarm detection and generation.

- Provides ESF bit-oriented code detection and an HDLC/LAPD interface for terminating the ESF facility data link.

- Provides Inband Loopback Code generation and detection.

- Indicates signaling state change, and two superframes of signaling debounce on a per-DS0 basis.

- Provides an HDLC interface with 127 bytes of buffering for terminating the facility data link.

- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.

- Provides an optional elastic store which may be used to time the ingress streams to a common clock and frame alignment in support of a H-MVIP interface.

- Provides DS-1 robbed bit signaling extraction and insertion, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and two superframes of signaling debounce on a per-channel basis.

- A pseudo-random sequence user selectable from $2^7 -1$, $2^{11} -1$, $2^{15} -1$ or $2^{20} - 1$, may be detected in the T1 stream in either the ingress or egress directions. The detector counts pattern errors using a 16-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire T1 or any combination of DS0s within a framed T1.

- Line side interface is either from the DS3 interface via the M13 multiplex or from the SONET/SDH Drop bus via the VT1.5, TU-11, VT2 or TU-12 demapper. Line side interface can also be configured as SBI bus.

- System side interface is either H-MVIP or SBI bus.

- Frames in the presence of and detects the "Japanese Yellow" alarm.

- Supports the alternate CRC-6 calculation for Japanese applications.

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- Provides external access for up to three de-jittered recovered T1 clocks.

**Each one of 63 E1 receiver sections:**

- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent ITU-T G.706 specifications.

- Provides an HDLC interface with 127 bytes of buffering for terminating the national use bit data link.

- Extracts 4-bit codewords from the E1 national use bits as specified in ETS 300 233.

- V5.2 link indication signal detection.

- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.

- Provides a two-frame elastic store buffer for backplane rate adaptation that performs controlled slips and indicates slip occurrence and direction.

- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling.  Alternatively, a common channel signaling data link may be extracted from timeslot 16.

- Can be programmed to generate an interrupt on change of signaling state.

- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.

- A pseudo-random sequence user selectable from $2^7 -1$, $2^{11} -1$, $2^{15} -1$ or $2^{20} - 1$, may be detected in the E1 stream in either the ingress or egress directions. The detector counts pattern errors using a 16-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire E1 or any combination of timeslots within the framed E1.

- Line side interface is from the SONET/SDH Drop bus via the VT2 or TU-12 demapper. Line side interface can also be configured as SBI bus.

- System side interface is either H-MVIP or SBI bus.

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- Provides external access for up to three de-jittered recovered E1 clocks.

**Each one of 84 T1 transmitter sections:**

- May be timed to its associated receive clock (loop timing) or may derive its timing from the data rate received at the system interface or a common transmit clock; the transmit line clock may be synthesized from an N*8 kHz reference.

- Provides minimum ones density through Bell (bit 7), GTE or "jammed bit 8" zero code suppression on a per-DS0 basis.

- Provides a 128 byte buffer to allow insertion of the facility data link using the host interface.

- Supports transmission of the alarm indication signal (AIS) or the Yellow alarm signal in SF, SLC®96 and ESF formats.

- Provides transparency for the F-bit to support SLC®96 data link insertion.

- Autonomously transmits an ESF Performance Report Message each second.

- Provides a digital phase locked loop for generation of a low jitter transmit clock.

- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter.

- Supports the alternate ESF CRC-6 calculation for Japanese applications.

- A pseudo-random sequence user selectable from $2^7 - 1$, $2^{11} - 1$, $2^{15} - 1$ or $2^{20} - 1$, may be inserted into the T1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire T1 or any combination of DS0s within the framed T1.

- Line side interface is through either DS3 Interface via the M13 multiplex or the SONET/SDH Add bus via the VT1.5, TU-11, VT2 or TU-12 mapper. Line side interface can also be configured as SBI bus.

- System side interface is either H-MVIP or SBI bus.

**Each one of 63 E1 transmitter sections:**

- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.

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- Transmits G.704 basic and CRC-4 multiframe formatted E1.

- Supports unframed mode and framing bit, CRC, or data link by-pass.

- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.

- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.

- Provides a digital phase locked loop for generation of a low jitter transmit clock.

- A pseudo-random sequence user selectable from $2^7 -1$, $2^{11} -1$, $2^{15} -1$ or $2^{20} - 1$, may be inserted into the E1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire E1 or any combination of timeslots within the framed E1.

- Optionally inserts a datalink in the E1 national use bits.

- Supports 4-bit codeword insertion in the E1 national use bits as specified in ETS 300 233

- Supports transmission of the alarm indication signal (AIS) and the remote alarm indication (RAI) signal.

- Line side interface is through the SONET/SDH Add bus via the VT2 or TU-12 mapper. Line side interface can also be configured as SBI bus.

- System side interface is either H-MVIP or SBI bus.

**Six full featured T1/E1 Pattern Generators and Detectors:**

- Each generator and detector pair may be associated with any one of the 84 T1s or 63 E1s.

- Any sub-set of DS0s within a tributary may be selected.

- Provides programmable pseudo-random test sequence generation (up to $2^{32}-1$ bit length sequences conforming to ITU-T O.151 standards) or any repeating pattern up to 32 bits. Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from $10^{-1}$ to $10^{-7}$.

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**Each one of three SONET/SDH Tributary Path Processing Sections:**

- Interfaces with a byte wide Telecom Add/Drop bus, interfacing directly with the PM5362 TUPP-PLUS and PM5342 SPECTRA-155 at 19.44 MHz.

- Seamlessly interfaces with 77.76 MHz Drop and 77.76 MHz Add buses.

- Compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level tributary pointers.

- Optionally frames to the H4 byte in the path overhead to determine tributary multi-frame boundaries and generates change of loss-of-frame status interrupts.

- Detects loss of pointer (LOP) and re-acquisition for each tributary and optionally generates interrupts.

- Detects tributary path alarm indication signal (AIS) and return to normal state for each tributary and optionally generates interrupts

- Detects tributary elastic store underflow and overflow and optionally generates interrupts.

- Provides individual tributary path signal label register that hold the expected label and detects tributary path signal label mismatch alarms (PSLM) and return to matched state for each tributary and optionally generates interrupts.

- Detects tributary path signal label unstable alarms (PSLU) and return to stable state for each tributary and optionally generates interrupts.

- Detects assertion and removal of tributary extended remote defect indications (RDI) for each tributary and optionally generates interrupts.

- Calculates and compares the tributary path BIP-2 error detection code for each tributary and configurable to accumulate the BIP-2 errors on block or bit basis in internal registers.

- Allows insertion of all-zeros or all-ones tributary idle code with unequipped indication and valid pointer into any tributary under software control.

- Allows software to force the AIS insertion on a per tributary basis.

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- Inserts valid H4 byte and all-zeros fixed stuff bytes. Remaining path overhead bytes (J1, B3, C2, G1, F2, Z3, Z4, Z5) are set to all-zeros.

- Inserts valid pointers and all-zeros transport overhead bytes on the outgoing Telecom Add bus, with valid control signals.

- Support in-band error reporting by updating the FEBE, RDI and RFI bits in the V5 byte with the status of the incoming stream and remote alarm pins.

- Calculates and inserts the tributary path BIP-2 error detection code for each tributary.

**Each one of three SONET/SDH VT/TU Mapper Sections:**

- Inserts up to 28 bit asynchronous mapped VT1.5 virtual tributaries into an STS-1 SPE from T1 streams.

- Inserts up to 28 bit asynchronous mapped TU-11 tributary units into a STM-1/VC4 TUG3 or STM-1/VC3 from T1 streams.

- Inserts up to 28 byte synchronous mapped VT1.5 virtual tributaries into an STS-1 SPE or TU-11 tributary units into an STM-1/VC3 or TUG3 from a STM-1/VC4.

- Inserts up to 21 bit asynchronous mapped VT2 virtual tributaries into an STS-1 SPE from E1 streams.

- Inserts up to 21 bit asynchronous mapped TU-12 tributary units into an STM-1/VC4 TUG3 or STM-1/VC3 from E1 or T1 streams.

- Processes the tributary trace message (J2) of the tributaries carried in each STS-1/TUG-3 synchronous payload envelope.

- Bit asynchronous mapping assigns stuff control bits for all streams independently using an all digital control loop. Stuff control bits are dithered to produce fractional mapping jitter at the receiving desynchronizer.

- Sets all fixed stuff bits for asynchronous mappings to zeros or ones per microprocessor control

- Extracts up to 28 bit asynchronous mapped VT1.5 virtual tributaries from an STS-1 SPE into T1 streams via an optional elastic store.

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- Extracts up to 28 bit asynchronous mapped TU-11 tributary units from an STM-1/VC4 TUG3 or STM-1/VC3 into T1 streams via an optional elastic store.

- Extracts up to 21 bit asynchronous mapped VT2 virtual tributaries from an STS-1 SPE into E1 streams via an optional elastic store.

- Extracts up to 21 bit asynchronous mapped TU-12 tributary units from an STM-1/VC4 TUG3 or STM-1/VC3 into E1 or T1 streams via an optional elastic store.

- Demapper ignores all transport overhead bytes, path overhead bytes and stuff (R) bits.

- Performs majority vote C-bit decoding to detect stuff requests.

**Each one of three SONET/SDH DS3 Mapper Sections:**

- Maps a DS3 stream into an STS-1 SPE (AU3).

- Sets all fixed stuff (R) bits to zeros or ones per microprocessor control.

- Extracts a DS3 stream from an STS-1 SPE (AU3).

- Demapper ignores all transport overhead bytes, path overhead bytes and stuff (R) bits.

- Performs majority vote C-bit decoding to detect stuff requests.

- Complies with DS3 to STS-1 asynchronous mapping standards.

**Each one of three DS3 Receiver Sections:**

- Frames to a DS3 signal with a maximum average reframe time of less than 1.5 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2).

- Decodes a B3ZS-encoded signal and indicates line code violations. The definition of line code violation is software selectable.

- Provides indication of M-frame boundaries from which M-subframe boundaries and overhead bit positions in the DS3 stream can be determined by external processing.

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- Detects the DS3 alarm indication signal (AIS) and idle signal. Detection algorithms operate correctly in the presence of a $10^{-3}$ bit error rate.

- Extracts valid X-bits and indicates far end receive failure (FERF).

- Accumulates up to 65,535 line code violation (LCV) events per second, 65,535 P-bit parity error events per second, 1023 F-bit or M-bit (framing bit) events per second, 65,535 excessive zero (EXZ) events per second, and when enabled for C-bit parity mode operation, up to 16,383 C-bit parity error events per second, and 16,383 far end block error (FEBE) events per second.

- Detects and validates bit-oriented codes in the C-bit parity far end alarm and control channel.

- Terminates the C-bit parity path maintenance data link with an integral HDLC receiver having a 128-byte deep FIFO buffer with programmable interrupt threshold. Supports polled or interrupt-driven operation. Selectable none, one or two address match detection on first byte of received packet.

- Programmable pseudo-random test-sequence detection–(up to $2^{32}-1$ bit length patterns conforming to ITU-T O.151 standards) and analysis features.

**Each one of three DS3 Transmit Sections:**

- Provides the overhead bit insertion for a DS3 stream.

- Provides a bit serial clock and data interface, and allows the M-frame boundary and/or the overhead bit positions to be located via an external interface.

- Provides B3ZS encoding.

- Generates a B3ZS encoded 100… repeating pattern to aid in pulse mask testing.

- Inserts far end receive failure (FERF), the DS3 alarm indication signal (AIS) and the idle signal when enabled by internal register bits.

- Provides optional automatic insertion of far end receive failure (FERF) on detection of loss of signal (LOS), out of frame (OOF), alarm indication signal (AIS) or red alarm condition.

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- Provides diagnostic features to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error  (FEBE) events.

- Supports insertion of bit-oriented codes in the C-bit parity far end alarm and control channel.

- Optionally inserts the C-bit parity path maintenance data link with an integral HDLC transmitter.  Supports polled and interrupt-driven operation.

- Provides programmable pseudo-random test sequence generation (up to $2^{32}$-1 bit length sequences conforming to ITU-T O.151 standards) or any repeating pattern up to 32 bits.  The test pattern can be framed or unframed. Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from $10^{-1}$ to $10^{-7}$.

**M23 Multiplexer Section:**

- Multiplexes 7 DS2 bit streams into a single M23 format DS3 bit stream.

- Performs required bit stuffing/destuffing including generation and interpretation of C-bits.

- Includes required FIFO buffers for rate adaptation in the multiplex path.

- Allows insertion and detection of per DS2 payload loopback requests encoded in the C-bits to be activated under microprocessor control.

- Internally generates a DS2 clock for use in integrated M13 or C-bit parity multiplex applications. Alternatively accepts external DS2 clock reference.

- Allows per DS2 alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.

- Allows DS2 alarm indication signal (AIS) to be activated or cleared in the demultiplex direction automatically upon loss of DS3 frame alignment or signal.

- Supports C-bit parity DS3 format.

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### DS2 Framer Section:

- Frames to a DS2 (ANSI T1.107 section 8) signal with a maximum average reframe time of less than 7 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2).

- Detects the DS2 alarm indication signal (AIS) in 9.9 ms in the presence of a $10^{-3}$ bit error rate.

- Extracts the DS2 X-bit remote alarm indication (RAI) bit and indicates far end receive failure (FERF).

- Accumulates up to 255 DS2 M-bit or F-bit error events per second.

### DS2 Transmitter Section:

- Generates the required X, F, and M bits into the transmitted DS2 bit stream. Allows inversion of inserted F or M bits for diagnostic purposes.

- Provides for transmission of far end receive failure (FERF) and alarm indication signal (AIS) under microprocessor control.

- Provides optional automatic insertion of far end receive failure (FERF) on detection of out of frame (OOF), alarm indication signal (AIS) or red alarm condition.

### M12 Multiplexer Section:

- Multiplexes four DS1 or three 2048 kbit/s (according to ITU-T Rec. G.747) bit streams into a single M12 format DS2 bit stream.

- Performs required bit stuffing including generation and interpretation of C-bits.

- Includes required FIFO buffers for rate adaptation in the multiplex path.

- Performs required inversion of second and fourth multiplexed DS1 streams as required by ANSI T1.107 Section 7.2.

- Allows insertion and detection of per DS1 payload loopback requests encoded in the C-bits to be activated under microprocessor control.

- Allows per tributary alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.

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- Allows automatic tributary AIS to be activated upon DS2 out of frame.

**Each one of three E3 Framer Sections:**

- Frames to G.751 and G.832 E3 unchannelized data streams.

- For G.832, terminates the Trail Trace and either the Network Requirement or the General Purpose data link.

**Each one of three E3 Transmit Sections:**

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features.

- for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.

**Synchronous System Interfaces:**

- Provides twenty one 8 Mbit/s H-MVIP data interfaces for synchronous access to all the DS0s of all 84 T1 links or all timeslots of all 63 E1s. T1 DS0s are bundled from four T1 links in sequential order, 1-4, 5-8, 9-12, ..., 81-84. E1 timeslots are bundled from 4 E1 links in sequential order, 1-4, 5-8, 9-12, ..., 57-60 and 61-63.

- Provides twenty one 8 Mbit/s H-MVIP interfaces for synchronous access to all channel associated signaling (CAS) bits for all T1 DS0s or E1 timeslots. The CAS bits occupy one nibble of every byte on the H-MVIP interfaces and are repeated over the entire T1 or E1 multi-frame.

- Provides three 8 Mbit/s H-MVIP interfaces for common channel signaling (CCS) channels as well as V5.1 and V5.2 channels. In T1 mode DS0 24 is available through this interface. In E1 mode timeslots 15, 16 and 31 are available through this interface. Optionally, timeslot 0 may be presented instead of timeslot 15.

- All links accessed via the H-MVIP interface will be synchronously timed to the common H-MVIP clock and frame alignment signals, CMV8MCLK, CMVFP, CMVFPC.

- H-MVIP access for Channel Associated Signaling is available with the Scaleable Bandwidth Interconnect bus as an optional replacement for CAS

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access over the SBI bus as well as with the H-MVIP data interface. Common Channel Signaling H-MVIP access is available with the SBI bus, serial PCM and H-MVIP data interfaces.

- Alarm status, T1 F-bit and inband signaling control is available using otherwise unused bit positions.

- Compatible with H-MVIP PCM backplanes supporting 8.192 Mbit/s.

**Scaleable Bandwidth Interconnect (SBI) Bus:**

- Provides a high density byte serial interconnect for all framed and unframed TEMUX 84 links. Utilizes an Add/Drop configuration to asynchronously mutliplex up to 84 T1s, 63 E1s or 3 DS3s, with multiple payload or link layer processors.  Line side and system side interfaces can be configured as SBI bus.

- System side SBI bus operates at either 19.44 MHz or 77.76 MHz.  Line side SBI bus operates at 19.44MHz to communicate with PM4318 OCTLIU or PM4319 OCTLIU SH.

- External devices can access unframed DS3, framed unchannelized DS3, unframed E3, framed unchannelized E3, unframed (clear channel) T1s, framed T1s, unframed (clear channel) E1s, framed E1s, arbitrary rate clear channel data stream (eg. fractional DS3), transparent virtual tributaries or transparent tributary units over this interface.

- Framed and unframed T1 access can be selected on a per T1 basis.  Framed and unframed E1 access can be selected on a per E1 basis.

- Up to three arbitrary rate data streams inserted into and extracted from the SBI via bit serial ports.

- Synchronous access for T1 DS0 channels or E1 timeslots is supported in a locked format mode.  Selectable on a per tributary basis.

- Transparent VT/TU access can be selected only when tributaries are mapped into SONET/SDH.

- Transparent VT1.5s and TU-11s can be selected on a per tributary basis in combination with framed and unframed T1s. Transparent VT2s and TU-12s can be selected on a per tributary basis in combination with framed and unframed E1s.

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- Channel associated signaling bits for channelized T1 and E1 are explicitly identified across the bus.

- Transmit timing is mastered either by the TEMUX 84 or a layer 2 device connecting to the SBI bus. Timing mastership is selectable on a per tributary basis, where a tributary is either an individual T1, E1, E3 or a DS3.

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## 2      APPLICATIONS

- High density T1 interfaces for multiplexers, multi-service switches, routers and digital modems.

- High density E1 interfaces for multiplexers, multi-service switches, routers and digital modems.

- Frame Relay switches and access devices (FRADS)

- SONET/SDH Add Drop Multiplexers

- SONET/SDH Terminal Multiplexers

- M23 Based M13 Multiplexer

- C-Bit Parity Based M13 Multiplexer

- Channelized and Unchannelized DS3 Frame Relay Interfaces

- Optical Access Equipment

- Digital Access Cross-Connect Systems

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## 3 **REFERENCES**

- American National Standard for Telecommunications - Digital Hierarchy - Synchronous DS3 Format Specifications, ANSI T1.103-1993

- American National Standard for Telecommunications – ANSI T1.105 – "Synchronous Optical Network (SONET) – Basic Description Including Multiplex Structure, Rates, and Formats," October 27, 1995.

- American National Standard for Telecommunications – ANSI T1.105.02 – "Synchronous Optical Network (SONET) – Payload Mappings," October 27, 1995.

- American National Standard for Telecommunications - Digital Hierarchy - Formats Specification, ANSI T1.107-1995

- American National Standard for Telecommunications - Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring, ANSI T1.231-1997

- American National Standard for Telecommunications - Carrier to Customer Installation - DS-1 Metallic Interface Specification, ANSI T1.403-1999

- American National Standard for Telecommunications - Customer Installation–to-Network - DS3 Metallic Interface Specification, ANSI T1.404-1994

- American National Standard for Telecommunications - Integrated Services Digital Network (ISDN) Primary Rate- Customer Installation Metallic Interfaces Layer 1 Specification, ANSI T1.408-1990

- Bell Communications Research, TR–TSY-000009 - Asynchronous Digital Multiplexes Requirements and Objectives, Issue 1, May 1986

- Bell Communications Research - DS-1 Rate Digital Service Monitoring Unit Functional Specification, TA-TSY-000147, Issue 1, October, 1987

- Bell Communications Research - Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986

- Bell Communications Research - Wideband and Broadband Digital Cross-Connect Systems Generic Criteria, TR-NWT-000233, Issue 3, November 1993

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- Bell Communications Research – Digital Interface Between The SLC®96 Digital Loop Carrier System And A Local Digital Switch, TR-TSY-000008, Issue 2, August 1987

- Bellcore GR-253-CORE – "SONET Transport Systems: Common Criteria," Issue 2, Revision 1, December 1997.

- Bell Communications Research - Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, TR-NWT-000303, Issue 2, December, 1992

- Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 5, December, 1993

- Bell Communications Research - OTGR: Network Maintenance Transport Surveillance - Generic Digital Transmission Surveillance, TR-TSY-000820, Section 5.1, Issue 1, June 1990

- AT&T - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, TR 54016, September, 1989.

- AT&T - Accunet T1.5 - Service Description and Interface Specification, TR 62411, December, 1990

- ITU Study Group XVIII – Report R 105, Geneva, 9-19 June 1992

- ETSI - ETS 300 011 - ISDN Primary Rate User-Network Interface Specification and Test Principles, 1992.

- ETSI - ETS 300 233 - Access Digital Section for ISDN Primary Rates, May 1994

- ETSI - ETS 300 324-1 - Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification, February, 1994.

- ETSI - ETS 300 347-1 - Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification, September 1994.

- ETSI ETS 300 417-1-1 – "Transmission and Multiplexing (TM); Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 1-1: Generic processes and performance," January, 1996.

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- ETSI, Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment, Jan 1996

- ITU-T - Recommendation G.704 - Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1995.

- ITU-T - Recommendation G.706 - Frame Alignment and CRC Procedures Relating to G.704 Frame Structures, 1991.

- ITU-T - Recommendation G.732 – Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s, 1993.

- ITU-T Recommendation G.707 – Network Node Interface for the Synchronous Digital Hierarchy, 1996

- ITU-T Recommendation G.747 – Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Multiplexing Three Tributaries at 2048 kbit/s, 1988

- ITU-T Recommendation G.775, - Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria, 11/94

- ITU-T Recommendation G.783 – Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, April, 1997.

- ITU-T Recommendation G.823, - The Control of Jitter and Wander within Digital Networks which are Based on  the  2048 kbit/s Hierarchy, 03/94

- ITU-T Recommendation G.964, - V-Interfaces at the Digital Local Ex–hange (LE) - V5.1 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), June 1994.

- ITU-T Recommendation G.965, - V-Interfaces at the Digital Local Ex–hange (LE) - V5.2 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), March 1995.

- ITU-T - Recommendation I.431 - Primary Rate User-Network Interface – Layer 1 Specification, 1993.

- ITU-T Recommendation O.151 – Error Performance Measuring Equipment Operating at the Primary Rate and Above, October 1992

- ITU-T Recommendation O.152 – Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and N x 64 kbit/s, October 1992

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- ITU-T Recommendation O.153 - Basic Parameters for the Measurement of Error Performance at Bit Rates below the Primary Rate, October 1992.

- ITU-T Recommendation Q.921 - ISDN User-Network Interface Data Link Layer Specification, March 1993

- International Organization for Standardization, ISO 3309:1984 - High-Level Data Link Control procedures - Frame Structure

- TTC Standard JT-G704 - Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.

- TTC Standard JT-G706 - Frame Synchronization and CRC Procedure

- TTC Standard JT-I431 - ISDN Primary Rate User-Network Interface Layer 1 - Specification, 1995.

- Nippon Telegraph and Telephone Corporation - Technical Reference for High-Speed Digital Leased Circuit Services, Third Edition, 1990.

- GO-MVIP, Multi-Vendor Integration Protocol, MVIP-90, Release 1.1, 1994

- GO-MVIP, H-MVIP Standard, Release1.1a, 1997

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## 4    APPLICATION EXAMPLES

### Figure 1        - Any-Service-Any-Port Application
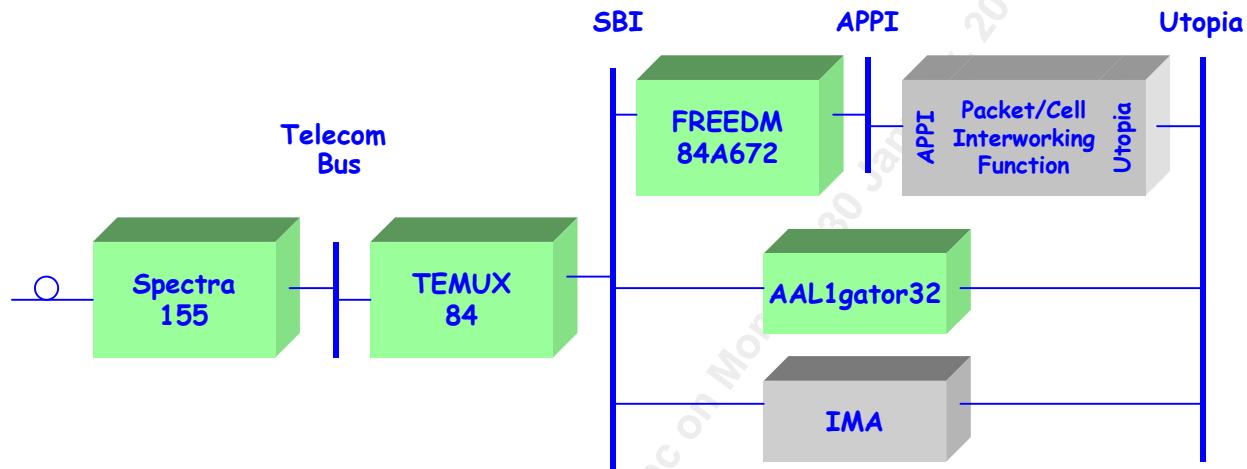


Figure 1 illustrates how frame relay (FREEDM84A672), circuit emulation (AAL1gator32) and ATM inverse multiplexing (IMA84) may all be supported on the same port with a common SBI bus as the enabling technology.

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## Figure 2        - High Density Frame Relay Application

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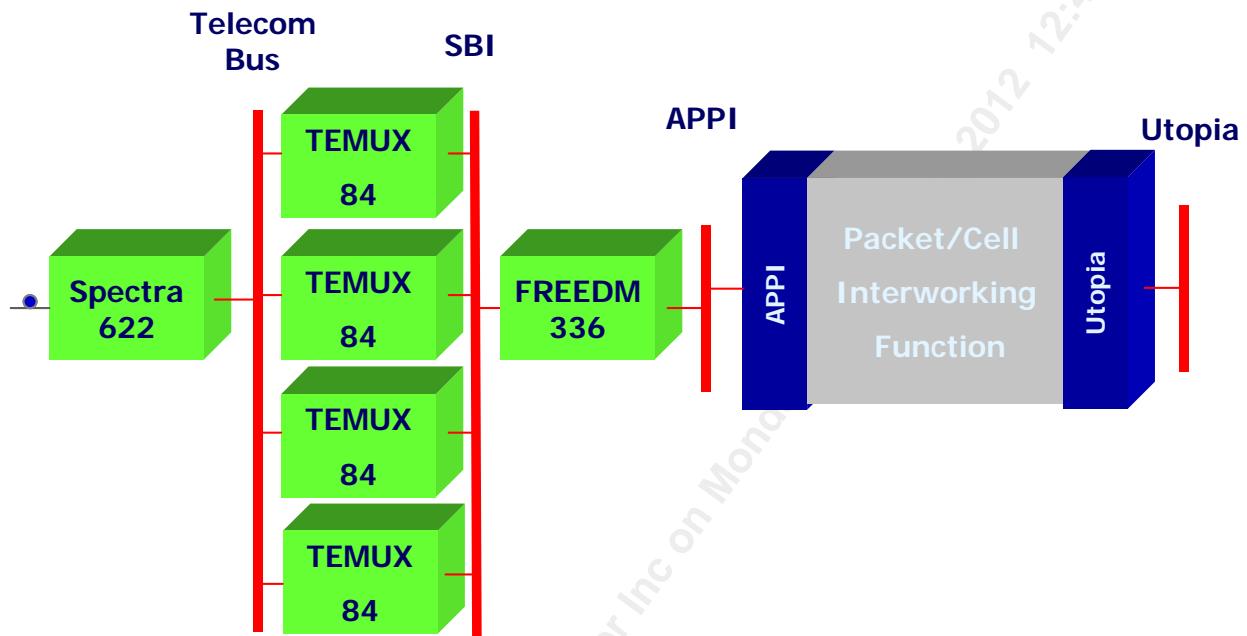
**Figure 3        - Fractional DS3 Application**
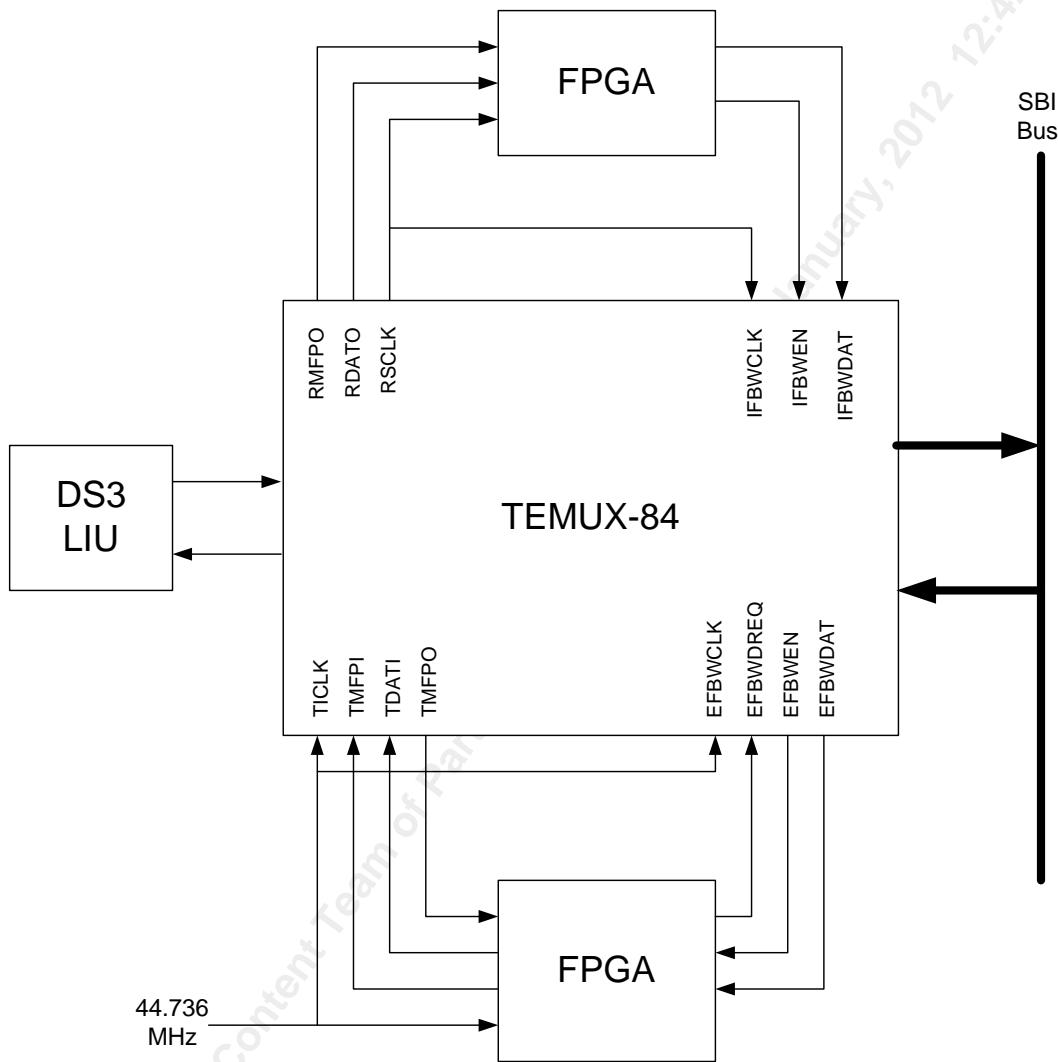


To support evolving fractional DS3 applications, flow-controlled ports provide access to SBI bus bandwidth.  Several non-standard schemes have been devised to use a portion of the DS3 payload.  Given that these protocols are subject to change, they are best supported by external programmable logic. Figure 3 illustrates one implementation.  Other implementations and applications are possible.

In the ingress direction, the framed DS3 is presented to an FPGA, whose responsibility it is to identify the utilitized bits of the payload.  Valid bits are indicated to the Ingress Flexible Bandwidth Port via an enable signal, IFBWEN.

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The bits are collected into bytes by the TEMUX 84 and inserted into the payload of the SBI Drop bus.

In the egress direction, an FPGA formats the payload of a DS3, while the TEMUX 84 inserts the DS3 frame overhead. The FPGA contains a data buffer. Based on the DS3 frame alignment dictated by the TMFPO signal, the FPGA inserts bits from the data buffer into the DS3 payload according to the protocol supported. To ensure the data buffer is replenished, the FPGA asserts the EFBWDREQ signal to initiate the transfer of a bit. The Egress Flexible Bandwidth Port responds by asserting EFWBEN coincident with EFWBDAT presenting valid data. The SBI Add bus participates by modulating its SAJUST_REQ output to match the SBI data rate to that required to keep internal FIFOs centered.

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## 5 BLOCK DIAGRAM

### 5.1 Top Level Block Diagram

Figure 4 shows the complete TEMUX 84. T1 links can be multiplexed into the DS3s or can be mapped into the telecom bus as SONET VT1.5 virtual tributaries or as SDH TU-11 or TU-12 tributary units. E1 links can be mapped into the telecom bus as SONET VT2 virtual tributaries or as SDH TU-12 tributary units. Line side interface can also be configured as SBI bus.

System side access to the T1s and E1s is available as Synchronous H-MVIP interfaces or the SBI bus. DS3 line side access is via the clock and data interface for line interface units (LIUs) or DS3 mapped into the SONET/SDH telecom bus. Unchannelized DS3 system side access is available through the SBI bus.

See Figure 10 for a block diagram of Transmux Mode.

## Figure 4 - TEMUX 84 Block Diagram
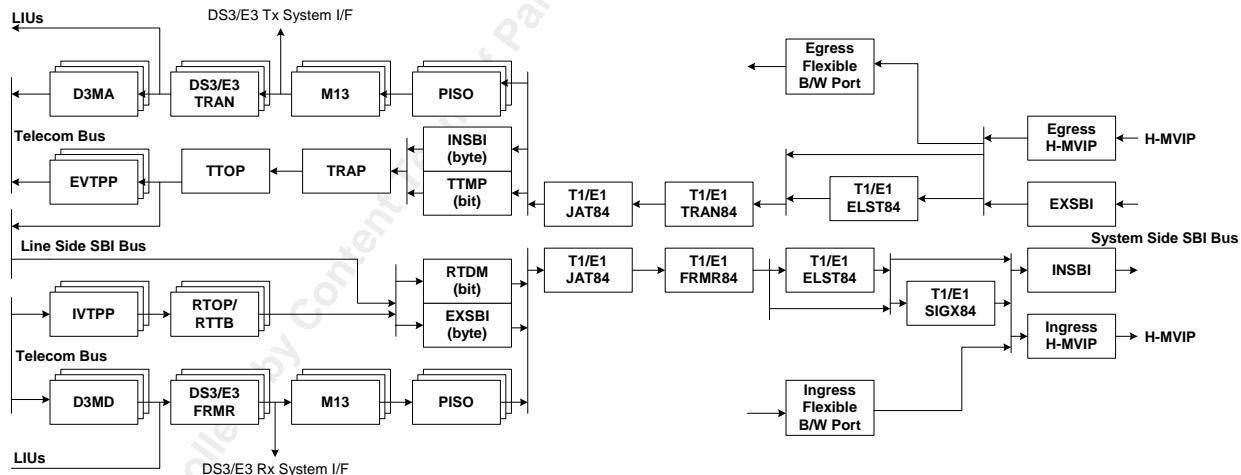
## 5.2   M13 Multiplexer Mode Block Diagram

Figure 5 shows the TEMUX 84, configured as a M13 multiplexer, connected to a synchronous H-MVIP system side bus.  In this example the TEMUX 84 provides synchronous access to the fully channelized T1s (access to all DS0s) multiplexed into the DS3.  There is also synchronous H-MVIP access to all channel associated signaling channels (CAS).  Additional H-MVIP interfaces can be used to provide synchronous access to the common channel signaling channels (CCS), although this same information is available within the data H-MVIP signals.

**Figure 5        - M13 Multiplexer Block Diagram**
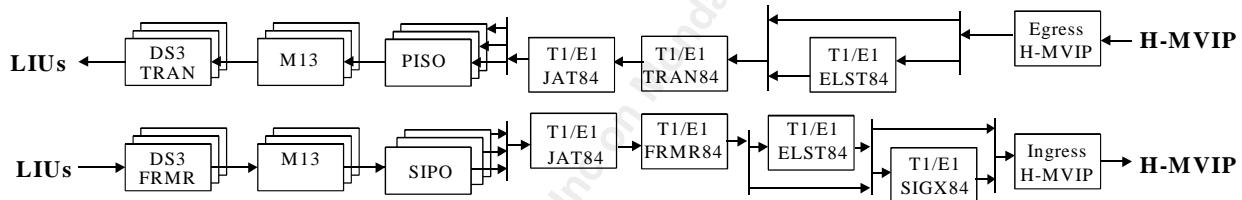
## 5.3    VT/TU Mapper Only Mode Block Diagram

Figure 6 shows the TEMUX 84 configured as a VT or TU mapper.  In this mode
the TEMUX 84 bypasses the T1 and E1 framers and provides access for up to 84
independent unframed 1.544 Mbit/s streams or 63 independent unframed
2.048 Mbit/s streams.  The 1.544 Mbit/s and 2.048 Mbit/s streams can be
accessed on the system side via the SBI bus.  The T1 or E1 framers can be used
to monitor the passing traffic in either the ingress or egress direction.  The M13
Multiplexer mode operates in much the same way as the VT and TU mapper
shown in Figure 6.

**Figure 6       - VT/TU Mapper Block Diagram**

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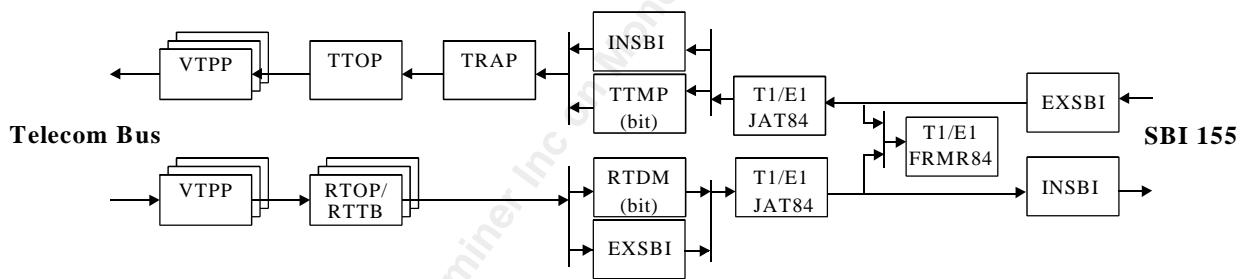
## 5.4   DS3/E3 Framer Only Block Diagram

Figure 7 shows the TEMUX 84 configured as a DS3 or E3 framer.  In this mode
the TEMUX 84 provides access up to three full DS3/E3 unchannelized payloads.
The payload access (right side of diagram) has two clock and data interfacing
modes, one utilizing a gapped clock to mask out the DS3/E3 overhead bits and
the second utilizing an ungapped clock with overhead indications on a separate
overhead signal.  The SBI bus can also be used to provide access to the
unchannelized DS3/E3.

Figure 7        - DS3/E3 Framer Only Mode Block Diagram
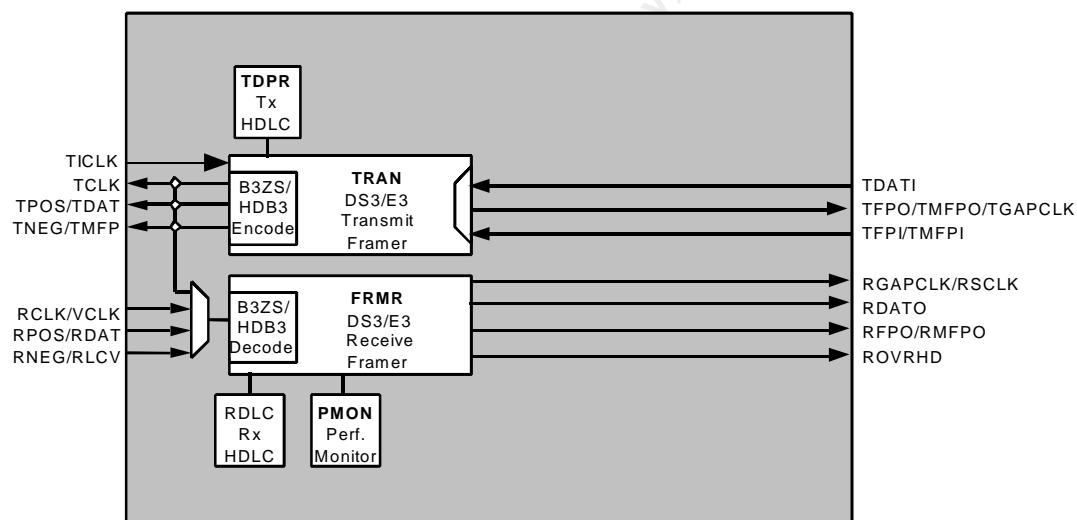


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## 5.5   T1/E1 FDL Extraction/Insertion and Alarm/Error Response

Figure 8 below shows the positioning and interaction of the TXFRMR and
RXFRMR when the TEMUX 84 is configured for High Density Framer mode. The
TXFRMR can insert HDLC PRM messages via software with the THDL. It can
also insert PRM messages automatically based upon the information gathered by
the RXFRMR. The RXFRMR collects the T1/E1 receieved PMON data and
optionally sends this information to the TXFRMR. The RXFRMR also sends the
received HDLC stream to the RDHL for PRM processing. Figure 8 also shows
the RXFRMR sending reponse indications to the TXFRMR informing it when to

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insert the T1 Yellow alarm, E1 FEBEs (E bits) and the E1 RAI Alarm (A bit)
towards the line side.

**Figure 8     - High Density Framer Mode T1/E1 Block Diagram**
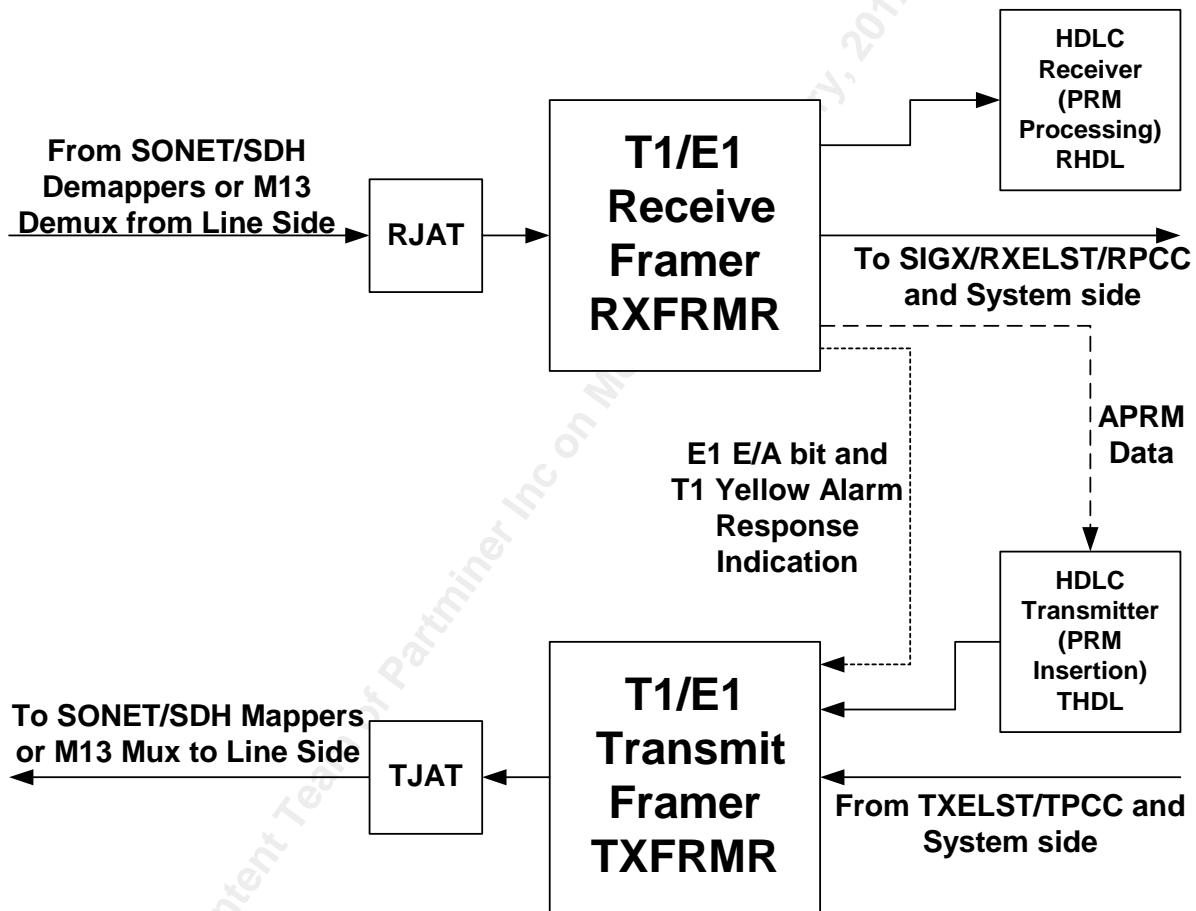


Figure 9 shows the T1/E1 PMON and FDL extraction block diagram when the
TEMUX 84 is configured for Mapper/Multiplexer mode. In this mode the T1/E1
data is carried clear channel bi-directionally between the line side and the system
side. There is the ability to collect T1/E1 PMON, via the RXFRMR and extract the
FDL, via the RHDL in either direction, but only one direction at a time. The
TXPMON bit of the RJAT Indirect Channel Data Register selects chooses the
direction of the PMON and FDL extraction.

The TXFRMR is not available in this mode, thus FDL HDLC insertion is not
possible, nor is the insertion of T1 Yellow, E1 FEBEs or E1 RAI.

**Figure 9     - Mapper/Multiplexer Mode T1/E1 Block Diagram**
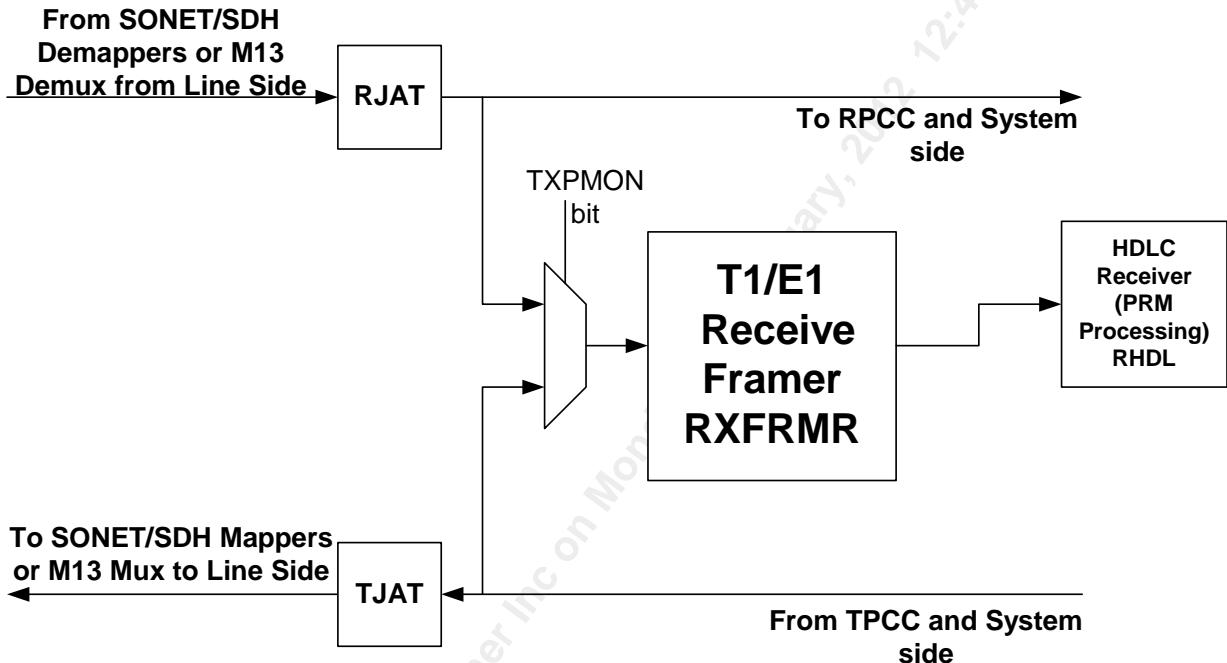


Figure 10 below shows the T1/E1 PMON and FDL extraction block diagram when the TEMUX 84 is configured for Transmux mode. In this mode the T1/E1 data is carried clear channel bi-directionally between the DS3 M13 Mulitplexers and the T1/E1 Mappers. There is the ability to collect T1/E1 PMON, via the RXFRMR and extract the FDL, via the RHDL in either direction, but only one direction at a time. The TXPMON bit of the RJAT Indirect Channel Data Register selects chooses the direction of the PMON and FDL extraction.

The TXFRMR is not available in this mode, thus FDL HDLC insertion is not possible, nor is the insertion of T1 Yellow, E1 FEBEs or E1 RAI.

For more information on Transmux, see section 9.2.

**Figure 10      - Transmux Mode T1/E1 Block Diagram**
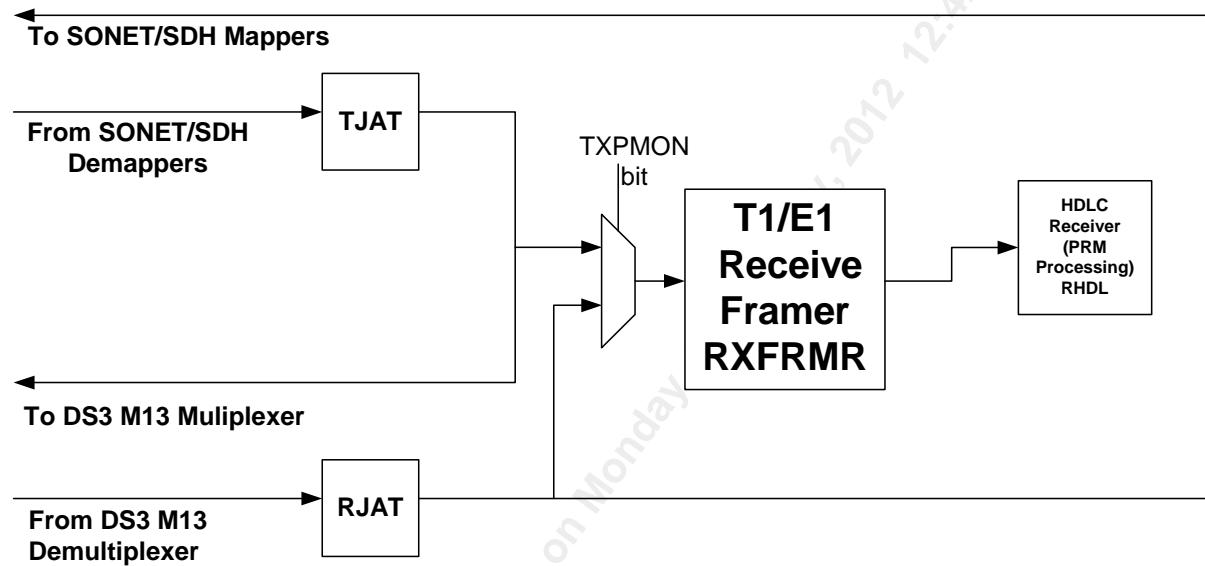
## 6      DESCRIPTION

The PM8316 High Density T1/E1 Framer with Integrated VT/TU Mappers and M13 Multiplexers (TEMUX 84) is a feature-rich device for use in any applications requiring high density link termination over T1 and E1 (G.747) channelized DS3 or T1 and E1 channelized SONET/SDH facilities.

The TEMUX 84 supports asynchronous multiplexing and demultiplexing of 84 DS1s or 63 E1s into three DS3 signals as specified by ANSI T1.107, Bell Communications Research TR-TSY-000009 and ITU-T Rec. G.747.  It supports bit asynchronous or byte synchronous mapping and demapping of 84 T1s or 63 E1s into SONET/SDH as specified by ANSI T1.105, Bell Communications Research GR-253-CORE and ITU-T Recommendation G.707.  The TEMUX 84 also supports mapping of 63 T1s into SDH via TU-12s.  Up to 84 Transparent VT1.5s and TU-11s or 63 Transparent VT2s and TU-12s can be transferred between the SONET/SDH interface and the SBI bus interface.

This device can also be configured as a DS3 or E3 framer, providing external access to the full DS3 or E3 payload, or a VT/TU mapper, providing access to unframed 1.544 Mbit/s and 2.048 Mbit/s links.

The TEMUX 84 can be used as a SONET/SDH VT/TU mapper or M13 multiplexer with performance monitoring in either the ingress or egress direction for up to 84 T1s or 63 E1s.  In this configuration the T1 and E1 transmit framers are disabled and either the ingress or egress T1 or E1 signals are routed to the T1 or E1 framers for performance monitoring purposes, which include error event accumulation, alarm monitoring and HDLC termination.

Each of the T1 and E1 framers and transmitters is independently software configurable, allowing timing master and feature selection without changes to external wiring.  T1 and E1 tributaries may be mixed at a VC-3/TUG-3/DS3 granularity.

In the ingress direction, each of the 84 T1 links is either demultiplexed from a channelized DS3 or extracted from SONET VT1.5, TU-11 or TU-12 mapped bus. Each T1 framer can be configured to frame to the common DS1 signal formats (SF, SLC®96, ESF and Japanese variants) or to be bypassed (unframed mode). Each T1 framer detects the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

T1 performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided.  The TEMUX

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84 also detects the presence of ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link.  The HDLC messages are terminated in a 127 byte FIFO.  An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TEMUX 84 also supports inband loopback code generation and detection, idle code substitution, digital milliwatt code insertion, data link extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation and detection on a per-DS0 basis.

In the egress direction, framing is generated for 84 T1s into either a DS3 multiplex or a SONET/SDH mapped add bus. Each T1 transmitter frames to SF or ESF DS1 formats, or framing can be optionally disabled.  The TEMUX 84 supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS0 basis.  PRBS generation and detection is supported on a framed and unframed T1 basis.

In the ingress direction, each of the 63 E1 links is either demultiplexed from a DS3 according to ITU-T Rec. G.747 or extracted from SONET/SDH VT2 or TU-12 mapped bus.  Each E1 framer detects and indicates the presence of remote alarm and AIS patterns and also integrates Red and AIS alarms.

The E1 framers support detection of various alarm conditions such as loss of frame, loss of signaling multiframe and loss of CRC multiframe.  The E1 framers also support reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal.

E1 performance monitoring with accumulation of CRC-4 errors, far end block errors and framing bit errors is provided.  The TEMUX 84 provides a receive HDLC controller for the detection and termination of messages on the national use bits.  Detection of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. V5.2 link ID signal detection is also supported.  An interrupt may be generated on any change of state of the Sa codewords. An elastic store for slip buffering and rate adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis.  Receive side data and signaling trunk conditioning is also provided.

In the egress direction, framing is generated for 63 E1s into either a DS3 multiplex according to ITU-T Rec. G.747 or a SONET/SDH mapped add bus. Each E1 transmitter generates framing for a basic G.704 E1 signal.  The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted.  Framing can be optionally disabled. Transmission of the

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4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported. PRBS generation or detection is supported on a framed and unframed E1 basis.

The TEMUX 84 can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path.  Three jitter attenuated recovered T1/E1 clocks can be routed outside the TEMUX 84 for network timing applications.

In synchronous backplane systems, 8 Mbit/s H-MVIP interfaces are provided for access to 2016 DS0 channels, channel associated signaling (CAS) for all 2016 DS0 channels and common channel signaling (CCS) for all 84 T1s or 63 E1s (or combination thereof).  The CCS signaling H-MVIP interface is independent of the DS0 channel and CAS H-MVIP access. The use of any of the H-MVIP interfaces requires that common clocks and frame pulse be used along with T1 slip buffers.

A Scaleable Bandwidth Interconnect (SBI) high density byte serial system interface provides higher levels of integration and dense interconnect.  The SBI bus interconnects up to 84 T1s or 63 E1 both synchronously or asynchronously. The SBI allows transmit timing to be mastered by either the TEMUX 84 or link layer device connected to the SBI bus.  In addition to framed T1s and E1s the TEMUX 84 can transport unframed T1 or E1 links and framed or unframed DS3 or E3 links over the SBI bus.

When configured as a DS3 multiplexer/demultiplexer or DS3 framer, the TEMUX 84 accepts and outputs either digital B3ZS-encoded bipolar or unipolar signals compatible with M23 and C-bit parity applications.

In the DS3 receive direction, the TEMUX 84 frames to DS3 signals with a maximum average reframe time of 1.5 ms in the presence of $10^{-3}$ bit error rate and detects line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, far end block errors, AIS, far end receive failure and idle code. The DS3 framer is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA) events.  The error events (C-BIT, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted.  HDLC receivers are provided for Path Maintenance Data Link support.  In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

Error event accumulation is also provided by the TEMUX 84.  Framing bit errors, line code violations, excessive zeros occurrences, parity errors, C-bit parity errors, and far end block errors are accumulated.  Error accumulation continues even while the off-line framers are indicating OOF.  The counters are intended to

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be polled once per second, and are sized so as not to saturate at a $10^{-3}$ bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

In the DS3 transmit direction, the TEMUX 84 inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals, Far End Receive Failure and idle signal can be inserted using either internal registers or can be configured for automatic insertion upon received errors. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at-1 C-bits for C-bit Parity application. Transmit timing is from an external reference or from the receive direction clock.

The TEMUX 84 also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms. A Pseudo Random Binary Sequence (PRBS) can be inserted into a DS3 payload and checked in the receive DS3 payload for bit errors. A fixed 100100… pattern is available for insertion directly into the B3ZS encoder for proper pulse mask shape verification.

The TEMUX 84 may be used as an E3 framer for the transport of framed but unchannelized E3 data streams complying to the ITU-T Recommendations G.751 or G.832. The line interface may be configured as either unipolar or HDB3-encoded.

When configured in DS3 multiplexer mode, seven 6312 kbit/s data streams are demultiplexed and multiplexed into and out of each DS3 signal. Bit stuffing and rate adaptation is performed. The C-bits are set appropriately, with the option of inserting DS2 loopback requests. Interrupts can be generated upon detection of loopback requests in the received DS3. AIS may be inserted in the any of the 6312 kbit/s tributaries in both the multiplex and demultiplex directions. C-bit parity is supported by sourcing a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%.

Framing to the demultiplexed 6312 kbit/s data streams supports DS2 (ANSI TI.107) frame formats. The maximum average reframe time is 7ms for DS2. Far end receive failure is detected and M-bit and F-bit errors are accumulated. The DS2 framer is an off-line framer, indicating both OOF and COFA events. Error

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events (FERF, MERR, FERR, PERR, RAI, framing word errors) are still indicated while the DS2 framer is indicating OOF, based on the previous alignment.

Each of the seven 6312 kbit/s multiplexers per DS3 may be independently configured to multiplex and demultiplex four 1544 kbit/s DS1s or three 2048 kbit/s according to ITU-T Rec. G.747 into and out of a DS2 formatted signal. Tributary frequency deviations are accommodated using internal FIFOs and bit stuffing. The C-bits are set appropriately, with the option of inserting DS1 loopback requests. Interrupts can be generated upon detection of loopback requests in the received DS2. AIS may be inserted in any of the low speed tributaries in both multiplex and demultiplex directions.

When configured as a DS3 or E3 framer the unchannelized payload of the DS3 and E3 links are available to an external device.

The SONET/SDH line side interface provides STS-1 SPE synchronous payload envelope processing and generation, TUG3 tributary unit group processing and generation within a VC4 virtual container and VC3 virtual container processing and generation. The payload processor aligns and monitors the performance of SONET virtual tributaries (VTs) or SDH tributary units (TUs). Maintenance functions per tributary include detection of loss of pointer, AIS alarm, tributary path signal label mismatch and tributary path signal label unstable alarms. Optionally interrupts can be generated due to the assertion and removal of any of the above alarms. Counts are accumulated for tributary path BIP-2 errors on a block or bit basis and for FEBE indications. The synchronous payload envelope generator generates all tributary pointers and calculates and inserts tributary path BIP-2. The generator also inserts FEBE, RDI and RFI in the V5 byte. Software can force AIS insertion on a per tributary basis.

A SONET/SDH mapper maps and demaps up to 84 T1s, 63 E1s or three DS3s into three STS-1 SPEs, TUG3s or VC3s through three elastic stores. The fixed stuff (R) bits are all set to zeros or ones under microprocessor control. The bit asynchronous demapper performs majority vote C-bit decoding to detect stuff requests for T1, E1 and DS3 asynchronous mappings. The VT1.5/VT2/TU-11/TU-12 mapper uses an elastic store and a jitter attenuator capability to minimize jitter introduced via bit stuffing.

The TEMUX 84 is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

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## 7    PIN DIAGRAM

The TEMUX 84 is packaged in a 324-pin PBGA package having a body size of
23mm by 23mm and a ball pitch of 1.0 mm. The center 36 balls are not used as
signal I/Os and are thermal balls.  Pin names and locations are defined in the Pin
Description Table in section 8.  Mechanical information for this package is in the
section 19.

**Figure 11    - Pin Diagram**
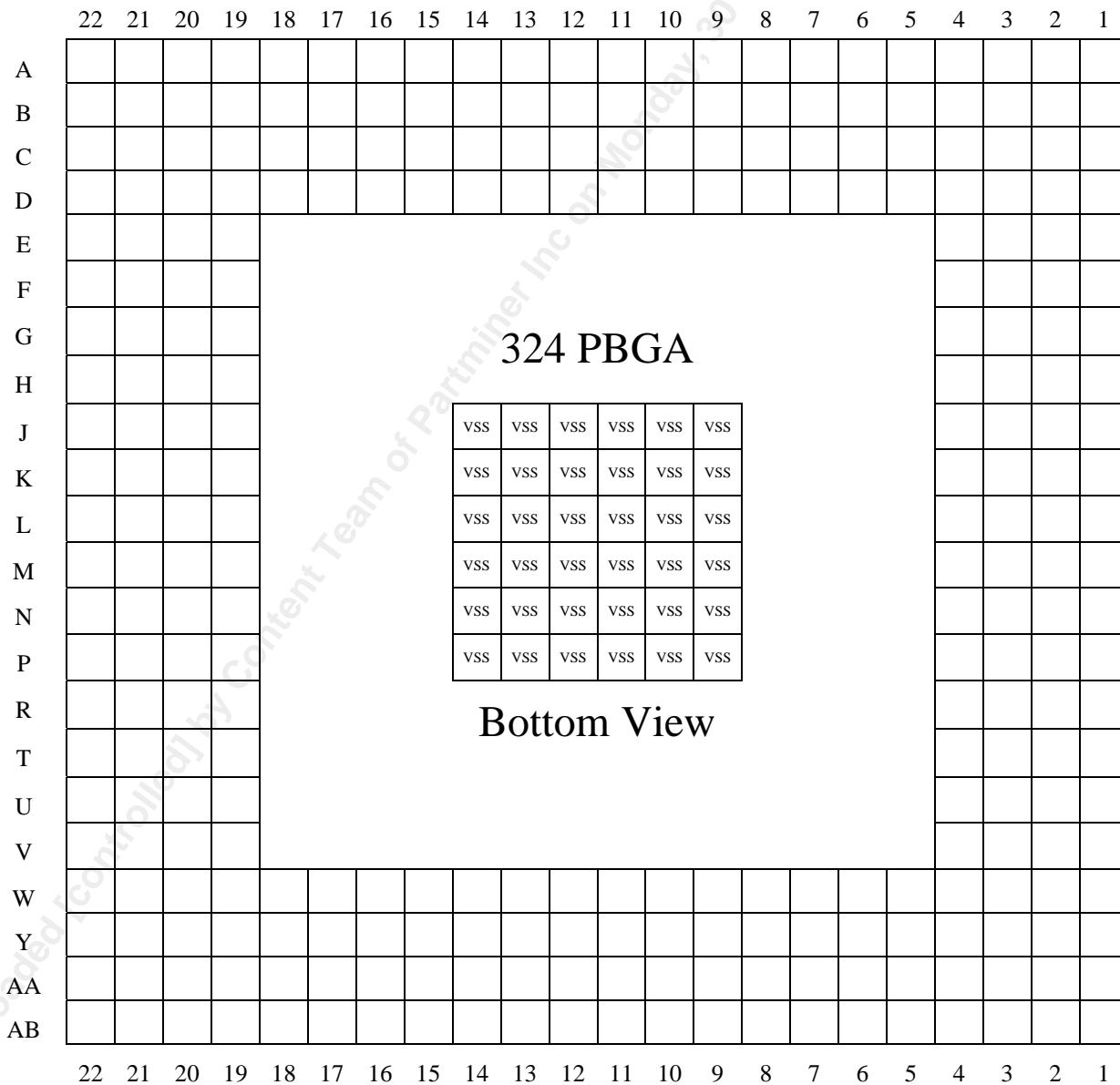
# 8    PIN DESCRIPTION

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| **DS3 and E3 Line Side Interface** | | | |
| RCLK[3]<br>RCLK[2]<br>RCLK[1] | Input | P1<br>T1<br>Y1 | **Receive Input Clocks (RCLK[3:1]).** RCLK[3:1] provide the receive direction timing for the three DS3s or E3s.  RCLK[3:1] are nominally 44.736 MHz or 34.368 MHz, 50% duty cycle clock inputs. The RCLK input frequency must always remain within +/-20 ppm such that the generated demultiplexed DS1 AIS frequency remains within +/- 32 ppm in channelized DS3 applications. |
| RPOS/RDAT[3]<br>RPOS/RDAT[2]<br>RPOS/RDAT[1] | Input | P2<br>U1<br>V3 | **Positive Input Pulse (RPOS[3:1]).**  RPOS[3:1] represent the positive pulses received on the B3ZS-encoded DS3s or HDB3-encoded E3s when dual rail input format is selected.<br><br>**Receive Data Input (RDAT[3:1]).**  RDAT[3:1] represent the NRZ (unipolar) DS3 or E3 input data streams when single rail input format is selected.<br><br>RPOS[3:1] and RDAT[3:1] are sampled on the rising edge of the associated RCLK by default and may be enabled to be sampled on the falling edge of the associated RCLK by setting the RFALL bit in the DS3/E3 Master Receive Line Options register. |
| RNEG/RLCV[3]<br>RNEG/RLCV[2]<br>RNEG/RLCV[1] | Input | P3<br>T3<br>W2 | **Negative Input Pulse (RNEG[3:1]).** RNEG[3:1] represent the negative pulses received on the B3ZS-encoded DS3s or HDB3-encoded E3s when dual rail input format is selected.<br><br>**Line code violation (RLCV[3:1]).** RLCV[3:1] represent receive line code violations when single rail input format is selected.<br><br>RNEG[3:1] and RLCV[3:1] are sampled on the rising edge of the associated RCLK by default and may be enabled to be sampled on the falling edge of RCLK by setting the RFALL bit in the DS3/E3 Master Receive Line Options register. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| TCLK[3]<br>TCLK[2]<br>TCLK[1] | Output | R3<br>V1<br>W3 | **Transmit Clock (TCLK[3:1]).**  TCLK[3:1] provide timing for circuitry downstream of the DS3 and E3 transmitters of the TEMUX 84.  TCLK[3:1] are nominally 44.736 MHz or 34.368 MHz, 50% duty cycle clocks. |
| TPOS/TDAT[3]<br>TPOS/TDAT[2]<br>TPOS/TDAT[1] | Output | R2<br>U2<br>AA1 | **Transmit Positive Pulse (TPOS[3:1]).**  TPOS[3:1] represent the positive pulses transmitted on the B3ZS-encoded DS3 or HDB3-encoded E3 lines when dual-rail output format is selected.<br><br>**Transmit Data Output (TDAT[3:1]).** TDAT[3:1] represent the NRZ (unipolar) DS3 output data streams when single rail output format is selected.<br><br>TPOS[3:1] and TDAT[3:1] are updated on the falling edge of  the associated TCLK by default but may be enabled to be updated on the rising edge of the associated TCLK by setting the TRISE bit in the DS3/E3 Master Transmit Line Options register. TPOS[3:1] and TDAT[3:1] are updated on TICLK[3:1] rather than TCLK[3:1] when the TICLK bit in the DS3/E3 Master Transmit Line Options register is set. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| TNEG/TMFP[3]<br>TNEG/TMFP[2]<br>TNEG/TMFP[1] | Output | U4<br>W1<br>AB1 | **Transmit Negative Pulse (TNEG[3:1]).** TNEG[3:1] represent the negative pulses transmitted on the B3ZS-encoded DS3 or HDB3-encoded E3 lines when dual-rail output format is selected.<br><br>**Transmit Multiframe Pulse (TMFP[3:1]).** These signals mark the transmit frame alignment when configured for single rail operation. TMFP[3:1] indicate the position of overhead bits in the transmit transmission system stream, TDAT[3:1]. TMFP[3:1] are high during the first bit (X1) of the multiframe or E3 frame.<br><br>TNEG[3:1] and TMFP[3:1] are updated on the falling edge of the associated TCLK by default but may be enabled to be updated on the rising edge of the associated TCLK by setting the TRISE bit in the DS3/E3 Master Transmit Line Options register. TNEG[3:1] and TMFP[3:1] are updated on TICLK[3:1] rather than TCLK[3:1] when the TICLK bit in the DS3/E3 Master Transmit Line Options register is set. |
| TICLK[3]<br>TICLK[2]<br>TICLK[1] | Input | T4<br>V4<br>Y2 | **Transmit input clock (TICLK[3:1]).** TICLK[3:1] provides the transmit direction timing for the three DS3s or E3s. TICLK[3:1] are nominally 44.736 MHz or 34.368 MHz, 50% duty cycle clocks. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| **DS3 and E3 System Side Interface** | | | |
| RGAPCLK/RSCLK [3]<br>RGAPCLK/RSCLK [2]<br>RGAPCLK/RSCLK [1] | Output | H4<br><br>L3<br><br>N3 | **Framer Recovered Gapped Clock (RGAPCLK[3:1]).** RGAPCLK[3:1] are valid when the TEMUX 84 is configured as DS3 or E3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers and the RXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register.<br><br>RGAPCLK[x] is the recovered clock and timing reference for RDATO[x].  RGAPCLK[3:1] are held either high or low during bit positions which correspond to overhead.<br><br>**Framer Recovered Clock (RSCLK[3:1]).**  RSCLK[3:1] are valid when the TEMUX 84 is configured as DS3 or E3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.  When a DS3 is demapped from SONET/SDH (i.e. LINEOPT_SPEx = 01), RSCLK is a gapped version of CLK52M.<br><br>The demapped DS3 RSCLK must be externally dejittered when connecting to the PM73122 AAL1gator32 device.<br><br>RSCLK[3:1] are the recovered clocks and timing references for RDATO[3:1], RFPO/RMFPO[3:1], and ROVRHD[3:1]. |
| RDATO[3]<br>RDATO[2]<br>RDATO[1] | Output | H2<br>K4<br>N2 | **Framer Receive Data (RDATO[3:1]).**  RDATO[3:1] are valid when the TEMUX 84 is configured as DS3 or E3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.  RDATO[3:1] are the received data aligned to RFPO/RMFPO[3:1] and ROVRHD[3:1].<br><br>RDATO[3:1] are updated on either the falling or rising edge of the associated RGAPCLK or RSCLK, depending on the value of the RSCLKR bit in the DS3 and E3 Master Unchannelized Interface Options register.  By default, RDATO[3:1] will be updated on the falling edge of the associated RGAPCLK[3:1] or RSCLK[3:1]. |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| RFPO/RMFPO[3]<br>RFPO/RMFPO[2]<br>RFPO/RMFPO[1] | Output | H1<br>K2<br>M2 | **Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO[3:1]).** RFPO/RMFPO[3:1] are valid when the TEMUX 84 is configured to be in framer only mode by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.<br><br>RFPO[3:1] are aligned to RDATO[3:1] and indicate the position of the first bit in each DS3 M-subframe and the first bit in each G.751 E3 or G.832 E3 frame.<br><br>RMFPO[3:1] are aligned to RDATO[3:1] and indicate the position of the first bit in each DS3 M-frame and the first bit in each G.751 or G.832 E3 frame. This is selected by setting the RXMFPO bit in the DS3 and E3 Master Unchannelized Interface Options Registers.<br><br>RFPO/RMFPO[3:1] are updated on either the falling or rising edge of the associated RSCLK depending on the setting of the RSCLKR bit in the DS3 and E3 Master Unchannelized Interface Options register. |
| ROVRHD[3]<br>ROVRHD[2]<br>ROVRHD[1] | Output | H3<br>K1<br>N1 | **Framer Receive Overhead (ROVRHD[3:1]).** ROVRHD[3:1] are valid when the TEMUX 84 is configured as DS3 or E3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.<br><br>ROVRHD[3:1] will be high whenever the data on RDATO[3:1] corresponds to an overhead bit position. ROVRHD[3:1] is updated on the either the falling or rising edge of the associated RSCLK depending on the setting of the RSCLKR bit in the DS3 and E3 Master Unchannelized Interface Options register. |

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HIGH DENSITY T1/E1 FRAMER  WITH
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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| TFPO/TMFPO/ TGAPCLK[3] TFPO/TMFPO/ TGAPCLK[2] TFPO/TMFPO/ TGAPCLK[1] | Output | F4 J4 M3 | **Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO[3:1]).**  TFPO/TMFPO[3:1] are valid when the TEMUX 84 is configured as DS3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers and setting the TXGAPEN bit to 0 in the DS3 and E3 Master Unchannelized Interface Options register. <br><br> In DS3 mode, TFPO[3:1] pulse high for 1 out of every 85 clock cycles, giving a reference M-subframe indication. In E3 mode, TFPO[3:1] pulse high to mark the first bit of the frame. <br><br> In DS3 mode, TMFPO[3:1] pulse high for 1 out of every 4760 clock cycles, giving a reference M-frame indication.  TMFPO[3:1] behaves the same as TFPO[3:1] for E3 applications.  This is selected by setting the TXMFPO bit in the DS3 and E3 Master Unchannelized Interface Options Registers. <br><br> TFPO/TMFPO[3:1] will be updated on the falling edge of TICLK when the associated TDATIFALL register bit is a logic 0 and on the rising edge when TDATIFALL is a logic 1. <br><br> **Framer Gapped Transmit Clock (TGAPCLK[3:1]).** TGAPCLK[3:1] are valid when the TEMUX 84 is configured as DS3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers and setting the TXGAPEN bit to 1 in the DS3 and E3 Master Unchannelized Interface Options register. <br><br> TGAPCLK[3:1] are derived from the transmit reference clocks TICLK[3:1] or from the receive clock if loop-timed.  The overhead bit (gapped) positions are generated internal to the device.  TGAPCLK[3:1] are held high during the overhead bit positions.  This clock is useful for interfacing to devices which source payload data only. |

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HIGH DENSITY T1/E1 FRAMER WITH
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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| | | | In DS3 mode, TGAPCLK is gapped for one bit every 85 TICLK cycles.  In E3 G.832 mode, TGAPCLK is gapped for the first two bytes of the frame.  In E3 G.751 mode, TGAPCLK is gapped during the frame alignment signal, remote alarm indication bit, the national use bit, the justification service bits (bits 1 to 4 of Sets II, III and IV), and optionally during the bits available for justification (bits 5 to 8 of Set IV) as determined by the PYLD&JUST bit of the E3 Data Link Control register.<br><br>TGAPCLK[3:1] are used to sample the associated TDATI[3:1] inputs. |
| TDATI[3]<br>TDATI[2]<br>TDATI[1] | Input | G2<br>J3<br>L2 | **Framer Transmit Data (TDATI[3:1]).**  TDATI[3:1] contain the serial data to be transmitted when the TEMUX 84 is configured as DS3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.   TDATI[3:1] are sampled on the rising edge of the associated TICLK if the TXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register is logic 0.  If TXGAPEN is logic 1, then TDATI[3:1] are sampled on the rising edge of TGAPCLK. TDATI[3:1] can be configured to be sampled on the falling edge of the associated TICLK or TGAPCLK by setting the TDATIFALL bit in the DS3 and E3 Master Unchannelized Interface Options register. |

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HIGH DENSITY T1/E1 FRAMER  WITH
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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| TFPI/TMFPI[3]<br>TFPI/TMFPI[2]<br>TFPI/TMFPI[1] | Input | G1<br>J1<br>M1 | **Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI[3:1]).** TFPI/TMFPI[3:1] are valid when the TEMUX 84 is configured as DS3 or E3 framers by setting the OPMODE_SPEx[2:0] bits in the SPE Configuration registers.<br><br>TFPI[3:1] indicate the position of all overhead bits in each DS3 M-subframe or the first bit in each G.751 E3 or G.832 E3 frame.  TFPI[3:1] are not required to pulse at every overhead bit.<br><br>TMFPI[3:1] indicate the position of the first bit in each 4760-bit DS3 M-frame or the first bit in each E3 frame.  TMFPI[3:1] are not required to pulse at every multiframe boundary.  This is selected by setting the TXMFPI bit in the DS3 and E3 Master Unchannelized Interface Options Registers.<br><br>TFPI/TMFPI[3:1] are sampled on the rising edge of the associated TICLK.  TFPI/TMFPI[3:1]  can be configured to be sampled on the falling edge of the associated TICLK by setting the TDATIFALL bit to 1 in the Register 0x0202 + 0x100*N: DS3 and E3 Master Unchannelized Interface Options. |
| **H-MVIP System Side Interfaces** | | | |
| CMV8MCLK | Input | T22 | **Common 8M H-MVIP Clock (CMV8MCLK).** The common 8.192 Mbit/s H-MVIP data provides the data clock for receive and transmit links configured for operation in 8.192 Mbit/s H-MVIP mode.<br><br>CMV8MCLK is used to sample data on MVID[1:21], MVED[1:21], CASID[1:21], CASED[1:21], CCSID[1:3], CCSED[1:3] and TS0ID.  CMV8MCLK is nominally a 50% duty cycle clock with a frequency of 16.384 MHz.<br><br>The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration register. If the TEMUX 84 is not configured for H-MVIP operation, this clock may be tied high or low. |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| CMVFPC | Input | R20 | **Common H-MVIP Frame Pulse Clock (CMVFPC).** The common 8.192 Mbit/s H-MVIP frame pulse clock provides the frame pulse clock for receive and transmit links configured for operation in 8.192 Mbit/s H-MVIP mode.<br><br>CMVFPC is used to sample CMVFPB. CMVFPC is nominally a 50% duty cycle clock with a frequency of 4.096 MHz. The falling edge of CMVFPC must be aligned with the falling edge of CMV8MCLK with no more than $\pm$10ns skew.<br><br>The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration registers. If the TEMUX 84 is not configured for H-MVIP operation, this clock may be tied high or low. |
| CMVFPB | Input | R22 | **Common H-MVIP Frame Pulse (CMVFPB).** The active low common frame pulse for 8.192 Mbit/s H-MVIP signals references the beginning of each frame for links operating in 8.192 Mbit/s H-MVIP mode.<br><br>If the CMMFP bit of the Master H-MVIP Interface Configuration register is a logic 1, the CMVFPB is becomes a multiframe pulse. Mulitframe alignment is only relevant when the T1 F-bit or the E1 TS0 is being carried transparently in the egress direction and alignment to CAS signaling is required. To support any combination of SF, SLC®96, ESF and E1, the CMVFPB must pulse low at a multiple of 48 frames at the beginning of the frame.<br><br>The H-MVIP interfaces are enabled via the SYSOPT[1:0] bits in the Global Configuration register. If the TEMUX 84 is not configured for H-MVIP operation, this frame pulse may be tied high or low.<br><br>The CMVFPB frame pulse occurs at multiples of 125us and is sampled on the falling edge of CMVFPC. |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| MVID[1]<br>MVID[2]<br>MVID[3]<br>MVID[4]<br>MVID[5]<br>MVID[6]<br>MVID[7]<br>MVID[8]<br>MVID[9]<br>MVID[10]<br>MVID[11]<br>MVID[12]<br>MVID[13]<br>MVID[14]<br>MVID[15]<br>MVID[16]<br>MVID[17]<br>MVID[18]<br>MVID[19]<br>MVID[20]<br>MVID[21] | Output | B3<br>A3<br>A2<br>C5<br>A4<br>B5<br>C6<br>A5<br>B6<br>C7<br>D6<br>A6<br>A7<br>C8<br>B8<br>A8<br>D7<br>C9<br>B9<br>A9<br>D9 | **H-MVIP Ingress Data (MVID[1:21]).** MVID[x] carries the recovered T1 or E1 channels which have passed through the elastic store.  Each MVID[x] signal carries the channels of four complete T1s or E1s.<br><br>MVID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVID[x] is updated on every second rising or falling edge of the common H-MVIP 16.384Mb /s clock, CMV8MCLK, as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master and H-MVIP Interface Configuration register.<br><br>T1 and E1 links may be mixed on a TUG-3/DS3 granularity.  Each of MVID[1:7], MVID[8:14] and MVID[15:21] carries 28 T1s or 21 E1s independent of the other two groups of seven.  For E1 mode, MVID[7], MVID[14] and MVID[21] are unused. |

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**PM8316 TEMUX 84**

*HIGH DENSITY T1/E1 FRAMER WITH*
*INTEGRATED VT/TU MAPPER AND M13 MUX*

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| CASID[1]<br>CASID[2]<br>CASID[3]<br>CASID[4]<br>CASID[5]<br>CASID[6]<br>CASID[7]<br>CASID[8]<br>CASID[9]<br>CASID[10]<br>CASID[11]<br>CASID[12]<br>CASID[13]<br>CASID[14]<br>CASID[15]<br>CASID[16]<br>CASID[17]<br>CASID[18]<br>CASID[19]<br>CASID[20]<br>CASID[21] | Output | B18<br>A19<br>A20<br>B19<br>B20<br>A21<br>B21<br>D20<br>B22<br>C21<br>D21<br>E20<br>E21<br>C20<br>E22<br>F21<br>E19<br>G20<br>F22<br>G21<br>G22 | **Channel Associated Signaling Ingress Data (CASID[1:21]).** Each CASID[x] signal carries CAS for four complete T1s or E1s. CASID[x] carries the corresponding CAS values of the channel carried in MVID[x]. It also carries the framer and alarm statuses.<br><br>CASID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASID[x] is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register.<br><br>T1 and E1 links may be mixed on a TUG-3/DS3 granularity. Each of CASID[1:7], CASID[8:14] and CASID[15:21] carries 28 T1s or 21 E1s independent of the other two groups of seven. For E1 mode, CASID[7], CASID[14] and CASID[21] are unused. |
| CCSID[1]<br>CCSID[2]<br>CCSID[3] | Output | C16<br>D18<br>B17 | **Common Channel Signaling Ingress Data (CCSID[1:3]).** In T1 mode, CCSID[1] carries the 84 common channel signaling channels extracted from each of the 84 T1s. In E1 mode, CCSID[1:3] carries up to 3 timeslots (15,16, 31) from each of the 63 E1s. CCSID is formatted according to the H-MVIP standard.<br><br>CCSID[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSID is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register. |

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**PM8316 TEMUX 84**

*HIGH DENSITY T1/E1 FRAMER  WITH*
*INTEGRATED VT/TU MAPPER AND M13 MUX*

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| TS0ID | Output | D17 | **E1 Timeslot 0 Ingress Data (TS0ID)**.  In E1 mode, TS0ID carries the first timeslot of each frame.<br><br>TS0ID is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB.  TS0ID is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master H-MVIP Interface Configuration register. |
| MVED[1]<br>MVED[2]<br>MVED[3]<br>MVED[4]<br>MVED[5]<br>MVED[6]<br>MVED[7]<br>MVED[8]<br>MVED[9]<br>MVED[10]<br>MVED[11]<br>MVED[12]<br>MVED[13]<br>MVED[14]<br>MVED[15]<br>MVED[16]<br>MVED[17]<br>MVED[18]<br>MVED[19]<br>MVED[20]<br>MVED[21] | Input | B10<br>A10<br>D10<br>B11<br>A11<br>D12<br>B12<br>C12<br>D13<br>B13<br>C13<br>D14<br>A14<br>B14<br>C14<br>A15<br>B15<br>A16<br>C15<br>B16<br>A17 | **H-MVIP Egress Data (MVED[1:21]).** The egress data streams to be transmitted are input on these pins. Each MVED[x] signal carries the channels of four complete T1s or E1s formatted according to the H-MVIP standard.<br><br>MVED[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVID[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register.<br><br>MVED[3] is a Schmitt triggered input.<br><br>T1 and E1 links may be mixed on a TUG-3/DS3 granularity.  Each of MVED[1:7], MVED[8:14] and MVED[15:21] carries 28 T1s or 21 E1s independent of the other two groups of seven.  For E1 mode, MVED[7], MVED[14] and MVED[21] are unused. |

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*HIGH DENSITY T1/E1 FRAMER WITH*
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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| CASED[1]<br>CASED[2]<br>CASED[3]<br>CASED[4]<br>CASED[5]<br>CASED[6]<br>CASED[7]<br>CASED[8]<br>CASED[9]<br>CASED[10]<br>CASED[11]<br>CASED[12]<br>CASED[13]<br>CASED[14]<br>CASED[15]<br>CASED[16]<br>CASED[17]<br>CASED[18]<br>CASED[19]<br>CASED[20]<br>CASED[21] | Input | H19<br>J20<br>J21<br>J22<br>J19<br>K20<br>K22<br>K19<br>L20<br>L22<br>M22<br>M21<br>M20<br>N19<br>N22<br>N20<br>P19<br>P22<br>P21<br>P20<br>R19 | **Channel Associated Signaling Egress Data (CASED[1:21]).** Each CASED[x] signal carries CAS for four complete T1s or E1s formatted according to the H-MVIP standard. CASED[x] carries the corresponding CAS values of the channel data carried in MVED[x]. CASED[x] may also present inband information for the control of signaling insertion.<br><br>CASED[x] is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASED[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master H-MVIP Interface Configuration register.<br><br>T1 and E1 links may be mixed on a TUG-3/DS3 granularity. Each of CASED[1:7], MVED[8:14] and CASED[15:21] carries 28 T1s or 21 E1s independent of the other two groups of seven. For E1 mode, CASED[7], CASED[14] and CASED[21] are unused. |
| CCSED[1],<br>CCSED[2],<br>CCSED[3] | Input | H20<br>H21<br>H22 | **Common Channel Signaling Egress Data (CCSED[1:3]).** In T1 mode CCSED[1] carries the common channel signaling channels to be transmitted in each of the T1s. In E1 mode CCSED carries up to 3 timeslots (15,16, 31) to be transmitted in each of the E1s. CCSED is formatted according to the H-MVIP standard.<br><br>CCSED is aligned to the common H-MVIP 16.384 Mbit/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSED is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master H-MVIP Interface Configuration register. |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| **Flexible Bandwidth Ports** | | | |
| **Port #1 is associated with SBI SPE #1.  Port #2 is associated with SBI SPE #2.  Port #3 is associated with SBI SPE #3.** | | | |
| IFBWCLK[3] IFBWCLK[2] IFBWCLK[1] | Input | N22 K19 H19 | **The Ingress Flexible Bandwidth Clocks (IFBWCLK[3:1]).**  The IFBWCLK[3:1] clocks provide the timing for an arbitrary bandwidth payload to be inserted into the System Drop Bus (SDDATA[7:0]). Each clock is associated with one SPE and is only used when the associated SPE is configured to carry a fractional payload by the OPMODE_SPEx[2:0] bits of the SPE Configuration registers.<br><br>IFBWCLK[3:1] may have a maximum frequency of 51.84 MHz and may be gapped if required.<br><br>Each IFBWCLK samples the associated IFBWDAT[3:1] and IFBWEN[3:1] inputs on the rising edge. |
| IFBWDAT[3] IFBWDAT[2] IFBWDAT[1] | Input | N20 L20 J20 | **The Ingress Flexible Bandwidth Data (IFBWDAT[3:1]).**  These inputs present bit serial data for insertion into the System Drop Bus (SDDATA[7:0]). Only bits for which the associated IFBWEN input is sampled high are accepted.  Each data input is associated with one SPE and is only used when the associated SPE is configured to carry a fractional payload by the OPMODE_SPEx[2:0] bits of the SPE Configuration registers.  The bit ordering is big-endian, i.e. data presented on SDDATA[7] is received earlier in time than data presented in the same byte on SDDATA[0].<br><br>IFBWDAT[3:1] are sampled on the rising edge of the associated IFBWCLK input. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| IFBWEN[3]<br>IFBWEN[2]<br>IFBWEN[1] | Input | P19<br>L22<br>J21 | **The Ingress Flexible Bandwidth Enables (IFBWEN[3:1]).** A logic high on any of these inputs indicates a valid bit on the associated IFBWDAT input. The IFBWEN[3:1] inputs are constrained such that the maximum data rate of each of IFBWDAT[3:1] is less than 48.96 Mbit/s.<br><br>IFBWEN[3:1] are sampled on the rising edge of the associated IFBWCLK input. |
| EFBWCLK[3]<br>EFBWCLK[2]<br>EFBWCLK[1] | Input | P22<br>M22<br>J22 | **The Egress Flexible Bandwidth Clocks (EFBWCLK[3:1]).** The EFBWCLK[3:1] clocks provide the timing for an arbitrary bandwidth payload extracted from the System Add Bus (SADATA[7:0]). Each clock is associated with one SPE and is only used when the associated SPE is configured to carry a fractional payload by the OPMODE_SPEx[2:0] bits of the SPE Configuration registers.<br><br>EFBWCLK[3:1] may have a maximum frequency of 51.84 MHz and may be gapped if required.<br><br>Each EFBWCLK samples the associated EBWDREQ on the rising edge and updates the associated EFBWDAT] and EFBWEN on the falling edge. |
| EFBWDREQ[3]<br>EFBWDREQ[2]<br>EFBWDREQ[1] | Input | P21<br>M21<br>J19 | **The Egress Flexible Bandwidth Data Requests (EFBWREQ[3:1]).** The data request input must be asserted high for a EFBWCLK cycle for each bit of data required. In response to sampling EFWBDREQ[3:1] high, the associated EFBWDAT output will either present an available bit a cycle later with an accompanying assertion of the associated EFBWEN or ignore the request if no data is ready. In many applications (eg. frame relay and ATM), every request will be acknowledged with data. In applications where the source data is fixed, it is permissible to hold EFBWDREQ[3:1] high, in which case EFBWEN identifies valid bytes.<br><br>EFBWDREQ[3:1] are sampled on the rising edge of the associated EFBWCLK input. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| EFBWDAT[3]<br>EFBWDAT[2]<br>EFBWDAT[1] | Output | F21<br>B22<br>A19 | **The Egress Flexible Bandwidth Data (EFBWDAT[3:1]).**  These outputs present bit serial data extracted from the System Add Bus (SADATA[7:0]).  Only bits for which the associated EFBWEN output is simultaneously high are valid.  Each data input is associated with one SPE and is only used when the associated SPE is configured to carry a fractional payload by the OPMODE_SPEx[2:0] bits of the SPE Configuration registers.  The bit ordering is big-endian, i.e. data received on SADATA[7] is transmitted earlier in time than data received in the same byte on SADATA[0].<br><br>EFBWDAT[3:1] are updated on the falling edge of the associated EFBWCLK input. |
| EFBWEN[3]<br>EFBWEN[2]<br>EFBWEN[1] | Output | E22<br>D20<br>B18 | **The Egress Flexible Bandwidth Enables (EFBWEN[3:1]).**  A logic high on any of  these outputs indicates a valid bit on the associated EFBWDAT output.  The EFBWEN[3:1] will only be asserted, with a one cycle latency, in response to a sampled logic high on the associated EFBWDREQ, and then only if data is available for presenting on the associated EFBWDAT.<br><br>EFBWEN[3:1] are updated on the falling edge of the associated EFBWCLK input. |
| **Recovered T1 and E1 Clocks** | | | |
| RECVCLK1 | Output | F2 | **Recovered Clock 1 (RECVCLK1).** This clock output is a recovered and de-jittered clock from any one of the 84 T1 framers or 63 E1 framers. |
| RECVCLK2 | Output | E4 | **Recovered Clock 2 (RECVCLK2).** This clock output is a recovered and de-jittered clock from any one of the 84 T1 framers or 63 E1 framers. |
| RECVCLK3 | Output | G3 | **Recovered Clock 3 (RECVCLK3).** This clock output is a recovered and de-jittered clock from any one of the 84 T1 framers or 63 E1 framers. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| XCLK_T1 | Input | E2 | **T1 Crystal Clock Input (XCLK_T1).**  This input clocks the digital phase locked loop that performs jitter attenuation on the T1 recovered clocks which drive the RECVCLK1/2/3 outputs.  XCLK_T1 is nominally a 37.056 MHz ± 32ppm, 50% duty cycle clock.<br><br>This input may be tied to ground in applications that do not use the RECVCLK1/2/3 outputs as s1.544 MHz clocks. |
| XCLK_E1 | Input | F3 | **E1 Crystal Clock Input (XCLK_E1).**  This input clocks the digital phase locked loop that performs jitter attenuation on the E1 recovered clocks which drive the RECVCLK1/2/3 outputs.  XCLK_E1 is nominally a 49.152 MHz ± 32ppm, 50% duty cycle clock when configured for E1 modes.<br><br>This input may be tied to ground in applications that do not use the RECVCLK1/2/3 outputs as 2.048 MHz clocks. |
| **Telecom Line Side Interface** | | | |
| LREFCLK | Input | Y4 | **Line Reference Clock (LREFCLK).** This signal provides reference timing for the SONET telecom bus interface. On the incoming byte interface of the telecom bus, LDC1J1V1, LDDATA[7:0], LDDP, LDPL, LDTPL, LDV5, LDAIS and LAC1 are sampled on the rising edge or LREFCLK. In the outgoing byte interface, LADATA[7:0], LADP, LAPL, LAC1J1V1 and LAOE/LATPL are updated on the rising edge of LREFCLK.<br><br>This clock may be held low if the Telecom Bus interface is unused.<br><br>This clock is nominally a 19.44 MHz +/-20ppm or 77.76 MHz +/-20ppm clock with a 50% duty cycle. This clock must be phase locked to SREFCLK and can be external connected to SREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| L77 | Input | AA4 | The Line 77.76 MHz select input determines the expected frequency of LREFCLK.  If L77 is low, LREFCLK is expected to be 19.44 MHz.  If L77 is high, LREFCLK is expected to be 77.76 MHz and data is driven and sampled every fourth cycle. L77 is a Schmitt triggered input.<br><br>L77 is expected to be held static. |
| LAC1 | Input | W10 | **Line Add C1 Frame Pulse (LAC1).** The Add bus timing signal identifies the frame and multiframe boundaries on the Add Data bus LADATA[7:0].<br><br>LAC1 is set high to mark the first C1 byte of the first transport envelope frame of the 4 frame multiframe on the LADATA[7:0] bus. LAC1 need not be presented on every occurrence of the multiframe.<br><br>LAC1 is sampled on the rising edge of LREFCLK. |

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| LAC1J1V1 | Output | AA11 | **Line Add Bus Composite Timing Signal (LAC1J1V1).** The Add bus composite timing signal identifies the frame, payload and tributary multiframe boundaries on the Line Add Data bus LADATA[7:0]. LAC1J1V1 pulses high with the Line Add Payload Active signal LAPL set low to mark the first STS-1 (STM-0/AU3) identification byte or equivalently the STM identification byte C1. Optionally the LAC1J1V1 signal pulses high with LAPL set high to mark the path trace byte J1. Optionally the LAC1J1V1 signal pulses high on the V1 byte to indicate tributary multiframe boundaries.<br><br>In a system with multiple TEMUX 84s sharing the same Line Add bus only one device should have LAC1J1V1 connected. All devices must be configured via the TXPTR[9:0] bits in the SONET/SDH Transmit Pointer Configuration and TTMP Telecom Interface Configuration registers for the same J1 location.<br><br>When L77 high, LAC1J1V1 is only valid (i.e. identifies the first C1, J1 and V1 of the concatenated STM-4 data stream) if the LSTM[1:0] bits in the Master Bus Configuration register (0x0006) are set to "00".<br><br>LAC1J1V1 is updated on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| LAOE/LATPL | Tristate Output | AB11 | The LATPLSEL bit of the SONET/SDH Master Egress VTPP Configuration register determines the function of this tristate output.  When LATPLSEL is logic 1, the signal is LATPL.  When LATPLSEL is logic 0, the signal is LAOE. |
| | | | **Line Add Bus Output Enable (LAOE).** The Add Bus output enable signal is asserted high whenever the Line Add Bus is being driven which is co-coincident with the Line Add bus outputs coming out of tri-state. |
| | | | This pin is intended to control an external multiplexer when multiple TEMUX 84s are driving the Telecom Add bus during their individual tributaries. This same function is accomplished with the Add bus tristate drivers but increased tolerance to tributary configuration problems is possible with an external mux.  This output is controlled via the LAOE bit in the TTMP Tributary Control registers when the egress VTPP is bypassed.  When the egress VTPP is not bypassed or a TU-3 is being mapped, LAOE is high. |
| | | | **Line Add Bus Tributary Payload Active (LATPL).** The tributary payload active signal marks the bytes carrying the tributary payload.  LATPL is high during each tributary payload byte on the LADATA[7:0] bus. LATPL will be low during transport overhead, path overhead, V1 bytes and V2 bytes.  To indicate pointer adjustments, LATPL will be asserted appropriately during the V3 byte and following byte for the tributary. |
| | | | By default, LATPL is only asserted during the SONET/SDH tributaries assigned to this device as determined by the LAOE bit in the TTMP Tributary Control registers and during the J1 and V1 byte positions.  As options, LATPL can be driven during transport overhead, for all bytes of an STM-1 when configured for 77.76MHz operation or all the time. |
| | | | LAOE/LATPL is updated on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| LADATA[0]<br>LADATA[1]<br>LADATA[2]<br>LADATA[3]<br>LADATA[4]<br>LADATA[5]<br>LADATA[6]<br>LADATA[7] | Output<br>Tristate | W14<br>Y13<br>AA13<br>AB13<br>W13<br>AA12<br>W12<br>W11 | **Line Add Bus Data (LADATA[7:0]).** The add bus data contains the SONET transmit payload data in byte serial format. All transport overhead bytes are set to 00h. The phase relation of the SPE (VC) to the transport frame is determined by the Add Bus composite timing signal LAC1J1V1 and is software programmable to any valid pointer offset. LADATA[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit to be transmitted).<br><br>By default, LADATA[7:0] is only asserted during the SONET/SDH tributaries assigned to this device as determined by the LAOE bit in the TTMP Tributary Control registers and during the J1 (when LAJ1EN bit is logic 1) and V1 (when LAJ1EN bit is logic 1) byte positions; otherwise, it is high impedance.  As options, LADATA[7:0] can be driven during transport overhead, for all bytes of an STM-1 when configured for 77.76MHz operation or all the time.<br><br>LADATA[7:0] is updated on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| LADP | Output Tristate | AB14 | **Line Add Bus Data Parity (LADP).** The Add Bus data parity signal carries the parity of the outgoing signals. The parity calculation encompasses the LADATA[7:0] bus and optionally the LAC1J1V1 and LAPL signals. LAC1J1V1 and LAPL can be included in the parity calculation by setting the INCLAC1J1V1 and INCLAPL register bits in the SONET/SDH Master Egress Configuration register high, respectively. Odd parity is selected by setting the LAOP register bit in the same register high and even parity is selected by setting the LAOP bit low.<br><br>By default, LADP is only asserted during the SONET/SDH tributaries assigned to this device as determined by the LAOE bit in the TTMP Tributary Control registers and during the J1 (when LAJ1EN bit is logic 1) and V1 (when LAJ1EN bit is logic 1) byte positions; otherwise, it is high impedance.  As options, LADP can be driven during transport overhead, for all bytes of an STM-1 when configured for 77.76MHz operation or all the time.<br><br>LADP is updated on the rising edge of LREFCLK. |
| LAPL | Output Tristate | AA14 | **Line Add Bus Payload Active (LAPL).** The Add Bus payload active signal identifies the payload bytes on LADATA[7:0]. LAPL is set high during path overhead and payload bytes and low during transport overhead bytes.<br><br>By default, LAPL is only asserted during the SONET/SDH tributaries assigned to this device as determined by the LAOE bit in the TTMP Tributary Control registers and during the J1 (when LAJ1EN bit is logic 1) and V1 (when LAJ1EN bit is logic 1) byte positions; otherwise, it is high impedance.  As options, LAPL can be driven during transport overhead, for all bytes of an STM-1 when configured for 77.76MHz operation or all the time.<br><br>LAPL is updated on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| LAV5 | Output Tristate | W15 | **Line Add Bus V5 Byte (LAV5).**  The outgoing tributary V5 byte signal marks the various tributary V5 bytes. LAV5 marks each tributary V5 byte on the LADATA[7:0] bus when high.<br><br>By default, LAV5 is only asserted during the SONET/SDH tributaries assigned to this device as determined by the LAOE bit in the TTMP Tributary Control registers and during the J1 (when LAJ1EN bit is logic 1) and V1 (when LAJ1EN bit is logic 1) byte positions; otherwise, it is high impedance.  As options, LAV5 can be driven during transport overhead, for all bytes of an STM-1 when configured for 77.76MHz operation or all the time.<br><br>LAV5 is updated on the rising edge of LREFCLK. |
| LDDATA[0]<br>LDDATA[1]<br>LDDATA[2]<br>LDDATA[3]<br>LDDATA[4]<br>LDDATA[5]<br>LDDATA[6]<br>LDDATA[7] | Input | W5<br>AA6<br>AB5<br>Y3<br>Y6<br>AA5<br>AB4<br>AB3 | **Line Drop Bus Data (LDDATA[7:0]).** The drop bus data contains the SONET/SDH receive payload data in byte serial format. LDDATA[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first.<br><br>LDDATA[7:0] is sampled on the rising edge of LREFCLK. |
| LDDP | Input | Y7 | **Line Drop Bus Data Parity (LDDP).** The incoming data parity signal carries the parity of the incoming signals. The parity calculation encompasses the LDDATA[7:0] bus and optionally the LDC1J1V1 and LDPL signals.  LDC1J1V1 and LDPL can be included in the parity calculation by setting the INCLDC1J1V1 and INCLDPL bits in the SONET/SDH Master Ingress Configuration register high, respectively. Odd parity is selected by setting the LDOP bit in the Master SONET/SDH Ingress Configuration register high and even parity is selected by setting the LDOP bit low.<br><br>LDDP is sampled on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| LDC1J1V1 | Input | AB6 | **Line Drop C1/J1 Frame Pulse (LDC1J1V1).** The input C1/J1 frame pulse identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming SONET stream. <br><br> LDC1J1V1 is set high while LDPL is low to mark the first C1 byte of the transport envelope frame on the LDDATA[7:0] bus. LDC1J1V1 is set high while LDPL is high to mark each J1 byte of the synchronous payload envelope(s) on the LDDATA[7:0] bus. LDC1J1V1 must be present at every occurrence of the first C1 and all J1 bytes. <br><br> Optionally LDC1J1V1 indicates multiframe alignment when high during the first V1 bytes of each envelope. <br><br> LDC1J1V1 is sampled on the rising edge of LREFCLK. |
| LDPL | Input | AB7 | **Line Drop Bus Payload Active (LDPL).** The payload active signal identifies the bytes on LDDATA[7:0] that carry payload bytes. <br><br> LDPL is set high during path overhead and payload bytes and low during transport overhead bytes. LDPL is set high during the H3 byte to indicate a negative pointer justification and low during the byte following H3 to indicate a positive pointer justification event. <br><br> LDPL is sampled on the rising edge of LREFCLK. |
| LDV5 | Input | W6 | **Line Drop Bus V5 Byte (LDV5).** The incoming tributary V5 byte signal marks the various tributary V5 bytes. LDV5 marks each tributary V5 byte on the LDDATA[7:0] bus when high.  The LDV5 input is only used if the Ingress VTPP is bypassed (i.e. the IVTPPBYP bit of the SONET/SDH Master Ingress Configuration register is logic 1.) <br><br> LDV5 is sampled on the rising edge of LREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| LDTPL | Input | Y8 | **Line Drop Bus Tributary Payload Active (LDTPL).** The tributary payload active signal marks the bytes carrying the tributary payload which have been identified by an external payload processor. When this signal is available, the internal pointer processor can be bypassed.  LDTPL is only respected for asynchronously mapped tributaries.<br><br>LDTPL is high during each tributary payload byte on the LDDATA[7:0] bus.  In floating mode, LDTPL contains valid data only for bytes in the VC3 or VC4 virtual containers, or the STS-1 SPE.  It should be ignored for bytes in the transport overhead.  In locked mode, LDTPL is low for transport overhead.<br><br>LDTPL is sampled on the rising edge of LREFCLK. |
| LDAIS | Input | AA8 | **Line Drop Bus Tributary Path Alarm Indication Signal (LDAIS).** The active high tributary path alarm indication signal identifies tributaries on the incoming data stream LDDATA[7:0] that are in AIS state. When this signal is available, the internal pointer processor can be bypassed. LDAIS is invalid when LDTPL is low. LDAIS is only respected for asynchronously mapped tributaries.<br><br>LDAIS is sampled on the rising edge of LREFCLK. |
| RADEASTCK | Input | W7 | **Remote Alarm Port East Clock (RADEASTCK).** The remote serial alarm port east clock provides timing for the east remote serial alarm port.  It is nominally a 9.72 MHz clock, but can range from 1.344 MHz to 10 MHz.<br><br>Inputs RADEASTFP and RADEAST are sampled on the rising edge of RADEASTCK. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| RADEASTFP | Input | Y9 | **Remote Alarm Port East Frame Pulse (RADEASTFP).** The remote serial alarm port east frame pulse is used to locate the alarm bits of the individual tributaries in the east remote serial alarm port.  RADEASTFP is set high to mark the first BIP-2 error bit of tributary TU #1 in TUG2 #1 of TUG3 #1 carried in RADEAST.  RADEASTFP must be set high to mark every occurrence of this bit.  TEMUX 84 will not flywheel on RADEASTFP in order to accommodate a variety of RADEASTCK frequencies.<br><br>RADEASTFP is sampled on the rising edge of RADEASTCK. |
| RADEAST | Input | AA9 | **Remote Alarm Port Data East (RADEAST).** The remote serial alarm port east carries the tributary path BIP-2 error count, RDI status, and RFI status in the east remote serial alarm port.  The first BIP-2 error bit of tributary TU #1 in TUG2 #1 of TUG3 #1 on RADEAST is marked by a high level on RADEASTFP.  The status carried on RADEAST is software selectable to be reported by the RDI, RFI and REI alarms and is selectable to be associated with any tributary on the outgoing data stream LADATA[7:0].<br><br>RADEAST is sampled on the rising edge of RADEASTCK. |
| RADWESTCK | Input | W9 | **Remote Alarm Port West Clock (RADWESTCK).** The remote serial alarm port west clock provides timing for the west remote serial alarm port.  It is nominally a 9.72 MHz clock, but can range from 1.344 MHz to 10 MHz.<br><br>Inputs RADWESTFP and RADWEST are sampled on the rising edge of RADWESTCK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| RADWESTFP | Input | Y10 | **Remote Alarm Port West Frame Pulse (RADWESTFP).** The remote serial alarm port west frame pulse is used to locate the alarm bits of the individual tributaries in the west remote serial alarm port.  RADWESTFP is set high to mark the first BIP-2 error bit of tributary TU #1 in TUG2 #1 of TUG3 #1 carried in RADWEST.  RADWESTFP must be set high to mark every occurrence of this bit.  TEMUX 84 will not flywheel on RADWESTFP in order to accommodate a variety of RADWESTCK frequencies.  RADWESTFP is sampled on the rising edge of RADWESTCK. |
| RADWEST | Input | AA10 | **Remote Alarm Port Data West (RADWEST).** The remote serial alarm port west carries the tributary path BIP-2 error count, RDI status, and RFI status in the west remote serial alarm port.  The first BIP-2 error bit of tributary TU #1 in TUG2 #1 of TUG3 #1 on RADWEST is marked by a high level on RADWESTFP.  The status carried on RADWEST is software selectable to be reported by the RDI, RFI and REI alarms and is selectable to be associated with any tributary on the outgoing data stream LADATA[7:0].  RADWESTFP is sampled on the rising edge of RADWESTCK. |
| CLK52M | Input | AB10 | **52 MHz Clock Reference (CLK52M).** This clock reference is used to generate a gapped DS3 clock when demapping a DS3 from the SONET stream and also to generate a gapped DS3/E3 clock when receiving a DS3/E3 from the SBI bus interface. This clock has two nominal values.  The first is a nominal 51.84 MHz 50% duty cycle clock that must be used when an E3 is received on the SBI Add bus interface. The second is a nominal 44.928 MHz 50% duty cycle clock that must be used when demapping a DS3 from SONET.  The expected frequency is determined by the FASTCLKFREQ bit of the SONET/SDH Master DS3 Clock Generation Control register. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| **Scaleable Bandwidth Interconnect Interface** | | | |
| CTCLK | Input | F19 | **Common Transmit Clock (CTCLK).** This input signal is used as a reference transmit tributary clock which can be used in egress Clock Master modes. CTCLK must be multiple of 8 kHz. The transmit clock is derived by the jitter attenuator PLL using CTCLK as a reference. <br><br> The TEMUX may be configured to ignore the CTCLK input and lock to the data or one of the recovered Ingress clocks instead, RECVCLK1, RECVCLK2 and RECVCLK3. The receive tributary clock is automatically substituted for CTCLK if line loopback or looptiming is enabled. |
| SREFCLK | Input | C10 | **System Reference Clock (SREFCLK).** This system reference clock is a nominal 19.44 MHz +/-20ppm or 77.76 MHz +/-20ppm 50% duty cycle clock. This clock is common to both the add and drop sides of the SBI bus. <br><br> SREFCLK must be active for all applications, except DS3/E3 framer only mode when the system interface is serial clock and data. When the SYSOPT register bits are binary 01 (H-MVIP interface), SREFCLK is required to be 19.44 MHz. <br><br> This clock must be phase locked to LREFCLK and can be external connected to LREFCLK. When passing transparent virtual tributaries between the telecom bus and the SBI bus, SREFCLK must be the same frequency as LREFCLK (i.e. S77 = L77). <br><br> When operating in serial DS3 mode, the SREFCLK can be +/- 50 ppm. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| S77 | Input | D10 | The SBI 77.76 MHz select input determines the expected frequency of SREFCLK.  If S77 is low, SREFCLK is expected to be 19.44 MHz.  If S77 is high, SREFCLK is expected to be 77.76 MHz and data is driven and sampled every fourth cycle. S77 is a Schmitt triggered input. |
| | | | This signal is a don't care when the SYSOPT register bits are binary 01 (H-MVIP interface).  In this mode, SREFCLK is required to be 19.44 MHz. |
| | | | S77 is expected to be held static. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| SDC1FP | I/O | B3 | **SBI Drop C1 Frame Pulse (SDC1FP).** The SDC1FP C1 frame pulse synchronizes devices interfacing to the Insert SBI bus. The frame pulse indicates SBI bus multiframe alignment which occurs every 500 $\mu$S, therefore this signal is pulsed every 9720 SREFCLK cycles (38880 cycles if S77 is high). This signal does not need to occur every SBI multiframe and is also used to indicate T1 and E1 multiframe alignment in synchronous SBI mode by pulsing at multiples of every 12 SBI multiframes (48 T1/E1 frames). In synchronous locked mode, as selected by the SYNCSBI context bit programmed through the RX-SBI-ELST Indirect Channel Data register, SDC1FP pulses every 116640 SREFCLK cycles (466560 cycles if S77 is high). If the SYNCSBI bit is logic 1 for at least one tributary, SDC1FP must indicate T1 and E1 multiframe alignment.<br><br>The TEMUX 84 can be configured to generate this frame pulse. Only one device on the SBI bus should generate this signal. By default this signal is not enabled to generate the frame pulse.<br><br>If a SDC1FP pulse is received at an unexpected cycle, the Drop bus with become high-impedance until two consecutive valid SDC1FP pulses occur.<br><br>The system frame pulse is a single SREFCLK cycle long and is updated on the rising edge of SREFCLK.<br><br>This signal must be held low if the SBI and H-MVIP buses are both not being used. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| SAC1FP | Input | B11 | **SBI Add C1 Frame Pulse (SAC1FP).** The Extract C1 frame pulse synchronizes devices interfacing to the Extract SBI bus. The frame pulse indicates SBI bus multiframe alignment which occurs every 500 $\mu$S, therefore this signal is pulsed every 9720 SREFCLK cycles (38880 cycles if S77 is high).  This signal does not need to occur every SBI multiframe.  SAC1FP is sampled on the rising edge of SREFCLK.<br><br>This signal must be held low if the SBI bus is not being used. |
| SADATA[0]<br>SADATA[1]<br>SADATA[2]<br>SADATA[3]<br>SADATA[4]<br>SADATA[5]<br>SADATA[6]<br>SADATA[7] | Input | A11<br>D12<br>B12<br>C12<br>D13<br>B13<br>C13<br>D14 | **System Add Bus Data (SADATA[7:0]).** The System add data bus is a time division multiplexed bus which carries the E1, T1 and DS3 tributary data is byte serial format over the SBI bus structure.  This device only monitors the add data bus during the timeslots assigned to this device.<br><br>SADATA[7:0] is sampled on the rising edge of SREFCLK. |
| SADP | Input | A14 | **System Add Bus Data Parity (SADP).** The system add bus signal carries the even or odd parity for the add bus signals SADATA[7:0], SAPL and SAV5.  The TEMUX 84 monitors the add bus parity during all cycles when S77 is low and during the entire selected STM-1 when S77 is high.<br><br>SADP is sampled on the rising edge of SREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|----------|------|---------|----------|
| SAPL | Input | B14 | **System Add Bus Payload Active (SAPL).** The add bus payload active signal indicates valid data within the SBI bus structure. This signal must be high during all octets making up a tributary. This signal goes high during the V3 or H3 octet of a tributary to indicate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet of a tributary to indicate positive timing adjustments between the tributary rate and the fixed SBI bus structure. <br><br>In the flexible bandwidth configuration, SAPL may only be asserted in response to a logic high on the SAJUST_REQ.  SAPL shall be high an equal or less number of cycles than SAJUST_REQ.  (Some applications require an exact one-to-one correspondence.) <br><br>The TEMUX 84 only monitors the add bus payload active signal during the tributary timeslots assigned to this device. <br><br>SAPL is sampled on the rising edge of SREFCLK. |
| SAV5 | Input | C14 | **System Add Bus Payload Indicator (SAV5).** The add bus payload indicator locates the position of the floating payloads for each tributary within the SBI bus structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure. <br><br>All timing adjustments indicated by this signal must be accompanied by appropriate adjustments in the SAPL signal. <br><br>The TEMUX 84 only monitors the add bus payload indicator signal during the tributary timeslots assigned to this device. <br><br>SAV5 is sampled on the rising edge of SREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| SAJUST_REQ | Output Tristate | A2 | **System Add Bus Justification Request (SAJUST_REQ).** The justification request signals the Link Layer device to speed up, slow down or maintain the rate which it is sending data to the TEMUX 84. This is only used when the TEMUX 84 is the timing master for the tributary transmit direction.<br><br>This active high signal indicates negative timing adjustments when asserted high during the V3 or H3 octet of the tributary. In response to this the Link Layer device sends an extra byte in the V3 or H3 octet of the next SBI bus multi-frame.<br><br>Positive timing adjustments are requested by asserting justification request high during the octet following the V3 or H3 octet. The Link Layer device responds to this request by not sending an octet during the V3 or H3 octet of the next multi-frame.<br><br>SAJUST_REQ has a different significance in the flexible bandwidth mode. In this mode, SAJUST_REQ is high for one SREFCLK cycle for each byte that can be accepted. A valid byte on SADATA[7:0] with an accompanying SAPL assertion is expected in response.<br><br>The TEMUX 84 only drives the justification request signal during the tributary timeslots assigned to this device. When operating in 19.44 MHz mode (i.e. S77 low), SAJUST_REQ is aligned by the SAC1FP input. When operating in 77.76 MHz mode (i.e. S77 high), SAJUST_REQ's alignment is relative to the SDC1FP signal.<br><br>SAJUST_REQ is updated on the rising edge of SREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| SDDATA[0]<br>SDDATA[1]<br>SDDATA[2]<br>SDDATA[3]<br>SDDATA[4]<br>SDDATA[5]<br>SDDATA[6]<br>SDDATA[7] | Output<br>Tristate | C5<br>A4<br>B5<br>C6<br>A5<br>B6<br>C7<br>D6 | **System Drop Bus Data (SDDATA[7:0]).** The System drop data bus is a time division multiplexed bus which carries the E1, T1 and DS3 tributary data is byte serial format over the SBI bus structure. This device only drives the data bus during the timeslots assigned to this device.<br><br>SDDATA[7:0] is updated on the rising edge of SREFCLK. |
| SDDP | Output<br>Tristate | A6 | **System Drop Bus Data Parity (SDDP).** The system drop bus signal carries the even or odd parity for the drop bus signals SDDATA[7:0], SDPL and SDV5. Whenever the TEMUX 84 drives the data bus, the parity is valid.<br><br>SDDP is updated on the rising edge of SREFCLK. |
| SDPL | Output<br>Tristate | A7 | **System Drop Bus Payload Active (SDPL).** The payload active signal indicates valid data within the SBI bus structure. This signal is asserted during all octets making up a tributary. This signal goes high during the V3 or H3 octet of a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet of a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure.<br><br>In the flexible bandwidth configuration, SDPL is asserted for each byte as it becomes available. Therefore, SDPL may be high or low arbitrarily during any SREFCLK cycle.<br><br>The TEMUX 84 only drives the payload active signal during the tributary timeslots assigned to this device.<br><br>SDPL is updated on the rising edge of SREFCLK. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| SDV5 | Output Tristate | C8 | **System Drop Bus Payload Indicator (SDV5).** The payload indicator locates the position of the floating payloads for each tributary within the SBI bus structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure.<br><br>All timing adjustments indicated by this signal are accompanied by appropriate adjustments in the SDPL signal.<br><br>The TEMUX 84 only drives the payload Indicator signal during the tributary timeslots assigned to this device.<br><br>SDV5 is updated on the rising edge of SREFCLK. |
| SBIACT | Output | A3 | **SBI Output Active (SBIACT).** The SBI Output Active indicator is high whenever the TEMUX 84 is driving the SBI drop bus signals. This signal is used by other TEMUX 84s or other SBI devices to detect SBI configuration problems by detecting other devices driving the SBI bus during the same tributary as the device listening to this signal.<br><br>This output is updated on the rising edge or SREFCLK. |
| SBIDET[0] SBIDET[1] | Input | A15 B15 | **SBI Bus Activity Detection (SBIDET[1:0]).** The SBI bus activity detect input detects tributary collisions between devices sharing the same SBI bus. Each SBI device driving the bus also drives an SBI active signal (SBIACT). This pair of activity detection inputs monitors the active signals from two other SBI devices. When unused this signal should be connected to ground.<br><br>These inputs only have effect when the SBI bus is configured for 19.44MHz (i.e. S77 is low).<br><br>A collision is detected when either of SBIDET[1:0] signals are active concurrently with this device driving SBIACT. When collisions occur the SBI drivers are disabled and an interrupt is generated to signal the collision. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| **Microprocessor Interface** | | | |
| INTB | Output OD | T21 | **Active low Open-Drain Interrupt (INTB).**  This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources.  Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source. |
| CSB | Input | AA15 | **Active Low Chip Select (CSB).** This signal is low during TEMUX 84 register accesses. The CSB input has an integral pull up resistor. |
| RDB | Input | W17 | **Active Low Read Enable (RDB).** This signal is low during TEMUX 84 register read accesses.  The TEMUX 84 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. |
| WRB | Input | AB16 | **Active Low Write Strobe (WRB).** This signal is low during a TEMUX 84 register write access.  The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. |
| D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] | I/O | U22 T20 V19 U21 U20 W22 Y22 Y21 | **Bidirectional Data Bus (D[7:0]).** This bus provides TEMUX 84 register read and write accesses. |

| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| A[0]<br>A[1]<br>A[2]<br>A[3]<br>A[4]<br>A[5]<br>A[6]<br>A[7]<br>A[8]<br>A[9]<br>A[10]<br>A[11]<br>A[12] | Input | AB22<br>AA21<br>Y19<br>AA20<br>AA19<br>AB20<br>AA18<br>W19<br>AB18<br>AA17<br>W18<br>Y16<br>AA16 | **Address Bus (A[12:0]).** This bus selects specific registers during TEMUX 84 register accesses.<br><br>Signal A[12] selects between normal mode and test mode register access. A[12] has an integral pull down resistor. Tie A[12] directly to ground unless access to bit HIZIO in test register 0x1000 is required. |
| RSTB | Input | W20 | **Active Low Reset (RSTB).** This signal provides an asynchronous TEMUX 84 reset. RSTB is a Schmitt triggered input with an integral pull up resistor. |
| ALE | Input | AA22 | **Address Latch Enable (ALE).** This signal is active high and latches the address bus A[12:0] when low. When ALE is high, the internal address latches are transparent. It allows the TEMUX 84 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor. |
| **JTAG Interface** | | | |
| TCK | Input | B1 | **Test Clock (TCK).** This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. |
| TMS | Input | D2 | **Test Mode Select (TMS).** This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor. |
| TDI | Input | E3 | **Test Data Input (TDI).** This signal carries test data into the TEMUX 84 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| TDO | Output | D1 | **Test Data Output (TDO).** This signal carries test data out of the TEMUX 84 via the IEEE P1149.1 test access port.  TDO is updated on the falling edge of TCK.  TDO is a tri-state output which is inactive except when scanning of data is in progress. |
| TRSTB | Input | C1 | **Active low Test Reset (TRSTB).** This signal provides an asynchronous TEMUX 84 test access port reset via the IEEE P1149.1 test access port.  TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence.<br><br>Note that if not used, TRSTB must be connected to the RSTB input. |
| **Power and Ground Pins** | | | |
| VDD3.3[19]<br>VDD3.3[18]<br>VDD3.3[17]<br>VDD3.3[16]<br>VDD3.3[15]<br>VDD3.3[14]<br>VDD3.3[13]<br>VDD3.3[12]<br>VDD3.3[11]<br>VDD3.3[10]<br>VDD3.3[9]<br>VDD3.3[8]<br>VDD3.3[7]<br>VDD3.3[6]<br>VDD3.3[5]<br>VDD3.3[4]<br>VDD3.3[3]<br>VDD3.3[2]<br>VDD3.3[1] | Power | A18<br>A22<br>AB17<br>D11<br>D16<br>D4<br>E1<br>F20<br>L1<br>L19<br>R21<br>R4<br>V2<br>W16<br>W4<br>W8<br>Y18<br>Y20<br>Y5 | **Power (VDD3.3[19:1]).**  The VDD3.3[19:1] pins should be connected to a well decoupled +3.3V DC power supply. |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| VDD1.8[19] | Power | C2 | **Power (VDD1.8[19:1]).** The VDD1.8[19:1] pins should be connected to a well-decoupled +1.8V DC power supply. |
| VDD1.8[18] | | D3 | |
| VDD1.8[17] | | J2 | |
| VDD1.8[16] | | R1 | |
| VDD1.8[15] | | U3 | |
| VDD1.8[14] | | AB2 | |
| VDD1.8[13] | | AB9 | |
| VDD1.8[12] | | Y12 | |
| VDD1.8[11] | | Y15 | |
| VDD1.8[10] | | AB19 | |
| VDD1.8[9] | | N4 | |
| VDD1.8[8] | | V20 | |
| VDD1.8[7] | | U19 | |
| VDD1.8[6] | | N21 | |
| VDD1.8[5] | | K21 | |
| VDD1.8[4] | | C22 | |
| VDD1.8[3] | | C18 | |
| VDD1.8[2] | | A13 | |
| VDD1.8[1] | | B7 | |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| VSS[69] | Ground | C4 | **Ground (VSS3.3[69:1]).**  The VSS[69:1] pins should be connected to GND. |
| VSS[68] | | A12 | |
| VSS[67] | | AA2 | |
| VSS[66] | | AA3 | |
| VSS[65] | | AA7 | |
| VSS[64] | | AB12 | |
| VSS[63] | | AB15 | |
| VSS[62] | | AB21 | |
| VSS[61] | | AB8 | |
| VSS[60] | | B4 | |
| VSS[59] | | C11 | |
| VSS[58] | | C17 | |
| VSS[57] | | C19 | |
| VSS[56] | | C3 | |
| VSS[55] | | D15 | |
| VSS[54] | | D19 | |
| VSS[53] | | D22 | |
| VSS[52] | | D5 | |
| VSS[51] | | D8 | |
| VSS[50] | | F1 | |
| VSS[49] | | G19 | |
| VSS[48] | | G4 | |
| VSS[47] | | J10 | |
| VSS[46] | | J11 | |
| VSS[45] | | J12 | |
| VSS[44] | | J13 | |
| VSS[43] | | J14 | |
| VSS[42] | | J9 | |
| VSS[41] | | K10 | |
| VSS[40] | | K11 | |
| VSS[39] | | K12 | |
| VSS[38] | | K13 | |
| VSS[37] | | K14 | |
| VSS[36] | | K3 | |
| VSS[35] | | K9 | |
| VSS[34] | | L10 | |
| VSS[33] | | L11 | |
| VSS[32] | | L12 | |
| VSS[31] | | L13 | |
| VSS[30] | | L14 | |

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| Pin Name | Type | Pin No. | Function |
|---|---|---|---|
| VSS[29] | | L21 | |
| VSS[28] | | L9 | |
| VSS[27] | | M10 | |
| VSS[26] | | M11 | |
| VSS[25] | | M12 | |
| VSS[24] | | M13 | |
| VSS[23] | | M14 | |
| VSS[22] | | M19 | |
| VSS[21] | | M4 | |
| VSS[20] | | M9 | |
| VSS[19] | | N10 | |
| VSS[18] | | N11 | |
| VSS[17] | | N12 | |
| VSS[16] | | N13 | |
| VSS[15] | | N14 | |
| VSS[14] | | N9 | |
| VSS[13] | | P10 | |
| VSS[12] | | P11 | |
| VSS[11] | | P12 | |
| VSS[10] | | P13 | |
| VSS[9] | | P14 | |
| VSS[8] | | P9 | |
| VSS[7] | | T2 | |
| VSS[6] | | V21 | |
| VSS[5] | | V22 | |
| VSS[4] | | W21 | |
| VSS[3] | | Y11 | |
| VSS[2] | | Y14 | |
| VSS[1] | | Y17 | |
| **Unconnected** | | | |
| Unconnected | | A1 B2 L4 P4 T19 | These balls have no internal connections.  They may be left floating or tied to a static logic level. |

**Notes on Pin Descriptions:**

1. All TEMUX 84 inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

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2. All TEMUX 84 outputs and bi-directionals have at least 2 mA drive capability. The bidirectional data bus outputs, D[7:0], have 4 mA drive capability. The outputs TCLK[3:1], TPOS/TDAT[3:1], TNEG/TMFP[3:1], RGAPCLK/RSCLK[3:1], RDATO[3:1], RFPO/RMFPO[3:1], ROVRHD[3:1], TFPO/TMFPO/TGAPCLK[3:1], SBIACT, RECVCLK1, RECVCLK2, RECVCLK3, CASID[21:1], CCSID, MVID[21:1], TS0ID, TDO and INTB have 4 mA drive capability. The SBI outputs and telecom bus outputs, SDDATA[7:0], SDDP, SDPL, SDV5, SAJUST_REQ, LAV5, LAC1J1V1, LADATA[7:0], LADP, LAOE/LATPL and LAPL, have 8mA drive capability. The bidirectional SBI signal SDC1FP has 8mA drive capability.

3. Inputs CSB, RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

4. Input A[12] has an internal pull-down resistor.

5. All unused inputs should be connected to GROUND.

6. Power to the VDD3.3 pins should be applied *before* power to the VDD1.8 pins is applied.  Similarly, power to the VDD1.8 pins should be removed *before* power to the VDD3.3 pins is removed.

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# 9 FUNCTIONAL DESCRIPTION

The TEMUX 84 supports a total throughput of 155.52Mbit/s (including overhead) in both transmit (a.k.a. egress) and receive (a.k.a. ingress) directions. The bandwidth is divided into three approximately equal data streams, each independently configured relative to the others. Configurations include, but are not limited to:

- 28 1.544Mbit/s or 21 2.048Mbit/s tributaries multiplexed into a DS3 or mapped directly into a SONET/SDH structure. The tributaries may be framed T1s, framed E1s, transparent virtual tributaries (TVTs) or clear channel. Optionally, the DS3 may be mapped into a SONET/SDH structure.

- A single 44.736Mbit/s or 34.386Mbit/s stream. It may be a T3, E3 or clear channel. The 44.736Mbit/s data stream may be mapped into a SONET/SDH structure.

## 9.1 Transparent Virtual Tributaries

Transparent virtual tributaries (TVTs) are supported when performing VT1.5/TU11 or VT2/TU12 mapping into the Telecom Bus and the SBI Bus is being used. Conceptually, a TVT is passed straight from the Telecom Bus to the SBI Bus (and visa versa) with no knowledge of the mapping protocol or T1/E1 framing.

On the SBI Add Bus there are two methods of indicating transmit pointers. If the ETVTPTRDIS or EPTRBYP bit is logic 1, the SAV5 input must indicate the location of the V5 byte and the V1/V2 bytes need not be valid at the SBI Add Bus. If both ETVTPTRDIS and EPTRBYP bit are logic 0, the V1/V2 bytes at the SBI Add Bus must contain a pointer to the V5 byte. The Egress VTPPs accommodate the arbitrary alignment of the SBI and Telecom Add buses by encoding a new V1/V2 value and generating a LAV5 output pulse to match. The H1/H2 value is not encoded. The Telecom bus may be formatted as AU3s or as an AU4; the VTPPs will translate the AU3s to the AU4 format of the SBI bus.

A TVT presented by the Telecom Drop bus must contain a valid V1/V2 pointer. The V1/V2 will be modified in the process of mapping the TVT into the SBI Drop Bus, which by definition has a SPE alignment equivalent to a pointer of 522 decimal. Tributary and path pointer justifications on the Telecom Drop Bus will result in corresponding rate justifications at the SBI Drop Bus as indicated by the SDPL signal. The SDV5 output will always indicate the V5 byte location.

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The Clock and Frame Synchronization Constraints section indicates constraints on bus alignments imposed by TVT support.

## 9.2   Transmultiplexing

Transmultiplexing ("transmux") is the operating mode that enables 1.544 Mb/s and 2.048 Mb/s unstructured tributaries to be exchanged between the SONET/SDH Telecom Bus and the DS3 line interface.  It is enabled on a per-SPE/DS3 basis by setting an SPE Configuration register's OPMODE_SPEx[2:0] bits to 010 and it's LINEOPT_SPEx[1:0] bits to 00.  The system interface is unused in this mode.

The TEMUX 84 will receive a channelized DS3 stream from the serial clock and data inputs.  It will frame up to the DS3 and de-multiplex the individual 1.544 Mb/s or 2.048 Mb/s tributaries.  The tributaries are jitter attenuated, bit asynchronously mapped into VT1.5/TU11s or VT2/TU12s and presented on the Telecom Add bus.  Byte synchronous mapping is not an option in transmux mode.

In the reverse direction, VT1.5/TU11s or VT2/TU12s are bit asynchronously de-mapped from the Telecom Drop bus.  The 1.544 Mb/s or 2.048 Mb/s tributaries are jitter attenuated and multiplexed into a DS3, which is presented on the serial clock and data outputs.

The correspondence between the DS3 tributaries and the SONET/SDH VT/TUs is provided in the Tributary Indexing section.

Performance monitoring as documented in the T1/E1 Performance Monitoring section can be performed on the tributaries.  In addition, HDLC channels and PRBS patterns may be monitored.  With the exception of unframed PRBS reception, the performance monitoring assumes the tributaries are standard T1 or E1 data streams.  On a per-tributary basis, the TXPMON context bit programmed through the RJAT Indirect Channel Data Register selects either the SONET/SDH mapper transmit or DS3 transmit tributary for performance monitoring.

The frame pulse constraints of Section 12.2.3 must be adhered to when the TEMUX 84 is operating in transmux mode with the TelecomBus operating at 77.76 MHz.

A specific register configuration sequence must be followed to enable transmux mode correctly. This sequence is defined in section 4.7 of the TEMUX 84 Programmer's Guide, PMC-2010270 Issue 3.

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## 9.3   T1 Framing

T1 framing can be performed on up to three sets of 28 tributaries.  Each set of tributaries may be multiplexed into a DS3 or mapped into a SPE via VT1.5s/TU-11s.

The T1 framing function searches for the framing bit pattern in the standard Superframe (SF), SLC®96 or Extended Superframe (ESF) framing formats.  When searching for frame each of the 193 (SF or SLC®96) or each of the 772 (ESF) framing bit candidates is simultaneously examined.

The time required to acquire frame alignment to an error-free ingress stream, containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0), is dependent upon the framing format.  For SF format, the T1 framer will determine frame alignment within 4.4ms 99 times out of 100.  For SLC®96 format, the T1 framer will determine frame alignment within 13ms.  For ESF format, the T1 framer will determine frame alignment within 15 ms 99 times out of 100.

Once the T1 framer has found frame, the ingress data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or a CRC-6 error in ESF), and severely errored framing events.  The performance data is accumulated for each tributary.  The T1 framer also detects out-of-frame, based on a selectable ratio of framing bit errors.  For ESF, out-of-frame declaration is based strictly on Frame Alignment Signal (F1-F6) bit errors; a new frame search is never initiated upon excessive CRC-6 errors.

The framing function can also be disabled to allow reception of unframed data.

### 9.3.1  Inband Code Detection

The framer detects the presence of either of two programmable inband loopback activate and deactivate code sequences in either framed or unframed data streams (whether data stream is framed or unframed is not programmable) .  The loopback codes will be detected in the presence of a mean bit error rate of up to $10^{-2}$.  When the inband code is framed, the framing bits overwrite the code bits, thus appearing to the receiver as a $2.6 \times 10^{-3}$ BER (which is within the tolerable BER of $10^{-2}$).

Code indication is provided on the active high loopback activate (LBA) and loopback deactivate (LBD) status bits.  Changes in these status bits result in the setting of corresponding interrupt status bits, LBAI and LBDI respectively, and can also be configured to result in the setting of a maskable interrupt indication.

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The inband loopback activate condition consists of a repetition of the programmed activate code sequence in all bit positions for a minimum of 5.08 seconds (± 40 ms).  The inband loopback deactivate condition consists of a repetition of the programmed deactivate code sequence in all bit positions for a minimum of 5.08 seconds (± 40 ms).  Programmed codes can be from three to eight bits in length.

The code sequence detection and timing is compatible with the specifications defined in T1.403, TR-TSY-000312, and TR-TSY-000303.

### 9.3.2  T1 Bit Oriented Code Detection

The presence of 63 of the possible 64 bit oriented codes transmitted in the T1 Facility Data Link channel in ESF framing format is detected, as defined in ANSI T1.403 and in TR-TSY-000194.  The 64th code (111111) is similar to the HDLC flag sequence and is used to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0).  The receiver declares a received code valid if it has been observed for two consecutive times.  The code is declared removed if two code sequences containing code values different from the detected code are received two consecutive times.

Valid BOC are indicated through the BOCI status bit.  The BOC bits are set to all ones (111111) if no valid code has been detected.  An interrupt is generated to signal when a detected code has been validated or when a valid code goes away (i.e. the BOC bits go to all ones).

### 9.3.3  T1 Alarm Integration

The presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, SLC®96 or ESF formats is detected and integrated in accordance with the specifications defined in ANSI T1.403 and TR-TSY-000191.

The presence of Yellow alarm is declared when the Yellow pattern has been received for 400 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 400 ms (± 50 ms).  The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms).  The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 2.55

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sec (±40 ms); the AIS alarm is removed when the AIS condition has been absent for 16.6 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a $10^{-3}$ bit error rate.

### 9.3.3.1  Customer Interface Alarms

The RAI-CI and AIS-CI alarms defined in T1.403 are detected reliably.

By definition, RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds.  It consists of sequentially interleaving 0.99 seconds of 00000000 11111111 (right-to-left) with 90 ms of 00111110 11111111.

RAI-CI is declared when a bit oriented code of "00111110 11111111" is validated (i.e. two consecutive patterns) while RAI (a.k.a. Yellow alarm) is declared.  RAI-CI is cleared upon deassertion of RAI or upon 28 consecutive 40ms intervals without validation of "00111110 11111111".

By definition, AIS-CI is a repetitive pattern of 1.26 seconds.  It consists of 1.11 seconds of an unframed all ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature.  The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones.  AIS-CI is an unframed pattern, so it is defined for all framing formats.

AIS-CI is declared between 1.40 and 2.56 seconds after initiation of the AIS-CI signal and is deasserted 16.6 seconds after it ceases.

### 9.4   E1 Framing

E1 framing can be performed on up to three sets of 21 tributaries.  Each set of tributaries may be multiplexed into a DS3 according to the ITU-T Rec. G.747 standard or mapped into a SPE via VT2s/TU-12s.

The E1 framing function searches for basic frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once basic (or FAS) frame alignment has been found, the incoming PCM data stream is continuously monitored for FAS/NFAS framing bit errors, which are accumulated in a framing bit error counter dedicated to each tributary.  Once CRC multiframe alignment has been found, the PCM data stream is continuously monitored for CRC multiframe alignment pattern errors and CRC-4 errors, which

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are accumulated in a CRC error counter dedicated to each tributary.  Once CAS multiframe alignment has been found, the PCM data is continuously monitored for CAS multiframe alignment pattern errors.  The E1 framer also detects and indicates loss of basic frame, loss of CRC multiframe, and loss of CAS multiframe, based on user-selectable criteria.  The reframe operation can be initiated by software, by excessive CRC errors, or when CRC multiframe alignment is not found within 400 ms.

The E1 framer extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe).  Moreover, the framer also extracts submultiframe-aligned 4-bit codewords from each of the National bit positions Sa4 to Sa8, and stores them in microprocessor-accessible registers that are updated every CRC submultiframe.

The E1 framer identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe).  Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 4 (provided the RAIC bit is logic 1) and 3 consecutive occurrences, respectively, as per Recommendation O.162.  Detection of AIS and timeslot 16 AIS are provided.  AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms.  The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (INF, INSMF, INCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, TS16AISD, COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred.  Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

**Basic Frame Alignment Procedure**

The E1 framer searches for basic frame alignment using the algorithm defined in ITU-T Recommendation G.706 sections 4.1.2 and 4.2.

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The algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS ('0011011');

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed non-frame alignment sequence (NFAS) TS 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed TS 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the second 7-bit FAS sequence check. This "hold-off" is done to ensure that new frame alignment searches are done in the next bit position, modulo 512.  This facilitates the discovery of the correct frame alignment, even in the presence of fixed timeslot data imitating the FAS.

The algorithm provides robust framing operation even in the presence of random bit errors; the algorithm provides a 99.98% probability of finding frame alignment within 1 ms in the presence of $10^{-3}$ bit error rate and no mimic patterns.

Once frame alignment is found, the INF context bit is set to logic 1, a change of frame alignment is indicated (if it occurred), and the frame alignment signal is monitored for errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and the debounced value of the Remote Alarm bit (bit 3 of NFAS frames) is reported.  Loss of frame alignment is declared if 3 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions.  In the presence of a random $10^{-3}$ bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The E1 framer can be forced to initiate a basic frame search at any time when any of the following conditions are met:

- the software re-frame bit, REFR, in the T1/E1 Framer Indirect Channel Data registers is set to logic 1;

- the CRC Frame Find Block is unable to find CRC multiframe alignment; or

- the CRC Frame Find Block accumulates excessive CRC evaluation errors ($\geq$ 915 CRC errors in 1 second) and is enabled to force a re-frame under that condition.

## CRC Multiframe Alignment Procedure

The E1 framer searches for CRC multiframe alignment by observing whether the International bits (bit 1 of TS 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms

Once CRC multiframe alignment is found, the INCMF register bit is set to logic 1, and the E1 framer monitors the multiframe alignment signal (MFAS), indicating errors occurring in the 6-bit MFAS pattern, errors occurring in the received CRC and the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The E1 framer declares loss of CRC multiframe alignment if basic frame alignment is lost. However, once CRC multiframe alignment is found, it cannot be lost due to errors in the 6-bit MFAS pattern.

Under the CRC-to-non-CRC interworking algorithm, if the E1 framer can achieve basic frame alignment with respect to the incoming PCM data stream, but is unable to achieve CRC-4 multiframe alignment within the subsequent 400 ms, the distant end is assumed to be a non CRC-4 interface. The details of this algorithm are illustrated in the state diagram in Figure 12.

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**Figure 12    - CRC Multiframe Alignment Algorithm**

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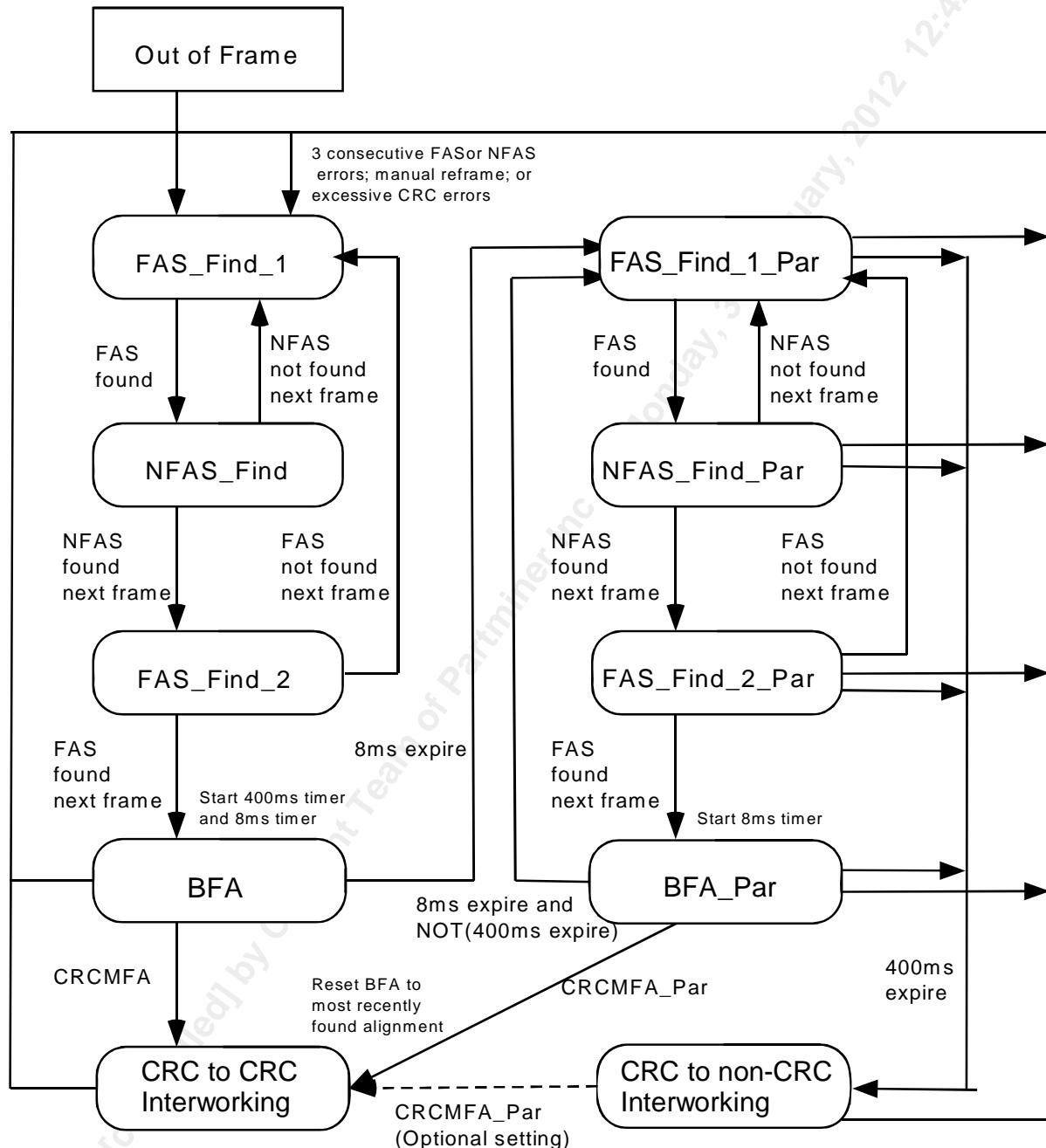
### Table 1        - E1 framer Framing States

| State | Out of Frame | Out of Offline Frame |
|-------|--------------|----------------------|
| FAS_Find_1 | Yes | No |
| NFAS_Find | Yes | No |
| FAS_Find_2 | Yes | No |
| BFA | No | No |
| CRC to CRC Interworking | No | No |
| FAS_Find_1_Par | No | Yes |
| NFAS_Find_Par | No | Yes |
| FAS_Find_2_Par | No | Yes |
| BFA_Par | No | No |
| CRC to non-CRC Interworking | No | No |

The states of the primary basic framer and the parallel/offline framer in the E1 framer block at each stage of the CRC multiframe alignment algorithm are shown in Table 1.

From an out of frame state, the E1 framer attempts to find basic frame alignment in accordance with the FAS/NFAS/FAS G.706 Basic Frame Alignment procedure outlined above.  Upon achieving basic frame alignment, a 400 ms timer is started, as well as an 8 ms timer.  If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared.

If the 8 ms timer expires without achieving multiframe alignment, a new offline search for basic frame alignment is initiated.  This search is performed in accordance with the Basic Frame Alignment procedure outlined above. However, this search does not immediately change the actual basic frame alignment of the system (i.e., PCM data continues to be processed in accordance with the first basic frame alignment found after an out of frame state while this frame alignment search occurs as a parallel operation).

When a new basic frame alignment is found by this offline search, the 8 ms timer is restarted.  If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared and the basic frame alignment is set accordingly (i.e., the basic frame alignment is set to correspond to the frame alignment found by the parallel offline search, which is also the basic frame alignment corresponding to the newly found CRC multiframe alignment).

Subsequent expirations of the 8 ms timer will likewise reinitiate a new search for basic frame alignment.  If, however, the 400 ms timer expires at any time during this procedure, the E1 framer stops searching for CRC multiframe alignment and declares CRC-to-non-CRC interworking.  In this mode, the E1 framer may be optionally set to either halt searching for CRC multiframe altogether, or may

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continue searching for CRC multiframe alignment using the established basic frame alignment.  In either case, no further adjustments are made to the basic frame alignment, and no offline searches for basic frame alignment occur once CRC-to-non-CRC interworking is declared:  it is assumed that the established basic frame alignment at this point is correct.

### AIS Detection

When an unframed all-ones receive data stream is received, an AIS defect is indicated by setting the AISD context bit to logic 1 when fewer than three zero bits are received in 512 consecutive bits or, optionally, in each of two consecutive periods of 512 bits.  The AISD bit is reset to logic 0 when three or more zeros in 512 consecutive bits or in each of two consecutive periods of 512 bits.  Finding frame alignment will also cause the AISD bit to be set to logic 0.

### Signaling Frame Alignment

Once the basic frame alignment has been found, the E1 framer searches for Channel Associated Signaling (CAS) multiframe alignment using the following G.732 compliant algorithm: signaling multiframe alignment is declared when at least one non-zero time slot 16 bit is observed to precede a time slot 16 containing the correct CAS alignment pattern, namely four zeros ("0000") in the first four bit positions of timeslot 16.

Once signaling multiframe alignment has been found, the E1 framer sets the INSMF context bit of the tributary to logic 1, and monitors the signaling multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signaling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe).

This E1 framer also indicates the reception of TS 16 AIS when time slot 16 has been received with three or fewer zeros in each of two consecutive multiframe periods.  The TS16AIS status is cleared when each of two consecutive signaling multiframe periods contain four or more zeros OR when the signaling multiframe signal is found.

The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in time slot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes.  Loss of CAS multiframe alignment is also declared if basic frame alignment has been lost.

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### National Bit Extraction

The E1 framer extracts and assembles the submultiframe-aligned National bit codewords Sa4[1:4] , Sa5[1:4] , Sa6[1:4] , Sa7[1:4] and Sa8[1:4].  The corresponding register values are updated upon generation of the CRC submultiframe interrupt.

This E1 framer also detects the V5.2 link ID signal, which is detected when 2 out of 3 Sa7 bits are zeros.  Upon reception of this Link ID signal, the V52LINKV context bit is set to logic 1.  This bit is cleared to logic 0 when 2 out of 3 Sa7 bits are ones.

### E1 Alarm Integration

The OOF and the AIS defects are integrated, verifying that each condition has persisted for 104 ms (± 6 ms) before indicating the alarm condition.  The alarm is removed when the condition has been absent for 104 ms (± 6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection).  The E1 framer counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS is present when 13 or more AISD indications (of a possible 16) have been received.  Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated.  An interval with no valid AIS presence indication decrements the interval counter.  The AIS Alarm declaration is removed when the counter reaches 0.  This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a $10^{-3}$ mean bit error rate.

The Red alarm algorithm monitors occurrences of out of frame (OOF) over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval.  Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated.  An interval with valid INF indication decrements the interval counter; the Red Alarm declaration is removed when the counter reaches 0.  This algorithm biases OOF occurrences, leading to declaration of Red alarm when intermittent loss of frame alignment occurs.

The E1 framer can also be disabled to allow reception of unframed data.

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## 9.5   T1/E1 Performance Monitoring

CRC error events, Frame Synchronization bit error events, and Out Of Frame events, or optionally, Change of Frame Alignment (COFA) events are accumulated with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second).  When the transfer clock signal is applied, the counter values are transferred into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed.  If the holding registers are not read between successive transfer clocks, the OVR context bit is asserted to indicate data loss.

A bit error event (BEE) is defined as an F-bit error for SF and SLC®96 framing format or a CRC-6 error for ESF framing format.  A framing bit error (FER) is defined as an $F_s$ or $F_t$ error for SF and SLC®96 and an $F_e$ error for ESF framing format.

The transfer clock within the TEMUX 84 chip is generated precisely once per second (i.e. 19440000 SREFCLK cycles) if the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1 or by writing to the Global PMON Update register with the FRMR bit set.  Coincident with the counter transfer, a Performance Report Message (PRM) is transmitted for each T1 tributary for which the PRMEN context bit is logic 1.

## 9.6   T1/E1 HDLC Receiver

The HDLC Receiver is a microprocessor peripheral used to receive HDLC frames on the 4 kHz ESF facility data link or the E1 Sa-bit data link.  A data link can also be extracted from any sub-set of bits within a single DS0.

The HDLC Receiver detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 127-byte FIFO buffer.  An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer.  Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The RHDL Indirect Channel Data Registers contain bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence end of message bytes written into the FIFO.  The RHDL Indirect Channel Data Registers also indicates the abort, flag, and end of message status of the data

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just read from the FIFO.  On end of message, the RHDL Indirect Channel Data Registers indicates the FCS status and if the packet contained a non-integer number of bytes.

## 9.7   T1/E1 Elastic Store (ELST)

Frame slip buffers exist in both the ingress and egress directions.

In the ingress direction, the Elastic Store (ELST) synchronizes ingress frames to the common ingress H-MVIP clock and frame pulse (CMV8MCLK, CMVFP, CMVFPC) in H-MVIP modes.  When using the SBI bus, the elastic store is required in locked or slave mode.

In the egress direction, the Elastic Store is required in H-VIP mode or in SBI slave or locked modes when the transmit data is loop timed or referenced to one of the recovered clocks (RECVCLK1, RECVCLK2, RECVCLK3).

The frame data is buffered in a two frame circular data buffer.  Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.  When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane/transmit clock, the write pointer will catch up to the read pointer and the buffer will be filled.  Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary.  The subsequent frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane/transmit clock, the read pointer will catch up to the write pointer and the buffer will be empty.  Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary.  The previous frame is repeated.

A slip operation is always performed on a frame boundary.

When the ingress timing is recovered from the receive data, the ingress elastic store can be bypassed to eliminate the 2 frame delay.

To allow for the extraction of signaling information in the data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ingress ELST may optionally insert a programmable idle code into all channels when the framer is out of frame synchronization.  This code is set to all 1's when the ELST is reset.

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## 9.8 T1/E1 Signaling Extraction

Channel associated signaling (CAS) is extracted from an E1 signaling multi-frame or from ESF, SLC®96 and SF T1 formats.

In T1 mode, signaling bits are extracted from the received data streams for ESF, SLC®96 and SF framing formats.  The signaling states are optionally debounced and serialized onto the CASID[x] H-MVIP outputs or CAS bits within the SBI Bus structure.  Debouncing is performed on the entire signaling state.  This CASID[x] output is channel aligned with the MVID[x] output, and the signaling bits are repeated for the entire superframe, allowing downstream logic to reinsert signaling into any frame, as determined by system timing.  The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5, 6, 7 and 8) in ESF framing format.  In SF and SLC®96 format, bits 5 and 6 contain the A and B bits from every second superfame and bits 7 and 8 contain the A and B bits from the alternate superframes.  The four bits are updated every 24 frames and are debounced collectively.

Three superframes for ESF and six superframes for SLC®96 and SF worth of signal are buffered to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801.  With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 ESF superframes or 4 SF/SLC®96 superframes before appearing on the serial output stream.

One superframe or signaling-multiframe of signal freezing is provided on the occurrence of slips.  When a slip event occurs, output signaling for the entire superframe in which the slip occurred is frozen; the signaling is unfrozen when the next slip-free superframe occurs.

Control over timeslot signaling bit fixing and signaling debounce is provided on a per-timeslot basis.

An interrupt is provided to indicate a change of signaling state on a per channel basis.

## 9.9 T1/E1 Receive Per-Channel Control

Data and signaling trunk conditioning may be applied on the ingress stream on a per-channel basis.  Also provided is per-channel control of data inversion and the detection and generation of pseudo-random patterns.  These operations occur on

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the data after its passage through frame slip buffer, so that data and signaling conditioning may overwrite the trouble code.

## 9.10  T1 Transmitter

The T1 transmitter generates the 1.544 Mbit/s T1 data streams according to SF, SLC®96 or ESF frame formats.

The transmitter provides per-channel control of idle code substitution, data inversion (either all 8 bits, sign bit magnitude or magnitude only), and zero code suppression.  Three types of zero code suppression (GTE, Bell and "jammed bit 8") are supported and selected on a per-channel basis to provide minimum ones density control.  Context bits provide per-channel control of robbed bit signaling and selection of the signaling source.  All channels can be forced into a trunk conditioning state by the Master Trunk Conditioning (MTRK) context bit.  The transmitter may source pseudo-random bit sequences (PRBS) in a selected sub-set of channels, while simultaneously monitoring the data from the system interface for PRBS errors.

A data link is provided for ESF mode.  The data link sources include bit oriented codes and HDLC messages.  If the T1_FDL_DIS context bit is logic 1, the data link is sourced from the F-bit position of the H-MVIP or SBI interface.  Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS, Yellow, AIS-CI and RAI-CI (ESF only) alarm signals for all formats.

If the AUTOUPDATE bit of the T1/E1 Framer Configuration and Status register is logic 1, the T1 transmitter automatically sends an ANSI T1.403-formatted performance report on the T1 facility data link once per second.

The F-bit may be passed transparently from either the H-MVIP or SBI interface.  To support alignment of the robbed bit signaling to the F-bits, the C8MVFPB input may be redefined as a superframe alignment pulse.

The transmitter can be disabled for framing via the FDIS context bit.

## 9.10.1 SLC®96

SLC®96 is partially supported.  The F-bits must be sourced from the system interface.  To pass the F-bits transparently, the FDIS context bit must be set.  Also, a superframe alignment must be provided to ensure the robbed-bit signaling is inserted in the correct frames relative to the F-bits.  To ensure the

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framing is not corrupted, the timing must be configured to avoid controlled frame slips.

When using the SBI interface, it is recommended the transmit frame slip buffer be bypassed and that the transmit clock be locked to the data stream (i.e. TJAT LOOPT and REFSEL context bits logic 0).

With an H-MVIP interface, the transmit elastic store cannot be bypassed, so the transmit clock must be locked to CTCLK which must be presented a clock that is locked to CMV8MCLK.

### 9.10.2 T1 Bit Oriented Code Generation

63 of the possible 64 bit oriented codes may be transmitted in the Facility Data Link (FDL) channel in ESF framing format, as defined in ANSI T1.403-1995. When transmission is disabled the FDL is set to all ones.

Bit oriented codes are transmitted on the T1 Facility Data Link as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. When driving the T1 facility data link, the transmitted bit oriented codes have priority over any data transmitted except for ESF Yellow Alarm. The code to be transmitted is programmed by writing to the BOC code context bits where it is held until the latest code has been transmitted at least 10 times. If a second code is written before ten repetitions of the first have been transmitted, the second code will be transmitted immediately after the tenth transmission of the first code. If a third consecutive code is desired, its write must be delayed until the transmission of the second code has started, lest the third code overwrite the second.

### 9.11 E1 Transmitter

The E1 transmitter generates a 2048 kbit/s data streams according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

The E1 transmitter provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signaling substitution) by use of the master trunk conditioning (MTRK) context bit. The transmitter may source pseudo-random bit sequences

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(PRBS) in a selected sub-set of channels, while simultaneously monitoring the data from the system interface for PRBS errors.

Common Channel Signaling (CCS) is supported in time slots 15, 16 and 31. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The National Use bits (Sa-bits) can be sourced from the National Bits Codeword context bits as 4-bit codewords aligned to the submultiframe. Only one of the E1 National Bits - SaX (where X = 4-8) can be modified at a given time with a user-selectable 4-bit repeating code word. All remaining Sa-bits will have to be inserted from the system interface if they are to be modified. Setting the INDIS bit to the T1/E1 TXFRMR block enables this.  Alternatively, the Sa-bits may individually carry data links sourced from the internal HDLC controller, or may be passed transparently from the MVED[x] inputs.

## 9.12  T1/E1 HDLC Transmitters

The HDLC transmitter provides a serial data link for the 4 kHz ESF facility data link or E1 Sa-bit data link.  The data link may also be presented in any sub-set of bits within a selected DS0.  The HDLC transmitter is used under microprocessor control to transmit HDLC data frames.  It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags.  If the HDLC transmitter data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the HDLC transmitter continuously transmits the flag sequence (01111110) until data is ready to be transmitted.

The default procedure provides automatic transmission of data once a complete packet is written.  All complete packets of data will be transmitted.  After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted.  The HDLC transmitter then returns to the transmission of flag characters until the next packet is available for transmission.  While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long.

A second mechanism transmits data when the FIFO depth has reached a user configured upper threshold.  The HDLC transmitter will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed.  In this mode,

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the user must be careful to avoid overruns and underruns.  An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO falls below a lower threshold, when the FIFO is full,  or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output.  This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting the ABT bit.  During packet transmission, an underrun situation can occur if data is not written before the previous byte has been depleted.  In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

## 9.13  T1/E1 Receive and Transmit Digital Jitter Attenuators

The TEMUX 84 contains two separate jitter attenuators, one between the receive demultiplexed or demapped T1 or E1 link and the ingress interface and the other between the egress interface and the transmit T1 or E1 link to be multiplexed into DS3 or mapped into SONET/SDH.  Each jitter attenuator receives jittered data and stores the stream in a FIFO timed to the associated clock.  The jitter attenuated data emerges from the FIFO timed to the jitter attenuated clock.  In the receive jitter attenuator, the jitter attenuated clock is referenced to the demultiplexed or demapped tributary receive clock.   In the transmit jitter attenuator, the jitter attenuated transmit tributary clock feeding the M13 multiplexer or SONET/SDH mapper may be referenced to either the data stream, the CTCLK primary input, or the tributary receive clock.

The following describes the T1/E1 jitter attenuators in isolation.  Other active functions such as SBI mapping, M13 multiplexing and SONET/SDH mapping may alter the jitter characteristics of the T1/E1 tributaries.

### Jitter Characteristics

The jitter attenuators provide excellent jitter tolerance and jitter attenuation while generating minimal residual jitter.  In T1 mode, each jitter attenuator can accommodate up to 48 UIpp of input jitter at jitter frequencies above 4 Hz.  For jitter frequencies below 4 Hz, more correctly called wander, the tolerance increases 20 dB per decade.  In E1 mode each  jitter attenuator can

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accommodate up to 48 UIpp of input jitter at jitter frequencies above 5 Hz.  For jitter frequencies below 5 Hz, more correctly called wander, the tolerance increases 20 dB per decade.  In most applications, each jitter attenuator will limit jitter tolerance at lower jitter frequencies only.  The jitter attenuator meet the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and ITU-T Recommendation G.823, and thus allow compliance with these standards and the other less stringent jitter tolerance standards cited in the references.

The jitter attenuators exhibit negligible jitter gain for jitter frequencies below 3.4 Hz, and attenuate jitter at frequencies above 3.4 Hz by 20 dB per decade in T1 mode. They exhibit negligible jitter gain for jitter frequencies below 5 Hz, and attenuates jitter at frequencies above 5 Hz by 20 dB per decade in E1 mode.  In most applications the jitter attenuators will determine jitter attenuation for higher jitter frequencies only.  Wander, below 10 Hz for example, will essentially be passed unattenuated through the jitter attenuators.  Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the waiting time jitter introduced by the multiplexing into DS3 or mapping into SBI or SONET/SDH.  The jitter attenuator allows the implied T1 jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.  The  jitter attenuator meets the E1 jitter attenuation requirements of the ITU-T Recommendations G.737, G.738, G.739 and G.742.

**Jitter Tolerance**

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data.  For T1 modes the jitter attenuator input jitter tolerance is 48 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 278 Hz.  For E1 modes the input jitter tolerance is 48 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 369 Hz.

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**Figure 13     - Jitter Tolerance T1 Modes**
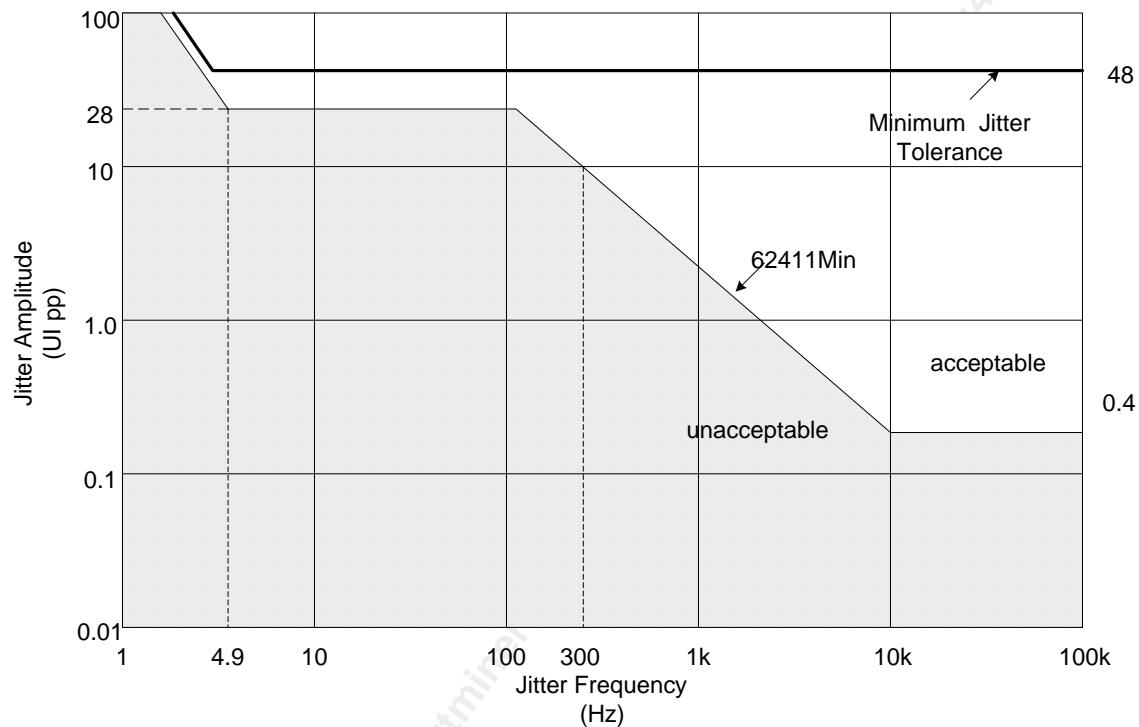
### Figure 14     - Jitter Tolerance E1 Modes
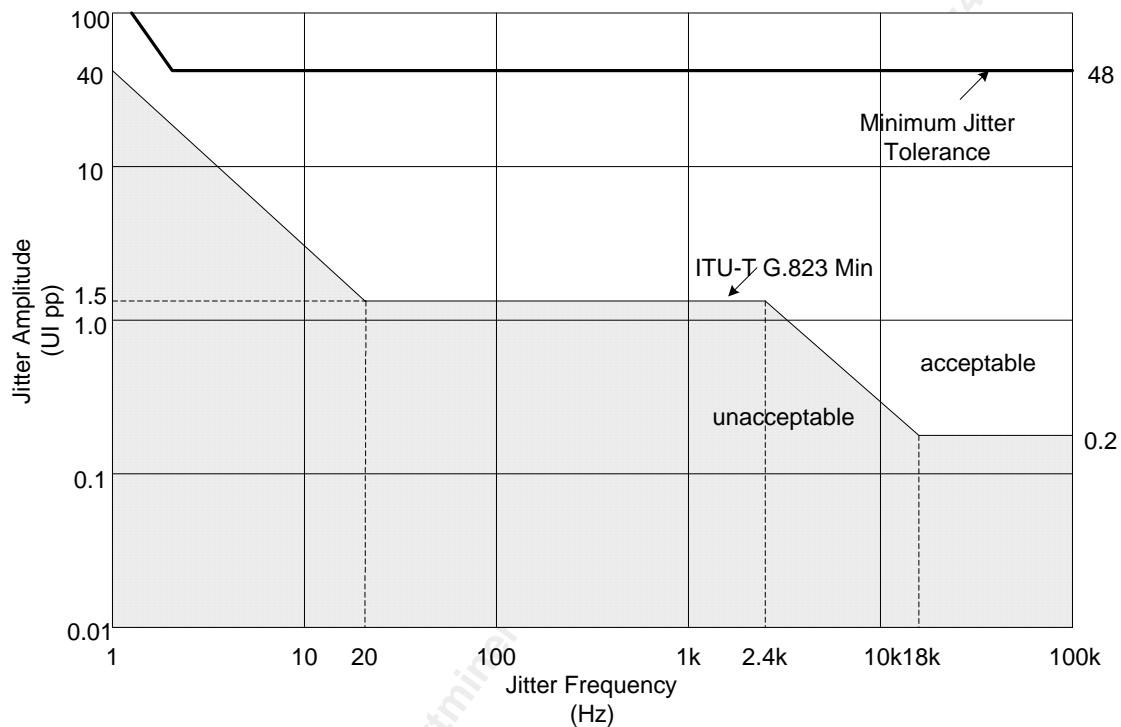


### Jitter Transfer

The output jitter in T1 mode for jitter frequencies from 0 to 3.4 Hz is no more than
0.1 dB greater than the input jitter, excluding the residual jitter.  Jitter frequencies
above 3.4 Hz are attenuated at a level of 20 dB per decade, as shown in Figure
15.

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**Figure 15     - Jitter Transfer T1 Modes**
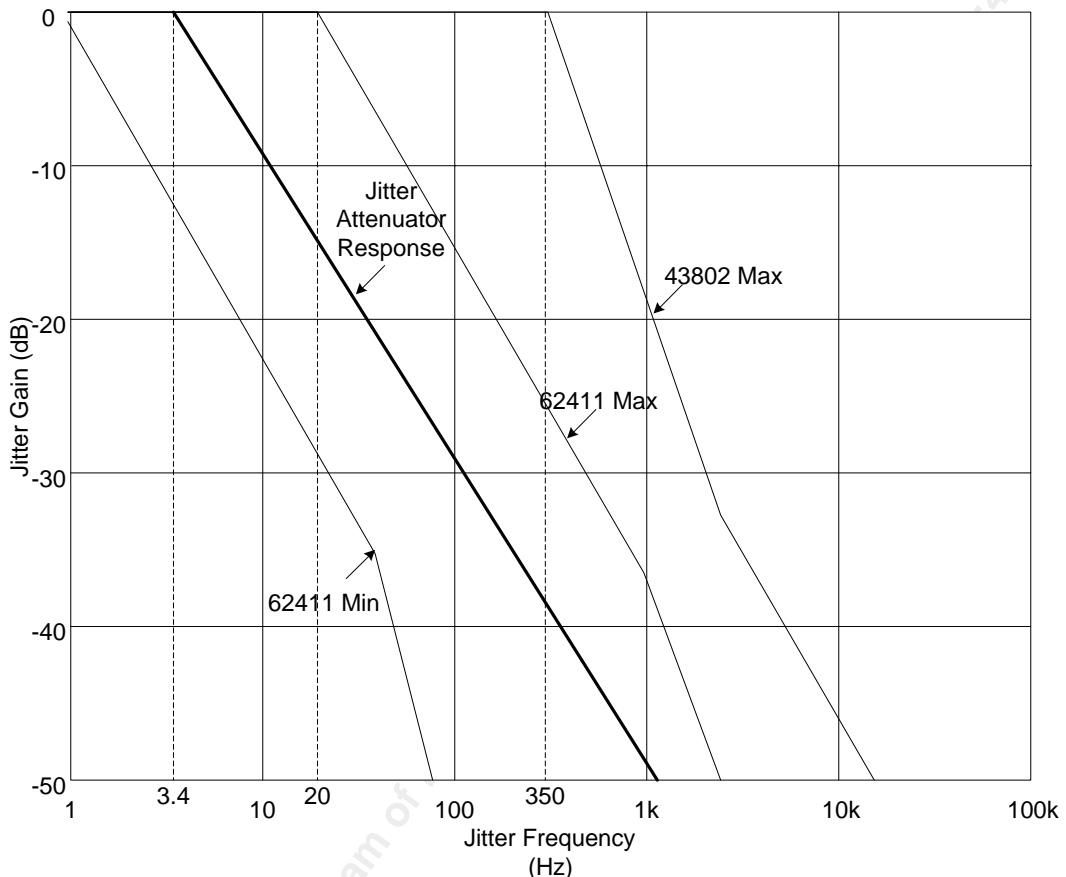


The output jitter in E1 mode for jitter frequencies from 0 to 5.0 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter.  Jitter frequencies above 2.5 Hz are attenuated at a level of 20 dB per decade, as shown in Figure 16.

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**Figure 16      - Jitter Transfer E1 Modes**
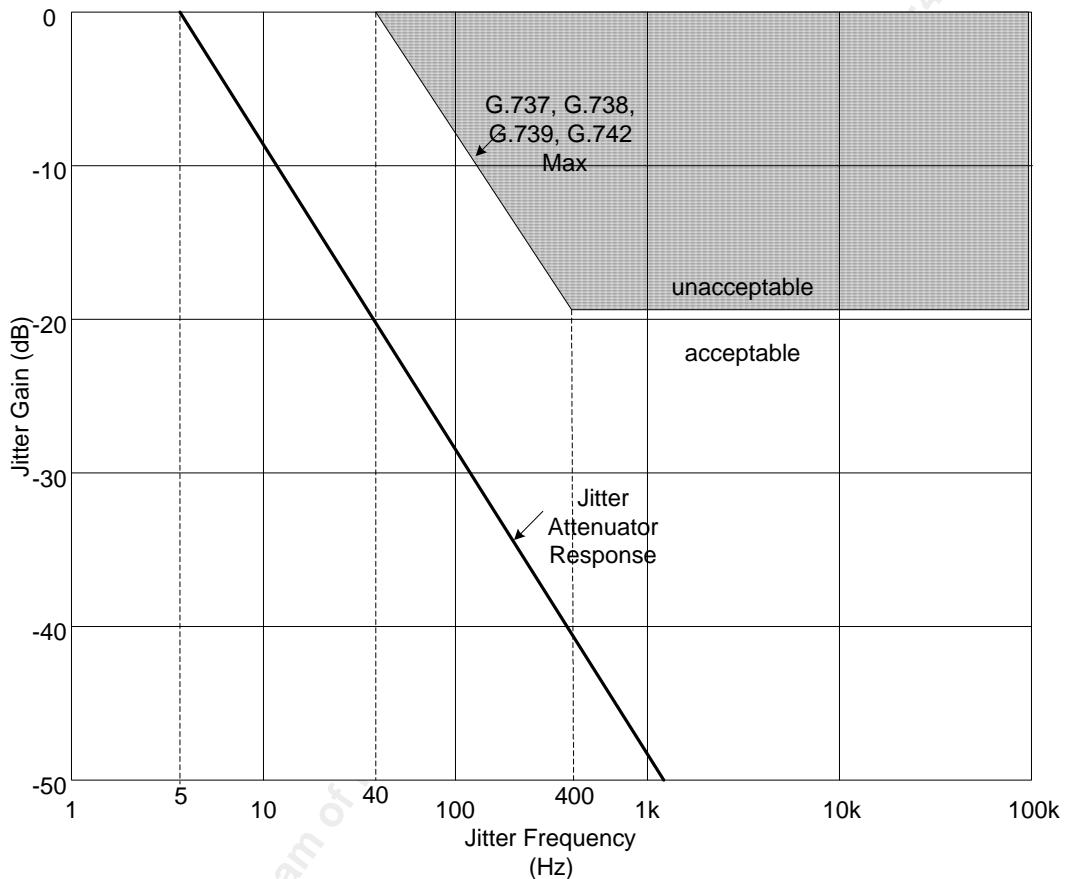


### Frequency Range

The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (48 UIpp) and maximum SREFCLK frequency offset (± 50 ppm).  The tracking range is 1.544 MHz ± 997 Hz with no jitter or SREFCLK frequency offset.

The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 266 Hz with worst case jitter (48 UIpp) and maximum SREFCLK frequency offset (± 50 ppm).  The tracking range is 2.048 MHz ± 999 Hz with no jitter or SREFCLK frequency offset.

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## 9.14  T1/E1 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) is a software selectable PRBS generator and checker for $2^7$-1, $2^{11}$-1, $2^{15}$-1 or $2^{20}$-1 PRBS polynomials for use in the T1 and E1 links.  PRBS patterns may be generated and monitored in both the transmit or receive directions for all T1 and E1 links simultaneously.  The generator is capable of inserting single bit errors under microprocessor control.

The following pseudo random bit sequences are supported:

| Sequence Length | Polynomial |
|---|---|
| $2^{11} - 1$ | $x^{11} + x^9 + 1$ |
| $2^{15} - 1$ | $x^{15} + x^{14} + 1$ |
| $2^{20} - 1$ (QRSS) | $x^{20} + x^{17} + 1$ with zero suppression |
| $2^{20} - 1$ | $x^{20} + x^3 + 1$ |
| $2^7 - 1$ | $x^7 + x^3 + 1$ with XOR in the feedback path |
| $2^7 - 1$ | $x^7 + x^3 + 1$ with XNOR in the feedback path |

The detector auto-synchronizes to the expected PRBS pattern and accumulates the total number of bit errors in a 16-bit counter.  The error count accumulates over the interval defined by writes to the Global PMON Update register.  When a transfer is triggered, the holding register is updated, and the counter reset to begin accumulating for the next interval.  The counter is reset in such a way that no events are missed.  The data is then available until the next transfer.

In addition to the basic PRBS generators and receivers associated with each T1/E1 link, six full-featured pattern generator/detector pairs are available for association with any software selectable link.  Any subset of bits within a frame (except the T1 F-bit) may be programmed to carry either a pseudo-random or fixed pattern.

The six generators can be programmed to generate any pseudo-random pattern with length up to $2^{32}$-1 bits or any user programmable bit pattern from 1 to 32 bits in length.  It also can generate the four DDS codes specified by Bellcore GR-819-CORE.  In addition, the pattern generator can insert single bit errors or a bit error rate between $10^{-1}$ to $10^{-7}$.

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The six receivers can be programmed to check for the generated pseudo random pattern.  The receivers can perform an auto synchronization to the expected pattern and accumulates the total number of bits received and the total number of bit errors in two 32-bit counters.  If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity.  A bit error accumulates when a bit disagrees with the original bit sequence synchronized to.  The counters accumulate either over intervals defined by writes to the Pattern Detector registers or upon writes to the Global PMON Update Register.  When a transfer is triggered, the holding registers are updated, and the counters reset to begin accumulating for the next interval.  The counters are reset in such a way that no events are missed.  The data is then available in the holding registers until the next transfer.

## 9.15  DS3/E3 Framing, Performance Monitoring and Multiplexing

There are three identical instances of the DS3/E3 subsystem provided.  It is important to note the subsystems are active simply by providing appropriate clocks; this is independent of the settings of the SYSOPT[1:0] and OPMODE_SPEx[2:0] register bits.  From this observation, the following TEMUX 84 abilities arise:

- The TPOS/TDAT and TNEG/TMFP present data simply if a DS3/E3 transmit clock is present.  This is independent of whether mapping of a DS3 into SONET/SDH is selected by LINEOPT_SPEx[1:0] register bits.  The source of the clock is dependent on the SBICLKMODE, LOOPT and TICLK register bits.

- When T1/E1 Mapper/Multiplexer mode is selected via the OPMODE_SPEx[2:0] register bits, the DS3 multiplexing in the transmit direction occurs independent of the state of the LINEOPT_SPEx register bits.  The same cannot be said of the receive direction; the demultiplexed T1/E1s are not presented on the system interface if LINEOPT_SPEx[1] is logic 1.

- The RDATO, RFPO/RMFPO and ROVRHD outputs present data simply if a receive DS3/E3 clock is present.  The receive clock (RGAPCLK/RSCLK) will be associated with a demapped DS3 if the LINEOPT_SPEx[1:0] register bits are binary 01 or the transmit DS3/E3 if a diagnostic loopback is selected. Otherwise, it is derived from the RCLK input.

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- The DS3/E3 performance monitoring capability only requires a DS3/E3 line rate clock to actively maintain alarm statuses and accumulate statistics.

Source and destination of the DS3/E3 clocks and data are dependent on configuration.  Figure 17 is a simplified block diagram that illustrates the effect of the configuration of microprocessor accessible register bits.  To preserve clarity, the registers that affect clock polarity or data format have been omitted.

### Figure 17    - DS/E3 Configuration Options
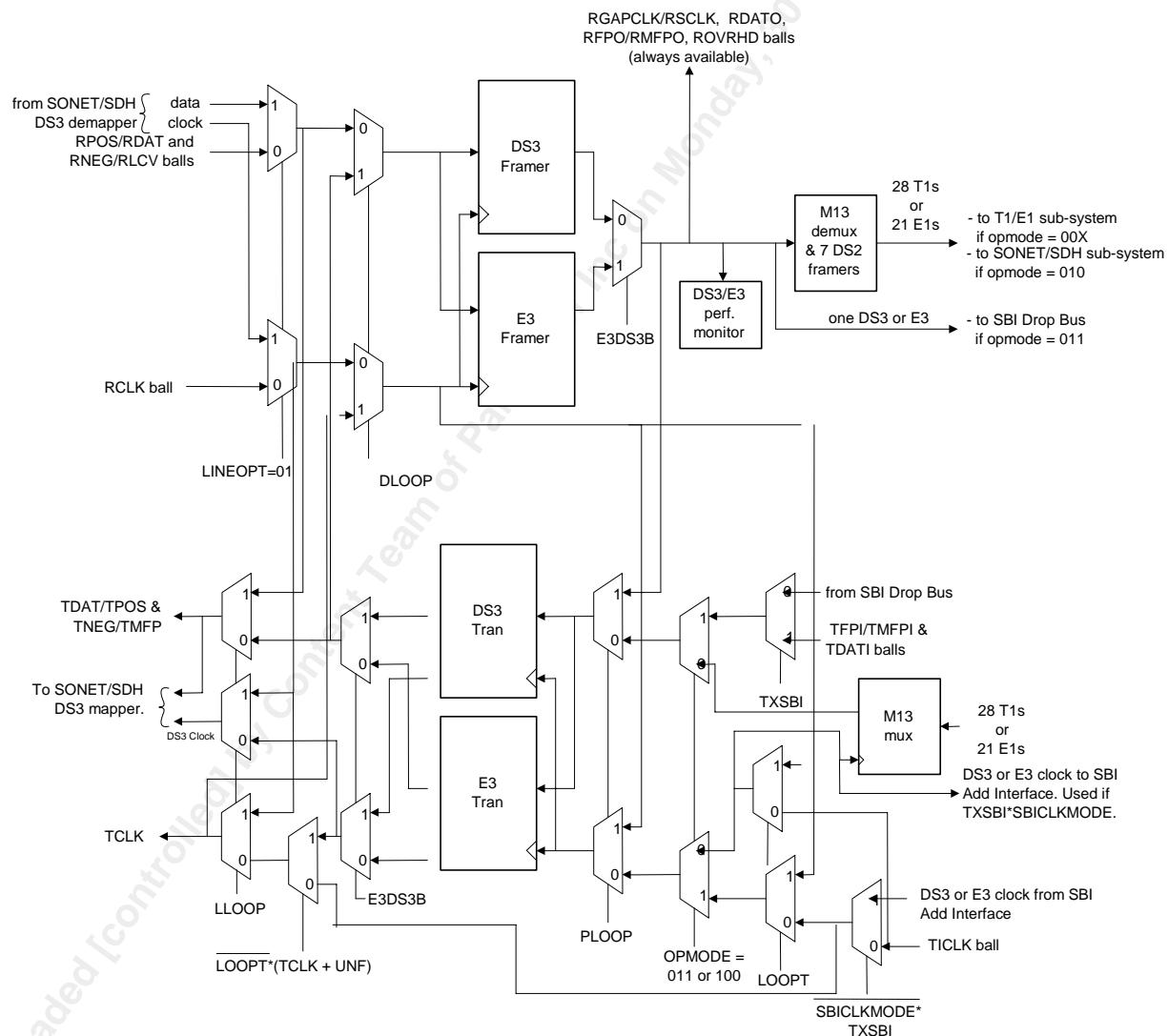
### 9.15.1 DS3 Framer (DS3-FRMR)

Three instances of the DS3 Framer are independently programmed. From each the framed data is presented on RDATO[x], mapped into the SBI bus or may be demultiplexed to 28 DS1s or 21 E1s (ITU-T Rec. G.747).

The DS3 Framer (DS3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The DS3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The DS3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the DS3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as

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well as the line code violation and excessive zeros indication, are accumulated over 1 second intervals with the Performance Monitor (DS3-PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the DS3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a $10^{-3}$ bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is deasserted.

Valid X-bits are extracted by the DS3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

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When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted.  Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC).  HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The DS3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS.  The DS3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The DS3-FRMR may be configured to generate interrupts on error events or status changes.  All sources of interrupts can be masked or acknowledged via internal registers.  Internal registers are also used to configure the DS3-FRMR. Access to these registers is via a generic microprocessor bus.

### 9.15.2 DS3 Bit Oriented Code Detection

The presence of 63 of the possible 64 bit oriented codes transmitted in the T1 Facility Data Link channel in ESF framing format is detected, as defined in ANSI T1.403 and in TR-TSY-000194 or in the DS3 C-bit parity far-end alarm and control (FEAC) channel. The 64th code (111111) is similar to the HDLC flag sequence and is used to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel or FEAC channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0).  BOCs are validated when repeated at least 10 times.  The receiver can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC context bit.  The code is declared removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOC are indicated through the RBOC Interrupt Status register.  The BOC bits are set to all ones (111111) if no valid code has been detected.  An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

### 9.15.3 DS3/E3 HDLC Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive HDLC frames on the DS3 C-bit parity Path Maintenance Data Link, E3 G.832 Network Operator byte,

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E3 G.832 General Purpose Communications Channel or E3 G.751 National Use bit.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO.  The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-byte FIFO buffer.  An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer.  Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO.  The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO.  On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

### 9.15.4 DS3/E3 Performance Monitor Accumulator (DS3/E3-PMON)

The Performance Monitor (PMON) Block interfaces directly with the DS3 Framer (DS3-FRMR) and E3 Framer.  Saturating counters are used to accumulate:

- line code violation (LCV) events

- parity error (PERR) events

- path parity error (CPERR) events

- far end block error (FEBE) events

- excess zeros (EXZS)

- framing bit error (FERR) events

Due to the off-line nature of the DS3 and E3 Framers, PMON continues to accumulate performance metrics even while the framer has declared OOF.

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When an accumulation interval is signaled by a write to the PMON register address space or to the Global PMON Update register, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval.  The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled.  If the holding registers have not been read since the last interrupt, an overrun status bit is set.  In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

Whenever counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled.  If the holding registers have not been read since the last interrupt, an overrun status bit is set.

## 9.15.5 DS3 Transmitter (DS3-TRAN)

Three DS3 transmitters are instantiated.  Each may be programmed to provide framing for unchannelized data from TDATI[x] or the SBI bus, or framing for multiplexed T1s or E1s (ITU-T Rec. G.747).

The DS3 Transmitter (DS3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal.  The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits.  FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the DS3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the DS3-TRAN.  When C-bit parity mode is selected, the path parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the bit-oriented code transmitter.  The path maintenance data link messages are sourced by the TDPR data link transmitter.

The DS3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

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### 9.15.5.1 DS3 Bit Oriented Code Generation

63 of the possible 64 bit oriented codes may be transmitted in the DS3 C-bit parity Far-End Alarm and Control (FEAC) channel.  The 64th code (111111) is similar to the HDLC Flag sequence and is used to disable transmission of any bit oriented codes.  When transmission is disabled the FEAC channel is set to all ones.

Bit oriented codes are transmitted on the DS3 Far-End Alarm and Control channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111.  The code to be transmitted is programmed by writing to the XBOC code registers when it is held until the latest code has been transmitted at least 10 times.  An interrupt or polling mechanism is used to determine when the most recent code written the XBOC register is being transmitted and a new code can be accepted.

### 9.15.6 DS3 Transmitter Timing Sources

DS3 transmitter timing has three possible sources:

1.      TICLK[3:1] input pins.  If the system interface is SBI, then TEMUX 84 is the SBI bus clock master, and uses the SAJUST_REQ output signal to issue timing justification requests to the link-layer device.  If the system interface is serial clock and data, TEMUX 84 derives TGAPCLK[3:1] from TICLK[3:1].)

2.      Integral DS3 clock synthesizer, which generates a gapped DS3 clock from the CLK52M input pin, in response to SBI bus timing justification requests from the link-layer device.  TEMUX 84 is the SBI bus clock slave in this mode, and the SBI bus must be the system side option. External jitter attenuation is recommended when using this DS3 timing option.

3.      Recovered DS3 clock from the RCLK[3:1] input pins.  If the system interface is SBI, then TEMUX 84 is the SBI bus clock master, as in case 1 above.  If the system interface is serial clock and data, TEMUX 84 derives TGAPCLK[3:1] from the recovered DS3 clock.)

In each case, the DS3 transmitter drives the selected DS3 clock source onto the TCLK output pins of the DS3/E3 line side interface.

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### 9.15.7 DS3/E3 HDLC Transmitters

The HDLC transmitter provides a serial data link for the DS3 C-bit parity path maintenance data link, E3 G.832 Network Operator byte, E3 G.832 General Purpose Communications Channel or E3 G.751 National Use bit. The HDLC transmitter is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags. If the HDLC transmitter data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the HDLC transmitter continuously transmits the flag sequence (01111110) until data is ready to be transmitted.

The default procedure provides automatic transmission of data once a complete packet is written. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The HDLC transmitter then returns to the transmission of flag characters until the next packet is available for transmission. While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long. The HDLC transmitter will force transmission if the FIFO is filled up regardless of whether or not the packet has been completely written into the FIFO.

A second mechanism transmits data when the FIFO depth has reached a user configured upper threshold. The HDLC transmitter will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed. In this mode, the user must be careful to avoid overruns and underruns. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO falls below a lower threshold, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

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Abort characters can be continuously transmitted at any time by setting the ABT bit. During packet transmission, an underrun situation can occur if data is not written before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

### 9.15.8 DS3/E3 Pseudo Random Pattern Generation and Detection (PRGD)

The Pseudo Random Pattern Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer for the DS3/E3 payload. Patterns may be generated in the transmit direction, and detected in the receive direction. The patterns consume the entire payload; the overhead bits are ignored. Unframed patterns are not supported. Two types of ITU-T O.151 compliant test patterns are provided : pseudo-random and repetitive.

The PRGD can be programmed to generate any pseudo-random pattern with length up to $2^{32}-1$ bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between $10^{-1}$ to $10^{-7}$.

The PRGD can be programmed to check for the generated pseudo random pattern. The PRGD can perform an auto synchronization to the expected pattern and accumulates the total number of bits received and the total number of bit errors in two 32-bit counters. If a repetitive pattern is selected, the receiver will synchronize to any bit sequence that repeats with the programmed periodicity. A bit error accumulates when a bit disagrees with the original bit sequence synchronized to. The counters accumulate either over intervals defined by writes to the Pattern Detector registers or upon writes to the Global PMON Update Register. When a transfer is triggered, the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next transfer.

### 9.15.9 M23 Multiplexer (MX23)

The M23 Multiplexer (MX23) integrates circuitry required to asynchronously multiplex and demultiplex seven DS2 streams into, and out of, an M23 or C-bit Parity formatted DS3 serial stream.

When multiplexing seven DS2 streams into an M23 formatted DS3 stream, the MX23 function performs rate adaptation to the DS3 by integral FIFO buffers. The C-bits are also generated and inserted. Software control is provided to transmit DS2 AIS and DS2 payload loopback requests. The loopback request is coded by

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inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7). The MX23 also supports generation of a C-bit Parity formatted DS3 stream by providing an internally generated DS2 rate clock corresponding to a 100% stuffing ratio. Integrated M13 applications are supported by providing an internally generated DS2 rate clock corresponding to a 39.1% stuffing ratio.

When demultiplexing seven DS2 streams from an M23 formatted DS3, the MX23 performs bit destuffing via interpretation of the C-bits. The MX23 also detects and indicates DS2 payload loopback requests encoded in the C-bits. As per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS2 payload loopback can be activated or deactivated under software control. During payload loopback the DS2 stream being looped back still continues unaffected in the demultiplex direction to the DS2 Framer. All seven demultiplexed DS2 streams can also be replaced with AIS on an individual basis under register control or they can be configured to be replaced automatically on detection of out of frame, loss of signal, RED alarm or alarm indication signal.

### 9.15.10    DS2 Framer (DS2 FRMR)

The DS2 Framer (DS2-FRMR) integrates circuitry required for framing to a DS2 bit stream and is directly compatible with the M12 DS2 application.

The DS2 FRMR frames to a DS2 signal with a maximum average reframe time of less than 7 ms. Both the F-bits and M-bits must be correct for a significant period of time before frame alignment is declared. Once in frame, the DS2 FRMR provides indications of the M-frame and M-subframe boundaries, and identifies the overhead bit positions in the incoming DS2 signal.

Depending on configuration, declaration of DS2 out-of-frame occurs when 2 out of 4 or 2 out of 5 consecutive F-bits are in error (These two ratios are recommended in TR-TSY-000009 Section 4.1.2) or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames.   The M-bit error criteria for OOF can be disabled via the MBDIS bit in the DS2 Framer configuration register. Note that the DS2 framer is an off-line framer, indicating both OOF and

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COFA.  Error events continue to be indicated even when the FRMR is indicating OOF, based on the previous frame alignment.

The RED alarm and alarm indication signal are detected by the DS2 FRMR in 9.9 ms for DS2 format.   The framer employs a simple integration algorithm (with a 1:1 slope) that is based on the occurrence of "valid" DS2 M-frame intervals.  For the RED alarm, a DS2 M-frame is said to be a "valid" interval if it contains a RED defect, defined as the occurrence of an OOF event during that M-frame.  For AIS, a DS2 M-frame is said to be a "valid" interval if it contains AIS, defined as the occurrence of less than 9 zeros while the framer is out of frame during that M-frame. The discrepancy threshold ensures the detection algorithm operates in the presence of bit error rates of up to $10^{-3}$.  Each "valid" DS2 M-frame causes an integration counter to increment; "non-valid" DS2 M-frame intervals cause a decrement.  RED or AIS is declared if the associated integrator count saturates at 53, resulting in a detection time of 9.9 ms.  RED or AIS declaration is deasserted when the associated count decrements to 0.

The DS2 X-bit is extracted by the DS2 FRMR to provide an indication of far end receive failure.  The FERF status is set to the current X/RAI state only if  the two successive X/RAI bits were in the same state. The extracted FERF status is buffered for 6 DS2 M-frames before being reported within the DS2 FRMR Status register.  This buffer ensures a virtually 100% probability of freezing the FERF status in a valid state during an out of frame occurrence. When an OOF occurs, the FERF value is held at the state contained in the last buffer location corresponding to the previous sixth M-frame. This location is not updated until the OOF condition is deasserted.  Meanwhile, the last four of the remaining five buffer locations are loaded with the frozen FERF state while the first buffer location corresponding to the current M-frame is continually updated every M-frame based on the above FERF definition. Once correct frame alignment has been found and OOF is deasserted, the first buffer location will contain a valid FERF status and the remaining five buffer locations are enabled to be updated every M-frame.

DS2 M-bit and F-bit framing errors are indicated.  These error indications are accumulated for performance monitoring purposes in internal, microprocessor readable counters.  The performance monitoring accumulators continue to count error indications even while the framer is indicating OOF.

The DS2 FRMR may be configured to generate interrupts on error events or status changes.  All sources of interrupts can be masked or acknowledged via internal registers.  Internal registers are also used to configure the DS2 FRMR.

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## 9.15.11     M12 Multiplexer (MX12)

The M12 Multiplexer (MX12) integrates circuitry required to asynchronously multiplex and demultiplex four DS1 streams into, and out of, an M12 formatted DS2 serial stream as defined in ANSI T1.107 Section 7.  The M12 multiplexer also supports the ITU-T Rec. G.747 standard for the multiplexing of three 2048 kbit/s streams into a 6312 kbit/s stream.

When multiplexing four DS1 streams into an M12 formatted DS2 stream, the MX12 function performs logical inversion on the second and fourth tributary streams. Rate adaptation to the DS2 is performed by integral FIFO buffers, controlled by timing circuitry.  The FIFO buffers accommodate in excess of 5.0 UIpp of sinusoidal jitter on the DS1 clocks for all jitter frequencies.  X, F, M, and C bits are also generated and inserted by the timing circuitry. Software control is provided to transmit Far End Receive Failure (FERF) indications, DS2 AIS, and DS1 payload loopback requests. The loopback request is coded by inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7).Two diagnostic options are provided to invert the transmitted F or M bits.

When demultiplexing four DS1 streams from an M12 formatted DS2, the MX12 performs bit destuffing via interpretation of the C-bits.  The MX12 also detects and indicates DS1 payload loopback requests encoded in the C-bits.  As per ANSI T1.107 Section 7.2.1.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2.  Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported.  As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection.  Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS1 payload loopback can be activated or deactivated under software control. During payload loopback the DS1 stream being looped back still continues unaffected in the demultiplex direction.  The second and fourth demultiplexed DS1 streams are logically inverted. All four demultiplexed DS1 streams can be replaced with AIS on an individual basis or can be configured for automatic replacement with AIS on detection of out of frame or RED alarm conditions.

Similar functionality is supplied for supporting ITU-T Recommendation G.747. Software control is provided to transmit Remote Alarm Indication (RAI), 6312 kbit/s AIS, and the reserved bit.  A diagnostic option is provided to invert the transmitted frame alignment signal and parity bit.

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When demultiplexing three 2048 kbit/s streams from a G.747 formatted
6312 kbit/s stream, bit destuffing is performed via interpretation of the C-bits.
Tributary payload loopback can be activated or deactivated under software
control.  Although no remote loopback request has been defined for G.747,
inversion of the one of the C-bits, as selected by the Loopback Code Select
Register, triggers a loopback request detection indication in anticipation of
Recommendation G.747 refinement.  All three demultiplexed 2048 kbit/s streams
can be replaced with AIS on an individual basis.

### 9.15.12    E3 Framer

Three instances of the E3 Framer are independently programmed to frame to
34368 kbit/s frame formats.  From each, the framed data is presented on
RDATO[x] or mapped into the SBI bus.

The E3-FRMR searches for frame alignment in the incoming serial stream based
on either the G.751 or G.832 formats.  For the G.751 format, the E3-FRMR
expects to see the selected framing pattern error-free for three consecutive
frames before declaring frame alignment.  For the G.832 format, the E3-FRMR
expects to see the selected framing pattern error-free for two consecutive frames
before declaring frame alignment.  Once the frame alignment is established, the
incoming data is continuously monitored for framing bit errors and byte
interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and
processes them according to the framing format selected:

**In G.832 E3 format, the E3-FRMR extracts:**

- the Trail Trace bytes;

- the FERF bit and indicates an alarm when the FERF bit is a logic 1 for 3 or 5
  consecutive frames.  The FERF indication is removed when the FERF bit is a
  logic 0 for 3 or 5 consecutive frames;

- the FEBE bit for accumulation in PMON;

- the Payload Type bits and buffers them so that they can be read by the
  microprocessor;

- the Timing Marker bit and asserts the Timing Marker indication when the
  value of the extracted bit has been in the same state for 3 or 5 consecutive
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- the Network Operator byte for processing by the HDLC receiver when the RNETOP bit in the E3 Data Link Control register is logic 1;

- the General Purpose Communication Channel byte for processing by the HDLC receiver when the RNETOP bit in the E3 Data Link Control register is logic 0.

**In G.751 E3 mode, the E3-FRMR extracts:**

- the Remote Alarm Indication bit  (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic 1 for 3 or 5 consecutive frames.  Similarly, the Remote Alarm is removed when the RAI bit is logic 0 for 3 or 5 consecutive frames;

- the National Use reserved bit (bit 12 of the frame) for further processing in the HDLC receiver when the RNETOP bit in the E3 Data Link Control register is logic 0.  Optionally, an interrupt can be generated when the National Use bit changes state.

The E3-FRMR declares out of frame alignment if the framing pattern is in error for four consecutive frames.  The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment.  Once the framer has determined the new frame alignment, the out-of-frame indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than 5 zeros in a frame are detected while OOF in G.751 mode.  This algorithm provides a probability of detecting AIS within a single frame in the presence of a $10^{-3}$ BER as 92.9% in G.832 and  98.0% in G.751.  After five frames, the probability of detection rises to >99.999% for both formats.

Loss of signal is LOS is declared when no marks have been received for 32 consecutive bit periods.  Loss of signal is de-asserted after 32 bit periods during which there is no sequence of four consecutive zeros.

E3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms.  While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of

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Frame condition.  Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or AIS.  The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

### 9.15.13 E3 Transmitter

Three E3 transmitters provide framing insertion for 34368 kbit/s unchannelized data from TDATI[3:1] or the SBI bus.

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal.  The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats.  All overhead and status bits in each frame format can be individually controlled by register bits. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

**In G.832 E3 format, the E3-TRAN:**

- inserts the BIP-8 byte calculated over the preceding frame;

- inserts the Trail Trace bytes;

- inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared;

- inserts the FEBE bit, which is set to logic 1 when one or more BIP-8 errors are detected by the receive framer.  If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic 0;

- inserts the Payload Type bits based on the register value set by the microprocessor;

- inserts the Tributary Unit multiframe indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor;

- inserts the Timing Marker bit via a register bit;

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- inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the E3 Data Link Control register is logic 1; otherwise, the NR byte is set to all ones.  All 8 bits of the Network Operator byte are available for use as a datalink;

- inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the E3 Data Link Control register is logic 0; otherwise, the byte is set to all ones.

**In G.751 E3 mode, the E3-TRAN :**

- inserts the Remote Alarm Indication bit  (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF;

- inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the HDLC transmitter as configured by the TNETOP bit in the E3 Data Link Control register and the NATUSE bit in the E3 TRAN Configuration register;

- optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload for payload mappings that take advantage of the full bandwidth.

Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single line code violations for diagnostic purposes.

### 9.15.13.1    E3 Transmitter Timing Sources

E3 transmitter timing has three possible sources:

1. TICLK[3:1] input pins.  If the system interface is SBI, then TEMUX 84 is the SBI bus clock master, and uses the SAJUST_REQ output signal to issue timing justification requests to the link-layer device.  If the system interface is serial clock and data, TEMUX 84 derives TGAPCLK[3:1] from TICLK[3:1].)

2. Integral E3 clock synthesizer, which generates a gapped E3 clock from the CLK52M input pin, in response to SBI bus timing justification requests from the link-layer device.  TEMUX 84 is the SBI bus clock slave in this mode, and the SBI bus must be the system side option.  External jitter attenuation is recommended when using this E3 timing option.

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3.    Recovered E3 clock from the RCLK[3:1] input pins.  If the system interface is SBI, then TEMUX 84 is the SBI bus clock master, as in case 1 above.  If the system interface is serial clock and data, TEMUX 84 derives TGAPCLK[3:1] from the recovered E3 clock.)

In each case, the E3 transmitter drives the selected E3 clock source onto the TCLK output pins of the DS3/E3 line side interface.

### 9.15.14      E3 Trail Trace Buffer

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream.  The message is used by the OS (operating system) to prevent delivery of traffic from the wrong source and is 16 bytes in length.  The 16-byte message is framed by the PTI Multiframe Alignment Signal (TMFAS = 'b10000000 00000000).  One bit of the TMFAS is placed in the most significant bit of each message byte.  In the receive direction, the extracted message is stored in the internal RAM for review by an external microprocessor.  By default, the byte of a 16-byte message with its most significant bit set high will be written to the first location in the RAM.  The extracted trail trace message is checked for consistency between consecutive multiframes.  A message received unchanged three or five times (programmable) is accepted for comparison with the copy previously written into the internal RAM by the external microprocessor.  Alarms are raised to indicate reception of unstable and mismatched messages.  In the transmit direction, the trail trace message is sourced from the internal RAM for insertion into the TR byte by the E3-TRAN.

The Payload Type label carried in the MA byte of the G.832 E3 stream is also extracted.  The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source.  The Payload Type label is check for consistency between consecutive multiframes.  A Payload Type label received unchanged for five frames is accepted for comparison with the copy previously written into the TTB by the external microprocessor.  Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

## 9.16  Tributary Payload Processor (VTPP)

Each one of three tributary payload processors (VTPP) processes the virtual tributaries within an STS-1, AU3, or TUG3.  The VTPP can be configured to process either VT1.5s or VT2s within an STS-1 or either TU11s or TU12s within an AU3 or TUG3.  The number of tributaries managed by each VTPP ranges from 21 (when configured to process all VT2s or equivalently all TU12s) to 28 (when configured to process all VT1.5s or equivalently all TU11s).

The Tributary payload processor is used in both the ingress and egress data paths.  In the egress direction the pointer interpreter section of the VTPP can be bypassed on a per tributary basis to allow for pointer generator in the absence of valid pointers which is necessary when mapping floating transparent virtual tributaries from the SBI bus.

### 9.16.1 Incoming Multiframe Detector

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits.  If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift.  The primary process will enter out of multiframe state (OOM).  A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected.  Loss of multiframe (LOM) is declared after residing in the OOM state at the ninth H4 byte without re-alignment.  In counting to nine, the out of sequence H4 byte that triggered the transition to the OOM state is counted as the first.  A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected.  Changes in multiframe alignments are detected and reported.

### 9.16.2 Pointer Interpreter

The pointer interpreter is a time-sliced state machine that can process up to 28 independent tributaries.  The state vector is saved in RAM as directed by the incoming timing generator.  The pointer interpreter processes the incoming tributary pointers such that all bytes within the tributary synchronous payload envelope can be identified and written into the unique payload first-in first-out buffer for the tributary in question.  A marker that tags the V5 byte is passed through the payload buffer.  The incoming timing generator directs the pointer interpreter to the correct payload buffer for the tributary being processed.

The pointer interpreter processes the incoming pointers (V1/V2) as specified in the references.  The pointer value is used to determine the location of the tributary path overhead byte (V5) in the incoming TUG3 or STS-1 (AU3) stream.

### 9.16.3 Payload Buffer

The payload buffer is a bank of FIFO buffers.  It is synchronous in operation and is based on a time-sliced RAM.  The three 19.44 MHz clock cycles in each 6.48 MHz period are shared between the read and write operations.  The pointer interpreter writes tributary payload data and the V5 tag into the payload buffer.  A 16 byte FIFO buffer is provided for each of the (up to 28) tributaries.  Address

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information is also passed through the payload buffer to allow FIFO fill status to
be determined by the pointer generator.

### 9.16.4 Pointer Generator

1. The pointer generator block generates the tributary pointers (V1/V2) as
   specified in the references. The pointer value is used to determine the
   location of the tributary path overhead byte (V5) on the outgoing stream.

The pointer generator does not encode an H1/H2 value. The H1 and H2 byte
contents are only valid on the Telecom Add bus when the Egress VTPP is
bypassed.

The pointer generator is a time-sliced state machine that can process up to 28
independent tributaries. The state vector is saved in RAM at the address
associated with the current tributary. The pointer generator fills the outgoing
tributary synchronous payload envelopes with bytes read from the associated
FIFO in the payload buffer for the current tributary. The pointer generator creates
pointers in the V1-V3 bytes of the outgoing data stream. The marker that tags
the V5 byte that is passed through the payload buffer is used to align the pointer.
The outgoing timing generator directs the pointer generator to the FIFO in the
payload buffer that is associated with the tributary being processed. The pointer
generator monitors the fill levels of the payload buffers and inserts outgoing
pointer justifications as necessary to avoid FIFO spillage. Normally, the pointer
generator has a FIFO dead band of two bytes. The dead band can be collapse
to one so that any incoming pointer justifications will be reflected by a
corresponding outgoing justification with no attenuation. Signals are output by
the pointer generator that identify outgoing V5 bytes and the tributary
synchronous payload envelopes. On a per tributary basis, tributary path AIS and
tributary idle (unequipped) can be inserted as controlled by microprocessor
accessible registers. The idle code is selectable globally for the entire VC3 or
TUG3 to be all-zeros or all-ones. It is also possible to force an inverted new data
flag on individual tributaries for the purpose of diagnosing downstream pointer
processors. Tributary path AIS is automatically inserted into outgoing tributaries
if the pointer interpreter detects tributary path AIS on the corresponding incoming
tributary.

### 9.17 Receive Tributary Path Overhead Processor (RTOP)

Each one of three tributary path overhead processors (RTOP) monitors the
outgoing stream of the tributary payload processor (VTPP) and processes the
tributaries within an STS-1, AU3, or TUG3. The RTOP can be configured to
process all the VT1.5s or VT2s that can be carried in an STS-1 or all the TU11s

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or TU12s that can be carried in an AU3 or TUG3. The number of tributaries managed by each RTOP ranges from 21 (when configured to process all VT2s or all TU12s) to 28 (when configured to process all VT1.5s or all TU11s).

The RTOP provides tributary performance monitoring of incoming tributaries. Bit interleaved parity of the incoming tributaries is computed and compared with the BIP-2 code encoded in the V5 byte of the tributary. Errors between the computed and received values are accumulated. RTOP also accumulates far end block error codes. Incoming path signal label is debounced and compared with the provisioned value. Path signal label unstable, path signal label mismatch and change of path signal label event are identified.

### 9.17.1 Error Monitor

The error monitor block contains a set of 12-bit counters that are used to accumulate tributary path BIP-2 errors, and a set of 11-bit counters to accumulate far end block errors (FEBE). The contents of the counters may be transferred to a holding RAM, and the counters reset under microprocessor control.

Tributary path BIP-2 errors are detected by comparing the tributary path BIP-2 bits in the V5 byte extracted from the current multiframe, to the BIP-2 value computed for the previous multiframe. BIP-2 errors may be accumulated on a block or nibble basis as controlled by software configurable registers. Far end block errors (FEBEs) are detected by extracting the FEBE bit from the tributary path overhead byte (V5).

Tributary path remote defect indication (RDI) and remote failure indication (RFI) are detected by extracting bit 8 and bit 4 respectively of the tributary path overhead byte (V5). The RDI is recognized when bit 8 of the V5 byte is set high for five or ten consecutive multiframes while RFI is recognized when bit 4 of V5 is set high for five or ten consecutive frames. The RDI and RFI bits may be treated as a two-bit code word. A code change is only recognized when the code is unchanged for five or ten frames.

The tributary path signal label (PSL) found in the tributary path overhead byte (V5) is processed. An incoming PSL is accepted when it is received unchanged for five consecutive multiframes. The accepted PSL is compared with the associated provisioned value. The PSL match/mismatch state is determined by the following:

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**Table 2        - Path Signal Label Mismatch State**

| Expected PSL | Accepted PSL | PSLM State |
|:---:|:---:|:---:|
| 000 | 000 | Match |
| 000 | 001 | Mismatch |
| 000 | XXX $\neq$ 000 | Mismatch |
| 001 | 000 | Mismatch |
| 001 | 001 | Match |
| 001 | XXX $\neq$ 001 | Match |
| XXX $\neq$ 000, 001 | 000 | Mismatch |
| XXX $\neq$ 000, 001 | 001 | Match |
| XXX $\neq$ 000, 001 | XXX | Match |

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| Expected PSL | Accepted PSL | PSLM State |
|---|---|---|
| XXX $\neq$ 000, 001 | YYY | Mismatch |

Each time an incoming PSL differs from the one in the previous multiframe, the
PSL unstable counter is incremented.  Thus, a single bit error in the PSL in a
sequence of constant PSL values will cause the counter to increment twice, once
on the errored PSL and again on the first error-free PSL.  The incoming PSL is
considered unstable when the counter reaches five.  The counter is cleared when
the same PSL is received for five consecutive multiframes.

## 9.18  Receive Tributary Trace Buffer (RTTB)

When configured for SONET compatible operation, each one of three receive
tributary trace buffers (RTTB) processes the tributary trace message of all the
tributaries in an STS-1 stream.  Each of the seven tributary groups (VT groups)
may be independently configured to accept any of the four tributary types (VT1.5,
VT2, VT3, and VT6).  The RTTB extracts tributary trace message from each
tributary and stores it in one of a set of internal buffers.  The RTTB may be
configured for SDH compatible operation.  The incoming stream may carry an
AU3 of an STM1 stream or a TUG3 in an AU4 of an STM1 stream.

The tributary trace message of each tributary is extracted form the J2 (J1 in TU3
mode) byte.  It is written to the internal buffer corresponding to the tributary.  The
internal buffer may behave as a simple circular buffer, or optionally, be
synchronized to the framing pattern embedded in the message.  For a 16-byte
trail trace identifier, the first byte is identified by a logic one in the most significant
bit.  For a 64-byte tributary trace message, the last two bytes are set to the ASCII
characters for carriage-return (CR) and linefeed (LF).

An extracted message is declared the accepted message, if it is received
unchanged for 3 multiframes.  The accepted message is compared with the
locally provisioned expected message.  A tributary trace identifier mismatch
alarm (TIM) is asserted when the accepted and expected messages differ.
Conversely, TIM is negated when the messages are identical.  An interrupt is
optionally generated upon a change in the TIM state.  Messages of all-zeros
bytes cannot become accepted and, therefore, have no effect on the TIM state.

The RTTB also monitors for tributary trace unstable conditions.  Each time a
tributary trace message that is received differs from the previous message, the
unstable counter is incremented by one.  The tributary trace unstable alarm (TIU)
is asserted when the unstable counter reaches eight.  The unstable counter is

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cleared and the unstable alarm negated when the extracted message remains unchanged for enough multiframes to meet the acceptance criteria.  An interrupt is optionally generated upon a change in the TIU state.

## 9.19  Receive Tributary Bit Asynchronous Demapper (RTDM)

Each one of three Receive Tributary Demappers (RTDM) demaps up to 28 T1 or 21 E1 bit asynchronous mapped signals from an STS-1 SPE, TUG3 within a STM-1/VC4 or STM-1 VC3 payload. The bit asynchronous T1 mapping consists of 104 octets every 500 µs (2 KHz) and is shown in Table 3. The bit asynchronous E1 mapping consists of 140 octets every 500us and is shown in Table 4.

**Table 3          - Asynchronous T1 Tributary mapping**

| |
|---|
| V5 |
| RRRRRRIR |
| 24 bytes - 8I |
| J2 |
| $C_1C_2OOOOIR$ |
| 24 bytes - 8I |
| Z6 |
| $C_1C_2OOOOIR$ |
| 24 bytes - 8I |
| Z7 |
| $C_1C_2RRRS_1S_2R$ |
| 24 bytes - 8I |

R: Fixed Stuff bit - set to logic '0' or '1'

C: Stuff Control bit - set to logic '1' for stuff indication

S: Stuff Opportunity bit - when stuff control bit is '0', stuff opportunity is I bit

O: Overhead

I: T1 payload information

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### Table 4        - Asynchronous E1 Tributary Mapping

| |
|---|
| V5 |
| R |
| 32 bytes - 8I |
| R |
| J2 |
| $C_1C_2OOOORR$ |
| 32 bytes – 8I |
| R |
| Z6 |
| $C_1C_2OOOORR$ |
| 32 bytes – 8I |
| R |
| Z7 |
| $C_1C_2RRRRRS_1$ |
| $S_2I\ I\ I\ I\ I\ I\ I$ |
| 31 bytes – 8I |
| R |

R: Fixed Stuff bit - set to logic '0' or '1'

C: Stuff Control bit - set to logic '1' for stuff indication

S: Stuff Opportunity bit - when stuff control bit is '0', stuff opportunity is I bit

O: Overhead

I: E1 payload information

The RTDM buffers the tributary synchronous payload envelope bytes of the incoming tributaries in individual FIFOs to accommodate tributary pointer justifications.

The RTDM performs majority voting on the tributary stuff control (C1, C2) bits.  If the majority of each set of the stuff control bits indicate a stuff operation, then the associated stuff opportunity bit (S1, S2) will not carry T1 or E1 payload.

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Conversely, if the majority of the stuff control bits indicate a data operation, the appropriate stuff opportunity bit(s) will carry T1 or E1 payload.

The RTDM, in cooperation with the T1/E1 jitter attenuator, attenuates jitter introduced by pointer justification events. The T1/E1 jitter attenuator may be bypassed, in which case an external device may use the SBI Link Rate Octet generated by RTDM to determine the clock phase. When a pointer justification is detected, the RTDM issues evenly spaced 1/12 UI T1 adjustments or 1/9 UI E1 adjustments encoded in the SBI Link Rate Octet.

The RTDM optionally acts as a time switch. When time switching is enabled, the association of timeslots on the system interface (SBI or H-MVIP) to incoming tributaries is software configurable. There are two pages in the time switch configuration RAM. One page is software selectable to be the active page and the other the stand-by page. The configuration in the active page is used to switch incoming tributaries. The stand-by page can be programmed to the next switch configuration. Change of page selection is effected immediately. The one constraint on switch configuration is that the all the remapped tributaries in an SPE must be of the same type (T1 or E1). Also, if at least one tributary in a TUG3 or VC-3 is a byte synchronously demapped T1, no bit asynchronously demapped TU12 is allowed.

## 9.20  Receive Tributary Byte Synchronous Demapper

Each one of three Receive Tributary Byte Synchronous Demappers demaps up to 28 T1 or 21 E1 byte synchronous mapped signals from an STS-1 SPE, TUG3 within a STM-1/VC4 or STM-1 VC3 payload. The demapping is done in accordance with ITU-T Recommendation G.709 and ANSI T1.105. If byte synchronous tributaries are being demapped from a VC-3, the Ingress VTPP must not be bypassed and the OTUG3 bit of the SONET/SDH Master Ingress VTPP Configuration register must be logic 1.

Byte synchronous demapping is enabled on a per-tributary basis by setting the ENBL bit through the Byte Synchronous Demapping Tributary Control RAM Indirect Access Data register and by bypassing the receive jitter attenuator by setting the RJATBYP bit through the RJAT Indirect Channel Data register.

Given that frame alignment is provided by the mapping function, the T1/E1 framer doesn't provide the frame alignment for the system interface. If the tributary 'F' bit position contains valid framing information, the T1/E1 framer may be used for performance and alarm monitoring.

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Signaling, if present, may be dealt with in two ways for T1. By default, the T1 framer attempts to find frame and extracts the signaling from the robbed bit signaling positions. Alternately, the values encoded in the $S_1S_2S_3S_4$ bit positions are presented on the system interface verbatim without debounce or freezing if the RAWSIG bit programmed through the SIGX Indirect Channel Data registers is logic 1. This is programmed on a per-tributary basis. For E1, the signaling is extracted from "Multiframe alignment signal" byte.

## 9.21 DS3 Mapper Drop Side (D3MD)

Each one of three DS3 Mapper DROP Side (D3MD) blocks demaps a DS3 signal from an STS-1 (STM-0/AU3) payload. The demapped DS3 is presented to the DS3 framer and subsequently presented on RDAT[x]. Optionally, it is mapped into the SBI bus or demultiplexed into 28 DS1s or 21 E1s.

The DS3 Mappers do not support the mapping of DS3s into an AU4 via TUG-3s. Therefore, the Telecom Drop bus must be configured for AU-3s when demapping DS3s. For bit asynchronous E1/T1s to coexist with mapped DS3s, either the ING_TUG3 bits of the RTDM Indirect Ingress Tributary Data register must be logic 0 or the ITUG3 bit of the SONET/SDH Master Ingress VTPP Configuration must be logic 0 depending on whether the Ingress VTPP is bypassed. For byte synchronous E1/T1s to coexist with mapped DS3s, the Ingress VTPP cannot be bypassed.

The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. The asynchronous DS3 mapping is shown in Table 5.

**Table 5        - Asynchronous DS3 mapping to STS-1 (STM-0/AU3)**

| J1 | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|-----|--------|----------|---------|--------|----------|---------|--------|----------|---------|
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
| STS | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
| POH | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |
|     | 2 x 8R | RRCIIIII | 25 x 8I | 2 x 8R | CCRRRRRR | 26 x 8I | 2 x 8R | CCRROORS | 26 x 8I |

R: Fixed Stuff bit - set to logic '0' or '1'

C: Stuff Control bit - set to logic '1' for stuff indication

S: Stuff Opportunity bit - when stuff control bit is '0', stuff opportunity is I bit

O: Overhead communication channel

I: DS3 payload information

### 9.21.1 DS3 Demapper

The D3MD performs majority vote on the received C-bits. If 3 out of 5 C-bits are '1's, the associated S bit is interpreted as a stuff bit. If 3 out of 5 C-bits are '0's, the associated S bit is interpreted as an Information bit. The information bits are written to an elastic store and the Fixed Stuff bits (R) are ignored.

Given a path signal label mismatch (PSLM) or path signal label unstable (PSLU), the D3MD ignores the STS-1 (STM-0/AU3) SPE and writes a DS3 AIS pattern to the elastic store. In addition, the desynchronization algorithm assumes a nominal ratio of data to stuff bits carried in the S bits (1 out of 3 S bits is assumed to be an information (data) bit).  DS3 AIS is shown in Table 6.

**Table 6        - DS3 AIS format.**

| X (1) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X (1) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
| P (p) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
| P (p) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
| M (0) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
| M (1) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |
| M (0) | D | F (1) | D | C (0) | D | F (0) | D | C (0) | D | F (0) | D | C (0) | D | F (1) | D |

- valid M-frame alignment bits (M-bits), M-subframe alignment bits (F-bits), and parity bit of the preceding M-frame (P-bits). The two P-bits are identical, either both are zeros or ones.

- all the C-bits in the M-frame are set to zeros

- the X-bits are set to ones

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- the information bit (84 Data bits with repeating sequence of 1010..)

### 9.21.2 DS3 Demapper Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS-3 stream extracted from the STS-1 (STM-0/AU3) SPE and the CLK52M clock input.  The DS3 Demapper extracts I bits from the STS-1 (STM-0/AU3) SPE and writes the bits into a 128 bit (16 byte) elastic store.  Eight bytes are provided for SONET/SDH overhead (3 bytes for TOH, 1 byte for a positive stuff, 1 byte for POH) and DS3 reserve stuffing bits (2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte).  The remaining 8 bytes are provided for path pointer adjustments.

Data is read out of the Elastic Store using a divide by 8 version of the input CLK52M clock.  If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

### 9.21.3 DS3 Desynchronizer

The Desynchronizer monitors the Elastic Store level to control the de-stuffing algorithm to avoid overflow and underflow conditions.  The Desynchronizer assumes a 44.928 MHz clock (provided via input CLK52M).

When using the 44.928 MHz CLK52M clock, the DS3 clock is generated using a fixed 8 KHz interval.  The 8KHz interval is subdivided into 9 rows.  Each row contains either 621 or 622 clock periods.  The CLK52M contains 624 cycles per row.  To generate 621 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 207 clocks + 1 clock gap is used.  To generate 622 pulses, a gap pattern of 207 clocks + 1 clock gap + 207 clocks + 1 clock gap + 208 clocks  is used.

The resulting output DS3 clock requires an external DS3 jitter attenuator circuit if it is to be used as a DS3 reference clock to an external LIU or the PM73122 AAL1gator32 ATM SAR device.

Table 7 illustrates the gap patterns used to generate the desynchronized DS3 clock under the normal, DS3 AIS, faster and slower status.  The faster pattern is used to drain the elastic store to avoid overflows.  The slower pattern is used to allow the elastic store to fill to avoid underflows.

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**Table 7     - DS3 desynchronizer clock gapping algorithm.**

| Row Number | Normal or DS3 AIS | Run Faster | Run Slower |
|:----------:|:-----------------:|:----------:|:----------:|
| 1 | 621 | 621 | 621 |
| 2 | 621 | 621 | 621 |
| 3 | 622 | 622 | 622 |
| 4 | 621 | 621 | 621 |
| 5 | 621 | 622 | 621 |
| 6 | 622 | 622 | 621 |
| 7 | 621 | 621 | 621 |
| 8 | 621 | 622 | 621 |
| 9 | 622 | 622 | 621 |

## 9.22  Transmit Tributary Path Overhead Processor (TTOP)

Each one of three  Transmit Tributary Path Overhead Processors (TTOP)
generates the path overhead for up to 28 VT1.5/TU-11s or 21 VT2/TU-12s.

When configured for SONET compatible operation, the TTOP inserts the four
tributary path overhead bytes (V5, J2, Z6, and Z7) to each tributary.  The TTOP
may also be configured for SDH compatible operation.  The incoming STM-1
stream may carry three AU3s or an AU4 with three TUG3s.

The TTOP computes the BIP-2 code in the current tributary SPE and inserts the
result into the BIP-2 bits of the V5 byte in the next tributary SPE.  The tributary
path signal label in the V5 byte of each tributary can be sourced from internal
registers.  The tributary far end block error bit in the V5 byte of each tributary is
inserted based of the BIP error count detected at a companion RTOP block.  The
tributary remote failure indication and remote defect indication bits in the V5 or
the Z7 byte of each tributary is inserted based on the tributary alarm status of the
companion RTOP TSB.

The TTOP inserts the tributary trail trace identifier (TTI) into the J2 byte.  Each
tributary is provided with a 64-byte buffer to store the identifier.  To transmit a 16-
byte message, one must write four identical copies to the buffer.  One shadow
buffer is available for temporary replacement of a selected transmitted TTI while
the 64-byte identifier buffer is being updated. Data is retrieved sequentially from
the active buffer at each J2 byte position.  No CRC insertion is performed; any
CRC must be written into the trail trace buffer.  The shadow buffer can be

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programmed with new messages without timing constraints when inactive. An inactive 64-byte identifier buffer can also be programmed with new messages without timing constraints.  Programming for TTI buffers is done one buffer at a time by first programming the shadow buffer, switching to the shadow buffer for the desired tributary, updating the desired tributary identifier buffer and finally switching back from the shadow buffer to the tributary buffer. Switching between the shadow buffer and normal buffer is synchronized to the start of each identifier on a per-tributary basis.

## 9.23 Transmit Remote Alarm Processor (TRAP)

When configured for SONET compatible operation, each one of three TRAP SONET/SDH Transmit Remote Alarm Processors processes remote alarm indications of tributaries in an STS-3 stream. The virtual tributaries within an STS-1 stream may be configured to accept either VT1.5 or VT2 tributary types. The TRAP may also be configured for SDH compatible operation.  The incoming STM-1 stream may carry three AU3s or an AU4 with three TUG3s.

Two methods of encoding tributary remote alarms are supported, as selected on a per-tributary basis by the ERDI bits of the TRAP Control registers and TTOP Control registers.  If the ERDI bits for a tributary are logic 0, RDI-V is transmitted by setting bit 8 of the V5 byte to logic 1 and RFI-V is transmitted by setting bit 4 of the V5 byte to logic 1.  Bits 6 and 7 of the Z7 will be zeros.  If the ERDI bits for a tributary are logic 1, extended RDI is effected.  The triggers for ERDI-V are programmable, but the following is always true if ERDI is configured:

- bit 8 of the V5 byte equals bit 5 of the Z7 byte,

- bit 7 of the Z7 byte is always the complement of bit 6 of the Z7 byte, and

- if byte synchronous mapping is being used, bit 4 of V5 will equal the value programmed through the Byte Synchronous Mapping Tributary Control Indirect Access Data register; otherwise, it will be logic 0.

If the FORCEEN bit of the TRAP Control register is logic 1 then bit 8 of V5 (plus bit 5 of Z7 if ERDI) reflects the state of the RDI bit of the TRAP Control register and the ARDI bit of the TRAP Control register sets bit 6 of Z7 if ERDI.  If FORCEEN is logic 0, the source for RDI-V and RFI-V can be any one of the RADEAST input, the RADWEST input or Telecom Drop bus alarms.

The TRAP may be configured to insert tributary remote defect indications (RDI-V), tributary remote fault indications (RFI-V) and tributary remote error indications (REI-V) based on alarms detected in tributaries received on the Telecom Drop bus, LDDATA[7:0].  The contents of the SONET/SDH Master

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Tributary Remote Defect Indication Control register determine which alarms affect the state of bit 8 of V5 and (if ERDI is set) bit 5 of Z7. The contents of the SONET/SDH Master Tributary Auxiliary Remote Defect Indication Control register determine which alarms affect the state of bit 6 of Z7 if ERDI is set.

Alternatively, the TRAP may also be configured to extract RDI-V, RFI-V and REI-V from two independent serial remote alarm ports, RADEAST and RADWEST.

In all cases, the RDI-V and RFI-V state will be sent for a minimum of 10 multiframes before changing, unless a higher priority alarm is required.

The TRAP provides selection between the Telecom Drop bus alarms and the two remote serial alarm ports for the source of remote alarm status on a per-tributary basis. By default, all three sources are disabled. Tributaries in any of the three sources of remote alarms can be mapped to arbitrary tributaries in the outgoing data stream. The mapping is configured through the TRAP Indirect Remote Alarm Page Address, TRAP Indirect Remote Alarm Tributary Address and TRAP Indirect Datapath Tributary Data registers. A valid TU designation written via the TRAP Indirect Datapath Tributary Data register is all that is required to enable the alarms for the outgoing tributary specified by the TRAP Indirect Remote Alarm Tributary Address register. Although it is possible to have any subset of the three sources enabled, it is usual to have only one of the three sources enabled for a particular tributary.

## 9.24 Transmit Tributary Bit Asynchronous Mapper (TTMP)

Each one of three Transmit Tributary Mapper blocks bit asynchronously maps up to 28 T1 or 21 E1 streams into an STS-1 SPE, TUG3 in a STM-1/VC4 or STM-1/VC3 payload. The TTMP compensates for any frequency differences between the incoming individual serial bit rates and the available STS-1 or STM-1/VC3 payload capacity. The asynchronous T1 mapping consists of 104 octets every 500 µs (2 KHz). The asynchronous E1 mapping consists of 140 octets every 500 µs (2 KHz). Refer to the RTDM block for a description of the asynchronous T1 and E1 mappings.

The tributary mapper is a time-sliced state machine which uses a payload buffer as an elastic store. The T1 or E1 streams are read from the payload buffer, and mapped into VT1.5 Payloads and VT2 Payloads using bit asynchronous mapping only.

The Tributary Mapper compensates for phase and frequency offsets using bit stuffing. A jitter-reducing control loop is used to monitor the Payload Buffer depth and reduce mapping jitter to 1.0 UI. To reduce mapping jitter even further, a

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dither technique is inserted between the control loop and the stuff bit generator resulting in an acceptable desynchronizer mapping jitter of about 0.3 UI.

The Tributary Mapper may optionally act as a time switch.  When Time Switch Enable is active, the association of Tributary Mapper VT Payloads to logical FIFO data streams is software configurable.  There are two pages in the time switch configuration RAM.  One page is software selectable to be the active page and the other the stand-by page.  The configuration in the active page is used to associate outgoing VT Payloads to logical FIFOs.  The stand-by page can be programmed to the next switch configuration.  Change of page selection is synchronized to incoming stream frame boundaries.  When Time Switch Enable is inactive, the association of outgoing VT Payloads to logical FIFOs is fixed.

The TTMP outputs the STS-1, TUG3 in a STM-1/VC4 or STM-1/VC3 with the bit asynchronous mapped T1s or E1s onto an internal bus for further processing by the Transmit Tributary Payload Processor block.

## 9.25  Transmit Tributary Byte Synchronous Mapper

Each one of three Transmit Tributary Mapper blocks byte synchronously maps up to 28 T1 or 21 E1 streams into an STS-1 SPE, TUG3 in a STM-1/VC4 or STM-1/VC3 payload.  The mapping is done inaccordance with ITU-T Recommendation G.709 and ANSI T1.105.  If byte synchronous tributaries are being mapped into a VC-3, the Egress VTPP must not be bypassed and the ITUG3 bit of the SONET/SDH Master Egress VTPP Configuration register must be logic 1.

Byte synchronous mapping is enabled on a per-tributary basis by setting the ENBL bit through the Byte Synchronous Mapping Tributary Control RAM Indirect Access Data register, by bypassing the transmit jitter attenuator by setting the TJATBYP bit through theTJAT Indirect Channel Data register and by disabling the egress VTPP pointer interpretation via the EPTRBYP or ETVTPTRDIS bits.

By default the T1/E1 framer inserts valid framing into the T1 'F' bit and E1 TS0.

The T1 signaling received from the system interface is encoded into the $S_1S_2S_3S_4$ bit positions.  Signaling is also inserted into the robbed bit signaling positions as enabled by the SIGC bits programmed through the TPCC Indirect Channel Data registers.  For E1, the signaling insertion is independent of the mapping.

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### 9.25.1 Jitter

The byte synchronous mapping protocol does not provide the capability to perform individual bit stuffs; rate adaptation is achieved through VT pointer justifications. A pointer justification introduces 8 UI of jitter. No special techniques are employed to shape the frequency spectrum of this jitter.

To avoid introducing jitter, it is recommended that one avoid VT pointer justifications. If transmit timing is derived from the SBI Add bus data rate, SBI bus pointer movements should be avoided. If transmit timing is locked to CTCLK, then CTCLK should be locked to SREFCLK.

### 9.26 DS3 Mapper ADD Side (D3MA)

Each one of three DS3 Mapper ADD Side (D3MA) blocks maps a DS3 signal into an STS-1 (STM-0/AU3) payload and compensate for any frequency differences between the incoming DS3 serial bit rate (TICLK) and the available STS-1 (STM-0/AU3) SPE mapped payload capacity. The asynchronous DS3 mapping consists of 9 rows every 125 µs (8 KHz). Each row contains 621 information bits, 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. Fixed stuff bytes are used to fill the remaining bytes. Please refer to section 9.21 for a description of the DS3 mapping.

The DS3 Mappers do not support the mapping of DS3s into an AU4 via TUG-3s. Therefore, the Telecom Add bus must be configured for AU-3s when demapping DS3s. For bit asynchronous E1/T1s to coexist with mapped DS3s, either the EGR_TUG3 bits of the TTMP Indirect Egress Tributary Address register must be logic 0 or the OTUG3 bit of the SONET/SDH Master Egress VTPP Configuration must be logic 0 depending on whether the Egress VTPP is bypassed. For byte synchronous E1/T1s to coexist with mapped DS3s, the Egress VTPP cannot be bypassed.

### 9.26.1 DS3 Mapper Serializer

High speed serial data from the DS3-TRAN block is deserialized and written into the Elastic Store.

### 9.26.2 DS3 Mapper Elastic Store

The elastic store block is provided to compensate for frequency differences between the DS3 stream from the DS3-TRAN block and the STS-1 (STM-0/AU3) SPE capacity. The DS3 Serializer writes data into the elastic store at the

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TICLK/8 rate while data is read out at the stuffed STS-1 (STM-0/AU3) byte rate. If an overflow or underflow condition occurs, an interrupt is optionally asserted and the Elastic Store read and write address are reset to the startup values (logically 180 degrees apart).

The Elastic store is 128 bits (16 bytes) to allow for a fixed read/write pointer lag of 7 bytes (3 bytes for TOH, 1 byte for POH, 2 bytes for R bits, and 3 overhead bits which is rounded-up to 1 byte).  Four bytes are also added on either side for positive and negative threshold detection.

### 9.26.3 DS3 Synchronizer

The DS3 Synchronizer performs the mapping of the DS3 into the STS-1 (STM-0/AU3) SPE.  The DS3 Synchronizer monitors the Elastic Store level to control the stuffing algorithm to avoid overflow (i.e. run faster)  and underflow (i.e. run slower) conditions.  The fill level of the elastic store is monitored and stuff opportunities in the DS3 mapping are used to center the Elastic Store.  To consume a stuff opportunity, the five C-bits on a row are set to ones and the S bit is used to carry an DS3 information bit.  When the S bit is not used to carry information, the C-bits on the row are set to zeros.

The DS3 synchronizer uses a fixed bit leaking algorithm which leaks 8 bits of phase buildup in 500 µs. The 8 kHz STS-1 (STM-0/AU3) frame interval is subdivided into 9 rows. Each row contains one stuff opportunity. Table 8 illustrates the stuffing implementation where S means stuff bit and I means an information bit (DS3 data).

**Table 8        - DS3 synchronizer bit stuffing algorithm.**

| Row Number | Normal or DS3 AIS | Run Faster | Run Slower |
|:----------:|:-----------------:|:----------:|:----------:|
| 1 | S | S | S |
| 2 | S | S | S |
| 3 | I | I | I |
| 4 | S | S | S |
| 5 | S | I | S |
| 6 | I | I | S |
| 7 | S | S | S |
| 8 | S | I | S |
| 9 | I | I | S |

Under microprocessor control, the incoming DS3 stream can be overwritten with the framed DS3 AIS.  When asserting DS3 AIS, a nominal stuff pattern is used as illustrated above.  Please refer to the D3MD functional description section for a description of the DS3 AIS frame.

The D3MA outputs the STS-1 (STM-0/AU3) with the mapped DS3 onto the Line Add bus, LADATA[7:0].

## 9.27  Egress H-MVIP System Interface

The Egress H-MVIP System Interface (Figure 18) provides system side H-MVIP access for up to 84 T1 or 63 E1 transmit streams.  There are three separate interfaces for data, CAS signaling and CCS signaling.  The H-MVIP signaling interfaces can be used in combination with the SBI interface in certain applications.  Control of the system side interface is global to TEMUX 84 and is selected through the SYSOPT[1:0] bits in the Global Configuration register.  The system interface options are H-MVIP, SBI bus and SBI bus with CAS or CCS H-MVIP.

### Figure 18      - Egress Clock Slave      - H-MVIP
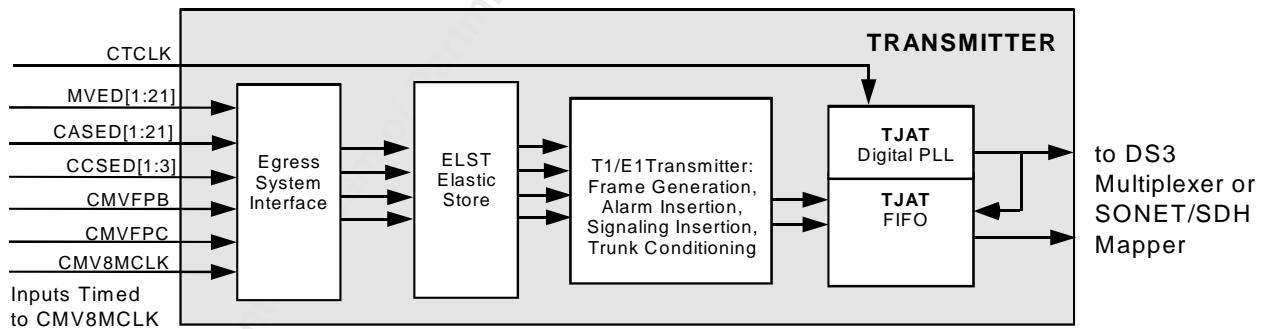


When Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP egress interface multiplexes up to 2016 channels from 84 T1s or 63 E1s, up to 2016 channel associated signaling (CAS) channels from 84 T1s or 63 E1s and common channel signaling from up to 84 T1s or 63 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Twenty-one H-MVIP data signals, MVED[1:21], share pins with the SBI inputs to provide H-MVIP access for up to 2016 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192 Mbit/s H-MVIP signal.  This mode is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to H-MVIP.

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The option exists to transmit at a rate locked to the CTCLK input, to a selected recovered clock or to be looped timed. Regardless of transmit timing source, the transmit elastic store can not be bypassed. To avoid controlled frame slips, the source of the transmit timing needs to be traceable to the source of the CMV8MCLK input.

A separate twenty-one signal H-MVIP interface is for access to the channel associated signaling for 2016 channels. The CAS H-MVIP interface is time division multiplexed exactly the same way as the data channels. The CAS H-MVIP is synchronized with the H-MVIP data channels when SYSOPT[1:0] is set to H-MVIP mode. Over a T1 or E1 multi-frame, the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte. Optionally, the third and fourth bit of each byte may be used as inband control of whether CAS signalling is inserted or whether the timeslot is 64 kbit/s clear channel.

The CAS H-MVIP interface can be used in parallel with the SBI Add bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to "SBI Interface with CAS or CCS H-MVIP Interface".

A separate H-MVIP interface consisting of three signals is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSED[1:3], is not multiplexed with any other pins. CCSED[1:3] can be used in parallel with the Clock Slave:H-MVIP mode when SYSOPT[1:0] is set to "H-MVIP Interface" or in parallel with the SBI Add bus when SYSOPT[1:0] is set to "SBI Interface with CAS or CCS H-MVIP Interface". The TS16 CCS and V5 channels for E1 tributaries and channel 24 CCS for T1 tributaries can be enabled when the CCS16EN, CCS15EN, CCS31EN and/or CCSEN context bits are set to logic 1 through the T1/E1 Transmitter Indirect Channel Data Registers.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a transmit signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

## 9.28  Ingress System H-MVIP Interface

The Ingress System Interface (Figure 19) provides H-MVIP access for up to 84 T1 or 63 E1 receive streams. When enabled for 8.192 Mbit/s H-MVIP there are three separate interfaces for data and signaling. The H-MVIP signaling interfaces can be used in combination with the SBI interface in certain applications. Control

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of the system side interface is global to TEMUX 84 and is selected through the SYSOPT[1:0] bits in the Global Configuration register at address 0x0002. The system interface options are  H-MVIP, SBI bus and SBI bus with CAS or CCS H-MVIP.  The ingress H-MVIP interface is always a clock slave.

**Figure 19     - Ingress Clock Slave     - H-MVIP**
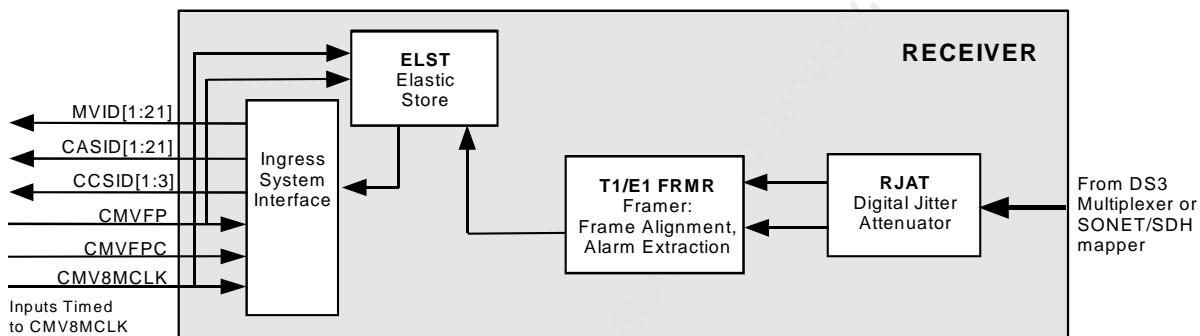


When Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP ingress interface multiplexes up to 2016 channels from 84 T1s or 63 E1s, up to 2016 channel associated signaling (CAS) channels from 84 T1s or 63 E1s and common channel signaling (CCS) from up to 84 T1s or 63 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

The three ingress H-MVIP interfaces operate independently except that using any one of these forces the T1 or E1 framer to operate in synchronous mode, meaning that elastic stores are used.

Twenty-one H-MVIP data signals, MVID[1:21] provide H-MVIP access for up to 2016 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192 Mbit/s H-MVIP signal.  This mode is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to H-MVIP.

A separate H-MVIP interface consisting of twenty-one pins is for access to the channel associated signaling for all of the 2016 data channels. The CAS is time division multiplexed exactly the same way as the data channels and is synchronized with the H-MVIP data channels. Over a T1 or E1 multi-frame, the four CAS bits per channel are repeated with each data byte.

The CAS H-MVIP interface can be used in parallel with the SBI Drop bus as an alternative method for accessing the CAS bits while data transfer occurs over the

SBI bus. This is selected when the SYSOPT[1:0] bits in the Global Configuration register are set to "SBI Interface with CAS or CCS H-MVIP Interface".

A separate H-MVIP interface consisting of three signals is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSID[1:3], is not multiplexed with any other pins.   The CCSID[1:3] outputs is always available provided CMV8MCLK, CMVFPB and CMVFPC are active.The TS0ID output provides the contents of E1 TS0.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a receive signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

## 9.29  Extract Scaleable Bandwidth Interconnect (EXSBI)

The Extract Scaleable Bandwidth Interconnect block demaps up to 84 1.544 Mbit/s links, 63 2.048 Mbit/s links, three 44.736 Mbit/s links, three 34.386 Mbit/s links or an arbitrary bit rate from the SBI shared bus.  The SBI bandwidth is evenly divided into three SPEs, each of which may carry a different payload type.  The 1.544 Mbit/s links can be unframed or they can be T1 framed and channelized for insertion into the DS3 multiplex or SONET/SDH mapping. The 2.048 Mbit/s links can be unframed or they can be E1 framed and channelized for insertion into the SONET/SDH mapping or G.747 multiplexer. The 44.736 Mbit/s links can also be unframed for mapping into SONET/SDH. The 44.736 Mbit/s links and 34.368 Mbit/s links can be DS3/E3 unchannelized when the TEMUX 84 is used as a DS3/E3 framer.  Finally, an arbitrary bandwidth signal may be carried for presentation on the Flexible Bandwidth Port.  The SBI Bus Data Formats section provides the details of the mapping formats.

All egress links extracted from the SBI bus can be timed from the source or from the TEMUX 84.  When timing is from the source, the 1.544 Mbit/s, 2.048 Mbit/s, 34.368 Mbit/s or 44.736 Mbit/s internal clocks are slaved to the arrival rate of the data.  For 34.368 Mbit/s or 44.736 Mbit/s data streams there is also the option of using timing link rate adjustments provided from the source and carried with the links over the SBI bus.   A T1/E1 tributary may be transmitted at a rate different from that of the SBI bus if the tributary is looped timed, locked to the CTCLK input or locked to a selected recovered clock.  In this case, the frame slip buffer (ELST) must be used to adapt the data rate.

The 44.736 Mbit/s or 34.368 Mbit/s clock is synthesized from the 51.84 MHz or 44.928 MHz reference clock, CLK52M.  Using either reference clock frequency, the 44.736 Mbit/s or 34.368 Mbit/s rate is generated by gapping the reference

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clock in a fixed way.  Timing adjustments are performed by adding or deleting four clocks over the 500 μS period.

When the TEMUX 84 is the SBI egress clock master for a link, clocks are sourced from within the TEMUX 84.  The data rate is set by the frequency of the CTCLK input, one of the three recovered clocks (RECVCLK1, RECVCLK2, or RECVCLK3) or the tributary receive clock if loop timed.  Based on buffer fill levels, the EXSBI sends link rate adjustment commands to the link source indicating that it should send one additional or one fewer bytes of data during the next 500 μS interval. Failure of the source to respond to these commands will ultimately result in overflows or underflows which can be configured to generate per link interrupts.

Channelized T1s extracted from the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s.

## 9.30  Insert Scaleable Bandwidth Interconnect (INSBI)

The Insert Scaleable Bandwidth Interconnect block maps up to 84 1.544 Mbit/s links, 63 2.048 Mbit/s links, three 44.736 Mbit/s links, three 34.386 Mbit/s links or an arbitrary bit rate into the SBI shared bus.  The SBI bandwidth is evenly divided into three SPEs, each of which may carry a different payload type.  The 1.544 Mbit/s links can be unframed when sourced directly from the DS3 multiplexer or SONET/SDH mapper, or they can be T1 channelized when sourced by the T1 framers. The 2.048 Mbit/s links can be unframed when sourced directly from the SONET/SDH mapper or G.747 demultiplexer, or they can be E1 channelized when sourced by the E1 framers. The 44.736 Mbit/s links and 34.368 Mbit/s links can also be unframed when sourced directly from the DS3/E3 interfaces or from the DS3 mapper.  The 44.736 Mbit/s links and 34.368 Mbit/s links can be unchannelized DS3/E3s when sourced from the DS3 or E3 framers.  Finally, an arbitrary bandwidth signal that has been received Flexible Bandwidth Port may be output.  The SBI Bus Data Formats section provides the details of the mapping formats.

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**Figure 20     - Insert SBI**
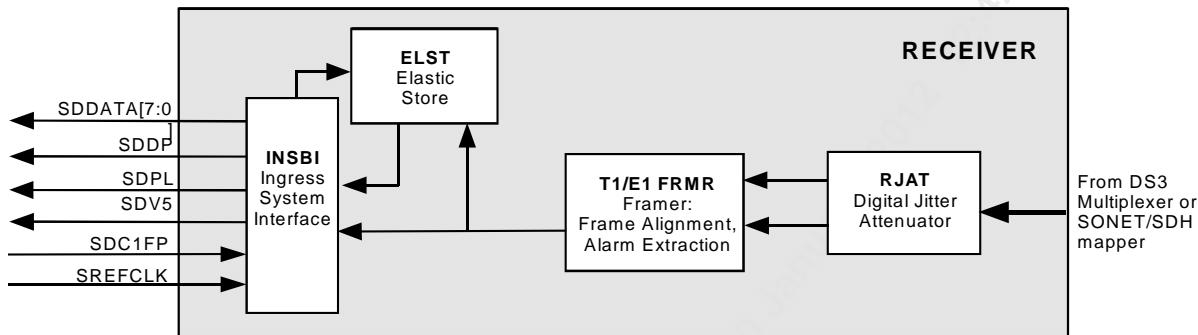


Links inserted into the SBI bus can be synchronous to the SBI bus (by setting SYNCH_TRIB=1 in the INSBI Control RAM) or timed from the upstream data source via the sonet/sdh mapper, M13, or DS3/E3 framer.   When SYNCH_TRIB is logic 0, the INSBI makes link rate adjustments by adding or deleting an extra byte of data over a 500 $\mu$S interval based on buffer fill levels.  Timing adjustments are detected by the receiving SBI interface by explicit signals in the SBI bus structure.  When SYNCH_TRIB is logic 1, the tributary is  "locked" in which no timing adjustments are allowed.  The frame slip buffer (ELST) must be in the datapath in "locked" mode.

The INSBI always sends valid link rate information across the SBI Drop bus, which contains both ClkRate(1:0) and Phase(3:0) field information. this gives an external device receiving data from the INSBI three methods of creating a recovered link clock: the ClkRate field, the Phase field, or just the rate of data flow across the SBI drop bus. INSBI does not generate the Phase field for DS3/E3 tribs.

Channelized T1s inserted into the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s or timeslots.

## 9.31  Flexible Bandwidth Ports

Three Flexible Bandwidth Ports are provided to supply arbitrary bandwidth signals to the SBI bus.  Each port is associated with one SPE on the SBI bus and may carry up to the capacity of the SPE (48.96 Mbit/s).

In the ingress direction, data is presented as a three wire interface: a clock of up to 51.84 MHz, bit serial data and an enable.  No flow control is provided, so the average data rate must be less than 48.96 Mbit/s.

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In the egress direction, a simple handshake controls the data flow.  For each cycle that the EFBWDREQ[n] input is high, a bit may be output on the EFBWDAT[n] output.  The data is supplied from the SBI bus FIFO, which will be kept half full through the SAJUST_REQ asserts as required.

### 9.31.1 Burst Lengths on Ingress Flexible Bandwidth Port

The SBI bus is capable of transporting flexible bandwidth data up to 48.96 Mbit/s. The SBI interface contains a FIFO for absorbing data bursts in excess of this rate, but there is a limit to the length of the bursts.  The limitations are dependent on the IFBWCLK frequency:

1.  IFBWCLK < 48.96 MHz: IFBWEN may be high indefinitely.

2.  IFBWCLK > 51.5 MHz: IFBWEN may only be high for up to eight consecutive cycles.  The DS3 demapper satisfies this constraint when configured to use a 51.84 MHz clock.

3.  48.96 MHz < IFBWCLK < 51.5MHz: The length of the burst is dependent on how much the IFBWCLK frequency exceeds 48.96 MHz, but 256 bits can be buffered before an overflow occurs.

### 9.32  JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan.  The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.  The TEMUX 84 identification code is 183160CD hexadecimal.

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## 9.33 <u>Microprocessor Interface</u>

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the TEMUX 84.

The Register Memory Map in Table 9 shows where the normal mode registers are accessed. The resulting register organization splits into sections: Master configuration registers, T1/E1 Framer registers, DS3 M13 multiplexing registers, SONET/SDH mapping registers and SBI registers.

On power up reset the TEMUX 84 defaults to 84 T1 framers multiplexed into the three M13 multiplexers using the DS3 M23 multiplex format. For proper operation some register configuration is necessary. System side access defaults to the SBI bus without any tributaries enabled which will leave the SBI Drop bus tristated. By default interrupts will not be enabled, automatic alarm generation is disabled, a dual rail DS3 LIU interface is expected and an external transmit reference clock is required.

**Table 9          - Register Memory Map**

| Address | Register |
|---------|----------|
| 0x0000 | Revision |
| 0x0001 | Global Reset |
| 0x0002 | Global Configuration |
| 0x0003 | SPE #1 Configuration |
| 0x0004 | SPE #2 Configuration |
| 0x0005 | SPE #3 Configuration |
| 0x0006 | Bus Configuration |
| 0x0007 | Global Performance Monitor Update |
| 0x0008 | Reference Clock Select |
| 0x0009 | Recovered Clock#1 Select |
| 0x000A | Recovered Clock#2 Select |
| 0x000B | Recovered Clock#3 Select |

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| Address | Register |
|---------|----------|
| 0x000C | Master H-MVIP Interface Configuration |
| 0x000D | Master Clock Monitor #1 |
| 0x0010 | Master Interrupt Source |
| 0x0011 | Master Interrupt Source T1E1 |
| 0x0012 | Master Interrupt Source SDH #1 |
| 0x0013 | Master Interrupt Source SDH #2 |
| 0x0014 | Master Interrupt Source SDH #3 |
| 0x0015 | Master Interrupt Source SBI |
| 0x0016 | Master Interrupt Source DS3/E3 #1 |
| 0x0017 | Master Interrupt Source DS2 #1 |
| 0x0018 | Master Interrupt Source MX12 #1 |
| 0x0019 | Master Interrupt Source DS3/E3 #2 |
| 0x001A | Master Interrupt Source DS2 #2 |
| 0x001B | Master Interrupt Source MX12 #2 |
| 0x001C | Master Interrupt Source DS3/E3 #3 |
| 0x001D | Master Interrupt Source DS2 #3 |
| 0x001E | Master Interrupt Source MX12 #3 |
| 0x0020 | Master SBIDET0 Collision Detect LSB |
| 0x0021 | Master SBIDET0 Collision Detect MSB |
| 0x0022 | Master SBIDET1 Collision Detect LSB |
| 0x0023 | Master SBIDET1 Collision Detect MSB |
| 0x0040 | T1/E1 Master Configuration |
| 0x0042 | T1/E1 PRGD #1 Tributary Select |
| 0x0043 | T1/E1 PRGD #2 Tributary Select |
| 0x0044 | T1/E1 PRGD #3 Tributary Select |
| 0x0045 | T1/E1 PRGD #4 Tributary Select |
| 0x0046 | T1/E1 PRGD #5 Tributary Select |

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| Address | Register |
|---------|----------|
| 0x0047 | T1/E1 PRGD #6 Tributary Select |
| 0x0048 | RJAT Indirect Status |
| 0x0049 | RJAT Indirect Channel Address Register |
| 0x004A | RJAT Indirect Channel Data Register |
| 0x004B | RJAT Programmable Corner Frequency Register |
| 0x004C | TJAT Indirect Status |
| 0x004D | TJAT Indirect Channel Address Register |
| 0x004E | TJAT Indirect Channel Data Register |
| 0x004F | TJAT Programmable Corner Frequency Register |
| 0x0050 | RPCC-MVIP Indirect Status/Time-slot Address |
| 0x0051 | RPCC-MVIP Indirect Channel Address Register |
| 0x0052-0x0056 | RPCC-MVIP Indirect Channel Data Registers |
| 0x0057 | RPCC-MVIP Configuration Bits |
| 0x0058 - 0x0062 | RPCC-MVIP Interrupt Status |
| 0x0063 | RPCC-MVIP PRBS Error Insertion |
| 0x0064 | RPCC-MVIP PRBS Error Insert Status |
| 0x0068 | RPCC-SBI Indirect Status/Time-slot Address |
| 0x0069 | RPCC-SBI Indirect Channel Address Register |
| 0x006A-0x006E | RPCC-SBI Indirect Channel Data Registers |
| 0x006F | RPCC-SBI Configuration Bits |
| 0x0070 - 0x007A | RPCC-SBI Interrupt Status |
| 0x007B | RPCC-SBI PRBS Error Insertion |
| 0x007C | RPCC-SBI PRBS Error Insert Status |
| 0x0083 | RX-MVIP-ELST Idle Code |
| 0x0084 - 0x008E | RX-MVIP-ELST Slip Status |
| 0x008F - 0x0099 | RX-MVIP-ELST Slip Direction |
| 0x009A | RX-MVIP-ELST Slip Interrupt Enable |

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| Address | Register |
|---|---|
| 0x00A0 | RX-SBI-ELST Indirect Status |
| 0x00A1 | RX-SBI-ELST Indirect Channel Address Register |
| 0x00A2 | RX-SBI-ELST Indirect Channel Data Register |
| 0x00A3 | RX-SBI-ELST Idle Code |
| 0x00A4 - 0x00AE | RX-SBI-ELST Slip Status |
| 0x00AF - 0x00B9 | RX-SBI-ELST Slip Direction |
| 0x00BA | RX-SBI-ELST Slip Interrupt Enable |
| 0x00C0 | TX-ELST Indirect Status |
| 0x00C1 | TX-ELST Indirect Channel Address Register |
| 0x00C2 | TX-ELST Indirect Channel Data Register |
| 0x00C4 - 0x00CE | TX-ELST Slip Status |
| 0x00CF - 0x00D9 | TX-ELST Slip Direction |
| 0x0DA | TX-ELST Slip Interrupt Enable |
| 0x0100 | TPCC Indirect Status/Time-slot Address |
| 0x0101 | TPCC Indirect Channel Address Register |
| 0x0102-0x0106 | TPCC Indirect Channel Data Registers |
| 0x0107 | TPCC Configuration |
| 0x0108 - 0x0112 | TPCC Interrupt Status |
| 0x0113 | TPCC PRBS Error Insertion |
| 0x0114 | TPCC PRBS Error Insert Status |
| 0x0118 | RHDL Indirect Status |
| 0x0119 | RHDL Indirect Channel Address Register |
| 0x011A - 0x011D | RHDL Indirect Channel Data Registers |
| 0x011E | RHDL Interrupt Control |
| 0x011F - 0x0129 | RHDL Interrupt Status |
| 0x0130 | THDL Indirect Status |
| 0x0131 | THDL Indirect Channel Address Register |

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| Address | Register |
|---------|----------|
| 0x0132 - 0x0136 | THDL Indirect Channel Data Registers |
| 0x0137 - 0x0141 | THDL Interrupt Status |
| 0x0150 | SIGX Indirect Status/Time-slot Address |
| 0x0151 | SIGX Indirect Channel Address Register |
| 0x0152 - 0x0156 | SIGX Indirect Channel Data Registers |
| 0x0157 | SIGX Configuration |
| 0x0158 - 0x0162 | Change of Signaling Status |
| 0x0163 | Change of Signaling Status Interrupt Enable |
| 0x0168 | T1/E1 Transmitter Indirect Status |
| 0x0169 | T1/E1 Transmitter Indirect Channel Address |
| 0x016A - 0x016F | T1/E1 Transmitter Indirect Channel Data Registers |
| 0x0170 | T1/E1 Framer Indirect Status |
| 0x0171 | T1/E1 Framer Indirect Channel Address Register |
| 0x0172 - 0x0186 | T1/E1 Framer Indirect Channel Data Registers |
| 0x0187 | T1/E1 Framer Configuration and Status |
| 0x0188 - 0x0192 | T1/E1 Framer Interrupt Status |
| 0x01C0 | SBI Master Reset / Bus Signal Monitor |
| 0x01C1 | SBI Master Configuration |
| 0x01C2 | SBI Bus Master Configuration |
| 0x01C4 | DLL Configuration (SBI Bus) |
| 0x01C6 | DLL Delay Tap Status (SBI Bus) |
| 0x01C7 | DLL Control Status (SBI Bus) |
| 0x01D0 | EXSBI Control |
| 0x01D1 | EXSBI FIFO Underrun Interrupt Status |
| 0x01D2 | EXSBI FIFO Overrun Interrupt Status |
| 0x01D3 | EXSBI Tributary RAM Indirect Access Address |
| 0x01D4 | EXSBI Tributary RAM Indirect Access Control |

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INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---------|----------|
| 0x01D6 | EXSBI Tributary Control Indirect Access Data |
| 0x01D7 | EXSBI SBI Parity Error Interrupt Status |
| 0x01D8 | EXSBI MIN_DEPTH for T1 and E1 Register |
| 0x01D9 | EXSBI MIN_DEPTH for DS3 and E3 Register |
| 0x01DA | EXSBI T1 Threshold Register |
| 0x01DB | EXSBI E1 Threshold Register |
| 0x01DC | EXSBI DS3 Threshold Register |
| 0x01DD | EXSBI E3 Threshold Register |
| 0x01DE | EXSBI Depth Check Interrupt Status |
| 0x01DF | Extract External ReSynch Interrupt Status |
| 0x01E0 | INSBI Control |
| 0x01E1 | INSBI FIFO Underrun Interrupt Status |
| 0x01E2 | INSBI FIFO Overrun Interrupt Status |
| 0x01E3 | INSBI Tributary Indirect Access Address |
| 0x01E4 | INSBI Tributary Indirect Access Control |
| 0x01E6 | INSBI Tributary Control Indirect Access Data |
| 0x01E7 | INSBI MIN_DEPTH for T1 and E1 Register |
| 0x01E9 | INSBI T1 Thresholds Register |
| 0x01EA | INSBI E1 Thresholds Register |
| 0x01F1 | INSBI Depth Check Interrupt Status |
| 0x01F2 | Insert External ReSynch Interrupt Status |
| **0x0200 – 0x2D5** | **DS3/E3 Framer and M13 Multiplex #1** |
| 0x0200 | DS3 and E3 Master Reset |
| 0x0201 | DS3 and E3 Master Data Source |
| 0x0202 | DS3 and E3 Master Unchannelized Interface Options |
| 0x0203 | DS3/E3 Master Transmit Line Options |
| 0x0204 | DS3/E3 Master Receive Line Options |

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| Address | Register |
|---------|----------|
| 0x0205 | DS3/E3 Master Alarm Enable |
| 0x0206 | DS2 Master Alarm Enable / DS3 Network Requirement Bit |
| 0x0207 | E3 Data Link Control |
| 0x0208 | DS3 TRAN Configuration |
| 0x0209 | DS3 TRAN Diagnostic |
| 0x020C | DS3 FRMR Configuration |
| 0x020D | DS3 FRMR Interrupt Enable (ACE=0) |
| 0x020D | DS3 FRMR Additional Configuration (ACE=1) |
| 0x020E | DS3 FRMR Interrupt Status |
| 0x020F | DS3 FRMR Status |
| 0x0210 | DS3/E3 PMON Performance Meters |
| 0x0211 | DS3/E3 PMON Interrupt Enable/Status |
| 0x0214 | DS3/E3 PMON Line Code Violation Event Count LSB |
| 0x0215 | DS3/E3 PMON Line Code Violation Event Count MSB |
| 0x0216 | DS3/E3 PMON Framing Bit Error Event Count LSB |
| 0x0217 | DS3/E3 PMON Framing Bit Error Event Count MSB |
| 0x0218 | DS3 PMON Excessive Zeros LSB |
| 0x0219 | DS3 PMON Excessive Zeros MSB |
| 0x021A | DS3/E3 PMON Parity Error Event Count LSB |
| 0x021B | DS3/E3 PMON Parity Error Event Count MSB |
| 0x021C | DS3 PMON Path Parity Error Event Count LSB |
| 0x021D | DS3 PMON Path Parity Error Event Count MSB |
| 0x021E | DS3/E3 PMON FEBE Event Count LSB |
| 0x021F | DS3/E3 PMON FEBE Event Count MSB |
| 0x0220 | DS3/E3 TDPR Configuration |

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| Address | Register |
|---------|----------|
| 0x0221 | DS3/E3 TDPR Upper Transmit Threshold |
| 0x0222 | DS3/E3 TDPR Lower Interrupt Threshold |
| 0x0223 | DS3/E3 TDPR Interrupt Enable |
| 0x0224 | DS3/E3 TDPR Interrupt Status/UDR Clear |
| 0x0225 | DS3/E3 TDPR Transmit Data |
| 0x0228 | DS3/E3 RDLC Configuration |
| 0x0229 | DS3/E3 RDLC Interrupt Control |
| 0x022A | DS3/E3 RDLC Status |
| 0x022B | DS3/E3 RDLC Data |
| 0x022C | DS3/E3 RDLC Primary Address Match |
| 0x022D | DS3/E3 RDLC Secondary Address Match |
| 0x0230 | PRGD Control |
| 0x0231 | PRGD Interrupt Enable/Status |
| 0x0232 | PRGD Length |
| 0x0233 | PRGD Tap |
| 0x0234 | PRGD Error Insertion |
| 0x0238 | PRGD Pattern Insertion #1 |
| 0x0239 | PRGD Pattern Insertion #2 |
| 0x023A | PRGD Pattern Insertion #3 |
| 0x023B | PRGD Pattern Insertion #4 |
| 0x023C | PRGD Pattern Detector #1 |
| 0x023D | PRGD Pattern Detector #2 |
| 0x023E | PRGD Pattern Detector #3 |
| 0x023F | PRGD Pattern Detector #4 |
| 0x0240 | MX23 Configuration |
| 0x0241 | MX23 Demux AIS Insert |
| 0x0242 | MX23 Mux AIS Insert |

| Address | Register |
|---------|----------|
| 0x0243 | MX23 Loopback Activate |
| 0x0244 | MX23 Loopback Request Insert |
| 0x0245 | MX23 Loopback Request Detect |
| 0x0246 | MX23 Loopback Request Interrupt |
| 0x0248 | FEAC XBOC Control |
| 0x0249 | FEAC XBOC Code |
| 0x024A | FEAC RBOC Configuration/Interrupt Enable |
| 0x024B | FEAC RBOC Interrupt Status |
| 0x0250 | DS2 FRMR #1 Configuration |
| 0x0251 | DS2 FRMR #1 Interrupt Enable |
| 0x0252 | DS2 FRMR #1 Interrupt Status |
| 0x0253 | DS2 FRMR #1 Status |
| 0x0254 | DS2 FRMR #1 Monitor Interrupt Enable/Status |
| 0x0255 | DS2 FRMR #1 FERR Count |
| 0x0256 | DS2 FRMR #1 PERR Count (LSB) |
| 0x0257 | DS2 FRMR #1 PERR Count (MSB) |
| 0x0258 | MX12 #1Configuration and Control |
| 0x0259 | MX12 #1 Loopback Code Select |
| 0x025A | MX12 #1 Mux/Demux AIS Insert |
| 0x025B | MX12 #1 Loopback Activate |
| 0x025C | MX12 #1 Loopback Interrupt |
| 0x0260 | DS2 FRMR #2 Registers |
| 0x0268 | MX12 #2 Registers |
| 0x0270 | DS2 FRMR #3 Registers |
| 0x0278 | MX12 #3 Registers |
| 0x0280 | DS2 FRMR #4 Registers |
| 0x0288 | MX12 #4 Registers |

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**HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MUX**

| Address | Register |
|---|---|
| 0x0290 | DS2 FRMR #5 Registers |
| 0x0298 | MX12 #5 Registers |
| 0x02A0 | DS2 FRMR #6 Registers |
| 0x02A8 | MX12 #6 Registers |
| 0x02B0 | DS2 FRMR #7 Registers |
| 0x02B8 | MX12 #7 Registers |
| 0x02C0 | E3 FRMR Framing Options |
| 0x02C1 | E3 FRMR Maintenance Options |
| 0x02C2 | E3 FRMR Framing Interrupt Enable |
| 0x02C3 | E3 FRMR Framing Interrupt Indication and Status |
| 0x02C4 | E3 FRMR Maintenance Event Interrupt Enable |
| 0x02C5 | E3 FRMR Maintenance Event Interrupt Indication |
| 0x02C6 | E3 FRMR Maintenance Event Status |
| 0x02C8 | E3 TRAN Framing Options |
| 0x02C9 | E3 TRAN Status and Diagnostic Options |
| 0x02CA | E3 TRAN BIP-8 Error Mask |
| 0x02CB | E3 TRAN Maintenance and Adaptation Options |
| 0x02D0 | TTB Control |
| 0x02D1 | TTB Trail Trace Identifier Status |
| 0x02D2 | TTB Indirect Address |
| 0x02D3 | TTB Indirect Data |
| 0x02D4 | TTB Expected Payload Type Label |
| 0x02D5 | TTB Payload Type Label Control/Status |
| **0x0300 – 0x03D5** | **DS3/E3 Framer and M13 Multiplex #2** |
| **0x0400 – 0x04D5** | **DS3/E3 Framer and M13 Multiplex #3** |
| 0x0500, 0x0520, 0x0540, 0x0560, 0x0580, 0x05A0 | T1/E1 Pattern Generator and Detector Control |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---------|----------|
| 0x0501, 0x0521, 0x0541, 0x0561, 0x0581, 0x05A1 | T1/E1 Pattern Generator and Detector Interrupt Enable/Status |
| 0x0502, 0x0522, 0x0542, 0x0562, 0x0582, 0x05A2 | T1/E1 Pattern Generator and Detector Length |
| 0x0503, 0x0523, 0x0543, 0x0563, 0x0583, 0x05A3 | T1/E1 Pattern Generator and Detector Tap |
| 0x0504, 0x0524, 0x0544, 0x0564, 0x0584, 0x05A4 | T1/E1 Pattern Generator and Detector Error Insertion |
| 0x0508, 0x0528, 0x0548, 0x0568, 0x0588, 0x05A8 | T1/E1 Pattern Generator and Detector Pattern Insertion #1 |
| 0x0509, 0x0529, 0x0549, 0x0569, 0x0589, 0x05A9 | T1/E1 Pattern Generator and Detector Pattern Insertion #2 |
| 0x050A, 0x052A, 0x054A, 0x056A, 0x058A, 0x05AA | T1/E1 Pattern Generator and Detector Pattern Insertion #3 |
| 0x050B, 0x052B, 0x054B, 0x056B, 0x058B, 0x05AB | T1/E1 Pattern Generator and Detector Pattern Insertion #4 |
| 0x050C, 0x052C, 0x054C, 0x056C, 0x058C, 0x05AC | T1/E1 Pattern Generator and Detector Pattern Detector #1 |
| 0x050D, 0x052D, 0x054D, 0x056D, 0x058D, 0x05AD | T1/E1 Pattern Generator and Detector Pattern Detector #2 |
| 0x050E, 0x052E, 0x054E, 0x056E, 0x058E, 0x05AE | T1/E1 Pattern Generator and Detector Pattern Detector #3 |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---------|----------|
| 0x050F, 0x052F, 0x054F, 0x056F, 0x058F, 0x05AF | T1/E1 Pattern Generator and Detector Pattern Detector #4 |
| 0x0510, 0x0530, 0x0550, 0x0570, 0x0590, 0x05B0 | Generator Controller Configuration |
| 0x0511, 0x0531, 0x0551, 0x0571, 0x0591, 0x05B1 | Generator Controller µP Access Status |
| 0x0512, 0x0532, 0x0552, 0x0572, 0x0592, 0x05B2 | Generator Controller Channel Indirect Address/Control |
| 0x0513, 0x0533, 0x0553, 0x0533, 0x0593, 0x05B3 | Generator Controller Channel Indirect Data Buffer |
| 0x0514, 0x0534, 0x0554, 0x0574, 0x0594, 0x05B4 | Receiver Controller Configuration |
| 0x0515, 0x0535, 0x0555, 0x0575, 0x0595, 0x05B5 | Receiver Controller µP Access Status |
| 0x0516, 0x0536, 0x0556, 0x0576, 0x0596, 0x05B6 | Receiver Controller Channel Indirect Address/Control |
| 0x0517, 0x0537, 0x0557, 0x0577, 0x0597, 0x05B7 | Receiver Controller Channel Indirect Data Buffer |
| 0x0700 | SONET/SDH Master Reset |
| 0x0701 | SONET/SDH Master Ingress Configuration |
| 0x0702 | SONET/SDH Master Egress Configuration |
| 0x0703 | SONET/SDH Master Ingress VTPP Configuration |
| 0x0704 | SONET/SDH Master Egress VTPP Configuration |
| 0x0705 | SONET/SDH Master RTOP Configuration |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---|---|
| 0x0706 | SONET/SDH Master Tributary Alarm AIS Control |
| 0x0707 | SONET/SDH Master Tributary Remote Defect Indication Control |
| 0x0708 | SONET/SDH Master Tributary Auxiliary Remote Defect Indication Control |
| 0x0709 | SONET/SDH Master DS3/E3 Clock Generation Control |
| 0x070A | SONET/SDH Master Loopback Control |
| 0x070B | SONET/SDH Telecom Bus Signal Monitor, Accumulation Trigger |
| 0x070C | SONET/SDH Transmit Pointer Configuration #1 (MSB) |
| 0x070D | SONET/SDH Transmit Pointer Configuration #2 (LSB) |
| 0x073C | DLL Configuration (TelecomBus) |
| 0x073E | DLL Delay Tap Status (TelecomBus) |
| 0x073F | DLL Control Status (TelecomBus) |
| **0x740 - 0x077F** | **Ingress VTPP #1** |
| 0x0740, 0x0742, 0x0744, 0x0746, 0x0748, 0x074A, 0x074C | VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0741, 0x0743, 0x0745, 0x0747, 0x0749, 0x074B, 0x074D | VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x074E | VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x074F | VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt |

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HIGH DENSITY T1/E1 FRAMER  WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---------|----------|
| 0x0750, 0x0752, 0x0754, 0x0756, 0x0758, 0x075A, 0x075C | VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0751, 0x0753, 0x0755, 0x0757, 0x0759, 0x075B, 0x075D | VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x075E | VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x075F | VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt |
| 0x0760, 0x0762, 0x0764, 0x0766, 0x0768, 0x076A, 0x076C | VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0761, 0x0763, 0x0765, 0x0767, 0x0769, 0x076B, 0x076D | VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x076E | VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x076F | VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt |
| 0x0770, 0x0772, 0x0774, 0x0776, 0x0778, 0x077A, 0x077C | VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0771, 0x0773, 0x0775, 0x0777, 0x0779, 0x077B, 0x077D | VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x077E | VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt |

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HIGH DENSITY T1/E1 FRAMER WITH
INTEGRATED VT/TU MAPPER AND M13 MUX

| Address | Register |
|---------|----------|
| 0x077F | VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt |
| **0x780 - 0x07BF** | **Ingress VTPP #2** |
| **0x7C0 - 0x07FF** | **Ingress VTPP #3** |
| 0x0800 - 0x85E | RTDM Tributary Control |
| 0x0860 | Reserved |
| 0x0862 | RTDM Time Switch Page Control |
| 0x0863 | RTDM Indirect Time Switch Tributary RAM Status and Control |
| 0x0864 | RTDM Indirect Time Switch Internal Link Address |
| 0x0865 | RTDM Indirect Ingress Tributary Data |
| **0x0900 – 0x93F** | **Egress VTPP #1** |
| 0x0900, 0x0902, 0x0904, 0x0906, 0x0908, 0x090A, 0x090C | VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0901, 0x0903, 0x0905, 0x0907, 0x0909, 0x090B, 0x090D | VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x090E | VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x090F | VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt |
| 0x0910, 0x0912, 0x0914, 0x0916, 0x0918, 0x091A, 0x091C | VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0911, 0x0913, 0x0915, 0x0917, 0x0919, 0x091B, 0x091D | VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status |

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HIGH DENSITY T1/E1 FRAMER  WITH
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| Address | Register |
|---|---|
| 0x091E | VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x091F | VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt |
| 0x0920, 0x0922, 0x0924, 0x0926, 0x0928, 0x092A, 0x092C | VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0921, 0x0923, 0x0925, 0x0927, 0x0929, 0x092B, 0x092D | VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x092E | VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x092F | VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt |
| 0x0930, 0x0932, 0x0934, 0x0936, 0x0938, 0x093A, 0x093C | VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0931, 0x0933, 0x0935, 0x0937, 0x0939, 0x093B, 0x093D | VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status |
| 0x093E | VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt |
| 0x093F | VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt |
| **0x0940 – 0x97F** | **Egress VTPP #2** |
| **0x0980 – 0x9BF** | **Egress VTPP #3** |
| 0x09C0 | Byte Synchronous Mapping Control Register |
| 0x09C3 | Byte Synchronous Mapping Tributary Indirect Access Address Register |

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| Address | Register |
|---|---|
| 0x09C4 | Byte Synchronous Mapping Tributary Indirect Access Control Register |
| 0x09C5 | Byte Synchronous Mapping Tributary Mapping Indirect Access Data Register |
| 0x09C6 | Byte Synchronous Mapping Tributary Control Indirect Access Data Register |
| 0x09C9 | Byte Synchronous Mapping T1 Thresholds Register |
| 0x09CA | Byte Synchronous Mapping E1 Thresholds Register |
| 0x09E0 | Byte Synchronous Demapping Control Register |
| 0x09E3 | Byte Synchronous Demapping Tributary RAM Indirect Access Address Register |
| 0x09E4 | Byte Synchronous Demapping Tributary RAM Indirect Access Control Register |
| 0x09E5 | Byte Synchronous Demapping Tributary Mapping RAM Indirect Access Data Register |
| 0x09E6 | Byte Synchronous Demapping Tributary Control RAM Indirect Access Data Register |
| 0x0x9EF | Byte Synchronous Demapping FIFO Control Register |
| **0x0A00 – 0x0AFD** | **Receive Tributary Overhead Processor (RTOP) #1** |
| 0x0A00, 0x0A08, 0x0A10, 0x0A18, 0x0A20, 0x0A28, 0x0A30 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, Configuration |
| 0x0A01, 0x0A09, 0x0A11, 0x0A19, 0x0A21, 0x0A29, 0x0A31 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status |
| 0x0A02, 0x0A0A, 0x0A12, 0x0A1A, 0x0A22, 0x0A2A, 0x0A32 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, Expected Path Signal Label |

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HIGH DENSITY T1/E1 FRAMER  WITH
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| Address | Register |
|---------|----------|
| 0x0A03, 0x0A0B, 0x0A13, 0x0A1B, 0x0A23, 0x0A2B, 0x0A33 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label |
| 0x0A04, 0x0A0C, 0x0A14, 0x0A1C, 0x0A24, 0x0A2C, 0x0A34 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB |
| 0x0A05, 0x0A0D, 0x0A15, 0x0A1D, 0x0A25, 0x0A2D, 0x0A35 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB |
| 0x0A06, 0x0A0E, 0x0A16, 0x0A1E, 0x0A26, 0x0A2E, 0x0A36 | RTOP, TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count LSB |
| 0x0A07, 0x0A0F, 0x0A17, 0x0A1F, 0x0A27, 0x0A2F, 0x0A37 | RTOP, TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count MSB |
| 0x0A38 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt |
| 0x0A39 | RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt |
| 0x0A3A | RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt |
| 0x0A3B | RTOP, TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt |
| 0x0A3C | RTOP, TU #1 in TUG2 #1 to TUG2 #7 RFI Interrupt |
| 0x0A3D | RTOP, TU #1 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration |
| 0x0A40, 0x0A48, 0x0A50, 0x0A58, 0x0A60, 0x0A68, 0x0A70 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration |

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*HIGH DENSITY T1/E1 FRAMER WITH
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| Address | Register |
|---------|----------|
| 0x0A41, 0x0A49, 0x0A51, 0x0A59, 0x0A61, 0x0A69, 0x0A71 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status |
| 0x0A42, 0x0A4A, 0x0A52, 0x0A5A, 0x0A62, 0x0A6A, 0x0A72 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, Expected Path Signal Label |
| 0x0A43, 0x0A4B, 0x0A53, 0x0A5B, 0x0A63, 0x0A6B, 0x0A73 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label |
| 0x0A44, 0x0A4C, 0x0A54, 0x0A5C, 0x0A64, 0x0A6C, 0x0A74 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB |
| 0x0A45, 0x0A4D, 0x0A55, 0x0A5D, 0x0A65, 0x0A6D, 0x0A75 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB |
| 0x0A46, 0x0A4E, 0x0A56, 0x0A5E, 0x0A66, 0x0A6E, 0x0A76 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB |
| 0x0A47, 0x0A4F, 0x0A57, 0x0A5F, 0x0A67, 0x0A6F, 0x0A77 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB |
| 0x0A78 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt |
| 0x0A79 | RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt |
| 0x0A7A | RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt |
| 0x0A7B | RTOP, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt |

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| Address | Register |
|---------|----------|
| 0x0A7C | RTOP, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt |
| 0x0A7D | RTOP, TU #2 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration |
| 0x0A80, 0x0A88, 0x0A90, 0x0A98, 0x0AA0, 0x0AA8, 0x0AB0 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration |
| 0x0A81, 0x0A89, 0x0A91, 0x0A99, 0x0AA1, 0x0AA9, 0x0AB1 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status |
| 0x0A82, 0x0A8A, 0x0A92, 0x0A9A, 0x0AA2, 0x0AAA, 0x0AB2 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, Expected Path Signal Label |
| 0x0A83, 0x0A8B, 0x0A93, 0x0A9B, 0x0AA3, 0x0AAB, 0x0AB3 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label |
| 0x0A84, 0x0A8C, 0x0A94, 0x0A9C, 0x0AA4, 0x0AAC, 0x0AB4 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB |
| 0x0A85, 0x0A8D, 0x0A95, 0x0A9D, 0x0AA5, 0x0AAD, 0x0AB5 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB |
| 0x0A86, 0x0A8E, 0x0A96, 0x0A9E, 0x0AA6, 0x0AAE, 0x0AB6 | TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB |
| 0x0A87, 0x0A8F, 0x0A97, 0x0A9F, 0x0AA7, 0x0AAF, 0x0AB7 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB |

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| Address | Register |
|---------|----------|
| 0x0AB8 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt |
| 0x0AB9 | RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt |
| 0x0ABA | RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt |
| 0x0ABB | RTOP, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt |
| 0x0ABC | RTOP, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt |
| 0x0ABD | RTOP, TU #3 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration |
| 0x0AC0, 0x0AC8, 0x0AD0, 0x0AD8, 0x0AE0, 0x0AE8, 0x0AF0 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration |
| 0x0AC1, 0x0AC9, 0x0AD1, 0x0AD9, 0x0AE1, 0x0AE9, 0x0AF1 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status |
| 0x0AC2, 0x0ACA, 0x0AD2, 0x0ADA, 0x0AE2, 0x0AEA, 0x0AF2 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, Expected Path Signal Label |
| 0x0AC3, 0x0ACB, 0x0AD3, 0x0ADB, 0x0AE3, 0x0AEB, 0x0AF3 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, Path Signal Label |
| 0x0AC4, 0x0ACC, 0x0AD4, 0x0ADC, 0x0AE4, 0x0AEC, 0x0AF4 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB |
| 0x0AC5, 0x0ACD, 0x0AD5, 0x0ADD, 0x0AE5, 0x0AED, 0x0AF5 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB |

| Address | Register |
|---|---|
| 0x0AC6, 0x0ACE, 0x0AD6, 0x0ADE, 0x0AE6, 0x0AEE, 0x0AF6 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB |
| 0x0AC7, 0x0ACF, 0x0AD7, 0x0ADF, 0x0AE7, 0x0AEF, 0x0AF7 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB |
| 0x0AF8 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt |
| 0x0AF9 | RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt |
| 0x0AFA | RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt |
| 0x0AFB | RTOP, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt |
| 0x0AFC | RTOP, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt |
| 0x0AFD | RTOP, TU #4 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration |
| **0x0B00 – 0x0BFD** | **Receive Tributary Overhead Processor (RTOP) #2** |
| **0x0C00 – 0x0CFD** | **Receive Tributary Overhead Processor (RTOP) #3** |
| 0x0D00 - 0x0D06 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D07 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control |
| 0x0D08 - 0x0D0E | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D0F | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control |
| 0x0D10 - 0x0D16 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1 Control |

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| Address | Register |
|---------|----------|
| 0x0D17 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control |
| 0x0D18 - 0x0D1E | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D1F | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control |
| 0x0D20 - 0x0D26 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0D27 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control |
| 0x0D28 - 0x0D2E | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0D2F | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control |
| 0x0D30 - 0x0D36 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0D37 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control |
| 0x0D38 - 0x0D3E | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0D3F | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control |
| 0x0D40 - 0x0D46 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0D47 | TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control |
| 0x0D48 - 0x0D4E | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0D4F | TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control |
| 0x0D50 - 0x0D56 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |

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| Address | Register |
|---------|----------|
| 0x0D57 | TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control |
| 0x0D58 - 0x0D5E | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0D5F | TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control |
| 0x0D60 | TRAP Indirect Remote Alarm Page Address |
| 0x0D61 | TRAP Indirect Remote Alarm Tributary Address |
| 0x0D62 | TRAP Indirect Datapath Tributary Data |
| 0x0D63 | TRAP RDI Control |
| 0x0D68 | TRAP Remote Parallel Alarm Port TUG2 #1 of TUG3 #1 Configuration |
| 0x0D69- 0x0D6E | TRAP Remote Parallel Alarm Port TUG2 #2 to TUG2 #7 of TUG3 #1 Configuration |
| 0x0D70 - 0x0D76 | TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #2 Configuration |
| 0x0D78 - 0x0D7E | TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #3 Configuration |
| 0x0D80 | TTOP TU #1 in TUG2 #1 of TUG3 #1, Control |
| 0x0D81 - 0x0D86 | TTOP TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control |
| 0x0D87 | TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control |
| 0x0D88 - 0x0D8E | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D8F | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control |
| 0x0D90 - 0x0D96 | TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D97 | TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control |

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| Address | Register |
|---------|----------|
| 0x0D98 - 0x0D9E | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control |
| 0x0D9F | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control |
| 0x0DA0 - 0x0DA6 | TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0DA7 | TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control |
| 0x0DA8 - 0x0DAE | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0DAF | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control |
| 0x0DB0 - 0x0DB6 | TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0DB7 | TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control |
| 0x0DB8 - 0x0DBE | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control |
| 0x0DBF | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control |
| 0x0DC0 - 0x0DC6 | TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0DC7 | TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control |
| 0x0DC8 - 0x0DCE | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0DCF | TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control |
| 0x0DD0 - 0x0DD6 | TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |
| 0x0DD7 | TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control |
| 0x0DD8 - 0x0DDE | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control |

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| Address | Register |
|---------|----------|
| 0x0DDF | TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control |
| 0x0DE0 | TTOP TUG3 #1 Control |
| 0x0DE1 | TTOP TUG3 #2 Control |
| 0x0DE2 | TTOP TUG3 #3 Control |
| 0x0DE4 | TTOP Trail Trace Identifier Page Select |
| 0x0DE5 | TTOP Indirect Trail Trace Identifier Tributary Select |
| 0x0DE6 | TTOP Indirect Trail Trace Identifier Buffer Address |
| 0x0DE7 | TTOP Indirect Trail Trace Identifier Buffer Data |
| 0x0E00 - 0x0E5E | TTMP Tributary Control |
| 0x0E61 | TTMP Time Switch Page Control |
| 0x0E62 | TTMP Indirect Time Switch RAM Control and Status |
| 0x0E63 | TTMP Indirect Egress Tributary Address |
| 0x0E64 | TTMP Indirect Time Switch Internal Link Data |
| 0x0E65 | TTMP Telecom Interface Configuration |
| **0x0E80 – 0x0E82** | **D3MD #1** |
| 0x0E80 | D3MD Control |
| 0x0E81 | D3MD Interrupt Status |
| 0x0E82 | D3MD Interrupt Enable |
| **0x0E84 – 0x0E86** | **D3MD #2** |
| **0x0E88 – 0x0E8A** | **D3MD #3** |
| **0x0E8C – 0x0E8E** | **D3MA #1** |
| 0x0E8C | D3MA Control |
| 0x0E8D | D3MA Interrupt Status |
| 0x0E8E | D3MA Interrupt Enable |
| **0x0E90 – 0x0E92** | **D3MA #2** |
| **0x0E94 – 0x0E96** | **D3MA #3** |
| **0x0F00 – 0x0F2B** | **RTTB #1** |

| Address | Register |
|---------|----------|
| 0x0F00 | RTTB TU3 or TU #1 in TUG2 #1, Configuration and Status |
| 0x0F01 to 0x0F06 | RTTB TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status |
| 0x0F08 to 0x0F0E | RTTB TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0F10H to 0x0F16 | RTTB TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0F18 to 0x0F1E | RTTB TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status |
| 0x0F20 + 0x40*N | RTTB TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt |
| 0x0F21 | RTTB TU #2 in TUG2 #1 to TUG2 #7, TIM Interrupt |
| 0x0F22 | RTTB TU #3 in TUG2 #1 to TUG2 #7, TIM Interrupt |
| 0x0F23 | RTTB TU #4 in TUG2 #1 to TUG2 #7, TIM Interrupt |
| 0x0F24 | RTTB TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt |
| 0x0F25 | RTTB TU #2 in TUG2 #1 to TUG2 #7, TIU Interrupt |
| 0x0F26 | RTTB TU #3 in TUG2 #1 to TUG2 #7, TIU Interrupt |
| 0x0F27 | RTTB TU #4 in TUG2 #1 to TUG2 #7, TIU Interrupt |
| 0x0F28 | RTTB TIU Threshold |
| 0x0F29 | RTTB Indirect Tributary Select |
| 0x0F2A | RTTB Indirect Address Select |
| 0x0F2B | RTTB Indirect Data Select |
| **0x0F40 – 0x0F6B** | **RTTB #2** |
| **0x0F80 – 0x0FAB** | **RTTB #3** |
| 0x1000 | Master Test |

For all register accesses, CSB must be low.

## 10   NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TEMUX 84.  Normal mode registers (as opposed to test mode registers) are selected when TRS (A[12]) is low.

The register descriptions are contained in a separate TEMUX 84 register description document.

**Notes on Normal Mode Register Bits:**

1.  Writing values into unused register bits typically has no effect.  However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0.  Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2.  All configuration bits that can be written into can also be read back.  This allows the processor controlling the TEMUX 84 to determine the programming state of the block.

3.  Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4.  Writing into read-only normal mode register bit locations does not affect TEMUX 84 operation unless otherwise noted.

## 11    <u>TEST FEATURES DESCRIPTION</u>

The TEMUX 84 contains test features for both production testing and board testing.

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TEMUX 84.  Test mode registers (as opposed to normal mode registers) are selected when TRS (A[12]) is high.

**Notes on Register Bits:**

1. Writing values into unused register bits has no effect.  Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

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### Register 0x1000: Master Test Register

| Bit | Type | Function | Default |
|-------|------|----------|---------|
| Bit 7 | R/W | Reserved | 0 |
| Bit 6 | | Unused | X |
| Bit 5 | | Unused | X |
| Bit 4 | R/W | PMCTST | 0 |
| Bit 3 | W | DBCTRL | X |
| Bit 2 | R/W | Reserved | 0 |
| Bit 1 | W | HIZDATA | X |
| Bit 0 | R/W | HIZIO | 0 |

This register is used to select TEMUX 84 test features.  All bits, except for PMCTST, are reset to zero by a hardware reset of the TEMUX 84; a software reset of the TEMUX 84 does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the TEMUX 84 for PMC's manufacturing tests.  When PMCTST is set to logic 1, the TEMUX 84 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors.  The PMCTST bit can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin while PMCTST is a logic 1.  When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus.  While the DBCTRL bit is set, holding the CSB pin high causes the TEMUX 84 to drive the data bus and holding the CSB pin low tri-states the data bus.  The DBCTRL bit overrides the HIZDATA bit.  The DBCTRL bit is used to measure the drive capability of the data bus driver pads. When PMCTST is logic 0, the DBCTRL bit is ignored.

Reserved:

These bits must be logic 0 for correct operation.

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HIZIO:

The HIZIO bit controls the tri-state modes of the output pins of the TEMUX 84.
While the HIZIO bit is a logic 1, all output pins of the TEMUX 84, except the
data bus, are held in a high-impedance state.  The microprocessor interface is
still active.

HIZDATA:

The HIZDATA bit controls the tri-state modes of the TEMUX 84.  While the
HIZIO bit is a logic 1, all output pins of the TEMUX 84, except the data bus,
are held in a high-impedance state. While the HIZDATA bit is a logic 1, the
data bus is held in a high-impedance state which inhibits microprocessor read
cycles.

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## 11.1  <u>JTAG Test Port</u>

The TEMUX 84 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan.  Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed.  For more details on the JTAG port, please refer to the Operations section.

**Table 10      - Instruction Register**

Length - 3 bits

| Instructions | Selected Register | Instruction Codes, IR[2:0] |
|---|---|---|
| EXTEST | Boundary Scan | 000 |
| IDCODE | Identification | 001 |
| SAMPLE | Boundary Scan | 010 |
| BYPASS | Bypass | 011 |
| BYPASS | Bypass | 100 |
| STCTEST | Boundary Scan | 101 |
| BYPASS | Bypass | 110 |
| BYPASS | Bypass | 111 |

**Table 11      - Identification Register**

| Length | 32 bits |
|---|---|
| Version number | 0x2 |
| Part Number | 0x8316 |
| Manufacturer's identification code | 0x0CD |
| Device identification | 0x283160CD |

The boundary scan register is made up of 302 boundary scan cells, divided into input observation (IN_CELL), output (OUT_CELL) and bidirectional (IO_CELL) cells. These cells are detailed in the following pages. The first 32 cells form the

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ID code register and carry the code 283160CDH.  The boundary scan chain
order is presented in Table 12.

## Table 12    - Boundary Scan Register

| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| SDC1FP_MVID_1 | 0 | IO_CELL | - | OEB_D_3 | 151 | OUT_CELL | - |
| OEB_SDC1FP_MVID_1 | 1 | OUT_CELL | - | D_4 | 152 | IO_CELL | - |
| SBIACT_MVID_2 | 2 | OUT_CELL | - | OEB_D_4 | 153 | OUT_CELL | - |
| OEB_SBIACT_MVID_2 | 3 | OUT_CELL | - | D_5 | 154 | IO_CELL | - |
| SAJUST_REQ_MVID_3 | 4 | OUT_CELL | - | OEB_D_5 | 155 | OUT_CELL | - |
| OEB_SAJUST_REQ_ MVID_3 | 5 | OUT_CELL | - | D_6 | 156 | IO_CELL | - |
| SDDATA_0_MVID_4 | 6 | OUT_CELL | - | OEB_D_6 | 157 | OUT_CELL | - |
| OEB_SDDATA_0_MVID_4 | 7 | OUT_CELL | - | D_7 | 158 | IO_CELL | - |
| SDDATA_1_MVID_5 | 8 | OUT_CELL | - | OEB_D_7 | 159 | OUT_CELL | - |
| OEB_SDDATA_1_MVID_5 | 9 | OUT_CELL | - | ALE | 160 | IN_CELL | - |
| SDDATA_2_MVID_6 | 10 | OUT_CELL | - | RSTB | 161 | IN_CELL | - |
| OEB_SDDATA_2_MVID_6 | 11 | OUT_CELL | - | A_0 | 162 | IN_CELL | - |
| SDDATA_3_MVID_7 | 12 | OUT_CELL | - | A_1 | 163 | IN_CELL | - |
| OEB_SDDATA_3_MVID_7 | 13 | OUT_CELL | - | A_2 | 164 | IN_CELL | - |
| SDDATA_4_MVID_8 | 14 | OUT_CELL | - | A_3 | 165 | IN_CELL | - |
| OEB_SDDATA_4_MVID_8 | 15 | OUT_CELL | - | A_4 | 166 | IN_CELL | - |
| SDDATA_5_MVID_9 | 16 | OUT_CELL | - | A_5 | 167 | IN_CELL | - |
| OEB_SDDATA_5_MVID_9 | 17 | OUT_CELL | - | A_6 | 168 | IN_CELL | - |
| SDDATA_6_MVID_10 | 18 | OUT_CELL | - | A_7 | 169 | IN_CELL | - |
| OEB_SDDATA_6_MVID_10 | 19 | OUT_CELL | - | A_8 | 170 | IN_CELL | - |
| SDDATA_7_MVID_11 | 20 | OUT_CELL | - | A_9 | 171 | IN_CELL | - |
| OEB_SDDATA_7_MVID_11 | 21 | OUT_CELL | - | A_10 | 172 | IN_CELL | - |
| SDDP_MVID_12 | 22 | OUT_CELL | - | A_11 | 173 | IN_CELL | - |
| OEB_SDDP_MVID_12 | 23 | OUT_CELL | - | A_12 | 174 | IN_CELL | - |
| SDPL_MVID_13 | 24 | OUT_CELL | - | WRB | 175 | IN_CELL | - |
| OEB_SDPL_MVID_13 | 25 | OUT_CELL | - | RDB | 176 | IN_CELL | - |
| SDV5_MVID_14 | 26 | OUT_CELL | - | CSB | 177 | IN_CELL | - |
| OEB_SDV5_MVID_14 | 27 | OUT_CELL | - | LAV5 | 178 | OUT_CELL | - |

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| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| MVID_15 | 28 | OUT_CELL | - | OEB_LAV5 | 179 | OUT_CELL | - |
| OEB_MVID_15 | 29 | OUT_CELL | - | LAPL | 180 | OUT_CELL | - |
| MVID_16 | 30 | OUT_CELL | - | OEB_LAPL | 181 | OUT_CELL | - |
| OEB_MVID_16 | 31 | OUT_CELL | - | LADP | 182 | OUT_CELL | - |
| MVID_17 | 32 | OUT_CELL | - | OEB_LADP | 183 | OUT_CELL | - |
| OEB_MVID_17 | 33 | OUT_CELL | - | LADATA_0 | 184 | OUT_CELL | - |
| MVID_18 | 34 | OUT_CELL | - | OEB_LADATA_0 | 185 | OUT_CELL | - |
| OEB_MVID_18 | 35 | OUT_CELL | - | LADATA_1 | 186 | OUT_CELL | - |
| MVID_19 | 36 | OUT_CELL | - | OEB_LADATA_1 | 187 | OUT_CELL | - |
| OEB_MVID_19 | 37 | OUT_CELL | - | LADATA_2 | 188 | OUT_CELL | - |
| MVID_20 | 38 | OUT_CELL | - | OEB_LADATA_2 | 189 | OUT_CELL | - |
| OEB_MVID_20 | 39 | OUT_CELL | - | LADATA_3 | 190 | OUT_CELL | - |
| MVID_21 | 40 | OUT_CELL | - | OEB_LADATA_3 | 191 | OUT_CELL | - |
| OEB_MVID_21 | 41 | OUT_CELL | - | LADATA_4 | 192 | OUT_CELL | - |
| SREFCLK | 42 | IN_CELL | - | OEB_LADATA_4 | 193 | OUT_CELL | - |
| MVED_1 | 43 | IN_CELL | - | LADATA_5 | 194 | OUT_CELL | - |
| MVED_2 | 44 | IN_CELL | - | OEB_LADATA_5 | 195 | OUT_CELL | - |
| S77_MVED_3 | 45 | IN_CELL | - | LADATA_6 | 196 | OUT_CELL | - |
| SAC1FP_MVED_4 | 46 | IN_CELL | - | OEB_LADATA_6 | 197 | OUT_CELL | - |
| SADATA_0_MVED_5 | 47 | IN_CELL | - | LADATA_7 | 198 | OUT_CELL | - |
| SADATA_1_MVED_6 | 48 | IN_CELL | - | OEB_LADATA_7 | 199 | OUT_CELL | - |
| SADATA_2_MVED_7 | 49 | IN_CELL | - | LAOE/LATPL | 200 | OUT_CELL | - |
| SADATA_3_MVED_8 | 50 | IN_CELL | - | OEB_LAOE | 201 | OUT_CELL | - |
| SADATA_4_MVED_9 | 51 | IN_CELL | - | LAC1J1V1 | 202 | OUT_CELL | - |
| SADATA_5_MVED_10 | 52 | IN_CELL | - | OEB_LAC1J1V1 | 203 | OUT_CELL | - |
| SADATA_6_MVED_11 | 53 | IN_CELL | - | LAC1 | 204 | IN_CELL | - |
| SADATA_7_MVED_12 | 54 | IN_CELL | - | CLK52M | 205 | IN_CELL | - |
| SADP_MVED_13 | 55 | IN_CELL | - | RADWEST | 206 | IN_CELL | - |
| SAPL_MVED_14 | 56 | IN_CELL | - | RADWESTFP | 207 | IN_CELL | - |
| SAV5_MVED_15 | 57 | IN_CELL | - | RADWESTCK | 208 | IN_CELL | - |
| SBIDET_0_MVED_16 | 58 | IN_CELL | - | RADEAST | 209 | IN_CELL | - |
| SBIDET_1_MVED_17 | 59 | IN_CELL | - | RADEASTFP | 210 | IN_CELL | - |

| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| MVED_18 | 60 | IN_CELL | - | RADEASTCK | 211 | IN_CELL | - |
| TS0ID | 61 | OUT_CELL | - | LDAIS | 212 | IN_CELL | - |
| OEB_TS0ID | 62 | OUT_CELL | - | LDTPL | 213 | IN_CELL | - |
| MVED_19 | 63 | IN_CELL | - | LDV5 | 214 | IN_CELL | - |
| MVED_20 | 64 | IN_CELL | - | LDPL | 215 | IN_CELL | - |
| MVED_21 | 65 | IN_CELL | - | LDC1J1V1 | 216 | IN_CELL | - |
| CCSID_1 | 66 | OUT_CELL | - | LDDP | 217 | IN_CELL | - |
| OEB_CCSID_1 | 67 | OUT_CELL | - | LDDATA_0 | 218 | IN_CELL | - |
| CCSID_2 | 68 | OUT_CELL | - | LDDATA_1 | 219 | IN_CELL | - |
| OEB_CCSID_2 | 69 | OUT_CELL | - | LDDATA_2 | 220 | IN_CELL | - |
| CCSID_3 | 70 | OUT_CELL | - | LDDATA_3 | 221 | IN_CELL | - |
| OEB_CCSID_3 | 71 | OUT_CELL | - | LDDATA_4 | 222 | IN_CELL | - |
| EFBWEN_1_CASID_1 | 72 | OUT_CELL | - | LDDATA_5 | 223 | IN_CELL | - |
| OEB_EFBWEN_1_CASID_1 | 73 | OUT_CELL | - | LDDATA_6 | 224 | IN_CELL | - |
| EFBWDAT_1_CASID_2 | 74 | OUT_CELL | - | LDDATA_7 | 225 | IN_CELL | - |
| OEB_EFBWDAT_1_CASID_2 | 75 | OUT_CELL | - | L77 | 226 | IN_CELL | - |
| CASID_3 | 76 | OUT_CELL | - | LREFCLK | 227 | IN_CELL | - |
| OEB_CASID_3 | 77 | OUT_CELL | - | TNEG_TMFP_1 | 228 | OUT_CELL | - |
| CASID_4 | 78 | OUT_CELL | - | OEB_TNEG_TMFP_1 | 229 | OUT_CELL | - |
| OEB_CASID_4 | 79 | OUT_CELL | - | TCLK_1 | 230 | OUT_CELL | - |
| CASID_5 | 80 | OUT_CELL | - | OEB_TCLK_1 | 231 | OUT_CELL | - |
| OEB_CASID_5 | 81 | OUT_CELL | - | TPOS_TDAT_1 | 232 | OUT_CELL | - |
| CASID_6 | 82 | OUT_CELL | - | OEB_TPOS_TDAT_1 | 233 | OUT_CELL | - |
| OEB_CASID_6 | 83 | OUT_CELL | - | TICLK_1 | 234 | IN_CELL | - |
| CASID_7 | 84 | OUT_CELL | - | RNEG_RLCV_1 | 235 | IN_CELL | - |
| OEB_CASID_7 | 85 | OUT_CELL | - | RPOS_RDAT_1 | 236 | IN_CELL | - |
| EFBWEN_2_CASID_8 | 86 | OUT_CELL | - | RCLK_1 | 237 | IN_CELL | - |
| OEB_EFBWEN_2_CASID_8 | 87 | OUT_CELL | - | TNEG_TMFP_2 | 238 | OUT_CELL | - |
| EFBWDAT_2_CASID_9 | 88 | OUT_CELL | - | OEB_TNEG_TMFP_2 | 239 | OUT_CELL | - |
| OEB_EFBWDAT_2_CASID_9 | 89 | OUT_CELL | - | TCLK_2 | 240 | OUT_CELL | - |

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| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| CASID_10 | 90 | OUT_CELL | - | OEB_TCLK_2 | 241 | OUT_CELL | - |
| OEB_CASID_10 | 91 | OUT_CELL | - | TPOS_TDAT_2 | 242 | OUT_CELL | - |
| CASID_11 | 92 | OUT_CELL | - | OEB_TPOS_TDAT_2 | 243 | OUT_CELL | - |
| OEB_CASID_11 | 93 | OUT_CELL | - | TICLK_2 | 244 | IN_CELL | - |
| CASID_12 | 94 | OUT_CELL | - | RNEG_RLCV_2 | 245 | IN_CELL | - |
| OEB_CASID_12 | 95 | OUT_CELL | - | RPOS_RDAT_2 | 246 | IN_CELL | - |
| CASID_13 | 96 | OUT_CELL | - | RCLK_2 | 247 | IN_CELL | - |
| OEB_CASID_13 | 97 | OUT_CELL | - | TNEG_TMFP_3 | 248 | OUT_CELL | - |
| CASID_14 | 98 | OUT_CELL | - | OEB_TNEG_TMFP_3 | 249 | OUT_CELL | - |
| OEB_CASID_14 | 99 | OUT_CELL | - | TCLK_3 | 250 | OUT_CELL | - |
| EFBWEN_3_CASID_15 | 100 | OUT_CELL | - | OEB_TCLK_3 | 251 | OUT_CELL | - |
| OEB_EFBWEN_3_ CASID_15 | 101 | OUT_CELL | - | TPOS_TDAT_3 | 252 | OUT_CELL | - |
| EFBWDAT_3_CASID_16 | 102 | OUT_CELL | - | OEB_TPOS_TDAT_3 | 253 | OUT_CELL | - |
| OEB_EFBWDAT_3_ CASID_16 | 103 | OUT_CELL | - | TICLK_3 | 254 | IN_CELL | - |
| CASID_17 | 104 | OUT_CELL | - | RNEG_RLCV_3 | 255 | IN_CELL | - |
| OEB_CASID_17 | 105 | OUT_CELL | - | RPOS_RDAT_3 | 256 | IN_CELL | - |
| CASID_18 | 106 | OUT_CELL | - | RCLK_3 | 257 | IN_CELL | - |
| OEB_CASID_18 | 107 | OUT_CELL | - | RGAPCLK_RSCLK_1 | 258 | OUT_CELL | - |
| CASID_19 | 108 | OUT_CELL | - | OEB_RGAPCLK_RSCLK_1 | 259 | OUT_CELL | - |
| OEB_CASID_19 | 109 | OUT_CELL | - | RDATO_1 | 260 | OUT_CELL | - |
| CASID_20 | 110 | OUT_CELL | - | OEB_RDATO_1 | 261 | OUT_CELL | - |
| OEB_CASID_20 | 111 | OUT_CELL | - | ROVRHD_1 | 262 | OUT_CELL | - |
| CASID_21 | 112 | OUT_CELL | - | OEB_ROVRHD_1 | 263 | OUT_CELL | - |
| OEB_CASID_21 | 113 | OUT_CELL | - | RFPO_RMFPO_1 | 264 | OUT_CELL | - |
| CTCLK | 114 | IN_CELL | - | OEB_RFPO_RMFPO_1 | 265 | OUT_CELL | - |
| CCSED_1 | 115 | IN_CELL | - | TFPO_TMFPO_ TGAPCLK_1 | 266 | OUT_CELL | - |
| CCSED_2 | 116 | IN_CELL | - | OEB_TFPO_TMFPO_ TGAPCLK_1 | 267 | OUT_CELL | - |
| CCSED_3 | 117 | IN_CELL | - | TFPI_TMFPI_1 | 268 | IN_CELL | - |
| IFBWCLK_1_CASED_1 | 118 | IN_CELL | - | TDATI_1 | 269 | IN_CELL | - |

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| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| IFBWDAT_1_CASED_2 | 119 | IN_CELL | - | RGAPCLK_RSCLK_2 | 270 | OUT_CELL | 1 |
| IFBWEN_1_CASED_3 | 120 | IN_CELL | - | OEB_RGAPCLK_RSCLK_2 | 271 | OUT_CELL | 0 |
| EFBWCLK_1_CASED_4 | 121 | IN_CELL | - | RDATO_2 | 272 | OUT_CELL | 1 |
| EFBWDREQ_1_CASED_5 | 122 | IN_CELL | - | OEB_RDATO_2 | 273 | OUT_CELL | 1 |
| CASED_6 | 123 | IN_CELL | - | ROVRHD_2 | 274 | OUT_CELL | 0 |
| CASED_7 | 124 | IN_CELL | - | OEB_ROVRHD_2 | 275 | OUT_CELL | 0 |
| IFBWCLK_2_CASED_8 | 125 | IN_CELL | - | RFPO_RMFPO_2 | 276 | OUT_CELL | 1 |
| IFBWDAT_2_CASED_9 | 126 | IN_CELL | - | OEB_RFPO_RMFPO_2 | 277 | OUT_CELL | 1 |
| IFBWEN_2_CASED_10 | 127 | IN_CELL | - | TFPO_TMFPO_TGAPCLK_2 | 278 | OUT_CELL | 0 |
| EFBWCLK_2_CASED_11 | 128 | IN_CELL | - | OEB_TFPO_TMFPO_TGAPCLK_2 | 279 | OUT_CELL | 0 |
| EFBWDREQ_2_CASED_12 | 129 | IN_CELL | - | TFPI_TMFPI_2 | 280 | IN_CELL | 0 |
| CASED_13 | 130 | IN_CELL | - | TDATI_2 | 281 | IN_CELL | 0 |
| CASED_14 | 131 | IN_CELL | - | RGAPCLK_RSCLK_3 | 282 | OUT_CELL | 0 |
| IFBWCLK_3_CASED_15 | 132 | IN_CELL | - | OEB_RGAPCLK_RSCLK_3 | 283 | OUT_CELL | 1 |
| IFBWDAT_3_CASED_16 | 133 | IN_CELL | - | RDATO_3 | 284 | OUT_CELL | 1 |
| IFBWEN_3_CASED_17 | 134 | IN_CELL | - | OEB_RDATO_3 | 285 | OUT_CELL | 0 |
| EFBWCLK_3_CASED_18 | 135 | IN_CELL | - | ROVRHD_3 | 286 | OUT_CELL | 1 |
| EFBWDREQ_3_CASED_19 | 136 | IN_CELL | - | OEB_ROVRHD_3 | 287 | OUT_CELL | 0 |
| CASED_20 | 137 | IN_CELL | - | RFPO_RMFPO_3 | 288 | OUT_CELL | 0 |
| CASED_21 | 138 | IN_CELL | - | OEB_RFPO_RMFPO_3 | 289 | OUT_CELL | 0 |
| CMVFPB | 139 | IN_CELL | - | TFPO_TMFPO_TGAPCLK_3 | 290 | OUT_CELL | 1 |
| CMVFPC | 140 | IN_CELL | - | OEB_TFPO_TMFPO_TGAPCLK_3 | 291 | OUT_CELL | 1 |
| CMV8MCLK | 141 | IN_CELL | - | TFPI_TMFPI_3 | 292 | IN_CELL | 0 |
| INTB | 142 | OUT_CELL | - | TDATI_3 | 293 | IN_CELL | 0 |
| OEB_INTB | 143 | OUT_CELL | - | RECVCLK_3 | 294 | OUT_CELL | 0 |
| D_0 | 144 | IO_CELL | - | OEB_RECVCLK_3 | 295 | OUT_CELL | 0 |
| OEB_D_0 | 145 | OUT_CELL | - | RECVCLK_2 | 296 | OUT_CELL | 0 |
| D_1 | 146 | IO_CELL | - | OEB_RECVCLK_2 | 297 | OUT_CELL | 1 |
| OEB_D_1 | 147 | OUT_CELL | - | RECVCLK_1 | 298 | OUT_CELL | 0 |

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| Pin/ Enable | Bit # | Cell Type | Id Bit | Pin/ Enable | Bit # | Cell Type | Id Bit |
|---|---|---|---|---|---|---|---|
| D_2 | 148 | IO_CELL | - | OEB_RECVCLK_1 | 299 | OUT_CELL | 1 |
| OEB_D_2 | 149 | OUT_CELL | - | XCLK_E1 | 300 | IN_CELL | 0 |
| D_3 | 150 | IO_CELL | - | XCLK_T1 | 301 | IN_CELL | 0 |

## Notes:

1. Register bit 301 is the first bit of the scan chain (closest to TDI).

2. Enable cell OEB_pinname, sets ball pinname to high-impedance when set high.

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## 12    OPERATION

### 12.1  Tributary Indexing

The TEMUX 84 is capable of transporting 84 1.544 Mbit/s (T1) or 63 2.048 Mbit/s (E1) tributaries.  This section explains the correspondence between the indexing systems of the various mapping and multiplexing formats: SBI Bus, Telecom Bus, M13 and H-MVIP.  The listed index systems are used throughout the document.

The SBI Bus tributary designation uses two integers: the first represents the byte interleaved SPE number (range 1 to 3) and the second is the link index within the SPE (range 1 to 28).

The Telecom Bus indexing follows the conventions of the ITU-T multiplexing structure.  The bandwidth is divided into three TUG-3s numbered 1 through 3, each of which is composed of seven TUG-2s numbered 1 through 7, each of which is composed of either three TU-12s numbered 1 through 3 or four TU-11s numbered 1 through 4.

The three DS3s are divided into seven DS2s, each of which is composed of either four 1.544 Mbit/s or three 2.048 Mbit/s tributaries.

The payload capacity is divided into three equal portions.  Each of the following lists represents one set of equivalent tributaries:

- SPE #1, TUG-3 #1, DS3 #1 and MVID/MVED[1:7]

- SPE #2, TUG-3 #2, DS3 #2 and MVID/MVED[8:14]

- SPE #3, TUG-3 #3, DS3 #3 and MVID/MVED[15:21]

Table 13 and Table 14 provide the equivalencies between the various multiplex and mapping formats.  Alternately, the formats can be equated with the following formulae:

$$
\begin{aligned}
\text{1.544Mbit/s SBI LINK \#} \quad &= 7*(TU11-1) + TUG2 \\
&= 4*(DS2-1)+DS1 \\
&= 4*(MVED \text{ index} - 7*(SPE-1) - 1) + DS1
\end{aligned}
$$

$$
\begin{aligned}
\text{2.048Mbit/s SBI LINK \#} \quad &= 7*(TU12-1) + TUG2 \\
&= 3*(DS2-1)+E1 \\
&= 4*(MVED \text{ index} - 7*(SPE-1) - 1) + E1
\end{aligned}
$$

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### Table 13        - Indexing for 1.544 Mbit/s Tributaries

| SBI Bus SPE, LINK | Telecom Bus TUG-3, TUG-2, TU11 | M13 DS3, DS2, DS1 | H-MVIP port index, DS1 |
|---|---|---|---|
| 1,1 | 1,1,1 | 1,1,1 | 1,1 |
| 1,2 | 1,2,1 | 1,1,2 | 1,2 |
| 1,3 | 1,3,1 | 1,1,3 | 1,3 |
| 1,4 | 1,4,1 | 1,1,4 | 1,4 |
| 1,5 | 1,5,1 | 1,2,1 | 2,1 |
| 1,6 | 1,6,1 | 1,2,2 | 2,2 |
| 1,7 | 1,7,1 | 1,2,3 | 2,3 |
| 1,8 | 1,1,2 | 1,2,4 | 2,4 |
| 1,9 | 1,2,2 | 1,3,1 | 3,1 |
| 1,10 | 1,3,2 | 1,3,2 | 3,2 |
| 1,11 | 1,4,2 | 1,3,3 | 3,3 |
| 1,12 | 1,5,2 | 1,3,4 | 3,4 |
| 1,13 | 1,6,2 | 1,4,1 | 4,1 |
| 1,14 | 1,7,2 | 1,4,2 | 4,2 |
| 1,15 | 1,1,3 | 1,4,3 | 4,3 |
| 1,16 | 1,2,3 | 1,4,4 | 4,4 |
| 1,17 | 1,3,3 | 1,5,1 | 5,1 |
| 1,18 | 1,4,3 | 1,5,2 | 5,2 |
| 1,19 | 1,5,3 | 1,5,3 | 5,3 |
| 1,20 | 1,6,3 | 1,5,4 | 5,4 |
| 1,21 | 1,7,3 | 1,6,1 | 6,1 |
| 1,22 | 1,1,4 | 1,6,2 | 6,2 |
| 1,23 | 1,2,4 | 1,6,3 | 6,3 |
| 1,24 | 1,3,4 | 1,6,4 | 6,4 |
| 1,25 | 1,4,4 | 1,7,1 | 7,1 |
| 1,26 | 1,5,4 | 1,7,2 | 7,2 |
| 1,27 | 1,6,4 | 1,7,3 | 7,3 |
| 1,28 | 1,7,4 | 1,7,4 | 7,4 |
| 2,1 | 2,1,1 | 2,1,1 | 8,1 |
| ... | ... | ... | ... |

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**Table 14        - Indexing for 2.048 Mbit/s Tributaries**

| SBI Bus<br>SPE, LINK | Telecom Bus<br>TUG-3, TUG-2, TU12 | M13<br>DS3, DS2, E1 | H-MVIP<br>port index, E1 |
|---|---|---|---|
| 1,1 | 1,1,1 | 1,1,1 | 1,1 |
| 1,2 | 1,2,1 | 1,1,2 | 1,2 |
| 1,3 | 1,3,1 | 1,1,3 | 1,3 |
| 1,4 | 1,4,1 | 1,2,1 | 1,4 |
| 1,5 | 1,5,1 | 1,2,2 | 2,1 |
| 1,6 | 1,6,1 | 1,2,3 | 2,2 |
| 1,7 | 1,7,1 | 1,3,1 | 2,3 |
| 1,8 | 1,1,2 | 1,3,2 | 2,4 |
| 1,9 | 1,2,2 | 1,3,3 | 3,1 |
| 1,10 | 1,3,2 | 1,4,1 | 3,2 |
| 1,11 | 1,4,2 | 1,4,2 | 3,3 |
| 1,12 | 1,5,2 | 1,4,3 | 3,4 |
| 1,13 | 1,6,2 | 1,5,1 | 4,1 |
| 1,14 | 1,7,2 | 1,5,2 | 4,2 |
| 1,15 | 1,1,3 | 1,5,3 | 4,3 |
| 1,16 | 1,2,3 | 1,6,1 | 4,4 |
| 1,17 | 1,3,3 | 1,6,2 | 5,1 |
| 1,18 | 1,4,3 | 1,6,3 | 5,2 |
| 1,19 | 1,5,3 | 1,7,1 | 5,3 |
| 1,20 | 1,6,3 | 1,7,2 | 5,4 |
| 1,21 | 1,7,3 | 1,7,3 | 6,1 |
| 2,1 | 2,1,1 | 2,1,1 | 8,1 |
| ... | ... | ... | ... |

## 12.2  Clock and Frame Synchronization Constraints

Depending on the modes of operation utilized, some coordination between
LREFCLK, SREFCLK, LAC1, LDC1J1V1, SDC1FP and SAC1FP is required.
Specifically, tighter constraints must be respected when supporting transparent
virtual tributaries (TVTs) or 77.76 MHz buses.

The following only applies when using the Telecom Bus.  LREFCLK may be tied
low when support is limited to DS3/E3 serial line interfaces.

### 12.2.1 H-MVIP and 77.76 MHz Telecom Bus

The constraints given in the "19.44 MHz SBI Bus and 77.76 MHz Telecom Bus"
section also apply when the system interface is H-MVIP.  Except for the
frequency tolerance allowed by the "TEMUX 84 Timing Characteristics" section,
there are no constraints on CMV8MCLK and CMVFPB relative to other clocks.

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## 12.2.2 SBI and Telecom Buses Both 19.44 MHz

The rising and falling edges of LREFCLK must be aligned with a tolerance of +/-
10ns to the corresponding edges of SREFCLK.

Restrictions on frame alignment pulses only exist when TVTs are supported:

- If the Egress VTPP is bypassed, the SAC1FP pulse must be
  precisely 13 SREFCLK cycles before the LAC1 pulse.

- If the Egress VTPP is not bypassed, the SAC1FP pulse must be $3n$
  + 1 (where $n = 0,1,2\ldots$) SREFCLK cycles before the LAC1 pulse.

- If the Ingress VTPP is bypassed, LDC1J1V1 pulse must be
  precisely four SREFCLK cycles before the SDC1FP pulse.

- If the Ingress VTPP is no bypassed, there is no restriction on the
  alignment of SDC1FP and LDC1J1V1.

## 12.2.3 SBI and Telecom Buses Both 77.76 MHz

The rising edge of LREFCLK must be aligned with a tolerance of +/- 5ns to the
rising edge of SREFCLK.

For reliable operation, the STM-1s used within the SBI and Telecom buses must
be aligned in time.  To this end, one may manipulate the LSTM[1:0] and
SSTM[1:0] register bits and the position of the LAC1 and SDC1FP pulses.  Table
15 summarizes the combinations.

The alignment below is also required when the TEMUX 84 is configured for
transmux mode with a 77.76 MHz LREFCLK and SREFCLK.

**Table 15    - 77.76 SBI and Telecom Bus Alignment Options**

| | Clock Cycles LAC1 leads SDC1FP ($n = 0, 1, 2\ldots$) | | | |
|---|---|---|---|---|
| SSTM[1:0] | LSTM[1:0] | | | |
| | 00 | 01 | 10 | 11 |
| 00 | $4n$ | $4n + 1$ | $4n + 2$ | $4n + 3$ |
| 01 | $4n + 3$ | $4n$ | $4n + 1$ | $4n + 2$ |
| 10 | $4n + 2$ | $4n + 3$ | $4n$ | $4n + 1$ |
| 11 | $4n + 1$ | $4n + 2$ | $4n + 3$ | $4n$ |

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As an alternate formulation, if SSTM[1:0] and LSTM[1:0] were converted to their decimal equivalents, one would have to satisfy the constraint:

$$(LSTM - SSTM) \bmod 4 = (\text{Clock Cycles LAC1 leads SDC1FP}) \bmod 4$$

When TVTs are supported an additional constraint exists between SAC1FP and LAC1. Table 16 gives the permissible combinations.

**Table 16       - TVT Constraints for 77.76MHz**

| | Clock Cycles SAC1FP leads LAC1 (n = 0, 1 , 2…) | | | |
|---|---|---|---|---|
| | LSTM[1:0] | | | |
| SSTM[1:0] | 00 | 01 | 10 | 11 |
| 00 | 12n | 12n - 1 | 12n - 2 | 12n + 1 |
| 01 | 12n + 1 | 12n | 12n - 1 | 12n + 2 |
| 10 | 12n + 2 | 12n + 1 | 12n | 12n + 3 |
| 11 | 12n + 3 | 12n + 2 | 12n + 1 | 12n |

Note: Only the cases where SSTM equals LSTM have been validated.

### 12.2.4 19.44 MHz SBI Bus and 77.76 MHz Telecom Bus

The rising edge of LREFCLK must be aligned with a tolerance of +/- 5ns to the rising edge of SREFCLK.

For reliable operation, the STM-1s used within the Telecom bus must be aligned to the SREFCLK input. To this end, one may manipulate the LSTM[1:0] register bits and the position of the LAC1 pulses. Table 15 summarizes the combinations.

**Table 17       - 19.44 MHz SBI to 77.76 MHz Telecom to Bus Alignment Options**

| LSTM[1:0] | LREFCLK Cycles LAC1 sampling edge leads SREFCLK rising edge |
|---|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 0 |

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As alternate formulation, if LSTM[1:0] was converted to its decimal equivalent, one would have to satisfy the constraint:

(LSTM + 1) mod 4   = Clock Cycles LAC1 leads SREFCLK

TVTs are not supported for this bus configuration.

### 12.2.5 77.76 MHz SBI Bus and 19.44 MHz Telecom Bus

The rising edge of LREFCLK must be aligned with a tolerance of +/- 5ns to the rising edge of SREFCLK.

For reliable operation, the STM-1s used within the SBI bus must be aligned to LREFCLK.  To this end, one may manipulate the SSTM[1:0] register bits and the position of the SDC1FP pulses.  Table 15 summarizes the combinations.

**Table 18       -  77.76 MHz SBI to 19.44 MHz Telecom to Bus Alignment Options**

| SSTM[1:0] | SREFCLK Cycles SDC1FP sampling edge leads LREFCLK rising edge |
|-----------|-----------------------------------------------------------------|
| 00        | 1                                                               |
| 01        | 2                                                               |
| 10        | 3                                                               |
| 11        | 0                                                               |

As alternate formulation, if SSTM[1:0] was converted to its decimal equivalent, one would have to satisfy the constraint:

(SSTM + 1) mod 4   = Clock Cycles SDC1FP leads LREFCLK

TVTs are not supported for this bus configuration.

### 12.3 SLC®96

The following is a comprehensive discussion of the roles and responsbilities of TEMUX 84 and external logic in the support of the SLC®96 standard, Bellcore TR-TSY-000008.  While the TEMUX 84 handles most of the protocol functions, some external processing is required, especially of the datalink transported in the Fs bits.

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### 12.3.1 Transmit

While the TEMUX 84 supports transmission of AIS and the Yellow alarm, and supports signaling insertion, it is the responsibility of external logic to generate all F-bits.  This means valid Ft and Fs bits as well as the datalink.  To pass the F-bits transparently, the FDIS context bit must be set to logic 1 through the T1/E1 Transmitter Indirect Channel Data registers.

The TEMUX 84 can insert robbed bit signaling.  For the TEMUX 84 to insert the signaling into the correct frames ($6^{th}$ and $12^{th}$), it must know the multiframe alignment consistent with the encoding of the F-bits.  Therefore, it is imperative a multiframe indication is provided by the system inteface.    For the SBI interface, the PPSSSSFR octets (those following V5) communicate multiframe alignment, signaling and the F-bits.  The TRIB_TYP[1:0] bits of the EXSBI Tributary Control Indirect Access Data register should be set to "00" to configure the tributary to "Framed with CAS".

Because the F-bits are being sourced from the system interface, controlled frame slips must be avoided, if the TX-ELST is being used, to maintain superframe integrity.  The T1/E1 transmit clock must be referenced to CTCLK.    For SBI, CTCLK must be frequency locked to SREFCLK.  Two alternate configurations for SBI avoid the need for the TX-ELST: the transmit clock is slaved to the data rate at the system interface or the TEMUX 84 acts as a timing master using the AJUST_REQ output to set the data rate.

Insertion of nine state signaling is straight forward.  A sixteen bit encoding (i.e. ABCD) is used regardless of whether the signaling is inserted from the system interface or via register access through the T1/E1 Transmit Per-Channel Controller.  The ABCD state is sampled every 24 frames.  The "AB" values are inserted into the first superframe and the "CD" values are inserted into the second.  Thus, if toggling A or B bits are required, it is sufficient that $A \neq C$ or $B \neq D$, respectively.

### 12.3.2 Receive

The T1 framer will determine frame alignment within 13ms if it is programmed to frame to SLC®96 (i.e. ESF=0, FMS[1:0]=10) and is provided with valid SLC®96 frame overhead.  The framer is tolerant to the existence of the data link.  Once in frame, only the Ft bits are used to determine loss of frame and for monitoring framing bit errors.

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The presence of Yellow, Red, and AIS Carrier Fail Alarms is detected and integrated in accordance with the specifications defined in Bellcore TR-TSY-000191.

The datalink is not terminated within the TEMUX 84. Instead, it is provided on the SBI for external processing. Because the tributary may be subject to controlled frame slips, the external logic should be tolerant to the infrequent duplication or deletion of bits within the F-bit sequence.

Signaling is terminated elegantly. The signaling for two consecutive superframes is captured as an aggregate presented as ABCD, with "CD" being the second set of A and B signaling bits. The ABCD bits are treated as cohesive state that is subject to debouncing (if enabled single bit errors will be filtered) and freezing. The four bits are available on the SBI Drop interface and through the SIGX Indirect Channel Data Register registers. $A \neq C$ is an indication that the A bit is toggling. $B \neq D$ is an indication that the B bit is toggling. (Note, the following signaling states are all equivalent; they all represent toggling A and B bits: 0110, 1100, 0011, 1001.) An interrupt on change of signaling will only occur if the collected ABCD state changes, but not just from toggling A or B bits.

## 12.4 DS3 Frame Format

The TEMUX 84 provides support for both the C-bit parity and M23 DS3 framing formats. The DS3 frame format is shown in Figure 13.

### Figure 21    - DS3 Frame Structure



### $X_X$: X-Bit Channel

Transmit: The TEMUX 84 inserts the FERF signal on the X-bits. FERF generation is controlled by either the FERF bit of the DS3 TRAN Configuration register or by detection of OOF, RED, LOS and AIS, as configured by the TEMUX 84 Master DS3 Alarm Enable register.

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Receive: The TEMUX 84 monitors the state and detects changes in the state of the FERF signal on the X-bits.

## $P_X$: P-Bit Channel

Transmit: The TEMUX 84 calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.

Receive: The TEMUX 84 calculates the parity for the received payload.  Errors are accumulated in the DS3 PMON Parity Error Event Count registers.

## $M_X$: M-Frame Alignment Signal

Transmit: The TEMUX 84 generates the M-frame alignment signal (M1 = 0, M2 = 1, M3 = 0).

Receive: The TEMUX 84 finds M-frame alignment by searching for the F-bits and the M-bits.  Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.  M-bit errors are counted in the DS3 PMON Framing Bit Error Event Count registers.  When one or more M-bit errors are detected in 3 out of 4 consecutive M-frames, an out-of-frame defect is asserted (if MBDIS in the DS3 Framer Configuration register is a logic 0).

## $F_X$: M-Subframe Alignment Signal

Transmit: The TEMUX 84 generates the M-Subframe Alignment signal (F1=1, F2=0, F3=0, F4=1).

Receive: The TEMUX 84 finds M-frame alignment by searching for the F-bits and the M-bits.  Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.  F-bit errors are counted in the DS3 PMON Framing Bit Error Event Count registers.  An out-of frame defect is asserted if 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration register).

## $C_X$: C-Bit Channels

Transmit: When configured for M23 applications, the C-bits used for stuffing indication.  When configured for C-bit parity applications, the C-bit Parity ID bit is forced to logic 1.  The second C-bit in M-subframe 1 is set to logic 1.  The third C-

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bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC channel is sourced by the DS3 XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. FEBE transmission is controlled by the DFEBE bit in the DS3 TRAN Diagnostic register and by the detection of receive framing bit and path parity errors. The 3 C-bits in M-subframe 5 contain the 28.2 kbit/s path maintenance datalink. These bits are inserted from the DS3 TDPR HDLC controller. The C-bits in M-subframes 2, 6, and 7 are unused and are set to logic 1.

Receive: The CBITV register bit in the DS3 FRMR Status register is used to report the state of the C-bit parity ID bit, and hence whether a M23 or C-bit parity DS3 signal stream is being received. The FEAC channel on the third C-bit in M-subframe 1 is detected by the DS3 RBOC block. Path parity errors and detected FEBEs on the C-bits in M-subframes 3 and 4 are reported in the DS3 PMON Path Parity Error Event Count and FEBE Event Count registers respectively. The path maintenance datalink signal is extracted by theDS3 RDLC HDLC receiver (if enabled).

## 12.5 Servicing Interrupts

The TEMUX 84 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the bits of the TEMUX 84 Master Interrupt Source register (0x0010) to identify which of the 14 interrupt registers (0x0011-0x001E) needs to be read to identify the interrupt. For example, a logic one read in the DS3E3INT register bit indicates that an interrupt identified in one of the three Master Interrupt Source DS3/E3 registers produced the interrupt.

2. Read the bits of the second level Master Interrupt Source register to identify the interrupt source.

3. Service the interrupt by reading the register containing the interrupt status bit that is asserted.

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB

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## 12.6  Using the Performance Monitoring Features

The counters in the DS3 PMON block has been sized as not to saturate if polled every second. The T1/E1 PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small (less than 0.001%).

An accumulation interval is initiated by writing to one of the PMON event counter register addresses or by writing to the Global PMON Update register.  After initiating an accumulation interval, 3.5 recovered clock periods  (RCLK for the DS3 PMON) must be allowed to elapse to permit the PMON counter values to be properly transferred before the PMON registers may be read.

The odds of any one of the T1/E1 counters saturating during a one second sampling interval go up as the bit error rate (BER) increases.  At some point, the probability of counter saturation reaches 50%.  This point varies, depending upon the framing format and the type of event being counted.  The BER at which the probability of counter saturation reaches 50% is shown for various counters in Table 19 for E1 mode, and in Table 20 for T1 mode.

**Table 19        - PMON Counter Saturation Limits (E1 mode)**

| Counter | BER |
|---------|-----|
| FER | $4.0 \times 10^{-3}$ |
| CRCE | cannot saturate |
| FEBE | cannot saturate |

**Table 20        - PMON Counter Saturation Limits (T1 mode)**

| Counter | Format | BER |
|---------|--------|-----|
| FER | SF | $1.6 \times 10^{-3}$ |
|  | ESF | $6.4 \times 10^{-2}$ |
| CRCE | SF | $1.28 \times 10^{-1}$ |
|  | ESF | cannot saturate |

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear.

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Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. The following figures show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above $10^{-3}$, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 22 illustrates the expected count values for a range of Bit Error Ratios in E1 mode.

**Figure 22     - FER Count vs. BER (E1 mode)**
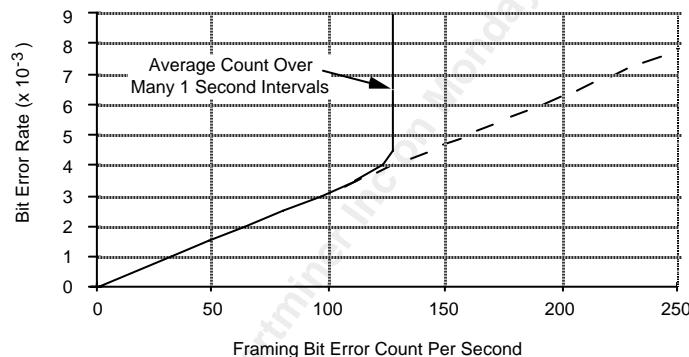


Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below $10^{-4}$, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above $10^{-4}$, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a $10^{-4}$ BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

The bit error rate for E1 can be calculated from the one-second PMON CRCE count by the following equation:

$$\textbf{Bit Error Rate} = 1 - 10^{\left(\dfrac{\log\left(1 - \dfrac{8}{8000}CRCE\right)}{8*256}\right)}$$

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**Figure 23      - CRCE Count vs. BER (E1 mode)**
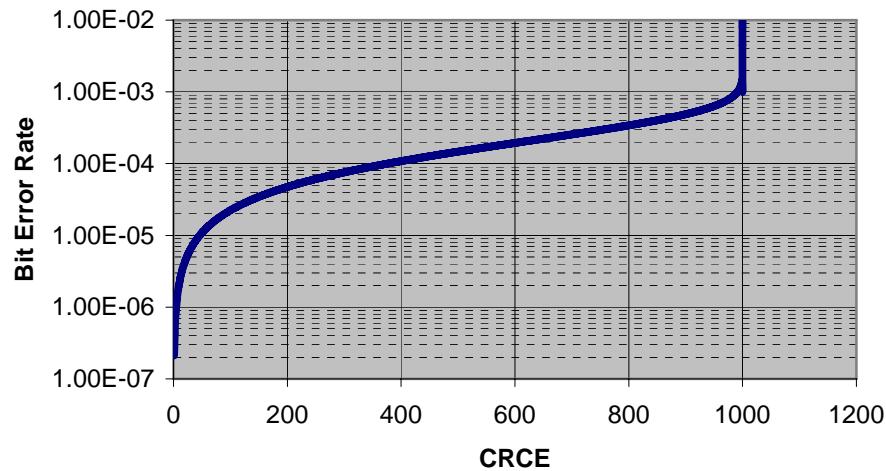


Figure 24 illustrates the expected count values for a range of Bit Error Ratios in T1 mode.

**Figure 24      - FER Count vs. BER (T1 ESF mode)**
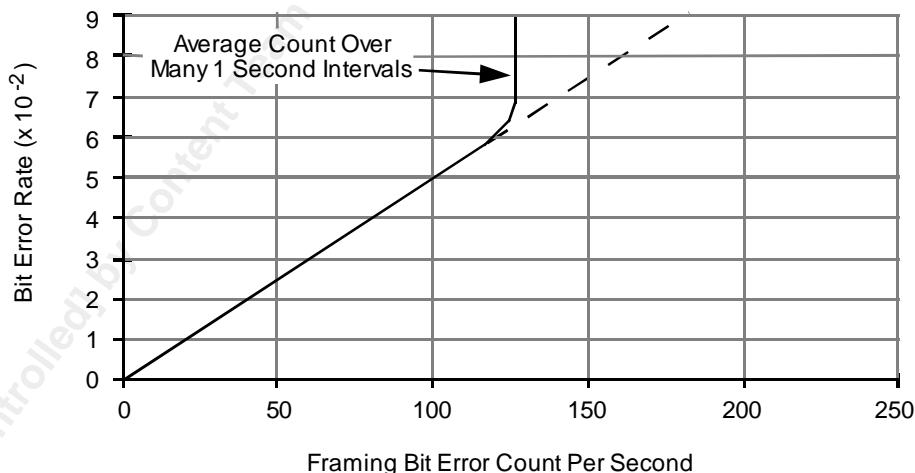


Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below $10^{-4}$, there tends to be no

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more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above $10^{-4}$, each CRC-6 error is often due to more than one bit error.  Thus, the relationship between BER and BEE count becomes non-linear above a $10^{-4}$ BER.  This must be taken into account when using ESF CRC-6 counts to determine the BER.

The bit error rate for T1 ESF can be calculated from the one-second PMON CRCE count by the following equation:

$$\text{Bit Error Rate} = 1 - 10^{\left(\frac{\log\left(1-\frac{24}{8000}BEE\right)}{24*193}\right)}$$

## Figure 25     - CRCE Count vs. BER (T1 ESF mode)
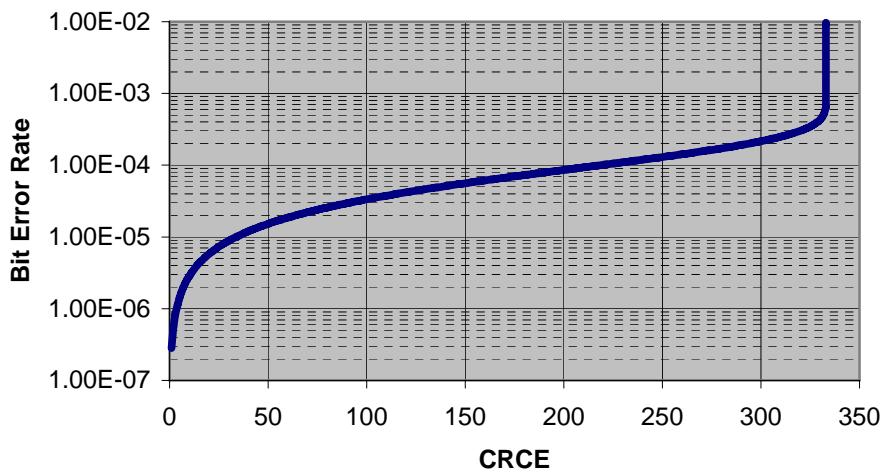


For T1 SF format, the CRCE and FER counts are identical, but the FER counter is smaller and should be ignored.

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**Figure 26　　- CRCE Count vs. BER (T1 SF mode)**
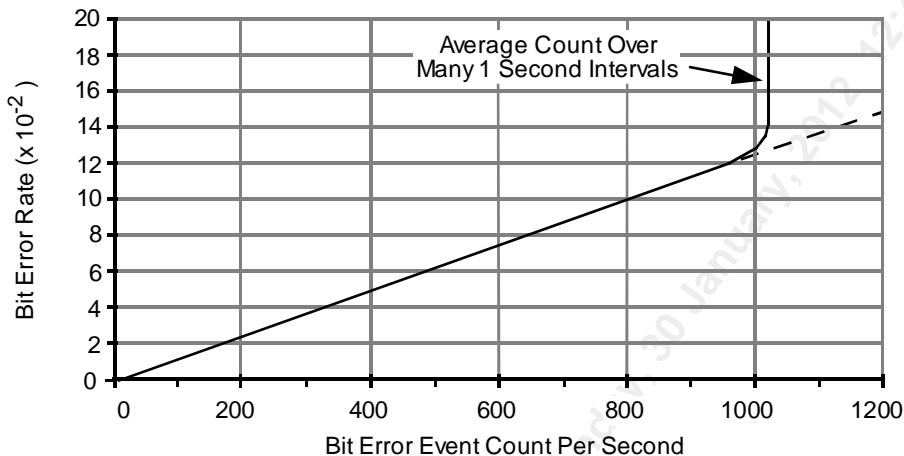


## 12.7  Using the Internal DS3 or E3 HDLC Transmitter

It is important to note that access rate to the TDPR registers is limited by the rate of the internal DS3/E3 clock.  Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the DS3 or E3 clock.  This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status.  Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the TEMUX 84, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value).  An HDLC all-ones Idle signal will be sent while in this state.  The TDPR is enabled by setting the EN bit to logic 1.  The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO.  The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set.  If FCS generation is desired, the CRC bit should be set to logic 1.  If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1.  The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values.  The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO.  Transmission will continue until the current packet is

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transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the one of the TEMUX 84 Master Interrupt Source registers, and the TEMUX 84 TDPR Interrupt Status registers to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

**Interrupt Driven Mode:**

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for a complete packet to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes of the packet have been written to the Transmit Data register, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will

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not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit.  The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

### TDPR Interrupt Routine:

Upon assertion of INTB, the source of the interrupt must first be identified by reading the TEMUX 84 Master Interrupt Source register (0020H) followed by reading one of the second level master interrupt source registers T1E1INT1, T1E1INT2, T1E1INT3, T1E1INT4 or DS3INT.  Once the source of the interrupt has been identified as the TDPR in use, then the following procedure should be carried out:

1.  Read the TDPR Interrupt Status register.

2.  If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted.  When the UDRI bit transitions to logic 1, one Abort sequence and continous flags will be transmitted.  The TDPR FIFO is held in reset state.  To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3.  If OVRI=1, then the FIFO has overflowed.  The packet of which the last byte written into the FIFO belongs to, has been corrupted and must be retransmitted.  Other packets in the FIFO are not affected.  Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

    If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted.  The FIFO is held in reset until a write to the TDPR Transmit Data register occurs.  This write contains the first byte of the next packet to be transmitted.

4.  If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written.  When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

    If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

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5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit.  If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs.  If there is no more data to transmit, then an EOM should be set at the end of the last packet byte.  Flags will then be transmitted once the last packet has been transmitted.

If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

## Polling Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO.  The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold.  The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet.  The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given.  The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure.  The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written.  Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1.  Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit.  Write the data into the TDPR Transmit Data register.  Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written.  Write the data into the TDPR Transmit Data register.  Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

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If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

## 12.8  Using the Internal DS3 or E3 Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal DS3 or E3 clock. Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the DS3 or E3 frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit

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will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated.  The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data.  In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register.  In the interrupt driven mode, the processor controlling the RDLC uses the TEMUX 84 INTB output and the TEMUX 84 Master Interrupt Source registers to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the TEMUX 84 is connected to the interrupt input of the processor.  The processor interrupt service routine verifies what block generated the interrupt by reading the TEMUX 84 Master Interrupt Source register followed by one of the  second level master interrupt source registers to identify one of the 3 HDLC receivers as the interrupt source.  Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1.         Read the RDLC Status register.  The INTR bit should be logic 1.

2.         If OVR = 1, then discard the last frame and go to step 1.  Overrun causes a reset of FIFO pointers.  Any packets that may have been in the FIFO are lost.

3.         If COLS = 1, then set the EMPTY FIFO software flag.

4.         If PKIN = 1, increment the PACKET COUNT.  If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag.  If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5.         Read the RDLC Data register.

6.         Read the RDLC Status register.

7.         If OVR = 1, then discard last frame and go to step 1.  Overrun causes a reset of FIFO pointers.  Any packets that may have been in the FIFO are lost.

8.         If COLS = 1, then set the EMPTY FIFO software flag.

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9.    If PKIN = 1, increment the PACKET COUNT.  If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag.  If the EMPTY FIFO software flag is not set, FIFO emptying will be delayed until the FIFO fill level is exceeded.

10.    Start the processing of FIFO data.  Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

If PBS[2:0] = 1XX, discard the data byte read in step 5, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

If PBS[2:0] = 000, store the packet data.

11.    If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable.  The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones.  The link state is active if the RDLC is receiving flags or data.

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

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**Figure 27      - Typical Data Frame**
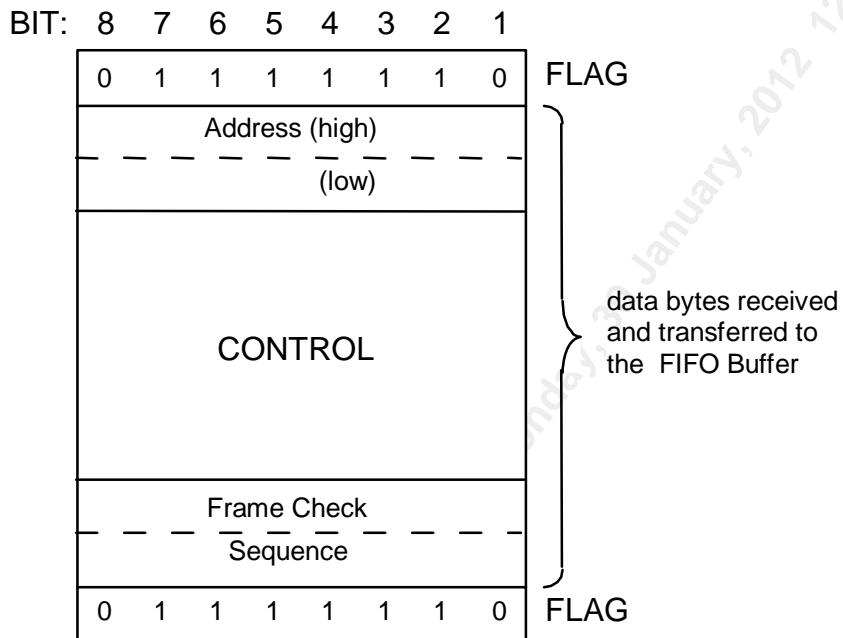


Bit 1 is the first serial bit to be received.  When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

**Figure 28      - Example Multi-Packet Operational Sequence**
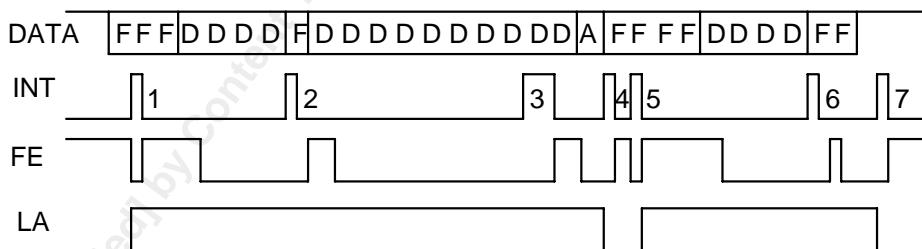


| F | - flag sequence (01111110) |
|---|---|
| A | - abort sequence (01111111) |
| D | - packet data bytes |
| INT | - active high interrupt output |
| FE | - internal FIFO empty status |
| LA | - state of the LINK ACTIVE software flag |

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Figure 28 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence.  The cause of each interrupt and the processing required at each point is described in the following paragraphs. The actual interrupt signal, INTB, is active low and will be the inverse of the INT signal shown in Figure 28.  Also in this example,  the programmable fill level set point is set at 8 bytes by writing this value into the INTC[6:0] bits of the RDLC Interrupt Control register.

At points 1 and 5 the first flag after all ones or abort is detected.  A dummy byte is written in the FIFO, FE goes low, and an interrupt goes active.  When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed.  The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty.  The interrupt is removed as soon as the RDLC Status register is read, since the FIFO fill level of 8 bytes has not been exceeded.  It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO.  The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high.  When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.  The LINK ACTIVE software flag is cleared.

## 12.9  Using the Internal T1/E1 Data Link Receiver

A time-sliced HDLC receiver processes the data links extracted from the tributaries.  Receive packets are queued in a dedicated 128 byte FIFO for each tributary.  The reading of the FIFOs by an external microprocessor is usually done in response to an interrupt, but polling is also supported.

On power up of the system, the receiver defaults to a disabled state.  One must use the RHDL Indirect Channel Data registers to program each tributary.  The configuration of each tributary is independent of all others.  The RHDL Interrupt Control register should then be initialized to enable the INTB output and to select

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the FIFO buffer fill level at which an interrupt will be generated. The FIFO threshold is a global setting optimized for a particular system by trading off minimizing the number of interrupts against avoiding FIFO overflows.

When the receiver is first enabled to delineate packets, it will assume the link is idle and immediately begin searching for flags. No bytes will be written into the FIFO until a flag is recognized. This is also true after an abort is detected. If packet delineation is disabled, all bytes are written raw into the FIFO.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The T1/E1 Receive HDLC processor (RHDL) can be used in a polled or interrupt driven mode for the transfer of packet data. In the polled mode, the processor controlling the RHDL must periodically read the RHDL Interrupt Status #1 register to determine if any tributaries need processing. In the interrupt driven mode, the processor controlling the RHDL uses the TEMUX 84 INTB output and the TEMUX 84 Master Interrupt Source registers to determine when to service the RHDL.

In the case of interrupt driven data transfer from the RHDL to the processor, the INTB output of the TEMUX 84 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the TEMUX 84 Master Interrupt Source register followed by the Master Interrupt Source T1E1 register to determine if RHDL is the interrupt source. Once it has identified that the RHDL has generated the interrupt, it processes the data in the following order:

1. Read the RHDL Interrupt Status #1 register. The value returned will indicate if any of RHDL Interrupt Status #2 through #11 should be read. Any bits returned as a logic 1 will indicate the associated tributary needs servicing. The bits in the RHDL Interrupt Status registers are write-one-to-clear, so the value read should be written back. Repeat steps 2 through 8 for each tributary with an INT bit set.

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2.  Write the RHDL Indirect Channel Address with the tributary index and set the FACCESS bit to logic 1.

3.  Write the RHDL Indirect Status with 0x40 to initiate an indirect read.

4.  Read RHDL Indirect Channel Data #2 register (0x011B) until CBUSY is returned as logic 0.  Store the last FE, OVR, PKIN and PBS[2:0] bits read.

5.  Read the HDLC data byte from the RHDL Indirect Channel Data #1 register (0x011A).

6.  If OVR = 1, then discard the last frame and go to step 2.  Overrun causes a reset of FIFO pointers and the loss of 128 bytes.  Because an overflow likely occurred in the midst of a packet, discard all byte up to the next end-of-packet read.

7.  Start the processing of FIFO data.  Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    If PBS[2:0] = 010, an abort has occur so discard the data byte read in step 5.

    If PBS[2:0] = 1XX, store the last byte of the packet and check the PBS[1:0] bits for CRC or non-integer-byte errors before deciding whether or not to keep the packet.

    If PBS[2:0] = 000, store the packet data.

8.  If FE = 0, go to step 3 else service the next tributary or exit this interrupt service routine to wait for the next interrupt.

If the RHDL data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

## 12.10  Using the Internal T1/E1 Data Link Transmitter

A time-sliced HDLC transmitter (THDL) formats the data links inserted into the T1/E1 tributaries.  Raw packets are written by an external microprocessor to a dedicated 128 byte FIFO for each tributary.  The HDLC transmitter reads the FIFO once a complete packet is written or when a specified FIFO fill threshold is passed.  Also, Performance Reporting Messages (PRMs) may be transmitted autonomously once a second.  The transmitter takes care of bit stuffing and insertion of the CRC protection and flags.

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By default, the HDLC transmitter operates in a clear channel mode in which the contents of the FIFO are transmitted verbatim without bit stuffing or CRC. If the FIFO becomes empty, flags will be transmitted. To enable the HDLC features, the DELIN context bit must be set via the THDL Indirect Channel Data registers.

FIFO thresholds must be set to avoid overflows and underflows, which result in lost data and an abort sequence. The actual thresholds depend on operating system latencies and algorithms used to write the packets. The Upper Transmit Threshold value determines how many bytes must be written before transmission of an incomplete packet starts. It should be set at a value large enough to ensure an underflow does not occur before the complete packet is written under worst case conditions, such as excessive interrupt servicing. Note that complete packets are always transmitted regardless of the Upper Transmit Threshold value. A large Upper Transmit Threshold value may result in FIFO overflows if large packets are being written. To avoid overflows, it is recommended writes only resume after the Lower Interrupt Threshold is reached.

The T1/E1 Transmit HDLC processor (THDL) can be used in a polled or interrupt driven mode for the transfer of packet data. Minimum packet size for THDL is 2 bytes. In the polled mode, the processor controlling the THDL must periodically read the THDL Interrupt Status #1 register to determine if there's been a change in FIFO status. In the interrupt driven mode, the processor controlling the THDL uses the TEMUX 84 INTB output and the TEMUX 84 Master Interrupt Source registers to determine when to service the THDL.

In the case of interrupt driven data transfer from the processor to THDL, the INTB output of the TEMUX 84 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the TEMUX 84 Master Interrupt Source register followed by the Master Interrupt Source T1E1 register to determine if HDLC Transmitter is the interrupt source. Once it has identified that the THDL has generated the interrupt, it processes the data in the following order:

1.      Read the THDL Interrupt Status #1 register. The value returned will indicate if any of THDL Interrupt Status #2 through #11 should be read. Any bits returned as a logic 1 will indicate the associated tributary needs servicing. The bits in the THDL Interrupt Status registers are write-one-to-clear, so the value read should be written back. Repeat steps 2 through 8 for each tributary with an INT bit set.

2. Write the THDL Indirect Channel Address with the tributary index and set the FACCESS bit to logic 1.

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3. Write the THDL Indirect Status register (0x0130) with 0x40 to initiate an indirect read.

4. Read the THDL Indirect Status register until CBUSY is returned as logic 0.

5. Read the THDL Indirect Channel Data #2 register (0x0133).

6. A logic 1 OVRI indicates the FIFO for the tributary has overflowed and a packet has been corrupted. The entire contents of the current packet should be written again to the FIFO.

7. A logic 1 UDRI indicates the FIFO for the tributary has underrun, a packet has been corrupted and an abort has been sent. The entire contents of the current packet should be written again to the FIFO.

8. A logic 1 LFILLI indicates the FIFO level has dropped below a programmed threshold or has become empty. Packet data may be written. If EMPTY is logic 1, 128 bytes may be written. If EMPTY is logic 0, 128 minus the LINT[6:0] value bytes may be written. Write the THDL Indirect Status register (0x0130) with 0x00 to configure indirect writes. Also, the EOM bit should be initialized to zero and need not be written for each byte except the last of the packet. For each byte, repeat the following:

   a. Read the THDL Indirect Status register (0x0130) until CBUSY is returned as logic 0.

   b. If the byte is the last of a packet, write a logic 1 to the EOM bit position of the second THDL Indirect Channel Data Register (0x0134).

   c. Write a byte to the first THDL Indirect Channel Data Register (0x0133). This initiates the indirect write.

## 12.11 Using the Time-Sliced T1/E1 Transceivers

### 12.11.1 Initialization

The configuration of the 84 T1/E1 framers is stored in context RAMs. These RAMs are initialized to all zeros upon release of reset. This effectively places the framers in T1 SF mode with frame slip buffers and jitter attenuators in both the ingress and egress paths. All trunk conditioning and alarm generation defaults to disabled.

## 12.12  T1 Automatic Performance Report Format

### Table 21       - Performance Report Message Structure and contents

| Octet No. | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1 | FLAG | | | | | | | |
| 2 | SAPI | | | | | | C/R | EA |
| 3 | TEI | | | | | | | EA |
| 4 | CONTROL | | | | | | | |
| 5 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 6 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 7 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 8 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 9 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 10 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 11 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 |
| 12 | FE | SE | LB | G1 | R | G2 | Nm | NI |
| 13 | FCS | | | | | | | |
| 14 | FCS | | | | | | | |
| 15 | FLAG | | | | | | | |

**Notes:**

1. The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

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**Table 22        - Performance Report Message Structure Notes**

| Octet No. | Octet Contents | Interpretation |
|---|---|---|
| 1 | 01111110 | Opening LAPD Flag |
| 2 | 00111000 | From CI:        SAPI=14, C/R=0, EA=0 |
|   | 00111010 | From carrier:   SAPI=14,C/R=1,EA=0 |
| 3 | 00000001 | TEI=0,EA=1 |
| 4 | 00000011 | Unacknowledged Frame |
| 5,6 | Variable | Data for latest second (T') |
| 7,8 | Variable | Data for Previous Second(T'-1) |
| 9,10 | Variable | Data for earlier Second(T'-2) |
| 11,12 | Variable | Data for earlier Second(T'-3) |
| 13,14 | Variable | CRC16 Frame Check Sequence |
| 15 | 01111110 | Closing LAPD flag |

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**Table 23      - Performance Report Message Contents**

| Bit Value | Interpretation |
|---|---|
| G1=1 | CRC ERROR EVENT =1 |
| G2=1 | 1<CRC ERROR EVENT ≤5 |
| G3=1 | 5<CRC ERROR EVENT ≤10 |
| G4=1 | 10<CRC ERROR EVENT ≤100 |
| G5=1 | 100<CRC ERROR EVENT ≤319 |
| G6=1 | CRC ERROR EVENT ≤ 320 |
| SE=1 | Severely Errored Framing Event ≥ 1(FE shall =0) |
| FE=1 | Frame Synchronization Bit Error Event ≥1 (SE shall=0 ) |
| LV=1 | Line code violation event ≥ 1.  This bit is always encoded as 0. |
| SL=1 | Slip Event ≥ 1.  This bit is always zero if the ELSTBYP bit of the RX-SBI-ELST Indirect Channel Data register has been set to logic 1.  When H-MVIP only mode is set (i.e. SYSOPT=01), the slips are relative to the CMV16MCLK input.  Otherwise, the slips are relative to the SREFCLK. |
| LB=1 | Payload Loopback Activated.  TEMUX 84 doesn't perform payload loopbacks; therefore, this bit is always encoded as 0. |
| U1,U2=0 | Under Study For Synchronization. |
| R=0 | Reserved ( Default Value =0) |
| NmNI=00,01,10,11 | One second Report Modulo 4 Counter |

## 12.13 T1/E1 Framer Loopback Modes

The TEMUX 84 provides two loopback modes for T1/E1 links to aid in network and system diagnostics.  The internal T1/E1 line loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected.  The system Diagnostic Digital loopback can be initiated at any

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time by the system via the µP interface to check the path of system data through the framer.

## T1/E1 Line Loopback

T1/E1 Line loopback is initiated by setting the LLOOP bit to a 1 through the TJAT Indirect Channel Data register. When in line loopback mode, the appropriate T1/E1 framer in the TEMUX 84 is configured to internally connect the jitter-attenuated clock and data from the RJAT to the transmit clock and data going to the M13 mux and SONET/SDH mapper.  The RJAT must not be bypassed except for SONET/SDH byte synchronously mapped tributaries.  Conceptually, the data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 29.

### Figure 29    - T1/E1 Line Loopback
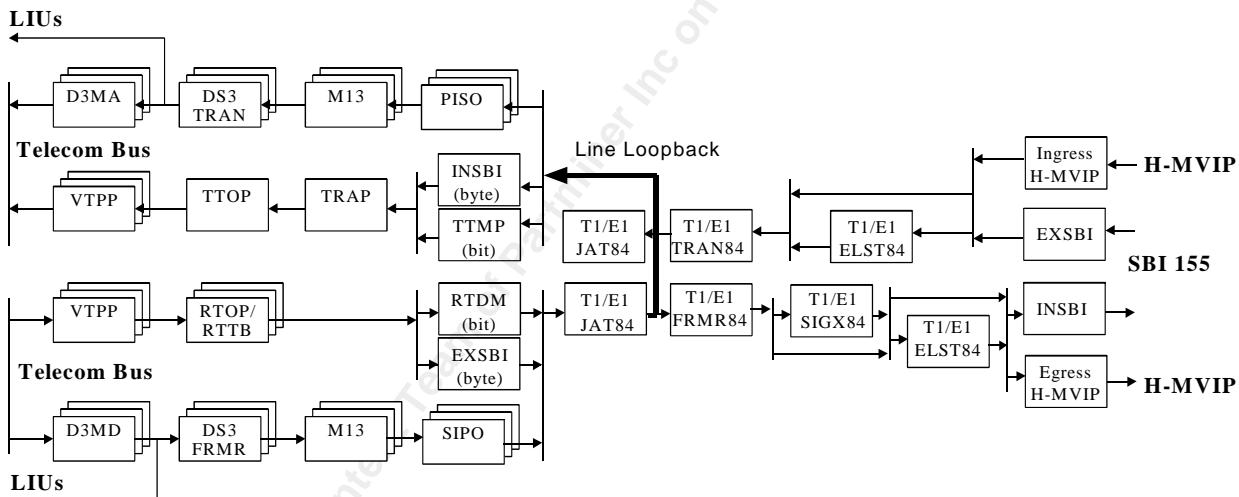


## T1/E1 Diagnostic Digital Loopback

When Diagnostic Digital loopback is initiated, by writing a 1 to the DLOOP bit through the RJAT Indirect Channel Data register, the appropriate T1/E1 framer in the TEMUX 84 is configured to internally connect its transmit clock and data to the receive clock and data The data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 30.

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### Figure 30     - T1/E1 Diagnostic Digital Loopback
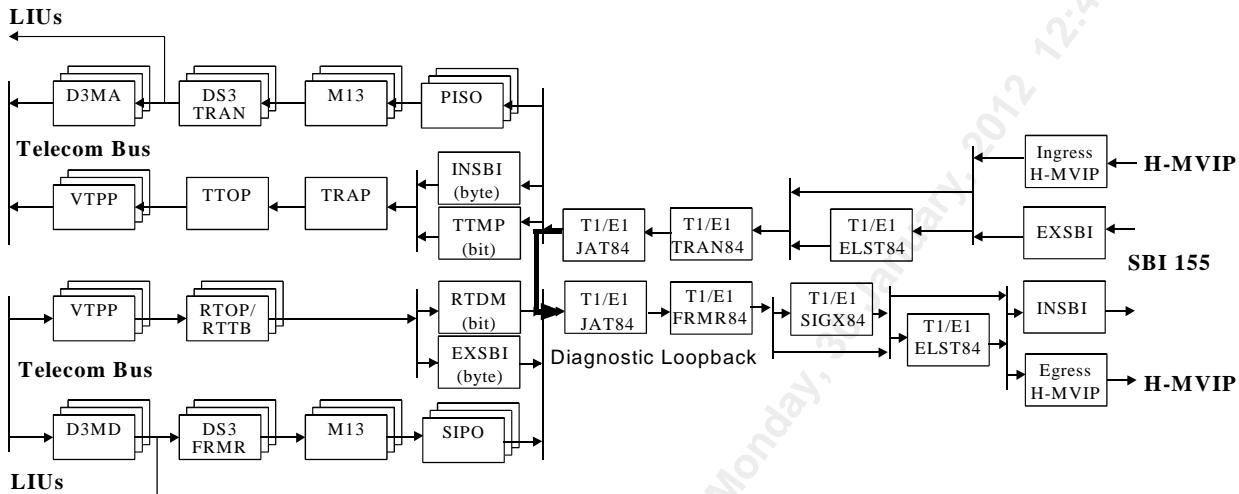


## 12.14  DS3 and E3 Loopback Modes

The TEMUX 84 provides two E3 and three DS3 M13 multiplexer loopback modes
to aid in network and system diagnostics at the DS3 interface. The DS3
loopbacks can be initiated via the µP interface whenever the DS3 framer/M13
multiplexer is enabled. The DS3 and E3 Master Data Source register controls the
DS3 loopback modes. These loopbacks are also available when the DS3 mux is
used with the DS3 mapper via the telecom bus interface.

### DS3 and E3 Diagnostic Loopback

DS3 and E3 Diagnostic Loopback allows the transmitted DS3 or E3 stream to be
looped back into the receive DS3 or E3 path, overriding the DS3 or E3 stream
received on the RDAT/RPOS and RNEG/RLCV inputs. The RCLK signal is also
substituted with the transmit DS3 or E3 clock, TCLK.  The configuration of the
receive interface determines how the TNEG/TMFP signal is handled during
loopback: if the UNI bit in the DS3 FRMR register is set, then the receive
interface is configured for RDAT and RLCV, therefore the TNEG/TMFP signal is
suppressed during loopback so that transmit MFP indications will not be seen nor
accumulated as input LCVs. If the UNI bit is clear, then the interface is configured
for bipolar signals RPOS and RNEG, therefore the TNEG is fed directly to the
RNEG input. This diagnostic loopback can be used when the TEMUX 84 is
configured as a multiplexer or as a framer only.  The DS3/E3 loopback mode is
shown diagrammatically in Figure 31.

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## Figure 31       - DS3/E3 Diagnostic Loopback Diagram
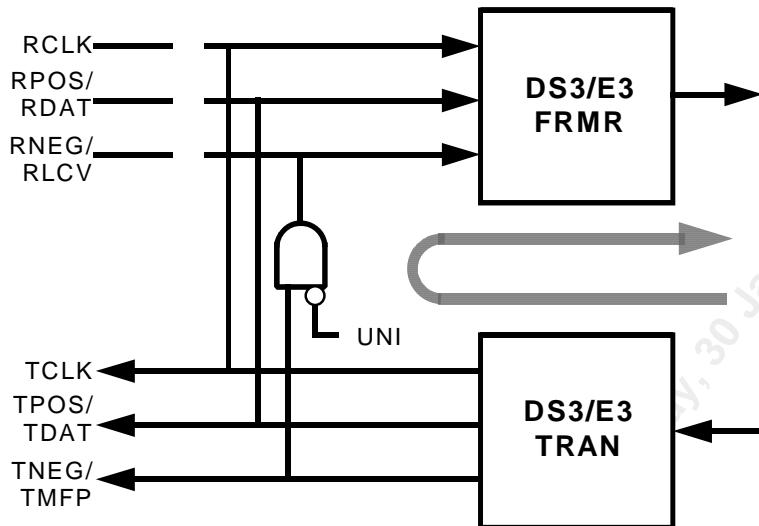


### DS3 and E3 Line Loopback

DS3 and E3 Line Loopbacks allow the received DS3/E3 streams to be looped back into the transmit DS3/E3 paths, overriding the DS3/E3 streams created internally by the framing unchannelized data or multiplexing of the lower speed tributaries.  The transmit signals on TPOS/TDAT and TNEG/TMFP are substituted with the receive signals from RPOS/RDAT and RNEG/RLCV.  The TCLK signal is also substituted with the receive DS3/E3 clock, RCLK. While this mode is active, AIS may be substituted for the DS3 payload being transmitted on the TPOS/TDAT and TNEG/TMFP outputs.  Note that the transmit interface must be configured to be the same as the DS3/E3 FRMR receive interface for this mode to work properly.  The DS3/E3 line loopback mode is shown diagrammatically in Figure 32.  There is a second form of line loopback which only loops back the DS3/E3 payload.  In this mode the DS3 framing overhead is regenerated for the received DS3/E3 stream and then retransmitted.  Line loopback is selected with the LLOOP bit in the DS3 and E3 Master Data Source register and payload loopback is selected by the PLOOP bit in the same register.

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## Figure 32    - DS3 and E3 Line Loopback Diagram
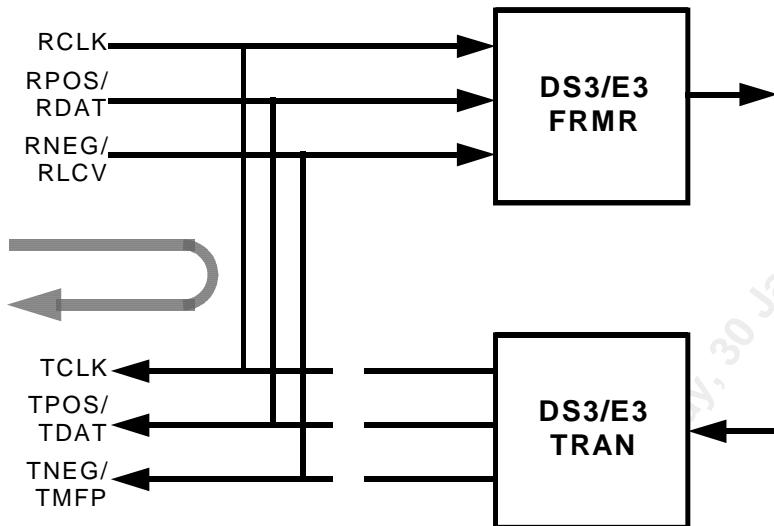


### DS2 Demultiplex Loopback

DS2 Demultiplex Loopbacks allow each of the seven demultiplexed DS2 streams to be looped back into the MX23 and multiplexed up into the transmit DS3 stream. This overrides the tributary DS2 streams coming from the MX12s.  The DS2 loopback mode is shown diagrammatically in Figure 33 and is enabled via the MX23 Loopback Activate register.

## Figure 33    - DS2 Loopback Diagram

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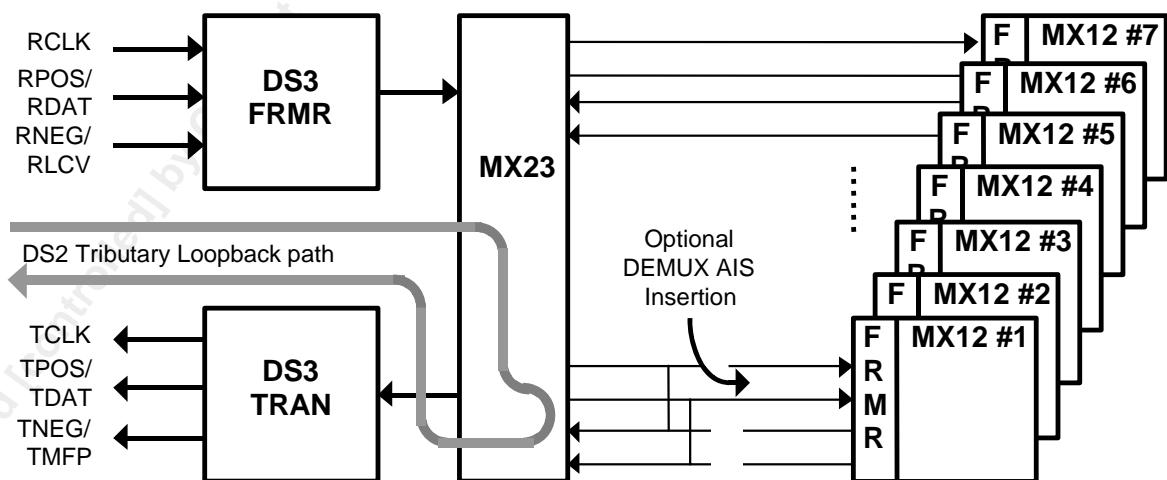
## 12.15 Telecom Bus Mapper/Demapper Loopback Modes

The TEMUX 84 provides two loopbacks at the telecom bus interface to aid in network and system diagnostics at the SONET/SDH interface. These loopback modes can be enabled via the microprocessor whenever the SONET/SDH block is enabled as the mapper for the T1/E1 framer slices or as the mapper for the DS3 framer or M13 Multiplexer.

### Telecom Diagnostic Loopback

The Telecom Bus Diagnostic Loopback allows the transmitted telecom bus stream to be looped back into the receive SONET/SDH receive path, overriding the data stream received on the telecom drop bus inputs. While Telecom diagnostic loopback is active, valid SONET/SDH data continues to be transmitted on the telecom add bus outputs. The entire telecom drop bus is overwritten by the diagnostic loopback even though only one STS-1 SPE, STM-1/VC4 TUG3 or STM-1/VC3 is generated by the egress VTPP onto the telecom add bus. This loopback is only available for VT1.5/VT2/TU11/TU12 mapped tributaries. DS3 mapped tributaries must use the DS3 diagnostic loopback. The telecom bus diagnostic loopback mode is shown diagrammatically in Figure 34.

**Figure 34       - Telecom Diagnostic Loopback Diagram**
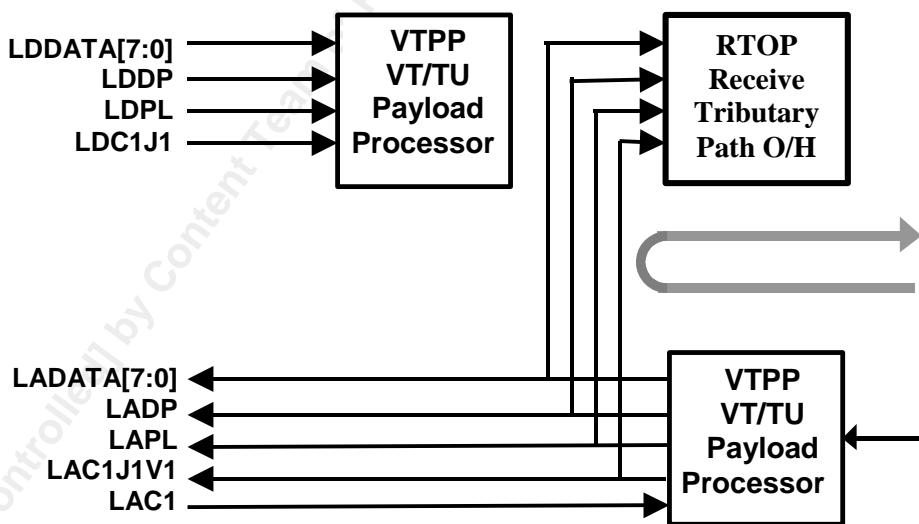


### Telecom Line Loopback

The Telecom Bus Line Loopback allows the received telecom drop bus data to be looped back out the telecom add bus after being processed by both the ingress

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and egress VTPPs. Both VTPP must be setup for the same STS-1 SPE, STM-1/VC4 TUG3 or STM-1/VC3 otherwise no loopback data will get through. The ingress data path is not affected by the telecom line loopback. This loopback is only available for VT1.5/VT2/TU11/TU12 mapped tributaries. DS3 mapped tributaries must use the DS3 line loopback. The Telecom bus line loopback mode is shown diagrammatically in Figure 35.

**Figure 35     - Telecom Line Loopback Diagram**
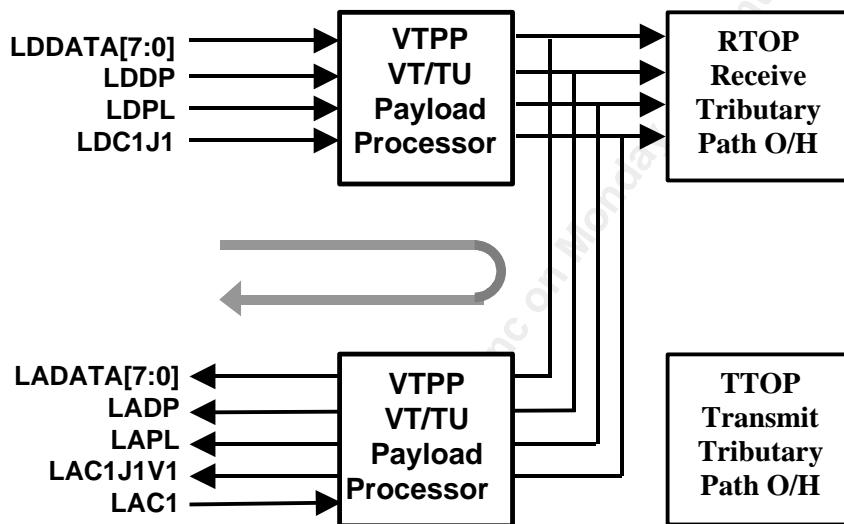


## 12.16  SBI Bus Data Formats

The TEMUX 84 uses the Scaleable Bandwidth Interconnect (SBI) bus as a high density link interconnect with devices processing T1s, E1s, DS3s, E3s, transparent virtual tributaries and arbitrary bandwidth payloads.  The SBI bus is a multi-point to multi-point bus capable of interconnecting up to four TEMUX 84 devices in parallel (if connected to a 77.76 MHz bus) with other link layer or tributary processing devices.

## Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1.  The SBI is also of fixed frequency and alignment as determined by the reference clock (SREFCLK) and frame indicator signals (SAC1FP and SDC1FP).  Frequency deviations are compensated by adjusting the location of the T1/E1/DS3/TVT1.5/TVT2 channels using floating

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tributaries as determined by the V5 indicator and payload signals (SDV5, SAV5, SDPL and SAPL). TVTs also allow for synchronous operation where SONET/SDH tributary pointers are carried within the SBI structure in place of the V5 indicator and payload signals (SDV5, SAV5, SDPL and SAPL).

Table 24 shows the bus structure for carrying T1, E1, TVT1.5, TVT2, DS3 and E3 tributaries in a SDH STM-1 like format. Up to 84 T1s, 63 E1s, 84 TVT1.5s, 63 TVT2s, 3 DS3s or 3 E3s are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (SAC1FP or SDC1FP) occurs during the octet labeled C1 in Row 1 column 7. The Add and Drop buses have independent frame signals to allow for arbitrary alignment of the two buses.

Table 24 represents a 19.44 Mbit/s signal. The structure is presented on a 77.76 MHz bus by byte interleaving it with three other like structures.

The multiplexed links are separated into three Synchronous Payload Envelopes called SPE1, SPE2 and SPE3. Each envelope carries up to 28 T1s, 21 E1, 28 TVT1.5s, 21 TVT2s, a DS3 or an E3. SPE1 carries the T1s numbered 1,1 through 1,28, E1s numbered 1,1 through 1,21, DS3 number 1,1 or E3 number 1,1. SPE2 carries T1s numbered 2,1 through 2,28, E1s numbered 2,1 through 2,21, DS3 number 2,1 or E3 number 2,1. SPE3 carries T1s numbered 3,1 through 3,28, E1s numbered 3,1 through 3,21, DS3 number 3,1 or E3 number 3,1. TVT1.5s are numbered the same as T1 tributaries and TVT2s are numbered the same as E1 tributaries.

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## Table 24      - Structure for Carrying Multiplexed Links

SBI Column



The TEMUX 84 when enabled for SBI interconnection will add and drop either 28 T1s, 21 E1s, a DS3 or an E3 into each of the three Synchronous Payload Envelopes, SPE1, SPE2 or SPE3. Each SPE is independent of the others. When T1 or E1 tributaries are sourced from the telecom bus via VT1.5, TU11, VT2 or TU12 mappings, the TEMUX 84 also supports a mix of transparent virtual tributaries with T1s and E1s. A restriction to this are that only VT1.5s, TU11s and T1s can be mixed together or VT2s, TU12s and E1s can be mixed together. Another restriction is that the telecom bus and SBI bus must run from the same clock with a fixed framing offset, ie. SREFCLK and LREFCLK are externally connected.

### Tributary Numbering

Tributary numbering for T1 and E1 uses the SPE number, followed by the Tributary number within that SPE and are numbered sequentially. Table 25 and Table 26 show the T1 and E1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure. Numbering for DS3 or E3 follows the same naming convention even though there is only one DS3 or E3 per SPE.  TVT1.5s and TVT2s follow the same numbering conventions as T1 and E1 tributaries respectively. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

## Table 25      - T1/TVT1.5 Tributary Column Numbering

| T1# | SPE1 Column | SPE2 Column | SPE3 Column | SBI Column |
|---|---|---|---|---|
| 1,1 | 7,35,63 | | | 19,103,187 |
| 2,1 | | 7,35,63 | | 20,104,188 |
| 3,1 | | | 7,35,63 | 21,105,189 |
| 1,2 | 8,36,64 | | | 22,106,190 |

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| | | | | |
|---|---|---|---|---|
| 2,2 | | 8,36,64 | | 23,107,191 |
| ••• | | | | |
| 1,28 | 34,62,90 | | | 100,184,268 |
| 2,28 | | 34,62,90 | | 101,185,269 |
| 3,28 | | | 34,62,90 | 102,186,270 |

**Table 26      - E1/TVT2 Tributary Column Numbering**

| E1# | SPE1 Column | SPE2 Column | SPE3 Column | SBI Column |
|---|---|---|---|---|
| 1,1 | 7,28,49,70 | | | 19,82,145,208 |
| 2,1 | | 7,28,49,70 | | 20,83,146,209 |
| 3,1 | | | 7,28,49,70 | 21,84,147,210 |
| 1,2 | 8,29,50,71 | | | 22,85,148,211 |
| 2,2 | | 8,29,50,71 | | 23,86,149,212 |
| ••• | | | | |
| 1,21 | 27,48,69,90 | | | 79,142,205,268 |
| 2,21 | | 27,48,69,90 | | 80,143,206,269 |
| 3,21 | | | 27,48,69,90 | 81,144,207,270 |

## SBI Timing Master Modes

The TEMUX 84 supports both synchronous and asynchronous SBI timing modes. Synchronous modes apply only to T1 and E1 tributaries and are used with ingress elastic stores to rate adapt the receive tributaries to the fixed SBI data rate. Asynchronous modes allow T1, E1, DS3 and transparent tributaries to float within the SBI structure to accommodate differences in timing.

In synchronous SBI mode, the T1 DS0s and E1 timeslots are in a fixed format and do not move relative to the SBI structure. The SBI frame pulse, SAC1FP or SDC1FP, in synchronous mode can be enabled to indicate CAS signaling multi-frame alignment by pulsing once every 12th 2KHz frame pulse period. SREFCLK sets the ingress rate from the receive elastic store.

In Asynchronous modes, timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures within the SBI. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations (H3 octet for DS3 and E3 mappings).  When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 or

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H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

Transparent VTs can float in the SBI structure in two ways. The first method uses valid V1 and V2 pointers to indicate positive and negative pointer justifications. The second methods uses the SBI signals SDV5, SAV5, SDPL and SAPL to indicate rate adjustments. In the DROP bus, the TEMUX 84 will always provide both valid pointers with valid SDV5 and SDPL signals. On the SBI Add Bus, the TEMUX 84 needs to be configured on a per tributary basis for either transparent VT mode. Transparent VT operation is configured on a per tributary basis via the ETVT and ETVTPTRDIS bits in the TTMP Tributary control registers.

On the DROP BUS the TEMUX 84 is timing master as determined by the arrival rate of data over the SBI.

On the ADD BUS the TEMUX 84 can be either the timing master or the timing slave. When the TEMUX 84 is the timing slave it receives its transmit timing information from the arrival rate of data across the SBI ADD bus. When the TEMUX 84 is the timing master it signals devices on the SBI ADD bus to speed up or slow down with the justification request signal, SAJUST_REQ. The TEMUX 84 as timing master indicates a speedup request to a Link Layer SBI device by asserting the justification request signal high during the V3 or H3 octet.  When this is detected by the Link Layer it will speed up the channel by inserting extra data in the next V3 or H3 octet.  The TEMUX 84 indicates a slow down request to the Link Layer by asserting the justification request signal high during the octet after the V3 or H3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

**Arbitrary Bandwidth Support**

Data streams of an arbitrary bit rate up to the capacitry of an SPE may be transported across the SPEs to and from the Flexible Bandwidth Ports.  When one (or more) of the SBI is programmed to support this, the SAPL and SDPL signals may be asserted and deasserted at arbitrary times to allow precise control of the payload bit rate.

On the DROP Bus, data received on the FBWDAT[3:1] signals are collected into complete bytes and are presented on SDDATA[7:0] with SDPL asserted high.  No flow control is implemented on the DROP bus.

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On the ADD Bus, the EFWBDREQ[3:1] signals request data at a specific rate. The data is read from a shallow FIFO. To keep the FIFO half full, the SAJUST_REQ output is asserted to fetch data across the ADD bus. In turn, the data source responds with data and the SAPL signal asserted an equal or less number of cycles than SAJUST_REQ is asserted. Significant latency is tolerated. Note that the some applications require an exact one-to-one correspondence between SAJUST_REQ and data bytes.

### SBI Link Rate Information

The TEMUX 84 SBI bus provides a method for carrying link rate information between devices. Two methods are specified, one for T1 and E1 channels and the second for DS3 and E3 channels. For T1 and E1, the link rate information is always generated on the Drop bus and always ignored on the Add bus. For DS3 and E3, only the ClkRate field of the link rate byte is valid on the Drop bus and the use is optional on the Add bus as specified by the CLK_MODE[1:0] bits of the EXSBI Tributary Control Indirect Access Data register. Link rate information is not available for TVTs. These methods use the reference 19.44 MHz SBI clock and the SAC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 and E1 method allows for a count of the number of T1 or E1 rising clock edges between 2 KHz SDC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the SDC1FP period. This method also counts the number of 19.44 MHz clock rising edges after sampling SDC1FP high to the next rising edge of the T1 or E1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 27.

Table 28 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Note that while the TEMUX 84 generates valid link rate information on the SBI Drop bus, it ignores the V4 byte on the Add bus.

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**Table 27        - SBI T1/E1 Link Rate Information**



| Bit # | 7 | 6 | 5:4 | 3:0 |
|-------|---|---|-----|-----|
| Link Rate Octet T1/E1 Format | ALM | 0 | ClkRate[1:0] | Phase[3:0] |
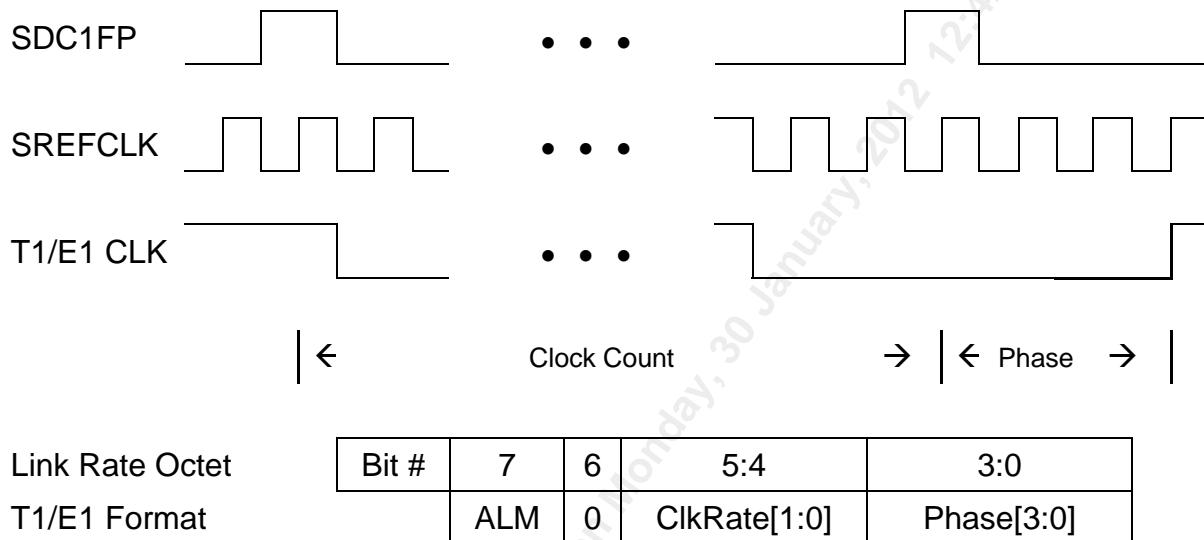
**Table 28        - SBI T1/E1 Clock Rate Encoding**

| ClkRate[1:0] | T1 Clocks / 2KHz | E1 Clocks / 2 KHz |
|--------------|------------------|-------------------|
| "00" – Nominal | 772 | 1024 |
| "01" – Fast | 773 | 1025 |
| "1x" – Slow | 771 | 1023 |

The method for transferring DS3 link rate information across the SBI passes the encoded count of DS3 clocks between 2KHz SAC1FP/SDC1FP pulses in the same method used for T1/E1 tributaries, but does not pass any phase information. The other difference from T1/E1 link rate is that ClkRate[1:0] indicates whether the nominal number of clocks are generated or if four fewer or four extra clocks are generated during the SAC1FP/SDC1FP period. The format of the DS3 link rate octet is shown in Table 29. This is passed across the SBI via the Linkrate octet which follows the H3 octet in the column, see Table 35. Table 30 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

N.B.  The ClkRate[1:0] information is not valid when the DS3 has been demapped from SONET/SDH by the D3MD function.

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**Table 29  - DS3 Link Rate Information**

| Link Rate Octet | Bit # | 7 | 6 | 5:4 | 3:0 |
|---|---|---|---|---|---|
| DS3 Format | | ALM | 0 | ClkRate[1:0] | Unused |

**Table 30  - DS3 Clock Rate Encoding**

| ClkRate[1:0] | DS3 Clocks / 2KHz |
|---|---|
| "00" – Nominal | 22368 |
| "01" – Fast | 22372 |
| "1x" – Slow | 22364 |

## SBI Alarms

The TEMUX 84 transfers alarm conditions across the SBI for T1, E1 and DS3 tributaries but not valid for transparent VTs.

Table 27 and Table 29 show the alarm indication bit, ALM, as bit 7 of the Link Rate Octet. Devices connecting to the TEMUX 84 which do not support alarm indications must set this bit to 0 on the SBI ADD bus.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. For T1 and E1 tributaries, either an out-of-frame condition or Red alarm (persistent out-of-frame) may set the ALM as determined by the IREDEN and IOOFEN per-tributary configuration bits. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. In the egress direction the TEMUX 84 can be configured to use the alarm bit to force AIS on a per link basis by the EALMEN or EGRALMEN register bits.

For DS3 and E3 Tributaries, the ALM bit reflects the alarm state of the receive tributary if the DS3ALME bit of the DS3/E3 Master Alarm Enable register is set to logic 1. For DS3, the propagated alarms are AIS and idle code with the option of either loss-of-signal and out-of-frame or RED alarm as selected by the REDALME bit of the DS3/E3 Master Alarm Enable register. For E3, the AIS, loss-of-signal and out-of-frame alarms are propagated.

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## T1 Tributary Mapping

Table 31 shows the format for mapping 84 T1s within the SPE octets.  The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications.  It is acceptable for the framing bit to not carry a valid framing bit on the Add Bus since the physical layer device will provide this information.  Unframed T1s use the exact same format for mapping 84 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1,V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface.  When enabled, the V4 octet is the Link Rate octet of Table 27.  It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus.  The V5 and R octets do not carry any information and are fixed to a zero value.  The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, DV5 and AV5, and payload signals, SDPL and SAPL.  The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead.  The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, SDV5 and SAV5, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location.  When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

## Table 31        - T1 Framing Format

| ROW # | COL #<br>1-18 | T1#1,1<br>19 | T1#2,1-3,28<br>20-102 | T1#1,1<br>103 | T1#2,1-3,28<br>104-186 | T1#1,1<br>187 | T1#2,1-3,28<br>188-270 |
|---|---|---|---|---|---|---|---|
| 1 | Unused | V1 | V1 | V5 | - | PPSSSSFR | - |
| 2 | Unused | DS0#1 | - | DS0#2 | - | DS0#3 | - |
| 3 | Unused | DS0#4 | - | DS0#5 | - | DS0#6 | - |
| 4 | Unused | DS0#7 | - | DS0#8 | - | DS0#9 | - |
| 5 | Unused | DS0#10 | - | DS0#11 | - | DS0#12 | - |
| 6 | Unused | DS0#13 | - | DS0#14 | - | DS0#15 | - |
| 7 | Unused | DS0#16 | - | DS0#17 | - | DS0#18 | - |
| 8 | Unused | DS0#19 | - | DS0#20 | - | DS0#21 | - |
| 9 | Unused | DS0#22 | - | DS0#23 | - | DS0#24 | - |

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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Unused | V2 | V2 | R | - | PPSSSSFR | - |
| 2 | Unused | DS0#1 | - | DS0#2 | - | DS0#3 | - |
| 3 | Unused | DS0#4 | - | DS0#5 | - | DS0#6 | - |
| 4 | Unused | DS0#7 | - | DS0#8 | - | DS0#9 | - |
| 5 | Unused | DS0#10 | - | DS0#11 | - | DS0#12 | - |
| 6 | Unused | DS0#13 | - | DS0#14 | - | DS0#15 | - |
| 7 | Unused | DS0#16 | - | DS0#17 | - | DS0#18 | - |
| 8 | Unused | DS0#19 | - | DS0#20 | - | DS0#21 | - |
| 9 | Unused | DS0#22 | - | DS0#23 | - | DS0#24 | - |
| 1 | Unused | V3 | V3 | R | - | PPSSSSFR | - |
| 2 | Unused | DS0#1 | - | DS0#2 | - | DS0#3 | - |
| 3 | Unused | DS0#4 | - | DS0#5 | - | DS0#6 | - |
| 4 | Unused | DS0#7 | - | DS0#8 | - | DS0#9 | - |
| 5 | Unused | DS0#10 | - | DS0#11 | - | DS0#12 | - |
| 6 | Unused | DS0#13 | - | DS0#14 | - | DS0#15 | - |
| 7 | Unused | DS0#16 | - | DS0#17 | - | DS0#18 | - |
| 8 | Unused | DS0#19 | - | DS0#20 | - | DS0#21 | - |
| 9 | Unused | DS0#22 | - | DS0#23 | - | DS0#24 | - |
| 1 | Unused | V4 | V4 | R | - | PPSSSSFR | - |
| 2 | Unused | DS0#1 | - | DS0#2 | - | DS0#3 | - |
| 3 | Unused | DS0#4 | - | DS0#5 | - | DS0#6 | - |
| 4 | Unused | DS0#7 | - | DS0#8 | - | DS0#9 | - |
| 5 | Unused | DS0#10 | - | DS0#11 | - | DS0#12 | - |
| 6 | Unused | DS0#13 | - | DS0#14 | - | DS0#15 | - |
| 7 | Unused | DS0#16 | - | DS0#17 | - | DS0#18 | - |
| 8 | Unused | DS0#19 | - | DS0#20 | - | DS0#21 | - |
| 9 | Unused | DS0#22 | - | DS0#23 | - | DS0#24 | - |

The $P_1P_0S_1S_2S_3S_4$FR octet carries T1 framing in the F bit and channel associated signaling in the $P_1P_0$ and $S_1S_2S_3S_4$ bits. Channel associated signaling is optional. The R bit is reserved and is set to 0. The $P_1P_0$ bits are used to indicate the phase of the channel associated signaling and the $S_1S_2S_3S_4$ bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 32 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-A24, B1-B24 in place of are A1-A24, B1-B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

When the SYNCH_TRIB bit is set for a tributary, the DS0 alignment is precisely as presented in Table 31, and the $P_1P_0$ and $S_1S_2S_3S_4$ bits in the first row of Table 32 are aligned to the multiframe indicated by the SDC1FP signal, be it an input or output. The F-bit positions in Table 32 have an arbitrary alignment relative to the

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$P_1P_0$ bits that will change with each controlled frame slip; that illustrated is only an example.  The signaling contained within the robbed bit positions of the DS0s will also have an arbitrary alignment relative to the $P_1P_0$ bits.

**Table 32      - T1 Channel Associated Signaling bits**

| | | | | SF | ESF | |
|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_3$ | $S_4$ | F | F | $P_1 P_0$ |
| A1 | A2 | A3 | A4 | F1 | M1 | 00 |
| A5 | A6 | A7 | A8 | S1 | C1 | 00 |
| A9 | A10 | A11 | A12 | F2 | M2 | 00 |
| A13 | A14 | A15 | A16 | S2 | F1 | 00 |
| A17 | A18 | A19 | A20 | F3 | M3 | 00 |
| A21 | A22 | A23 | A24 | S3 | C2 | 00 |
| B1 | B2 | B3 | B4 | F4 | M4 | 01 |
| B5 | B6 | B7 | B8 | S4 | F2 | 01 |
| B9 | B10 | B11 | B12 | F5 | M5 | 01 |
| B13 | B14 | B15 | B16 | S5 | C3 | 01 |
| B17 | B18 | B19 | B20 | F6 | M6 | 01 |
| B21 | B22 | B23 | B24 | S6 | F3 | 01 |
| C1 | C2 | C3 | C4 | F1 | M7 | 10 |
| C5 | C6 | C7 | C8 | S1 | C4 | 10 |
| C9 | C10 | C11 | C12 | F2 | M8 | 10 |
| C13 | C14 | C15 | C16 | S2 | F4 | 10 |
| C17 | C18 | C19 | C20 | F3 | M9 | 10 |
| C21 | C22 | C23 | C24 | S3 | C5 | 10 |
| D1 | D2 | D3 | D4 | F4 | M10 | 11 |
| D5 | D6 | D7 | D8 | S4 | F5 | 11 |
| D9 | D10 | D11 | D12 | F5 | M11 | 11 |
| D13 | D14 | D15 | D16 | S5 | C6 | 11 |
| D17 | D18 | D19 | D20 | F6 | M12 | 11 |
| D21 | D22 | D23 | D24 | S6 | F6 | 11 |

T1 tributary asynchronous timing is compensated via the V3 octet. T1 tributary link rate adjustments are optionally passed across the SBI via  the V4. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location.

In synchronous mode the T1 tributary mapping is fixed to that shown in Table 31 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

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## E1 Tributary Mapping

Table 33 shows the format for mapping 63 E1s within the SPE octets. The timeslots and framing bits within each E1 are easily located within this mapping for channelized E1 applications. It is acceptable for the framing bits to not carry valid framing information on the Add Bus since the physical layer device will provide this information. Unframed E1s use the exact same format for mapping 63 E1s into the SBI except that the E1 tributaries need not align with the timeslot locations associated with channelized E1 applications. The V1,V2 and V4 octets are not used to carry E1 data and are either reserved or used for control information across the interface. When enabled, the V4 octet carries clock phase information across the SBI. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries an E1 data octet but only during rate adjustments as indicated by the V5 indicator signals, SDV5 and SAV5, and payload signals, SDPL and SAPL. The PP octets carry channel associated signaling phase information and E1 multiframe alignment. TS#0 through TS#31 make up the E1 channel.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for E1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating E1 is identified via the V5 Indicator signals, SDV5 and SAV5, which locate the V5 octet. When the E1 tributary rate is faster than the E1 tributary nominal rate, the E1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the E1 tributary rate is slower than the nominal rate the E1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

When the SYNCH_TRIB bit is set for a tributary, the timeslot alignment is precisely as presented in Table 33.

## Table 33     – E1 Framing Format

| ROW # COL # | 1-18 | E1#1,1 19 | #2,1-3,21 20-81 | E1#1,1 82 | #2,1-3,21 83-144 | E1#1,1 145 | #2,1-3,21 146-207 | E1#1,1 208 | #2,1-3,21 209-270 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Unused | V1 | V1 | V5 | - | PP | - | TS#0 | - |
| 2 | Unused | TS#1 | - | TS#2 | - | TS#3 | - | TS#4 | - |
| 3 | Unused | TS#5 | - | TS#6 | - | TS#7 | - | TS#8 | - |
| 4 | Unused | TS#9 | - | TS#10 | - | TS#11 | - | TS#12 | - |
| 5 | Unused | TS#13 | - | TS#14 | - | TS#15 | - | TS#16 | - |
| 6 | Unused | TS#17 | - | TS#18 | - | TS#19 | - | TS#20 | - |

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| 7 | Unused | TS#21 | - | TS#22 | - | TS#23 | - | TS#24 | - |
| 8 | Unused | TS#25 | - | TS#26 | - | TS#27 | - | TS#28 | - |
| 9 | Unused | TS#29 | - | TS#30 | - | TS#31 | - | R | - |
| 1 | Unused | V2 | V2 | R | - | PP | - | TS#0 | - |
| 2 | Unused | TS#1 | - | TS#2 | - | TS#3 | - | TS#4 | - |
| 3 | Unused | TS#5 | - | TS#6 | - | TS#7 | - | TS#8 | - |
| 4 | Unused | TS#9 | - | TS#10 | - | TS#11 | - | TS#12 | - |
| 5 | Unused | TS#13 | - | TS#14 | - | TS#15 | - | TS#16 | - |
| 6 | Unused | TS#17 | - | TS#18 | - | TS#19 | - | TS#20 | - |
| 7 | Unused | TS#21 | - | TS#22 | - | TS#23 | - | TS#24 | - |
| 8 | Unused | TS#25 | - | TS#26 | - | TS#27 | - | TS#28 | - |
| 9 | Unused | TS#29 | - | TS#30 | - | TS#31 | - | R | - |
| 1 | Unused | V3 | V3 | R | - | PP | - | TS#0 | - |
| 2 | Unused | TS#1 | - | TS#2 | - | TS#3 | - | TS#4 | - |
| 3 | Unused | TS#5 | - | TS#6 | - | TS#7 | - | TS#8 | - |
| 4 | Unused | TS#9 | - | TS#10 | - | TS#11 | - | TS#12 | - |
| 5 | Unused | TS#13 | - | TS#14 | - | TS#15 | - | TS#16 | - |
| 6 | Unused | TS#17 | - | TS#18 | - | TS#19 | - | TS#20 | - |
| 7 | Unused | TS#21 | - | TS#22 | - | TS#23 | - | TS#24 | - |
| 8 | Unused | TS#25 | - | TS#26 | - | TS#27 | - | TS#28 | - |
| 9 | Unused | TS#29 | - | TS#30 | - | TS#31 | - | R | - |
| 1 | Unused | V4 | V4 | R | - | PP | - | TS#0 | - |
| 2 | Unused | TS#1 | - | TS#2 | - | TS#3 | - | TS#4 | - |
| 3 | Unused | TS#5 | - | TS#6 | - | TS#7 | - | TS#8 | - |
| 4 | Unused | TS#9 | - | TS#10 | - | TS#11 | - | TS#12 | - |
| 5 | Unused | TS#13 | - | TS#14 | - | TS#15 | - | TS#16 | - |
| 6 | Unused | TS#17 | - | TS#18 | - | TS#19 | - | TS#20 | - |
| 7 | Unused | TS#21 | - | TS#22 | - | TS#23 | - | TS#24 | - |
| 8 | Unused | TS#25 | - | TS#26 | - | TS#27 | - | TS#28 | - |
| 9 | Unused | TS#29 | - | TS#30 | - | TS#31 | - | R | - |

When using channel associated signaling (CAS) TS#16 carries the ABCD
signaling bits and the timeslots 17 through 31 are renumbered 16 through 30.
The PP octet is 0h for all frames except for the frame which carries the CAS for
timeslots 15/30 at which time the PP octet is C0h. The first octet of the CAS
multi-frame, RRRRRRRR, is reserved and should be ignored by the receiver
when CAS signaling is enabled. Table 34 shows the format of timeslot 16 when
carrying channel associated signaling.

## Table 34        - E1 Channel Associated Signaling bits

| TS#16[0:3] | TS#16[4:7] | PP |
|:---:|:---:|:---:|
| RRRR | RRRR | 00 |
| ABCD1 | ABCD16 | 00 |
| ABCD2 | ABCD17 | 00 |
| ABCD3 | ABCD18 | 00 |
| ABCD4 | ABCD19 | 00 |
| ABCD5 | ABCD20 | 00 |
| ABCD6 | ABCD21 | 00 |
| ABCD7 | ABCD22 | 00 |
| ABCD8 | ABCD23 | 00 |
| ABCD9 | ABCD24 | 00 |
| ABCD10 | ABCD25 | 00 |
| ABCD11 | ABCD26 | 00 |
| ABCD12 | ABCD27 | 00 |
| ABCD13 | ABCD28 | 00 |
| ABCD14 | ABCD29 | 00 |
| ABCD15 | ABCD30 | C0 |

E1 tributary asynchronous timing is compensated via the V3 octet. E1 tributary link rate adjustments are optionally passed across the SBI via  the V4 octet. E1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location.

In synchronous mode the E1 tributary mapping is fixed to that shown in Table 33 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

### DS3 Tributary Mapping

Table 35 shows a DS3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The DS3 framing format does not follow an 8KHz frame period so the floating DS3 multi-frame located by the V5 indicator, shown in heavy border grey region in Table 35, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will often be asserted twice per H1 frame, as is shown by the second V5 octet in Table 35. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

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**Table 35       - DS3 Framing Format**

| | SPE COL # | | DS3 1 | DS3 2-56 | DS3 57 | DS3 58-84 | DS3 Col 85 |
|---|---|---|---|---|---|---|---|
| ROW | SBI COL# 1,4,7,10 | 13 | 16 | ••• | 184 | ••• | 268 |
| 1 | Unused | **H1** | V5 | DS3 | DS3 | DS3 | DS3 |
| 2 | Unused | **H2** | DS3 | DS3 | DS3 | DS3 | DS3 |
| 3 | Unused | **H3** | DS3 | DS3 | DS3 | DS3 | DS3 |
| 4 | Unused | **Linkrate** | DS3 | DS3 | DS3 | DS3 | DS3 |
| 5 | Unused | Unused | DS3 | DS3 | DS3 | DS3 | DS3 |
| 6 | Unused | Unused | DS3 | DS3 | DS3 | DS3 | DS3 |
| 7 | Unused | Unused | DS3 | DS3 | DS3 | DS3 | DS3 |
| 8 | Unused | Unused | DS3 | DS3 | V5 | DS3 | DS3 |
| 9 | Unused | Unused | DS3 | DS3 | DS3 | DS3 | DS3 |

Because the DS3 tributary rate is less than the rate of the grey region, padding octets are interleaved with the DS3 tributary to make up the difference in rate. Interleaved with every DS3 multi-frame are 35 stuff octets, one of which is the V5 octet. These 35 stuff octets are spread evenly across seven DS3 subframes. Each DS3 subframe is eight blocks of 85 bits. The 85 bits making up a DS3 block are padded out to be 11 octets. Table 36 shows the DS3 block 11 octet format where R indicates a stuff bit, F indicates a DS3 framing bit and I indicates DS3 information bits. Table 37 shows the DS3 multi-frame format that is packed into the grey region of Table 35. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet and B indicates the 11 octet DS3 block. Each row in Table 37 is a DS3 multi-frame. The DS3 multi-frame stuffing format is identical for 5 multi-frames and then an extra stuff octet after the V5 octet is added every sixth frame.

**Table 36       - DS3 Block Format**

| Octet # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Data** | RRRFIIII | 8*I | 8*I | 8*I | 8*I | 8*I | 8*I | 8*I | 8*I | 8*I | 8*I |

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**Table 37        - DS3 Multi-frame Stuffing Format**

| V5 | 4*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| V5 | 4*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |
| V5 | 4*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |
| V5 | 4*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |
| V5 | 4*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |
| V5 | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B | 5*R | 8*B |

DS3 asynchronous timing is compensated via the H3 octet. DS3 link rate adjustments are optionally passed across the SBI via the Linkrate octet (N.B. The ClkRate[1:0] information is not valid when the DS3 has been demapped from SONET/SDH by the D3MD function.).  DS3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet.

## E3 Tributary Mapping

Table 38 shows a E3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The E3 framing format does not follow an 8KHz frame period so the floating frame located by the V5 indicator and shown in grey in Table 38, will jump around relative to the H1 frame on every pass.  In fact the V5 indicator will be asserted two or three times per H1 frame, as is shown by the second and third V5 octet in Table 38.  The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

## Table 38      - E3 Framing Format

| | SPE COL # | | E3 1 | E3 2-18 | E3 19 | E3 20-38 | E3 39 | E3 40-84 | E3 85 |
|---|---|---|---|---|---|---|---|---|---|
| ROW | SBI COL# 1,4,7,10 | 13 | 16 | ••• | 70 | ••• | 130 | ••• | 268 |
| 1 | Unused | **H1** | V5 | E3 | E3 | E3 | E3 | E3 | E3 |
| 2 | Unused | **H2** | E3 | E3 | E3 | E3 | E3 | E3 | E3 |
| 3 | Unused | **H3** | E3 | E3 | E3 | E3 | E3 | E3 | E3 |
| 4 | Unused | **Linkrate** | E3 | E3 | V5 | E3 | E3 | E3 | E3 |
| 5 | Unused | Unused | E3 | E3 | E3 | E3 | E3 | E3 | E3 |
| 6 | Unused | Unused | E3 | E3 | E3 | E3 | E3 | E3 | E3 |
| 7 | Unused | Unused | E3 | E3 | E3 | E3 | V5 | E3 | E3 |
| 8 | Unused | Unused | E3 | E3 | E3 | E3 | E3 | E3 | E3 |
| 9 | Unused | Unused | E3 | E3 | E3 | E3 | E3 | E3 | E3 |

When carrying framed E3, only the ITU-T Rec. G.751 format is supported. Unframed E3 is carried clear channel.

Because the E3 tributary rate is less than the rate of the gray region, padding octets are interleaved with the E3 tributary to make up the difference in rate. Interleaved with every E3 frame is an alternating pattern of 81 and 82 stuff octets, one of which is the V5 octet. These 81 or 82 stuff octets are spread evenly across the E3 frame. Each E3 subframe is 48 octet which is further broken into 4 equal blocks of 12 octets each. Table 39 shows the alternating E3 frame stuffing format that is packed into the gray region of Table 38. Note that there are 6 stuff octets after the V5 octet in one frame and 5 stuff octets after the V5 octet in the next frame. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet, D indicates an E3 data octet, FAS indicates the first byte of the 10 bit E3 Frame Alignment Signal.

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**Table 39      - E3 Frame Stuffing Format**

| V5 | 6*R | FAS | 11*D | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|----|-----|-----|------|-----|------|-----|------|-----|------|
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
| V5 | 5*R | FAS | 11*D | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |
|    | 5*R | 12*D |     | 5*R | 12*D | 5*R | 12*D | 5*R | 12*D |

E3 asynchronous timing is compensated via the H3 octet.  E3 link rate
adjustments are optionally passed across the SBI via the Linkrate octet.  E3
alarm conditions are optionally passed across the SBI bus via the Linkrate octet.

**Flexible Bandwidth Mapping**

When the OPMODE_SPEx[2:0] register bits for an SPE are binary 100, the SBI
is configured to transport an arbitrary bandwidth up to the capacity of an SPE.  In
this mode the SDPL and SAPL signals identify individual valid bytes.  For each
SPE, every third byte in columns 16 through 270, inclusive, has the potential for
presenting data.  Be aware that although columns 13 though 15 carry no
payload, the byte positions for rows 1 through 4 are driven by the Drop bus with
SDPL unconditionally low.

**Transparent VT1.5/TU11 Mapping**

VT1.5 and TU11 virtual tributaries, TVT1.5s, are transported across the SBI bus
in a similar manner to the T1 tributary mapping.  Table 40 shows the transparent
structure where "I" is used to indicate information bytes. There are two options
when carrying virtual tributaries on the SBI bus, the primary difference being how
the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT1.5/TU11 virtual
tributary indicated by the shaded region in Table 40. Locked is used to indicate
that the location of the V1,V2 pointer is locked.  The virtual tributary must have a
valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and
payload signals, SDV5, SAV5, SDPL and SAPL, may be generated but must be
ignored by the receiving device. In locked mode timing is always sourced by the

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transmitting side, therefore justification requests are not used and the SAJUST_REQ signal is ignored. Other than the V1 and V2 octets which must carry valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 40.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 40. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, SDV5, SAV5, SDPL and SAPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 40.

The TEMUX 84 supports both TVT modes simultaneously in the SBI DROP bus and is configurable on a per tributary basis in the SBI ADD bus.

## Table 40      - Transparent VT1.5/TU11 Format

|  | COL # | VT1.5#1,1 | #2,1-3,28 | VT1.5#1,1 | #2,1-3,28 | VT1.5#1,1 | #2,1-3,28 |
|---|---|---|---|---|---|---|---|
| **ROW #** | 1-18 | 19 | 20-102 | 103 | 104-186 | 187 | 188-270 |
| 1 | Unused | V1 | V1 | V5 | - | I | - |
| 2 | Unused | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - |
| 1 | Unused | V2 | V2 | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - |
| 1 | Unused | V3 | V3 | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - |

| 5 | Unused | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - |
| 1 | Unused | V4 | V4 | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - |

## Transparent VT2/TU12 Mapping

VT2 and TU12 virtual tributaries, TVT2s, are transported across the SBI bus in a similar manner to the E1 tributary mapping. The TEMUX 84 supports both TVT modes simultaneously in the SBI Drop bus and is configurable on a per tributary basis on the SBI ADD bus.

Table 41shows the transparent structure where "I" is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT2/TU12 virtual tributary indicated by the shaded region in Table 41.  The term locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, SDV5, SAV5, SDPL and SAPL, are optionally generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the SAJUST_REQ signal is ignored. Other than the V1 and V2 octets which are carrying valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 41.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 41.  In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, SDV5, SAV5, SDPL and SAPL, must be valid and are used to locate the floating payload. The justification

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request signal can be used to control the timing on the add bus. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 41.

The TEMUX 84 supports both TVT modes simultaneously in the SBI DROP bus and is configurable on a per tributary basis in the SBI ADD bus.

## Table 41 – Transparent VT2/TU12 Format

| ROW # | COL #<br>1-18 | E1#1,1<br>19 | #2,1-3,21<br>20-81 | E1#1,1<br>82 | #2,1-3,21<br>83-144 | E1#1,1<br>145 | #2,1-3,21<br>146-207 | E1#1,1<br>208 | #2,1-3,21<br>209-270 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Unused | V1 | V1 | V5 | - | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - | I | - |
| 1 | Unused | V2 | V2 | I | - | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - | I | - |
| 1 | Unused | V3 | V3 | I | - | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - | I | - |
| 8 | Unused | I | - | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - | I | - |
| 1 | Unused | V4 | V4 | I | - | I | - | I | - |
| 2 | Unused | I | - | I | - | I | - | I | - |
| 3 | Unused | I | - | I | - | I | - | I | - |
| 4 | Unused | I | - | I | - | I | - | I | - |
| 5 | Unused | I | - | I | - | I | - | I | - |
| 6 | Unused | I | - | I | - | I | - | I | - |
| 7 | Unused | I | - | I | - | I | - | I | - |

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| 8 | Unused | I | - | I | - | I | - | I | - |
| 9 | Unused | I | - | I | - | I | - | I | - |

## 12.17 H-MVIP Data Format

The H-MVIP data and Channel Associated Signaling interfaces on the TEMUX 84
are able to carry all the DS0s for the T1s or all timeslots for the E1s.  The E1s
and T1s may be mixed on a per TUG-3/DS3 basis, so each H-MVIP signal will be
carrying only E1 or T1 data.  When carrying timeslots from E1s the H-MVIP
frame is completely filled with 128 timeslots from four E1s but when carrying
DS0s from four T1s there are not enough DS0s to completely fill the 128 byte
frame.  Table 42 shows how the DS0s and CAS bits of four T1s are formatted in
the 128 timeslot H-MVIP frame.

Table 43 shows the timeslot and CAS bit H-MVIP format when in E1 mode.

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**Table 42    - Data and CAS T1 H-MVIP Format**

| Timeslot Number | First T1 DS0 Number | Second T1 DS0 Number | Third T1 DS0 Number | Fourth T1 DS0 Number |
|---|---|---|---|---|
| 0-3 | F-bit* | F-bit* | F-bit* | F-bit* |
| 4-7 | 1 | 1 | 1 | 1 |
| 8-11 | 2 | 2 | 2 | 2 |
| 12-15 | 3 | 3 | 3 | 3 |
| 16-19 | Undefined | Undefined | Undefined | Undefined |
| 20-23 | 4 | 4 | 4 | 4 |
| 24-27 | 5 | 5 | 5 | 5 |
| 28-31 | 6 | 6 | 6 | 6 |
| 32-35 | Undefined | Undefined | Undefined | Undefined |
| • | • | • | • | • |
| • | • | • | • | • |
| • | • | • | • | • |
| 108-111 | 21 | 21 | 21 | 21 |
| 112-115 | Undefined | Undefined | Undefined | Undefined |
| 116-119 | 22 | 22 | 22 | 22 |
| 120-123 | 23 | 23 | 23 | 23 |
| 124-127 | 24 | 24 | 24 | 24 |

*  For applications where the F-bit value is not overwritten by the transmitter, the least significant bit (latest in time) of this timeslot may be carried transparently.  In the ingress direction (i.e. MVID), the F-bit has an additional latency of 125us relative to the DS0 contents (i.e. It is presented at the beginning of the next frame after the one it was received with).

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**Table 43　　　- Data and CAS E1 H-MVIP Format**

| Timeslot Number | First E1 TS Number | Second E1 TS Number | Third E1 TS Number | Fourth E1 TS Number |
|---|---|---|---|---|
| 0-3 | 0 | 0 | 0 | 0 |
| 4-7 | 1 | 1 | 1 | 1 |
| 8-11 | 2 | 2 | 2 | 2 |
| 12-15 | 3 | 3 | 3 | 3 |
| 16-19 | 4 | 4 | 4 | 4 |
| • | • | • | • | • |
| • | • | • | • | • |
| • | • | • | • | • |
| 120-123 | 30 | 30 | 30 | 30 |
| 124-127 | 31 | 31 | 31 | 31 |

In the ingress direction, each CAS timeslot is encoded as follows (time increases to the right):

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|
| Unused | CGA | OOSMF | OOF | A | B | C | D |

The OOF bit is high when the framer has lost frame alignment.  The OOSMF bit is high when E1 signaling multiframe alignment has been lost.  It is also high when T1 frame alignment has been lost.  The CGA bit is high if an integrated AIS or RED alarm has been declared.

In the egress direction, each CAS timeslot is encoded as follows (time increases to the right):

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|
| Unused | Unused | SIGC[1] | SIGC[0] | A | B | C | D |

If the INBANDCTL bit of the TPCC Configuration register is logic 1, the SIGC[1:0] field takes on the same definition as the SIGC[1:0] context bits programmed

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through the TPCC Indirect Channel Data registers.  If INBANDCTL is logic 0, the SIGC[1:0] field is unused

In E1 mode, the H-MVIP Common Channel Signaling interface on TEMUX 84 carries timeslot 16 for ISDN signaling, timeslot 15 and timeslot 31 for V5.2 interfaces.  In T1 mode, the CCS H-MVIP interface only carries channel 28.  E1 and T1 signaling may be mixed on a DS-3/TUG-3 granularity.  Table 44 shows the H-MVIP format for carrying common channeling signaling and Time Slot 0 channels.  These formats are fixed so when a signaling or V5.2 channel is not in use the H-MVIP timeslot is filled with all ones.

**Table 44        - CCS and TS0 H-MVIP Format**

| H-MVIP Timeslot Number | CCSID[1], CCSED[1] | | CCSID[2], CCSED[2] | CCSID[3], CCSED[3] | TS0ID |
| | T1 Number (Ch 24) | E1 Number TS 16 | E1 Number TS 15 | E1 Number TS 31 | E1 Number TS0 |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 2 | 2 | 2 | 2 | 2 |
| 2 | 3 | 3 | 3 | 3 | 3 |
| 3 | 4 | 4 | 4 | 4 | 4 |
| 4 | 5 | 5 | 5 | 5 | 5 |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| 20 | 21 | 21 | 21 | 21 | 21 |
| 21 | 22 | undefined | undefined | undefined | undefined |
| 22 | 23 | undefined | undefined | undefined | undefined |
| 23 | 24 | undefined | undefined | undefined | undefined |
| 24 | 25 | undefined | undefined | undefined | undefined |
| 25 | 26 | undefined | undefined | undefined | undefined |
| 26 | 27 | undefined | undefined | undefined | undefined |
| 27 | 28 | undefined | undefined | undefined | undefined |

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| | | | | | |
|---|---|---|---|---|---|
| 28 | 29 | 22 | 22 | 22 | 22 |
| 29 | 30 | 23 | 23 | 23 | 23 |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | 41 | 41 | 41 | 41 |
| 48 | 49 | 42 | 42 | 42 | 42 |
| 49 | 50 | undefined | undefined | undefined | undefined |
| 50 | 51 | undefined | undefined | undefined | undefined |
| 51 | 52 | undefined | undefined | undefined | undefined |
| 52 | 53 | undefined | undefined | undefined | undefined |
| 53 | 54 | undefined | undefined | undefined | undefined |
| 54 | 55 | undefined | undefined | undefined | undefined |
| 55 | 56 | undefined | undefined | undefined | undefined |
| 56 | 57 | 43 | 43 | 43 | 43 |
| 57 | 58 | 44 | 44 | 44 | 44 |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| 75 | 76 | 62 | 62 | 62 | 62 |
| 76 | 77 | 63 | 63 | 63 | 63 |
| 77 | 78 | undefined | undefined | undefined | undefined |
| 78 | 79 | undefined | undefined | undefined | undefined |
| 79 | 80 | undefined | undefined | undefined | undefined |
| 80 | 81 | undefined | undefined | undefined | undefined |
| 81 | 82 | undefined | undefined | undefined | undefined |
| 82 | 83 | undefined | undefined | undefined | undefined |
| 83 | 84 | undefined | undefined | undefined | undefined |
| 84 | undefined | undefined | undefined | undefined | undefined |

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| 85 | undefined | undefined | undefined | undefined | undefined |
|-----|-----------|-----------|-----------|-----------|-----------|
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| • | • | • | • | • | • |
| 127 | undefined | undefined | undefined | undefined | undefined |

## 12.18 DS3 and Full Featured T1/E1 Pattern Generation and Detection

This section applies to the PRBS and fixed pattern generators and detectors accessible through the DS3/E3 PRGD Pseudo Random Pattern Generator and Detector Registers (0x0230 – 0x023F, 0x0330 – 0x033F, 0x0430 – 0x043F) and T1/E1 Pattern Generator and Detector Registers (0x0500 – 0x05B7).

The pattern generators can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 36 below:

**Figure 36     - PRGD Pattern Generator**



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

### Generating and detecting repetitive patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

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For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers.  The repetitive pattern will then be continuously generated.  The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream.  It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods.  It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences.  Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length.  The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

## Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T Recommendation O.151.  The register configurations required to generate these patterns and others are indicated in Table 45 and Table 46 below:

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## Table 45    - Pseudo Random Pattern Generation (PS bit = 0)

| Pattern Type | TR | LR | IR#1 | IR#2 | IR#3 | IR#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| $2^3$ -1 | 00 | 02 | FF | FF | FF | FF | 0 | 0 |
| $2^4$ -1 | 00 | 03 | FF | FF | FF | FF | 0 | 0 |
| $2^5$-1 | 01 | 04 | FF | FF | FF | FF | 0 | 0 |
| $2^6$ -1 | 04 | 05 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 | 00 | 06 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 (Fractional T1 LB Activate) | 03 | 06 | FF | FF | FF | FF | 0 | 0 |
| $2^7$ -1 (Fractional T1 LB Deactivate) | 03 | 06 | FF | FF | FF | FF | 1 | 1 |
| $2^9$ -1 (O.153) | 04 | 08 | FF | FF | FF | FF | 0 | 0 |
| $2^{10}$ -1 | 02 | 09 | FF | FF | FF | FF | 0 | 0 |
| $2^{11}$ -1 (O.152, O.153) | 08 | 0A | FF | FF | FF | FF | 0 | 0 |
| $2^{15}$ -1 (O.151) | 0D | 0E | FF | FF | FF | FF | 1 | 1 |
| $2^{17}$ -1 | 02 | 10 | FF | FF | FF | FF | 0 | 0 |
| $2^{18}$ -1 | 06 | 11 | FF | FF | FF | FF | 0 | 0 |
| $2^{20}$ -1 (O.153) | 02 | 13 | FF | FF | FF | FF | 0 | 0 |
| $2^{20}$ -1 (O.151 QRSS bit=1) | 10 | 13 | FF | FF | FF | FF | 0 | 0 |
| $2^{21}$ -1 | 01 | 14 | FF | FF | FF | FF | 0 | 0 |
| $2^{22}$ -1 | 00 | 15 | FF | FF | FF | FF | 0 | 0 |
| $2^{23}$ -1 (O.151) | 11 | 16 | FF | FF | FF | FF | 1 | 1 |
| $2^{25}$ -1 | 02 | 18 | FF | FF | FF | FF | 0 | 0 |
| $2^{28}$ -1 | 02 | 1B | FF | FF | FF | FF | 0 | 0 |
| $2^{29}$ -1 | 01 | 1C | FF | FF | FF | FF | 0 | 0 |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $2^{31}$ -1 | 02 | 1E | FF | FF | FF | FF | 0 | 0 |

**Table 46 - Repetitive Pattern Generation (PS bit = 1)**

| Pattern Type | TR | LR | IR#1 | IR#2 | IR#3 | IR#4 | TINV | RINV |
|---|---|---|---|---|---|---|---|---|
| All ones | 00 | 00 | FF | FF | FF | FF | 0 | 0 |
| All zeros | 00 | 00 | FE | FF | FF | FF | 0 | 0 |
| Alternating ones/zeros | 00 | 01 | FE | FF | FF | FF | 0 | 0 |
| Double alternating ones/zeros | 00 | 03 | FC | FF | FF | FF | 0 | 0 |
| 3 in 24 | 00 | 17 | 22 | 00 | 20 | FF | 0 | 0 |
| 1 in 16 | 00 | 0F | 01 | 00 | FF | FF | 0 | 0 |
| 1 in 8 | 00 | 07 | 01 | FF | FF | FF | 0 | 0 |
| 1 in 4 | 00 | 03 | F1 | FF | FF | FF | 0 | 0 |
| Inband loopback activate | 00 | 04 | F0 | FF | FF | FF | 0 | 0 |
| Inband loopback deactivate | 00 | 02 | FC | FF | FF | FF | 0 | 0 |

Notes for the Pseudo Random and Repetitive Pattern Generation Tables

 The PS bit and the QRSS bit are contained in the PRGD Control register

 TR = PRGD Tap Register

 LR = PRGD Length Register

 IR#1 = PRGD Pattern Insertion #1 Register

 IR#2 = PRGD Pattern Insertion #2 Register

 IR#3 = PRGD Pattern Insertion #3 Register

 IR#4 = PRGD Pattern Insertion #4 Register

 The TINV bit and the RINV bit are contained in the PRGD Control register

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## 12.19  JTAG Support

The TEMUX 84 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards.  The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers.  The TRSTB input is the active-low reset signal used to reset the TAP controller.  TCK is the test clock used to sample data on input, TDI and to output data on output, TDO.  The TMS input is used to direct the TAP controller through its states.  The basic boundary scan architecture is shown below.

**Figure 37      - Boundary Scan Architecture**

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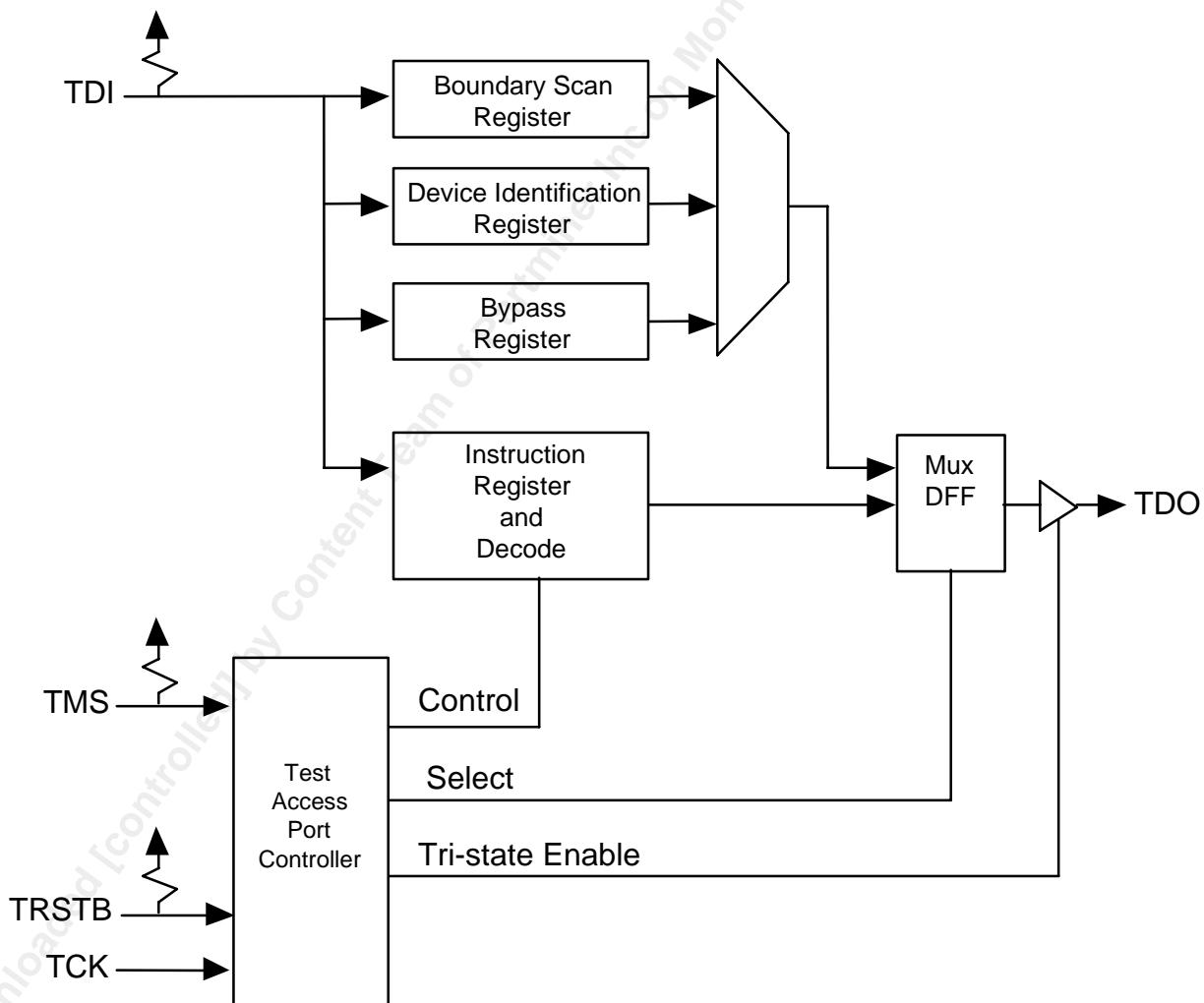
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

## 12.19.1    TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

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**Figure 38　　- TAP Controller Finite State Machine**



All transitions dependent on input TMS

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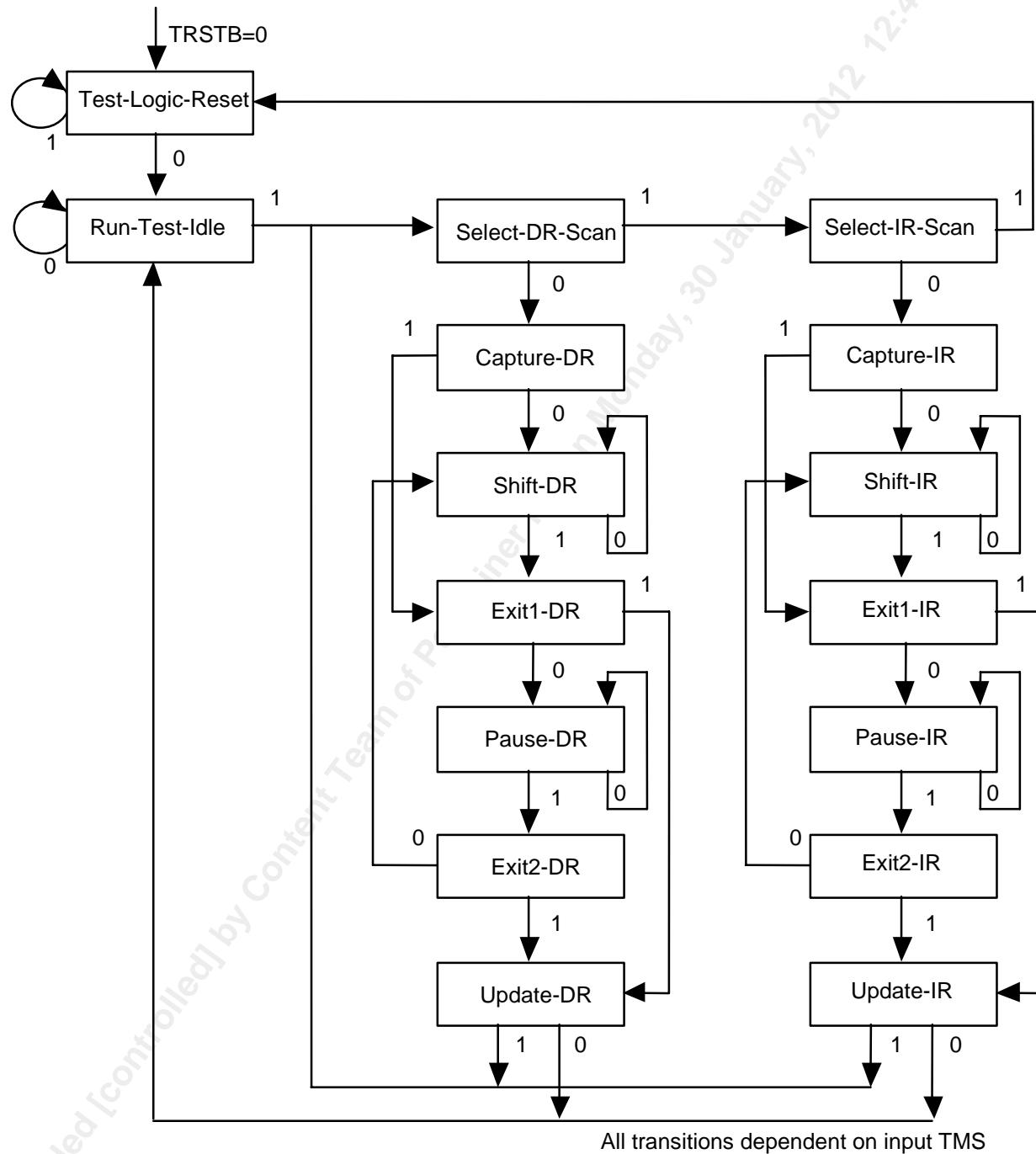
### Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

### Run-Test-Idle

The run test/idle state is used to execute tests.

### Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

### Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

### Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

### Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

### Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

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### Update-IR

The update instruction register state is used to load a new instruction into the instruction register.  The new instruction must be scanned in using the Shift-IR state.  The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

### Boundary Scan Instructions

The following is a description of the standard instructions.  Each instruction selects a serial test data register path between input, TDI and output, TDO.

### BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay.  The instruction is used to bypass the device.

### EXTEST

The external test instruction allows testing of the interconnection to other devices.  When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO.  Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state.  The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.  Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

### SAMPLE

The sample instruction samples all the device inputs and outputs.  For this instruction, the boundary scan register is placed between TDI and  TDO.  Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state.  The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

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### IDCODE

The identification instruction is used to connect the identification register between TDI and TDO.  The device's identification code can then be shifted out using the Shift-DR state.

### STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test.  When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO.  During the Capture-DR state, the device identification code is loaded into the boundary scan register.  The code can then be shifted out of the output, TDO, using the Shift-DR state.

### Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise.  The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table in the JTAG Test Port section 11.2.

### Figure 39       - Input Observation Cell (IN_CELL)

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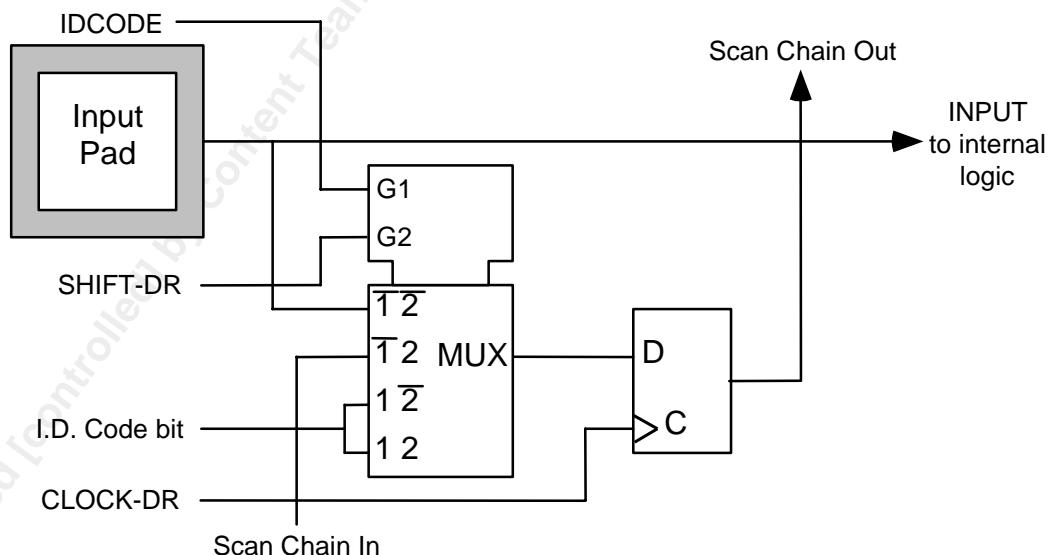
**Figure 40　　- Output Cell (OUT_CELL)**

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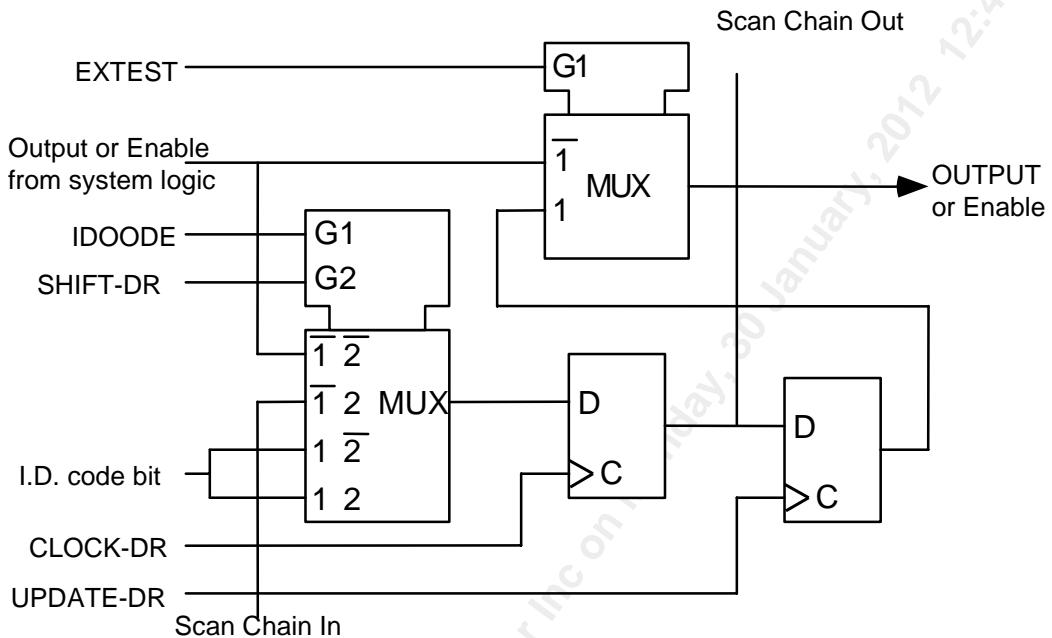
## Figure 41        - Bidirectional Cell (IO_CELL)
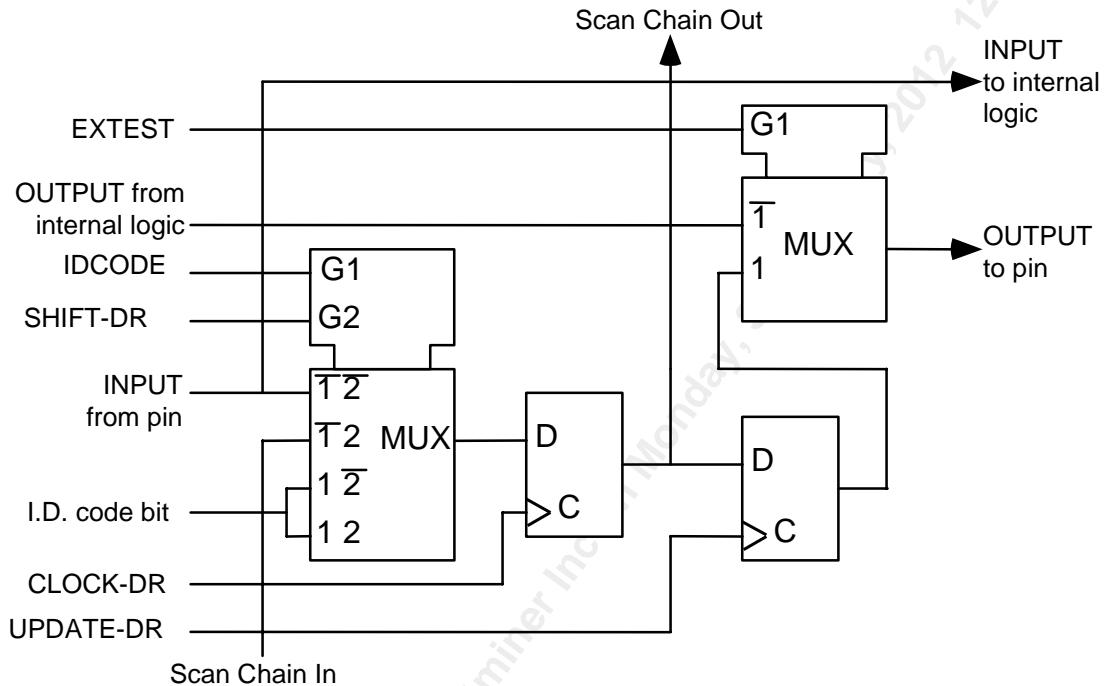


## Figure 42        - Layout of Output Enable and Bidirectional Cells

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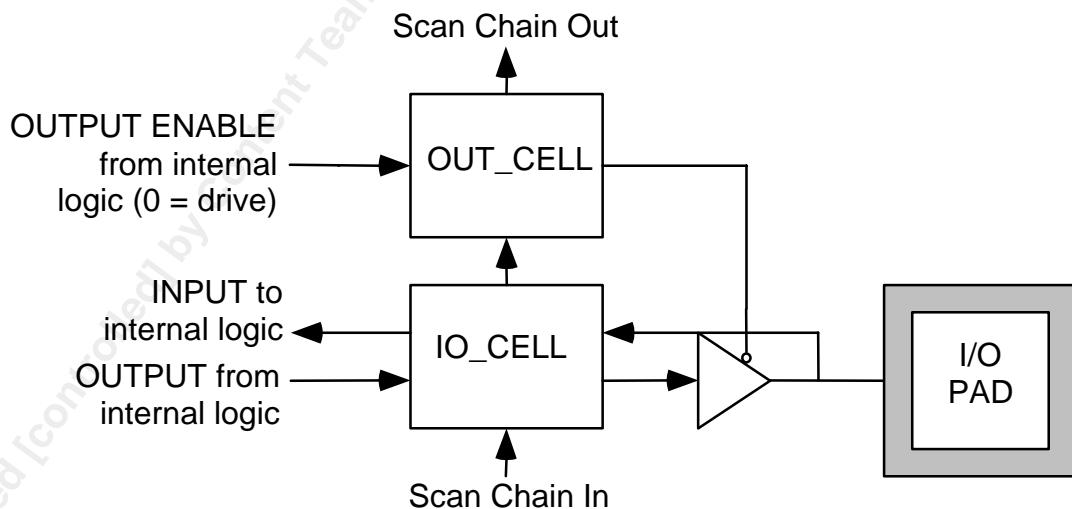
## 12.20  Configuring the Line Side SBI

This interface enables high-density, byte-serial SBI connectivity of the TEMUX 84 to PMC-Sierra's high-density T1/E1/J1 line interface units: PM4318 OCTLIU and PM4319 OCTLIU-SH.  Further, TEMUX 84's system-side SBI bus will still be available to seamlessly connect to the industry's highest-density link-layer devices, offered by PMC-Sierra, Inc. (S/UNI-IMA, FREEDM, AAL1gator, SBS family of devices).

### 12.20.1        Hardware

For the TEMUX 84 to use its line side SBI interface to connect with PM4318
OCTLIU or PM4319 OCTLIU-SH, the pin connection diagram shown below in
Figure 43 must be used:

**Figure 43      -Pin Connection Diagram for Line Side SBI**
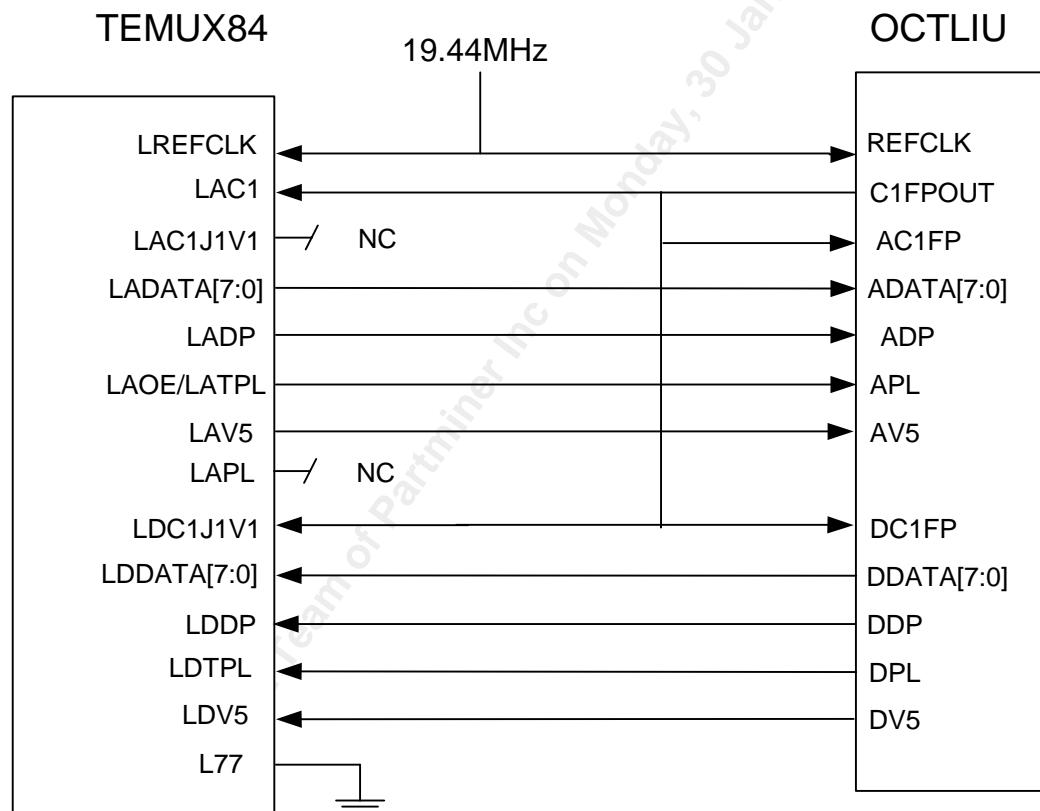


## Software

Using the line side SBI mode essentially means that the device is acting as a
T1/E1/J1 Framer only.  This line side interface will typically be connected to
multiple PMC-Sierra's T1/E1/J1 line interface units, PM4318 OCTLIU or PM4319
OCTLIU-SH.

The line side SBI bus is based upon the Byte-Synchronous Mapper mode,
currrently documented in the TEMUX 84 Register Descriptions (PMC-2000034).

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Therefore, one would essentially configure the TEMUX 84 for Byte Synchronous Mapper mode and with the following modifications to software; the Byte-Synchronous Mappers will simulate the SBI bus format:

1. Set IVTPPBYP=1 in Register 0x0701

2. Set EVTPPBYP=1 in Register 0x0704

3. Set LAJ1EN=1 in Register 0x0702

4. Set LAV1EN=1 in Register 0x0702

5. Set ITUG3=1 in Register 0x0704

6. Set OTUG3=1 in Register 0x0704

7. Set Reserved bit 7 in Register 0x0700 to '1'

8. Set LATPLSEL=1 in Register 0x704

9. Set OTUG3=1 in Register 0x0703

10. Set EPTRBYP[3:1]= '111' in Register 0x0704

11. Set Bit 7 in Register 0x0040 to 1

12. Set FI_EMPTY_ENBL=1 in Register 0x09EF

When enabling the individual tributaries in the Byte Synchronous Mapper:

1. Set the TRIB_TYP bits to '01'

2. Set ENBL=1

When enabling the individual tributaries in the Byte Synchronous Demapper:

1. Set ENBL=1.

In additional all TU11 bits in the device must be configured correctly. For T1 operation all TU11 bits must be set to 1, for E1 all TU11 bits must be set to 0.

The above-listed register accesses will enable connectivity between the TEMUX 84 device and multiple OCTLIU devices over TEMUX 84's line side SBI interface. The next revision of the production-release TEMUX 84 Software Device Driver will include support for line side SBI.

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## 13    **FUNCTIONAL TIMING**

### 13.1  **DS3 Line Side Interface Timing**

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the TEMUX 84 registers are set to their default states).

**Figure 44    - Receive Bipolar DS3 Stream**
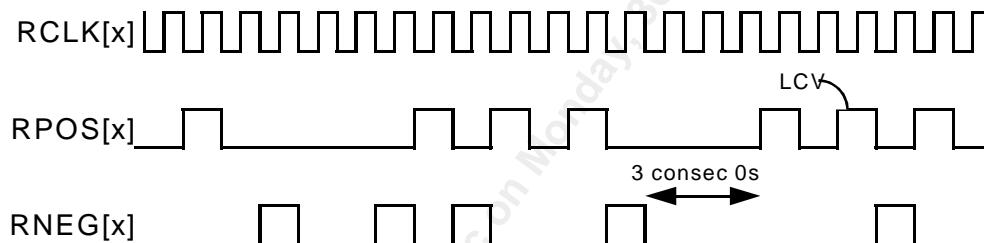


The Receive Bipolar DS3 Stream diagram (Figure 44) shows the operation of the TEMUX 84 while processing a B3ZS encoded DS3 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

**Figure 45    - Receive Unipolar DS3 Stream**
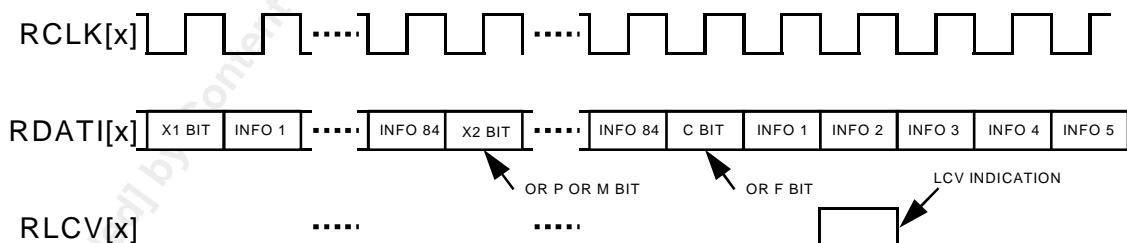


The Receive Unipolar DS3 Stream diagram (Figure 45) shows the complete DS3 receive signal on the RDAT input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

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**Figure 46        - Receive Bipolar E3 Stream**

HDB3 Signature Pattern

| X | 0 | 0 | V |

RCLK[x]

RPOS[x]

RNEG[x]

LCV       4 consec 0s

B  0   0  V

0   0   0  V
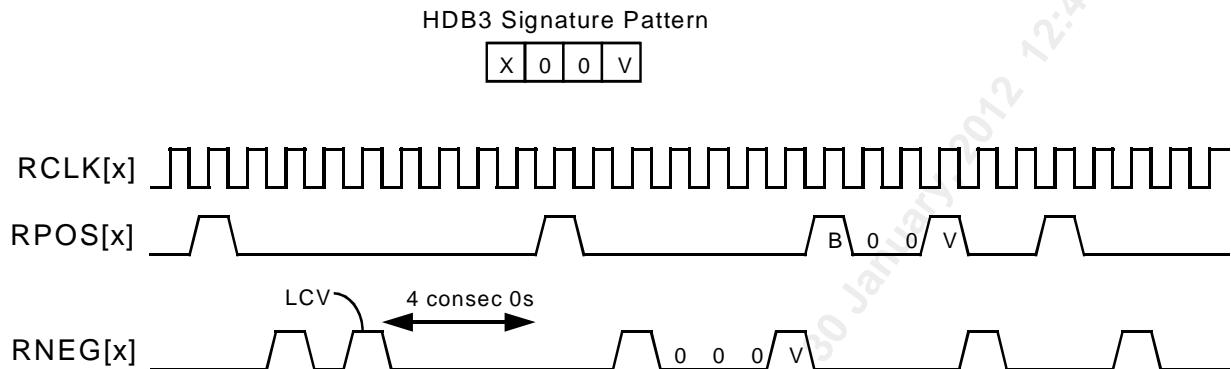
The Receive Bipolar E3 Stream diagram (Figure 46) shows the operation of the
TEMUX 84 while processing an HDB3-encoded E3 stream on inputs RPOS[x]
and RNEG[x].  It is assumed that the first bipolar violation (on RNEG[x])
illustrated corresponds to a valid HDB3 signature.  A line code violation is
declared upon detection of four consecutive zeros in the incoming stream, or
upon detection of a bipolar violation which is not part of a valid HDB3 signature.

**Figure 47        - Receive Unipolar E3 Stream**

RCLK[x]

RDATI[x]

| FA1₁ | FA1₂ | · · · · · | INFO X | INFO X+1 | · · · · · | INFO N | INFO N+1 | INFO N+2 | INFO N+3 | INFO N+4 | INFO N+5 | INFO N+6 |

LCV INDICATION

RLCV[x]
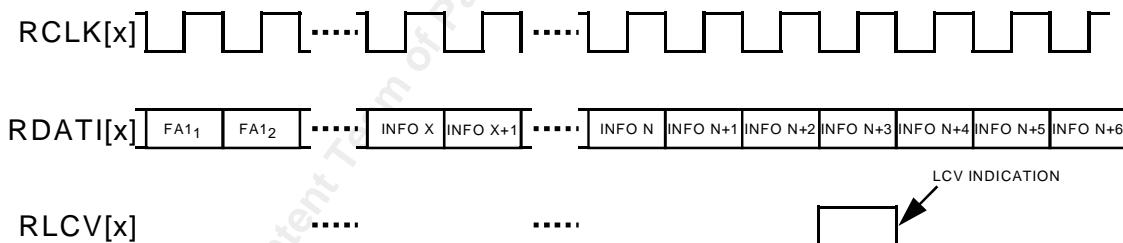
The Receive Unipolar E3 Stream diagram (Figure 47) shows the unipolar E3
receive signal on the RDATI[x] input.  Line code violation indications, detected by
an upstream HDB3 decoder, are indicated on input RLCV.  RLCV is sampled
each bit period.  The PMON Line Code Violation Event Counter is incremented
each time a logic 1 is sampled on RLCV.

### Figure 48        - Transmit Bipolar DS3 Stream
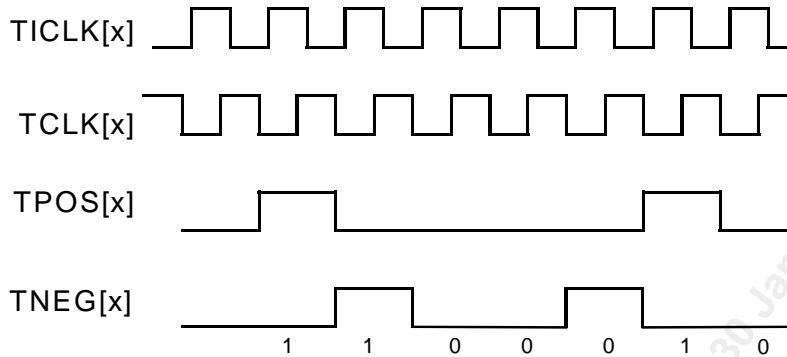


The Transmit Bipolar DS3 Stream diagram illustrates the generation of a bipolar DS3 stream.  The B3ZS encoded DS3  stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit.  Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

### Figure 49        - Transmit Unipolar DS3 Stream
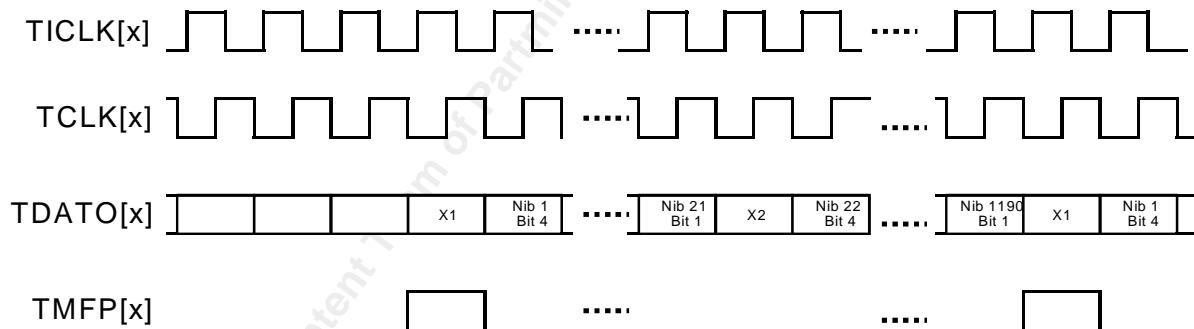


The Transmit Unipolar DS3 Stream diagram (Figure 49) illustrates the unipolar DS3 stream generation. The TMFP output marks the M-frame boundary, X1 bit, in the transmit stream.  Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

**Figure 50        - Transmit Bipolar E3 Stream**



HDB3 Signature Pattern
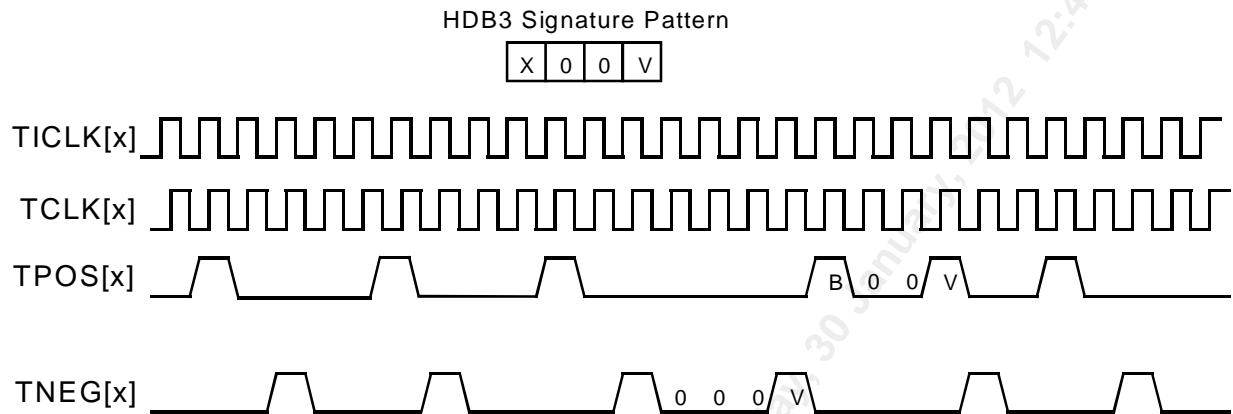
The Transmit Bipolar E3 Stream diagram (Figure 50) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

**Figure 51        - Transmit Unipolar E3 Stream**
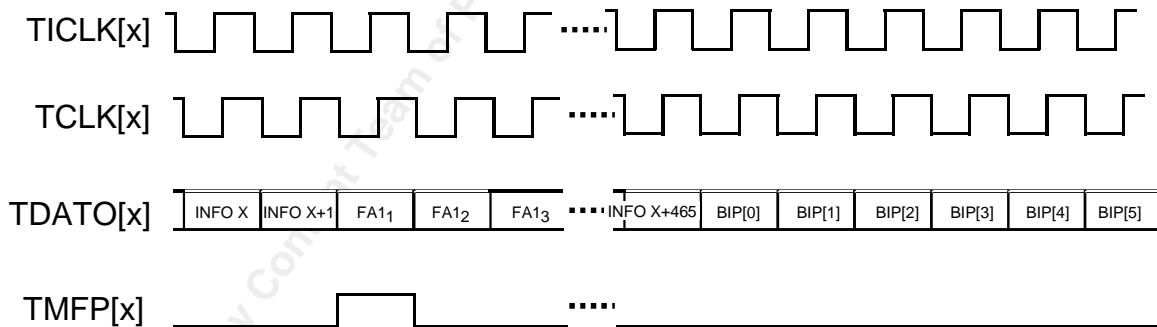


The Transmit Unipolar E3 Stream diagram (Figure 51) illustrates the unipolar E3 stream generation. The TMFP output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

## 13.2 DS3 and E3 System Side Interface Timing

### Figure 52    - Framer Mode DS3 Transmit Input Stream
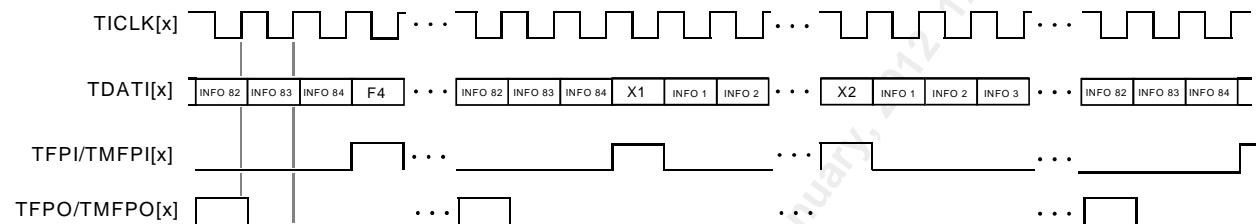


### Figure 53    - Framer Mode DS3 Transmit Input Stream With TGAPCLK
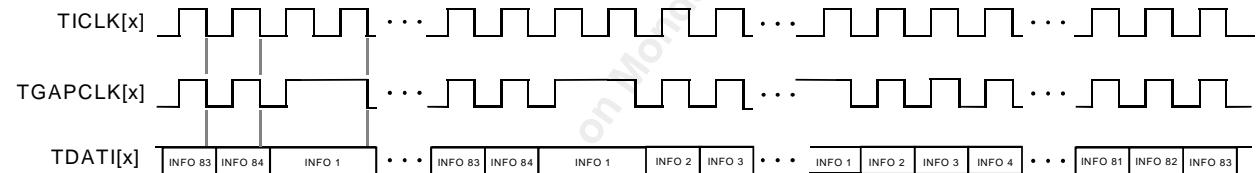


The Framer Mode DS3 Transmit Input Stream diagram (Figure 52) shows the expected format of the inputs TDAT and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the OPMODE_SPEx[2:0] bits are set to "DS3/E3 Framer Only mode" in the SPE Configuration registers.  If the TXMFPI bit in the DS3 and E3 Master Unchannelized Interface Options register is logic 0, then TFPI is valid, and the TEMUX 84 will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI.  If the TXMFPI register bit is logic 1, then TMFPI is valid, and the TEMUX 84 will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI.  If the TXMFPO bit in the DS3 and E3 Master Unchannelized Interface Options register is logic 0, then TFPO is valid, and the TEMUX 84 will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse.  If the TXMFPO register bit is logic 1, then TMFPO is valid and the TEMUX 84 will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse.  The alignment of TFPO or TMFPO is arbitrary.  There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.  The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register is set to logic 1, as in Figure 53.  TGAPCLK remains high during the overhead bit positions.

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### Figure 54 - Framer Mode DS3 Receive Output Stream
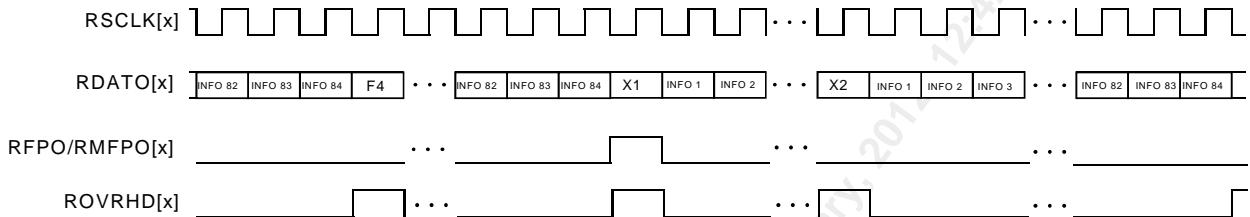


### Figure 55 - Framer Mode DS3 Receive Output Stream with RGAPCLK
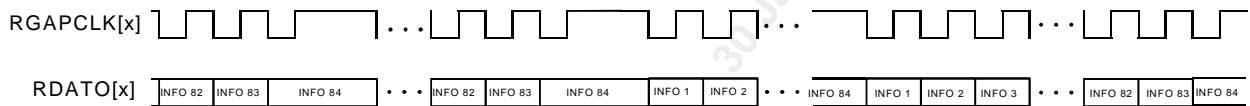


The DS3/E3 Framer Only Mode Receive Output Stream diagram (Figure 54) shows the format of the outputs RDATO, RFPO/RMFPO, RSCLK ROVRHD when the OPMODE_SPEx[2:0] bits are set to "DS3/E3 Framer Only mode" in the SPE Configuration registers. Figure 54 shows the data streams when the TEMUX 84 is configured for the DS3 receive format. If the RXMFPO bit in the DS3 and E3 Master Unchannelized Interface Options register is logic 0, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic 1 (as shown Figure 54), RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. Figure 55 shows the output data stream with RGAPCLK in place of RSCLK when the RXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register set to logic 1. RGAPCLK remains high during the overhead bit positions.

### Figure 56 - Framer Mode G.751 E3 Transmit Input Stream
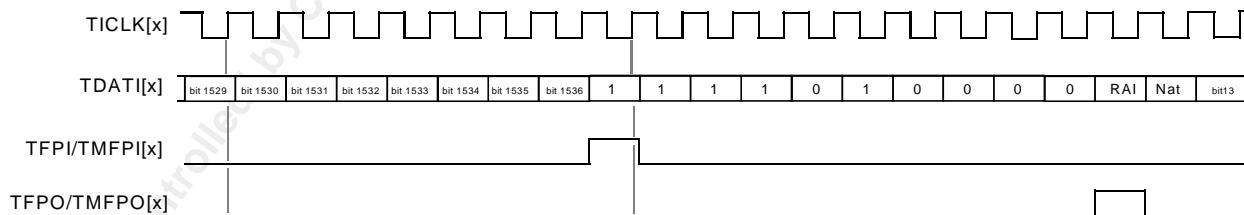
### Figure 57        - Framer Mode G.751 E3 Transmit Input Stream With TGAPCLK
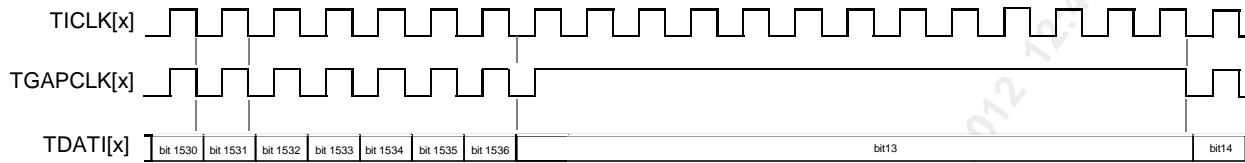


The Framer Mode G.751 E3 Transmit Input Stream diagrams (Figure 56 and Figure 57) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the TEMUX 84 is configured for the E3 G.751 transmit format.  TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the frame alignment signal in the G.751 E3 input data stream on TDATI.  TFPO or TMFPO will pulse high for one out of every 1536 TICLK cycles, providing upstream equipment with a reference frame pulse.  The alignment of TFPO or TMFPO is arbitrary.  There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.  The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register is set to logic 1, as in Figure 57. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

### Figure 58        - Framer Mode G.751 E3 Receive Output Stream
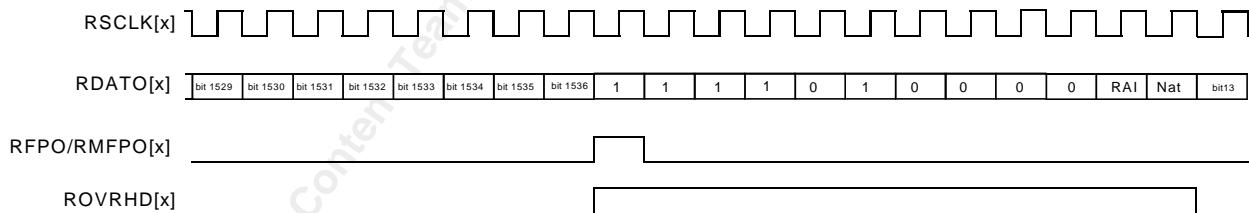


### Figure 59        - Framer Mode G.751 E3 Receive Output Stream with RGAPCLK
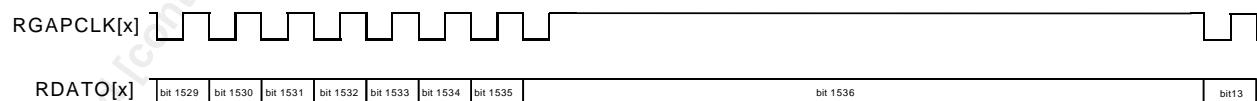


The Framer Mode G.751 E3 Receive Output Stream diagrams (Figure 58 and Figure 59) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and

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RGAPCLK), and ROVRHD when the TEMUX 84 is configured for the E3 G.751 receive format.  RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the framing alignment signal in the G.751 E3 output data stream on RDATO.  ROVRHD will be high for every overhead bit position on the RDATO data stream.  If the PYLD&JUST register bit in the E3 FRMR Maintenance Options register is set to logic 0, the $C_{jk}$ and $P_k$ bits in the RDATO stream will be marked as overhead bits.  If the PYLD&JUST register bit is set to logic 1, the $C_{jk}$ and $P_k$ bits in the RDATO stream will be marked as payload.  The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register is set to logic 1. RGAPCLK remains high during the overhead bit positions as shown in Figure 59.

**Figure 60      - Framer Mode G.832 E3 Transmit Input Stream**
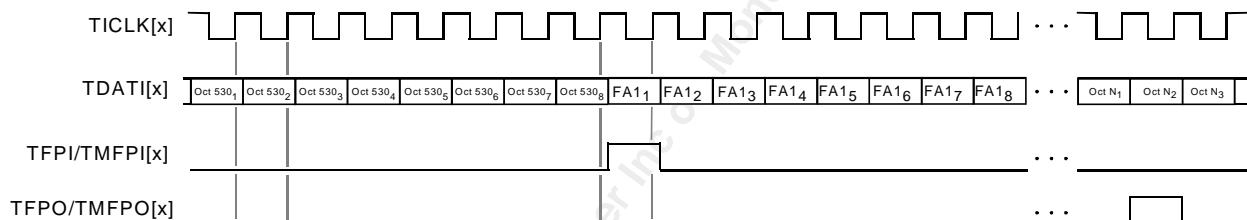


**Figure 61      - Framer Mode G.832 E3 Transmit Input Stream With TGAPCLK**
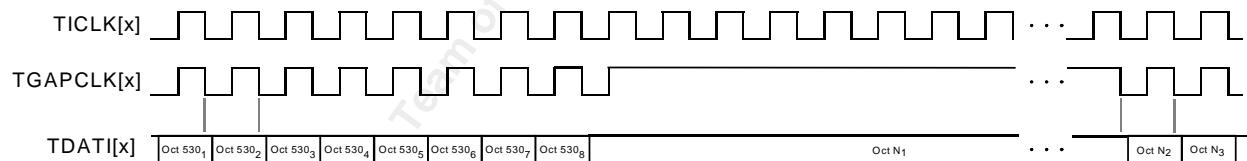


The Framer Mode G.832 E3 Transmit Input Stream diagrams (Figure 60 and Figure 61) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the TEMUX 84 is configured for the E3 G.832 transmit format.  TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 input data stream on TDATI.  TFPO or TMFPO will pulse high for one out of every 4296 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary.  There is no set relationship between TFPO/TMFPO and TFPI/TMFPI.  The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the DS3 and E3 Master Unchannelized Interface Options register is set to logic 1, as in Figure 61. TGAPCLK remains high during the overhead bit positions.  TDATI is sampled on the falling edge of TGAPCLK.

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**Figure 62       - Framer Mode G.832 E3 Receive Output Stream**
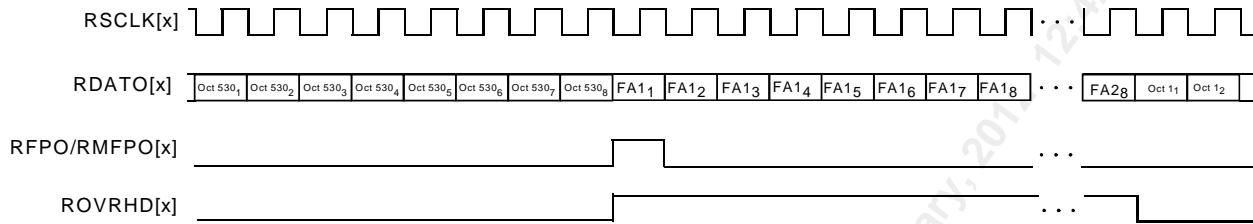


**Figure 63       - Framer Mode G.832 E3 Receive Output Stream with RGAPCLK**
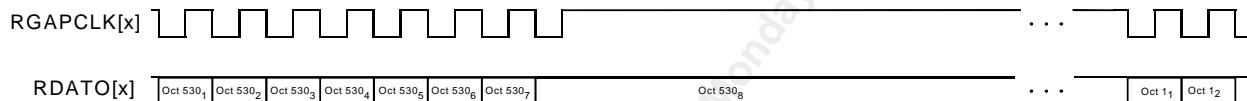


The Framer Mode G.832 E3 Receive Output Stream diagrams (Figure 62 and
Figure 63) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and
RGAPCLK), and ROVRHD when the TEMUX 84 is configured for the E3 G.832
receive format.  RFPO or RMFPO pulses high for one RSCLK cycle and is
aligned to the first bit of the FA1 byte in the G.832 E3 output data stream on
RDATO.  ROVRHD will be high for every overhead bit position on the RDATO
data stream.  The RGAPCLK output is available in place of RSCLK when the
RXGAPEN bit in DS3 and E3 Master Unchannelized Interface Options  register is
set to logic 1.  RGAPCLK remains high during the overhead bit positions as
shown in Figure 63.

## 13.3  Telecom DROP Bus Interface Timing

Figure 64 shows the function of the various telecom DROP bus signals in AU3
mode when LREFCLK is nominally 19.44 MHz.  Data on LDDATA[7:0] is sampled
on the rising edge of LREFCLK.  The bytes forming the three STS-1 synchronous
payload envelopes are identified when the LDPL signal is high.  In this diagram, a
negative stuff event is shown occurring on STS-1 #2 and a positive stuff event on
STS-1 #3.  The LDC1J1V1 signal pulses high, while LDPL is set low, to mark the
C1 byte of the first STS-1 in every frame of the STS-3 transport envelope.  The
LDC1J1V1 signal is high when the LDPL signal is high to mark every J1 byte of
each of the three STS-1 SPEs. The bytes forming the various tributary
synchronous payload envelopes are identified by the LDTPL when set high.  The
LDV5 signal pulses high to mark the V5 bytes of each tributary.  LDTPL and
LDV5 are invalid when LDPL is set low.  The three STS-1 SPEs can each have

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different alignments to the STS-3 transport envelope and the alignment is
changing for two of the STS-1 SPEs (STS-1 #2 and #3) due to the pointer
justification events shown.

### Figure 64    - 19.44 MHz Telecom DROP Bus Timing - STS-1 SPEs / AU3 VCs
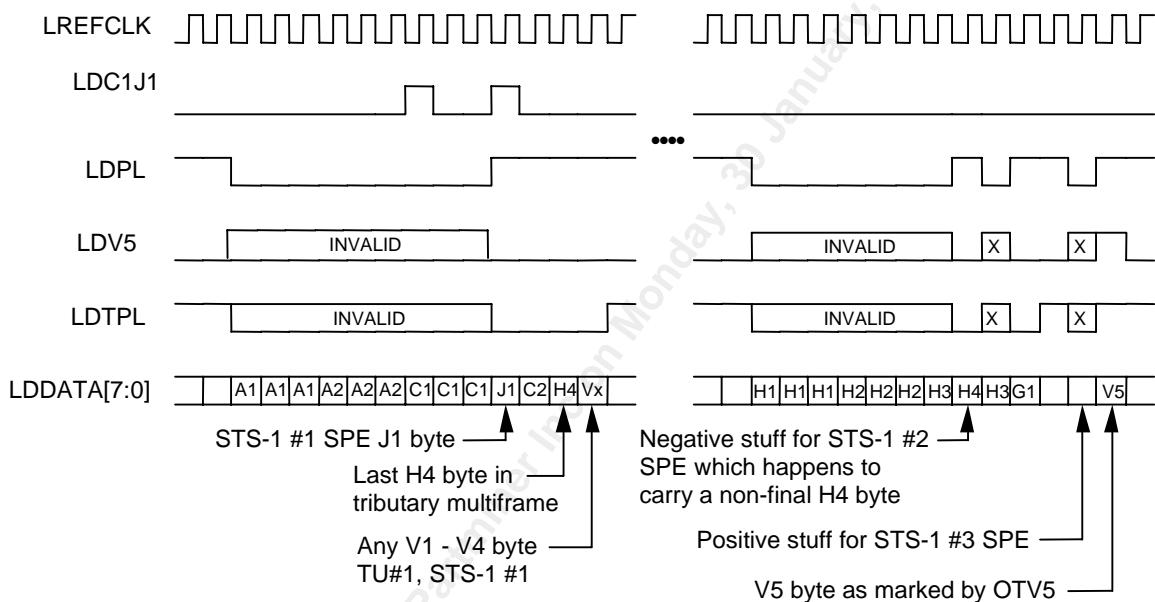


The LDV5 and LDTPL signals are optional when using the ingress VTPP within
the TEMUX 84 which will regenerate the LDV5 and LDTPL signals from
LDC1J1V1, LDPL and the pointers within LDDATA[7:0]. In order to bypass the
ingress VTPP, the data on the Telecom drop bus must be locked such that all
three STS-1 SPEs are aligned to the STS-3 transport envelope with the J1 bytes
immediately following the C1 bytes. This is shown in Figure 65.

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**Figure 65　　- 19.44 MHz Telecom DROP Bus Timing - Locked STS-1 SPEs / AU3 VCs**
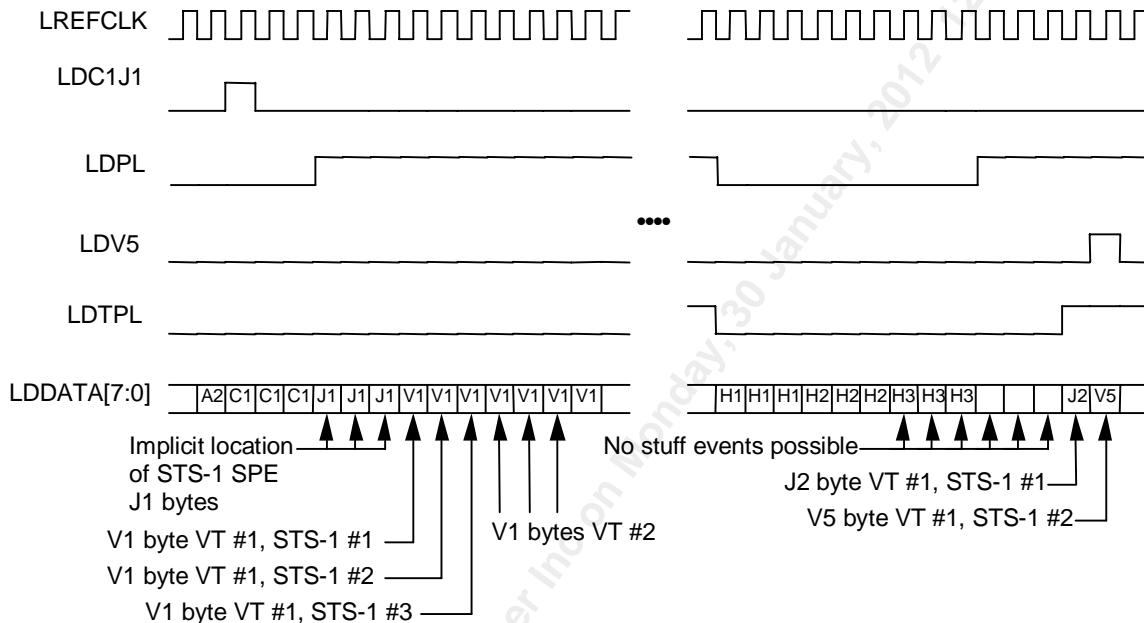


Figure 66 shows the function of the various telecom DROP bus signals in AU4 mode.  Data on LDDATA [7:0] is sampled on the rising edge of LREFCLK.  The bytes forming the VC4 virtual container are identified by the setting the LDPL signal high.  The LDC1J1V1 signal pulses high, while LDPL is set low, to mark the single C1 byte in every frame of the AU4 transport envelope.  The LDC1J1V1 signal is set high again with LDPL high to mark the J1 byte of the VC4. The bytes forming the various tributary synchronous payload envelopes are identified by the LDTPL signal being set high.  The LDV5 signal pulses high to mark the V5 bytes of each outgoing tributaries.

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**Figure 66    - 19.44 MHz Telecom DROP Bus Timing - AU4 VC**
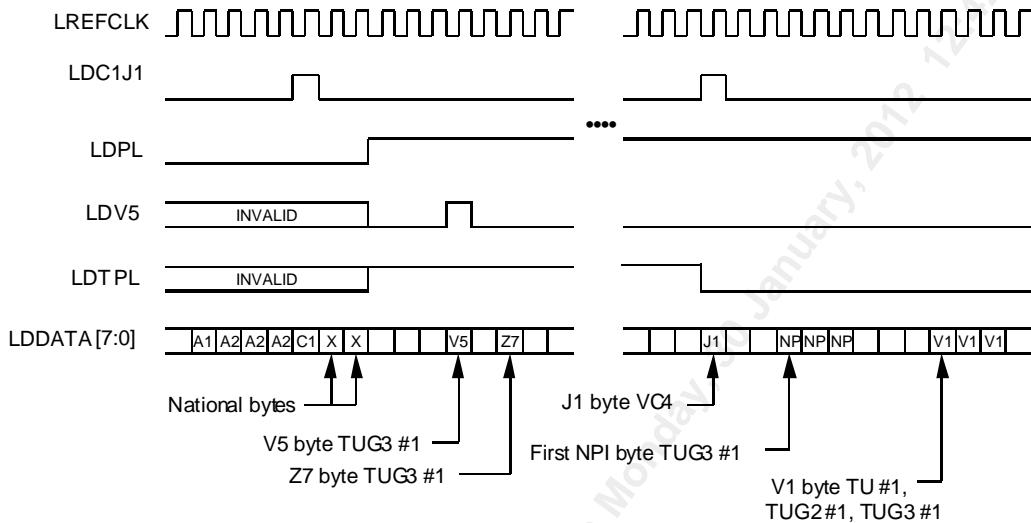


The LDV5 and LDTPL signals are optional when using the ingress VTPP within the TEMUX 84 which will regenerate the LDV5 and LDTPL signals from LDC1J1V1, LDPL and the pointers within LDDATA[7:0]. In order to bypass the ingress VTPP, the position of the single J1 byte and the VC4 is implicitly defined by the C1 byte position. In the locked AU4 mode, the VC4 is defined to be aligned to the AU4 transport envelope such that the J1 byte occupies the first available payload byte after the C1 byte, and no pointer justifications are possible.

Figure 67 provides one example of the Telecom Drop bus operating at 77.76 MHz. For specifics on differences to 19.44 MHz operation, refer to the "Notes on 77.76 MHz Telecom Bus Operation" sub-subsection.

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**Figure 67     -  77.76 MHz Telecom DROP Bus Timing**



Configuration: LSTM1=10, TUG3=0
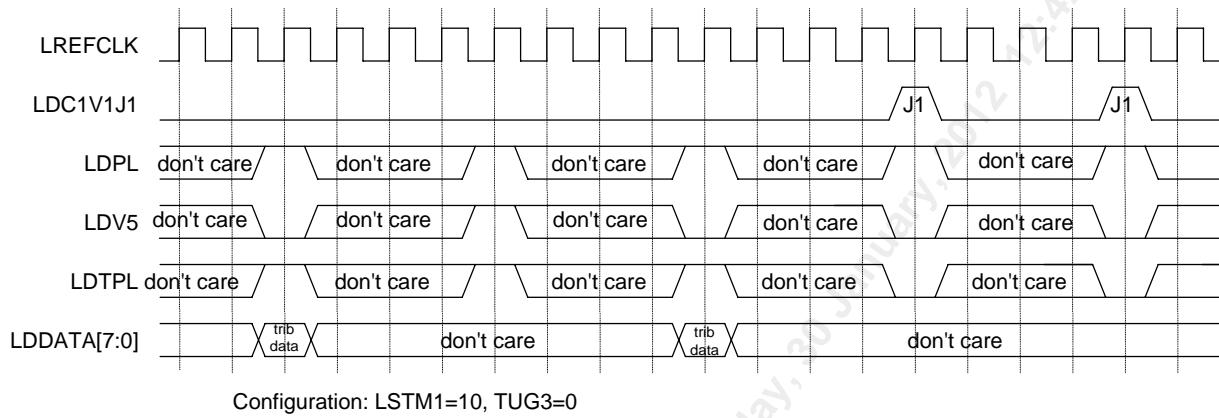
## 13.4  Telecom ADD Bus Interface Timing

Figure 68 shows the function of the telecom ADD bus signals in AU3 mode when LREFCLK is nominally 19.44 MHz.  Data on LADATA[7:0] is updated on the rising edge of LREFCLK.  The LAC1 input is sampled on the rising edge of LREFCLK and aligns all devices on the ADD bus by marking the first C1 byte of the first STS-1 in every fourth STS-3 transport envelope. LAC1 pulses every fourth STS-3 to indicate tributary multiframe alignment on the ADD bus. The bytes forming the three STS-1 synchronous payload envelopes are identified when the LAPL signal is high. The LAC1J1V1 signal pulses high, while LAPL is set low, to mark the C1 byte of the first STS-1 in every frame of the STS-3 transport envelope.  The LAC1J1V1 signal is high when the LAPL signal is high to mark every J1 byte of each of the three STS-1 SPEs. The LAV5 signal pulses high to mark the V5 bytes of each tributary.  LATPL, multiplexed with LAOE shown separately in Figure 68, indicates valid tributary payload when high. During the V3 location LATPL indicates a negative pointer justification when high and during the byte after the V3 location LATPL low indicates a positive pointer justification. The three STS-1 SPEs have an alignment determined by the SONET/SDH Transmit Pointer Configuration registers.  A pointer of 522 decimal is illustrated in Figure 68.

The LATPL signal is updated on the rising edge of LREFCLK. It is output during when the TEMUX 84 is outputing valid tributary data onto the ADD bus. It is asserted high for all bytes making up a tributary and is asserted low during overhead bytes.

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**Figure 68       - 19.44 MHz Telecom ADD Bus Timing - Locked STS-1 SPEs / AU3 VCs**
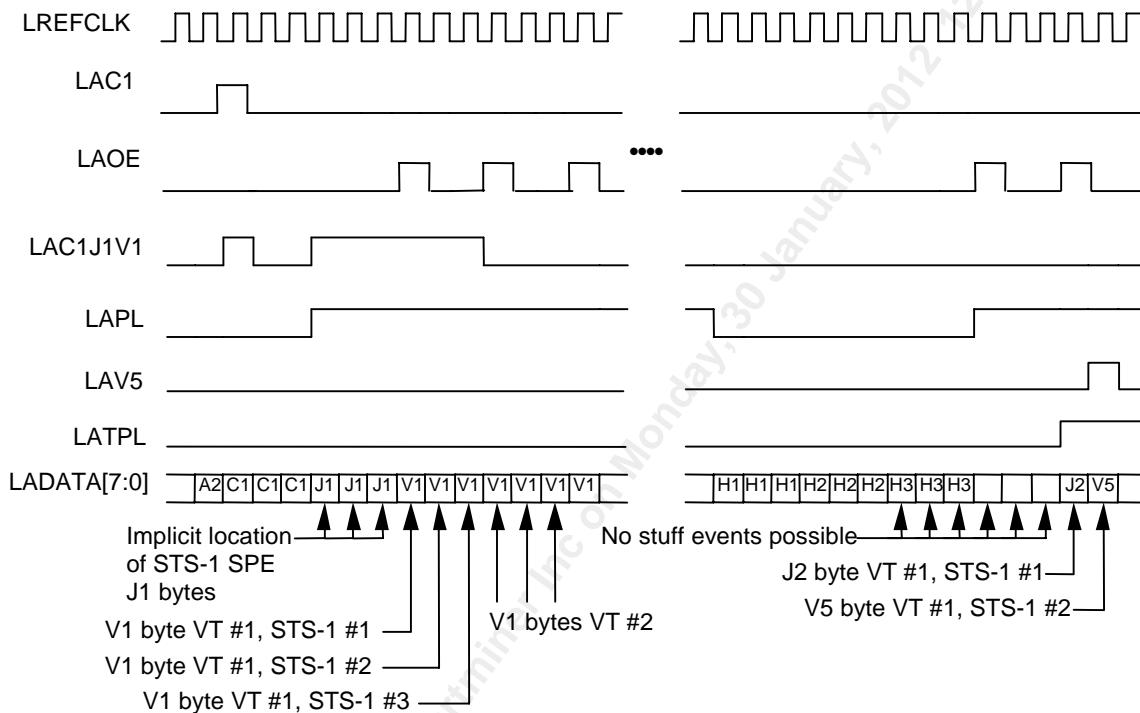


Figure 69 shows the function of the TEMUX 84 telecom ADD bus when operating in AU4 mode when LREFCLK is nominally 19.44 MHz.  In AU4 mode, the position of the single J1 byte and the VC4 is implicitly defined by the LAC1 byte position.  The VC4 is defined to be aligned to the AU4 transport envelope such that the J1 byte occupies the first available payload byte after the C1 byte. No pointer justification events take place on the ADD bus. LAC1J1V1 pulses high to mark the first C1 byte, the J1 byte and the third byte after J1 of the first tributary in the AU4 stream.  LAPL identifies the payload bytes on LADATA[7:0].

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**Figure 69     - 19.44 MHz Telecom ADD Bus Timing - Locked AU4 VC Case**
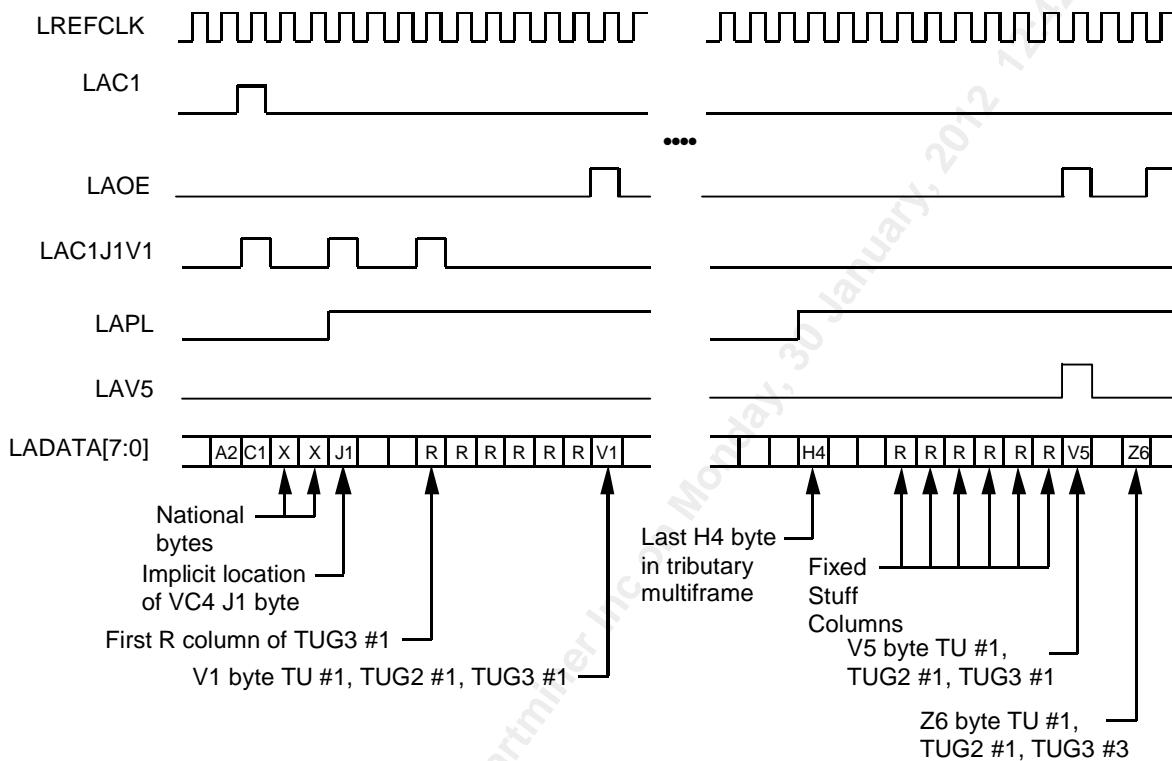


Figure 70 provides one example of the Telecom Add bus operating at 77.76 MHz. For specifics on differences to 19.44 MHz operation, refer to the "Notes on 77.76 MHz Telecom Bus Operation" sub-subsection.

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**Figure 70     - 77.76 Telecom ADD Bus Timing**
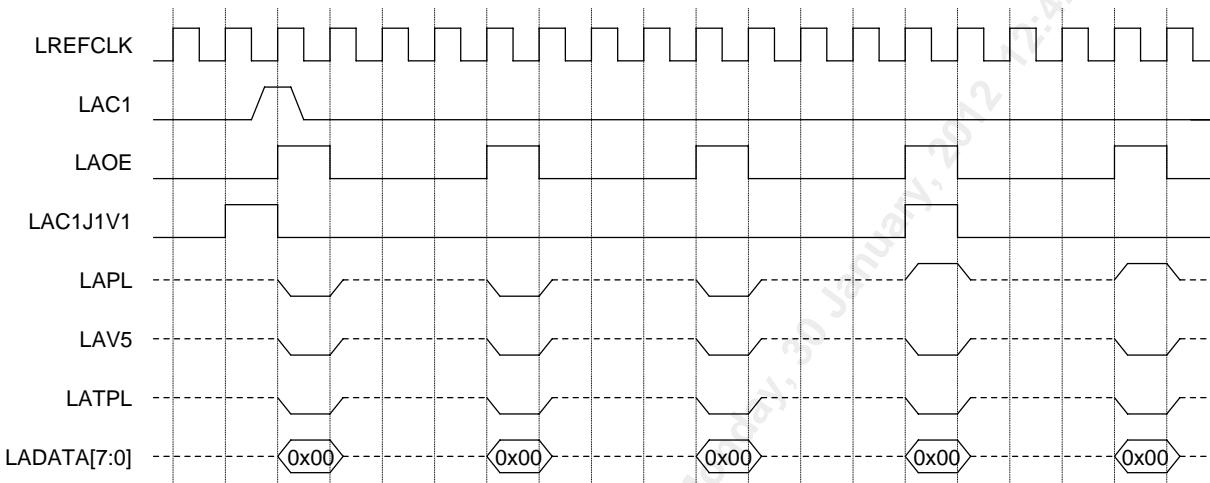


Configuration: LSTM1=01, LADDOE=0, LAJ1EN=1, LATOHEN=1, SC1FPEN=0, TUG3=1, TXPTR='d522

## 13.4.1 Notes on 77.76 MHz Telecom Bus Operation

Telecom bus operation at 77.76MHz is simply a byte interleaved multiplex of a 19.44 MByte/s stream with idle cycles.  The STM-1 of interest is identified by the LSTM[1:0] bits of the Master Bus Configuration register.  On the Drop bus, the three unused STM-1s are simply ignored, including parity.  On the Add bus, the unused STM-1s are high-impedance by default, but the bus may be configured to drive continuously.

Figure 67 and Figure 70 each illustrate one example set of waveforms; they are not intended to imply constraints on what is possible.

The following is of special note:

1.  Regardless of the state of the LSTM[1:0] bits, the LAC1 input pulse always identifies the first of the twelve C1 bytes.

2.  The LAC1J1V1 output is only valid if the LSTM[1:0] bits are "00".  The C1 indication will identify the first of the twelve C1 bytes.  The nature of the J1 and V1 pulses is dependent on the state of the LAJ1EN, LAV1EN and ECONCAT register bits.  The J1 will be high during either the first four J1 bytes or all 12 J1 bytes depending on the state of the ECONCAT bit.  The same is true of the V1 pulse.  If more than one device is driving the bus, all devices must use the same transmit payload pointer.

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3. Up to four devices may be directly connected to the same bus. Current consumption is minimized if all devices are the same (ie. all TEMUX 84s). All devices must receive the same LAC1 signal.

4. The INCLDC1J1V1 register bit may only be set if the LSTM[1:0] bits are "00".

5. The Telecom bus becomes unconditionally high-impedance upon either a hardware or software reset. All necessary configuration and at least one LAC1 pulse should precede the setting of the LADDOE or LAOE register bits.

6. If the LADDOE register bit is logic 1, the Add bus signals drive continuously. The LADATA[7:0], LAPL, LATPL, LAV5 outputs will be stable during the STM1 specified by the LSTM[1:0] bits, but they may transition at any time during the byte positions of the other three STM1s. The LAOE output may be used to identify the cycles containing valid data.

## 13.5  SONET/SDH Serial Alarm Port Timing

The timing relationships of the signals related to the remote serial alarm port are shown in Figure 71. The remote serial alarm port clocks, RADEASTCK and RADWESTCK, are nominally 9.72 MHz clocks but can range from 1.344 MHz to 10 MHz. The remote serial alarm port frame pulses, RADEASTFP and RADWESTFP, mark the first BIP-2 error bit (B1 in Figure 71) of the first tributary (TU #1 of TUG2 #1, TUG3 #1) on RADEAST and RADWEST, respectively. The frame pulses must be set high to mark every first BIP-2 error bit of the first tributary. Tributaries on RADEAST and RADWEST are arranged in the order of transmission of an STM-1 stream as defined in the references. I.e., TU #1 of TUG2 #1 in TUG3 #1, TU#1 of TUG2 #1 in TUG3 #2, TU#1 of TUG2 #1 in TUG3 #3, TU#1 of TUG2 #2 in TUG3 #1, ... TU #1 of TUG2 #7 in TUG3 #3, TU #2 of TUG2 #1 in TUG3 #1, ... TU #2 of TUG2 #7 in TUG3 #3, TU #3 of TUG2 #1 in TUG3 #1, ... TU #4 of TUG2 #7 in TUG3 #3. Timeslot assignment on RADEAST and RADWEST is unrelated to the configuration of the TUG2. Timeslots are always reserved for four tributaries in every TUG2 even if it is configured for tributaries with higher bandwidth than TU11, such as TU12. At timeslots devoted to non-existent tributaries, for example, tributary 4 of a TUG2 configured for TU12, RADEAST and RADWEST will be ignored.

Each tributary in the remote serial alarm port is allocated eight timeslots. The first two timeslots, labeled B1 and B2 in Figure 71, reports the two possible BIP-2 errors in the tributary payload frame. An alarm contributing to remote defect indications is reported in the third timeslot and is labeled D in Figure 71. The timeslot labeled F report alarms contributing to remote failure indications. In extended RDI mode, the D and F bits are considered as two bit codepoint and

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will be reported on the RDI and RFI signals.  Out of extended RDI mode, the D
and F bits are independent.  The remaining four timeslots are unused and are
ignored.

### Figure 71    - Remote Serial Alarm Port Timing
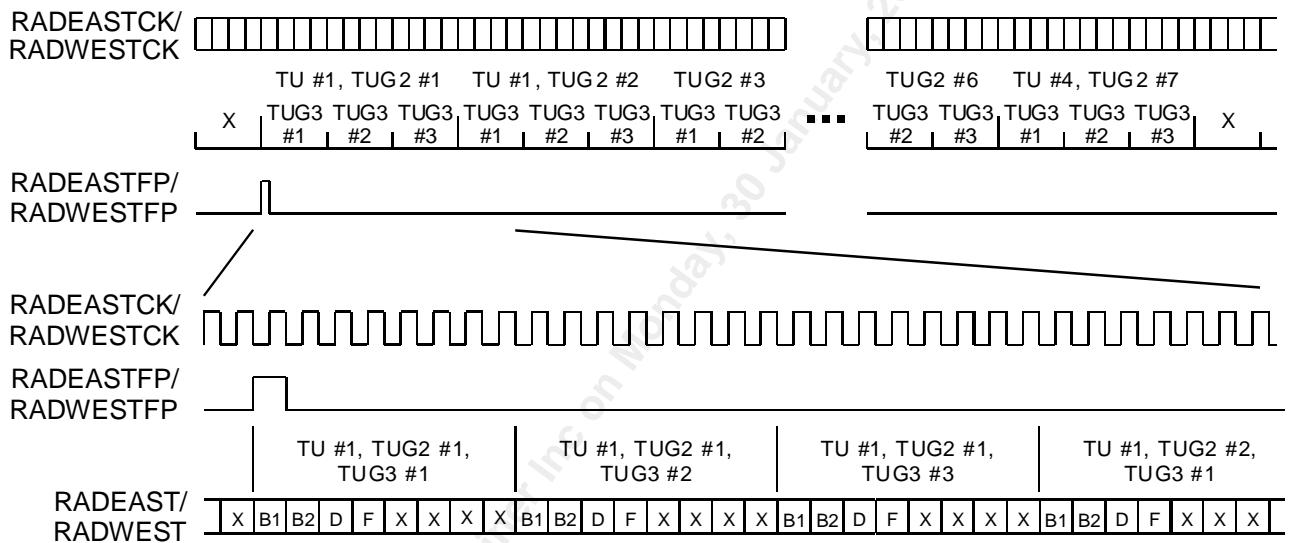


## 13.6  SBI DROP Bus Interface Timing

### Figure 72    - SBI DROP Bus T1/E1 Functional Timing
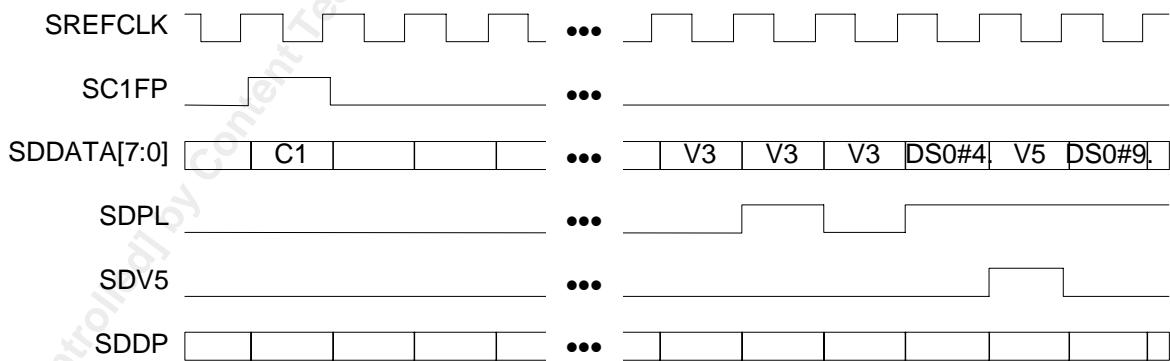


Figure 72 illustrates the operation of the SBI DROP Bus, using a negative
justification on the second to last V3 octet as an example.  The justification is
indicated by asserting SDPL high during the V3 octet.  The timing diagram also

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shows the location of one of the tributaries by asserting SDV5 high during the V5 octet.

**Figure 73    - SBI DROP Bus DS3/E3 Functional Timing**
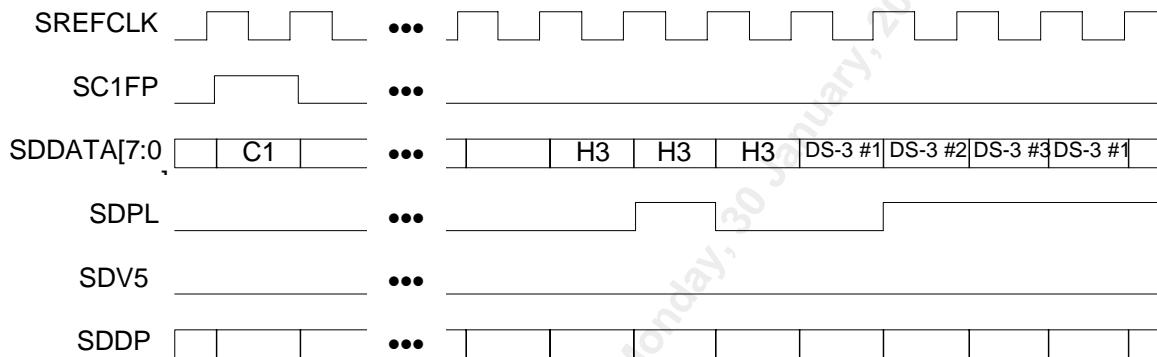


Figure 73 shows three DS-3 tributaries mapped onto the SBI bus. A negative justification is shown for DS-3 #2 during the H3 octet with SDPL asserted high. A positive justification is shown for DS-3#1 during the first DS-3#1 octet after H3 which has SDPL asserted low. E3 is transported by the same mechanism.

## 13.7 <u>SBI ADD Bus Interface Timing</u>

The SBI ADD bus functional timing for the transfer of tributaries whether T1/E1 or DS3 is the same as for the SBI DROP bus. The only difference is that the SBI ADD bus has one additional signal: the SAJUST_REQ output. The SAJUST_REQ signal is used to by the TEMUX 84 in SBI master timing mode to provide transmit timing to SBI link layer devices.

## Figure 74    -  SBI ADD Bus Justification Request Functional Timing
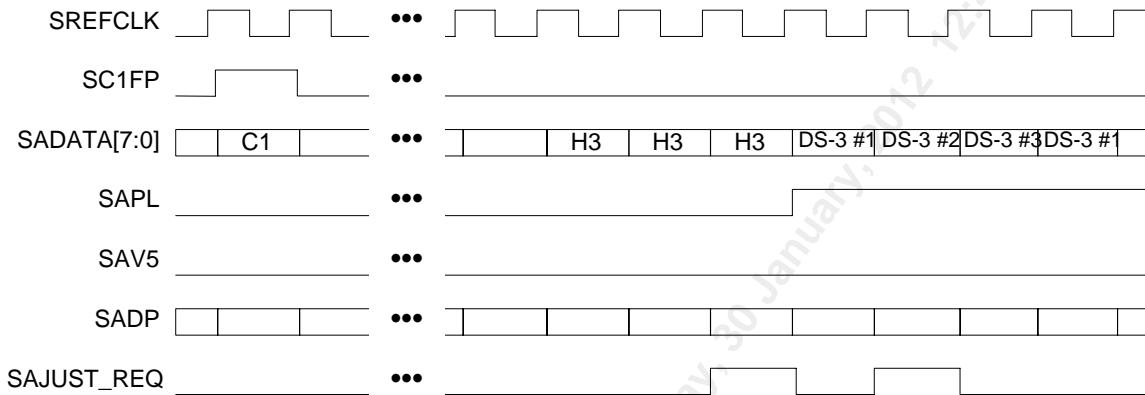


Figure 74 illustrates the operation of the SBI ADD Bus, using positive and negative justification requests as an example.  (The responses to the justification requests would take effect during the next multi-frame.)  The negative justification request occurs on the DS-3#3 tributary when SAJUST_REQ is asserted high during the H3 octet. The positive justification occurs on the DS-3#2 tributary when SAJUST_REQ is asserted high during the first DS-3#2 octet after the H3 octet.

### 13.7.1 Notes on 77.76 MHz SBI Bus Operation

SBI bus operation at 77.76MHz is simply a byte interleaved multiplex of a 19.44 MByte/s stream with idle cycles.  The STM-1 of interest is identified by the LSTM[1:0] bits of the Master Bus Configuration register.  On the Add bus, the three unused STM-1s are simply ignored, including parity.  On the Drop bus, the unused STM-1s are high-impedance.  The following is of special note:

1. Regardless of the state of the SSTM[1:0] bits, the SAC1FP and SDC1FP pulses always identify the 25th byte of the frame.

2. Up to four devices may be directly connected to the same bus.  Current consumption is minimized if all devices are of the same type (ie. all TEMUX 84s).  All devices must receive the same SAC1FP and SDC1FP signals.

3. The SBI bus becomes unconditionally high-impedance upon either a hardware or software reset.  All necessary configuration and at least one SDC1FP pulse should precede the setting of the GSOE register bit.

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## 13.8  Egress H-MVIP Link Timing

The timing relationship of the common H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVED[x], CASED[x] or CCSED, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 75.  The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation.  The TEMUX 84 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame.  The TEMUX 84 samples the data provided on MVED[x], CASED[x] and CCSED at the ¾ point of the data bit using the rising edge of CMV8MCLK as indicated for bit 1 (B1) of time-slot 1 (TS 1) in Figure 75.  B1 is the most significant bit and B8 is the least significant bit of each octet.

**Figure 75     - Egress 8.192 Mbit/s H-MVIP Link Timing**
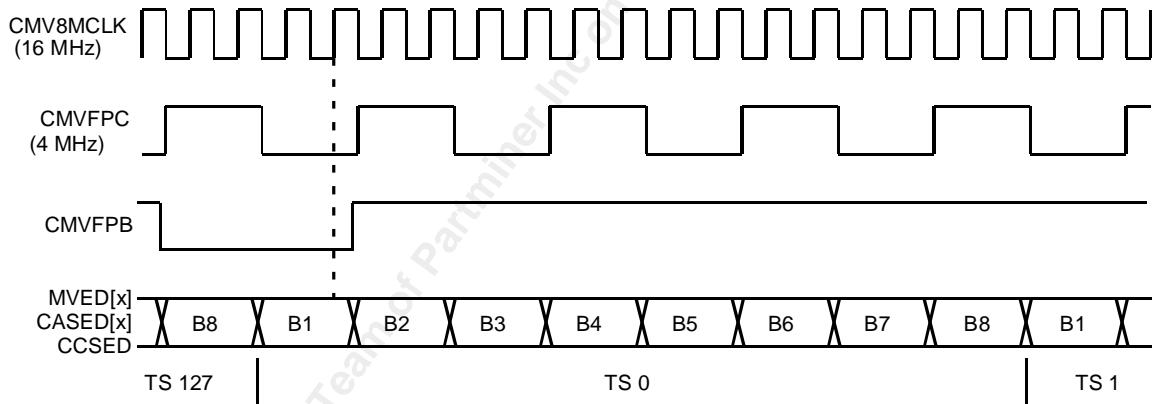


## 13.9  Ingress H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVID[x], CASID[x] or CCSID, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 76.  The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation.  The TEMUX 84 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame.  The TEMUX 84 updates the data provided on MVID[x], CASID[x] and CCSID on every second falling edge of CMV8MCLK as indicated for bit 2 (B2) of time-slot 1 (TS 1) in Figure 76.  The first bit of the next frame is updated on MVID[x], CASID[x] and CCSID on the falling CMV8MCLK clock edge for which CMVFPB is also sampled low.  B1 is the most significant bit and B8 is the least significant bit of each octet.

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**Figure 76     - Ingress 8.192 Mbit/s H-MVIP Link Timing**
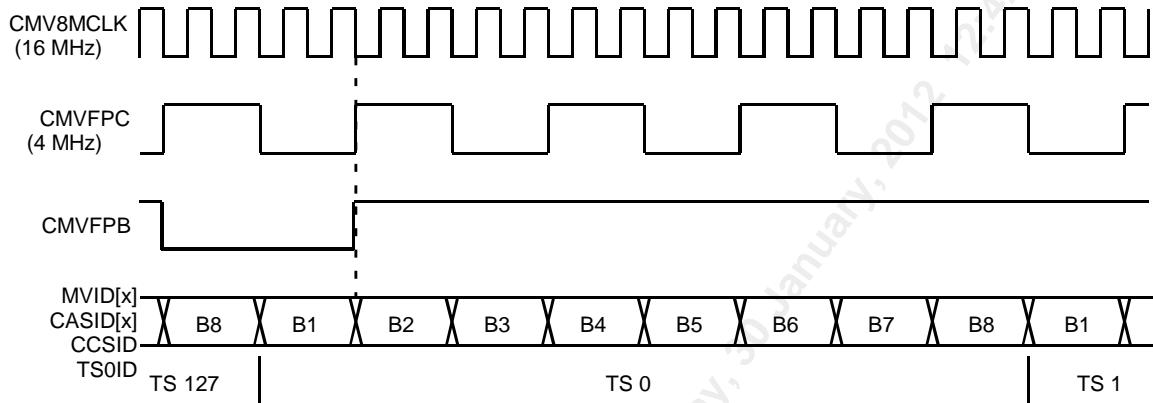


## 13.10  Egress Flexible Bandwidth Timing

The three Egress Flexible Bandwidth ports provide the ability to transport three arbitrary bit rate data streams across the SBI Add bus.  Two regimes are most common: the data rate is set by the device connected to the SBI Add bus (Figure 77) or the data rate is set by the external device connected to this port (Figure 78).

When the data rate is determined by the SBI Add bus device, it ignores the SAJUST_REQ output and asserts the SAPL signal whenever it has data to send. In this situation as illustrated by Figure 77, EFBWDREQ[n] is typically tied high to indicate a willingness to accept all data.  With each byte received on the SBI bus, a burst of eight cycles will occur with EFBWEN[n] asserted high to indicate the presence of valid data.  Because bytes are transmitted as soon as they are received, latency is minimized.

When the external device connected to the Egress Flexible Bandwidth port sets the data rate, EFBWDREQ[n] input may be modulated to control the rate bits are emitted on EFBWDAT[n].  In this case as illustrated by Figure 78, the device on the SBI Add bus is expected to respect the SAJUST_REQ output.  The TEMUX 84 will assert SAJUST_REQ in an attempt to keep the fill level of the SBI Add bus FIFO at 32 or 256 bytes as determined by the FRACT_THR_HIGH register bit.  The SAPL signal is expected to be asserted in response to the SAJUST_REQ assertion.  Typically, the 128-byte setting is only used if there is a large latency between the assertion of the SAJUST_REQ output and the corresponding response by SAPL.  A one-to-one relationship is not mandatory between SAJUST_REQ and SAPL; additional SAJUST_REQ assertions will be made to achieve the desired rate.  A byte is read from the SBI Add bus FIFO for every eight EFBWCLK cycles that EFBWDREQ[n] is asserted high.  Provided the

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SBI Add bus responds to the SAJUST_REQ appropriately, the TEMUX 84's SBI
Add bus FIFO will remain non-empty and a one-to-one relationship between
EFBWDREQ[n] and EFBWEN[n] will be maintained.  If for any reason the SBI
Add bus FIFO becomes empty, the contemporaneous EFBWDREQ[n] assertions
will be disregarded.  Figure 78 includes this pathelogical case.

**Figure 77        - Egress Flexible Bandwidth Port Functional Timing – SBI
Slave**
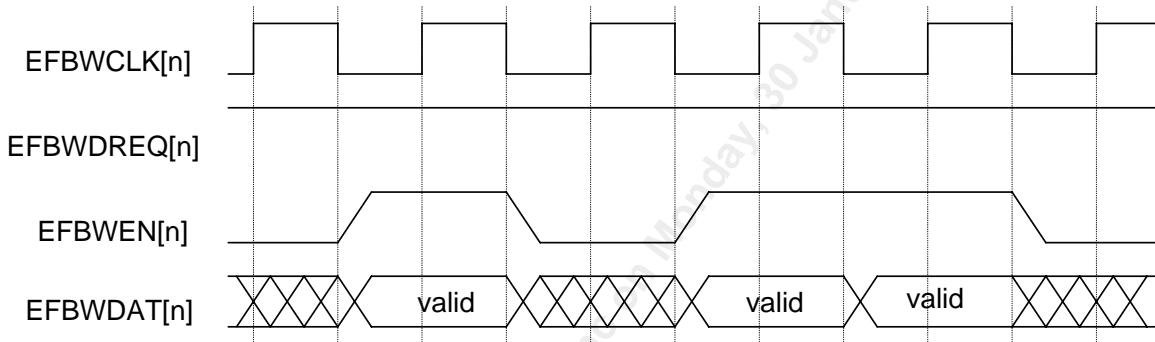


N.B.  The EFBWEN[n] waveform is not typical.  Provided EFBWDREQ[n] is held
high, EFBWEN[n] will always be high for at least 8 consecutive EFBWCLK[n]
periods.

**Figure 78        - Egress Flexible Bandwidth Port Functional Timing – SBI
Master**
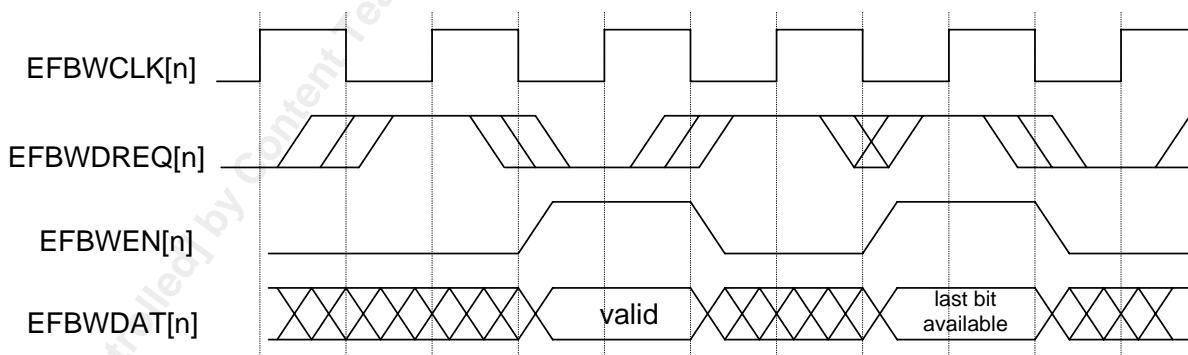


## 13.11  Ingress Flexible Bandwidth Timing

The three Ingress Flexible Bandwidth ports provide the ability to transport three
arbitrary bit rate data streams across the SBI Drop bus.  A bit rate of 48.96 Mbit/s
is supported for each port provided the constaints given in the Burst Lengths on

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Ingress Flexible Bandwidth Port section are respected.  It is assumed the devices on the SBI Drop bus are capable of accepting all data presented, as no back-pressure flow control is provided.  The value on IFBWDAT[n] is accepted as valid whenever IFBWEN[n] is coincidentally sampled as a logic high by IFBWCLK[n]. Figure 79 illustrates typical operation.

**Figure 79      - Ingress Flexible Bandwidth Port Functional Timing**

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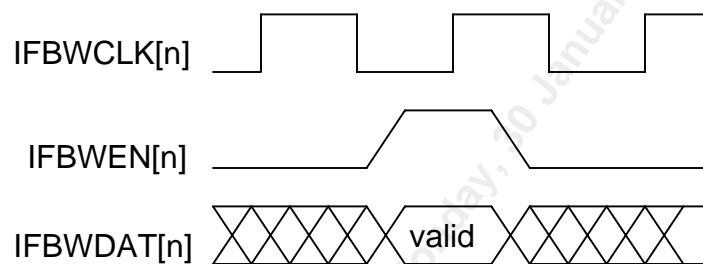
## 14 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

**Table 47 - Absolute Maximum Ratings**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Case Temperature under Bias | | -40 to +85 | °C |
| Storage Temperature | $T_{ST}$ | -40 to +125 | °C |
| Supply Voltage | $V_{DD1.8}$ | -0.3 to + 3.6 | $V_{DC}$ |
| Supply Voltage | $V_{DD3.3}$ | -0.3 to + 5.5 | $V_{DC}$ |
| Voltage on Any Pin | $V_{IN}$ | -0.3 to 5.5 | $V_{DC}$ |
| Static Discharge Voltage | | ±1000 | V |
| Latch-Up Current | | ±100 | mA |
| DC Input Current | $I_{IN}$ | ±20 | mA |
| Lead Temperature | | +225 | °C |
| Junction Temperature | $T_J$ | +150 | °C |

**Notes on Power Supplies:**

1. VDD3.3 should power up before VDD1.8.

2. VDD3.3 should not be allowed to drop below the VDD1.8 voltage level except when VDD1.8 is not powered.

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## 15    D.C. CHARACTERISTICS

$T_A$ = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%
(Typical Conditions: $T_A$ = 25°C, $V_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = 1.8V)

### Table 48    - D.C. Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| VDD3.3 | Power Supply | 2.97 | 3.3 | 3.63 | Volts | |
| VDD1.8 | Power Supply | 1.65 | 1.8 | 1.95 | Volts | |
| VIL | Input Low Voltage | 0 | | 0.8 | Volts | Guaranteed Input LOW Voltage |
| VIH | Input High Voltage | 2.0 | | | Volts | Guaranteed Input HIGH Voltage |
| VOL | Output or Bidirectional Low Voltage | 0 | 0.1 | 0.4 | Volts | VDD = min, IOL = -4mA for D[7:0], RECVCLK1, RECVCLK2, RECVCLK3, MVID[7:0], CASID[7:0], CCSID, TCLK[3:1], TPOS/TDAT[3:1], TNEG/TMFP[3:1], RGAPCLK/RSCLK[3:1], RDATAO[3:1], RFPO/RMFPO[3:1], ROVRHD[3:1], TFPO/TMFPO/TGAPCLK[3:1], SBIACT, IOL = -8mA for SDDATA[7:0], SDDP, SDPL, SDV5, SAJUST_REQ, SDC1FP, LAC1J1V1, LADATA[7:0], LADP, LAPL, LAOE/LATPL IOL = -2mA for others. Note 3 |

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| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------|-----------|-----|-----|-----|-------|-----------|
| VOH | Output or Bidirectional High Voltage | 2.4 | | VDD3.3 | Volts | VDD = min,<br>IOH = 4mA for D[7:0], RECVCLK1, RECVCLK2, RECVCLK3, MVID[21:1], CASID[21:1], CCSID, TCLK, TPOS/TDAT, TNEG/TMFP, RGAPCLK/RSCLK, RDATAO, RFPO/RMFPO, ROVRHD, TFPO/TMFPO/TGAPCLK, SBIACT,<br>IOH = 8mA for SDDATA[7:0], SDDP, SDPL, SDV5, SAJUST_REQ, SDC1FP, LAC1J1V1, LADATA[7:0], LADP, LAPL, LAOE/LATPL<br>IOH = 2mA for others.<br>Note 3 |
| VT+ | Reset Input High Voltage | 2.0 | | | Volts | TTL Schmidt |
| VT- | Reset Input Low Voltage | | | 0.6 | Volts | |
| VTH | Reset Input Hysteresis Voltage | | TBD | | Volts | |
| IILPU | Input Low Current | +20 | | +300 | µA | VIL = GND.  Notes 1, 3 |
| IIHPU | Input High Current | -10 | | +10 | µA | VIH = VDD.  Notes 1, 3 |
| IILPD | Input Low Current for Input A[12] | -10 | | +10 | µA | VIL = GND.  Notes 3, 4 |
| IIHPD | Input High Current for Input A[12] | +20 | | +350 | µA | VIH = VDD.  Notes 3, 4 |
| IIL | Input Low Current | -10 | | +10 | µA | VIL = GND.  Notes 2, 3 |
| IIH | Input High Current | -10 | | +10 | µA | VIH = VDD.  Notes 2, 3 |
| CIN | Input Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| COUT | Output Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| CIO | Bidirectional Capacitance | | 5 | | pF | Excluding Package, Package Typically 2 pF |
| IDDOP1 | Operating Current<br>    IDD1.8<br>    IDD3.3 | | 340<br>5 | 500 | mA | VDD1.8 = 1.94 V<br>VDD3.3 = 3.56 V<br>Outputs Unloaded,<br>Telecom to SBI mode |

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| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------|-----------|-----|-----|-----|-------|-----------|
| IDDOP2 | Operating Current | | | | | VDD1.8 = 1.94 V |
| | IDD1.8 | | 340 | 500 | mA | VDD3.3 = 3.56 V |
| | IDD3.3 | | 5 | | | Outputs Unloaded, |
| | | | | | | DS3 to MVIP mode |

## Notes on D.C.  Characteristics:

1.  Input pin or bi-directional pin with internal pull-up resistor.

2.  Input pin or bi-directional pin without internal pull-up resistor

3.  Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4.  Input pin or bi-directional pin with internal pull-down resistor.

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# 16    MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

($T_A$ = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%)

**Table 49       - Microprocessor Interface Read Access**

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| tSAR | Address to Valid Read Set-up Time | 10 | | ns |
| tHAR | Address to Valid Read Hold Time | 5 | | ns |
| tSALR | Address to Latch Set-up Time | 10 | | ns |
| tHALR | Address to Latch Hold Time | 10 | | ns |
| tVL | Valid Latch Pulse Width | 20 | | ns |
| tSLR | Latch to Read Set-up | 0 | | ns |
| tHLR | Latch to Read Hold | 5 | | ns |
| tPRD | Valid Read to Valid Data Propagation Delay | | 30 | ns |
| tZRD | Valid Read Negated to Output Tri-state | | 20 | ns |
| tZINTH | Valid Read Negated to Output Tri-state | | 50 | ns |

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### Figure 80     - Microprocessor Interface Read Timing
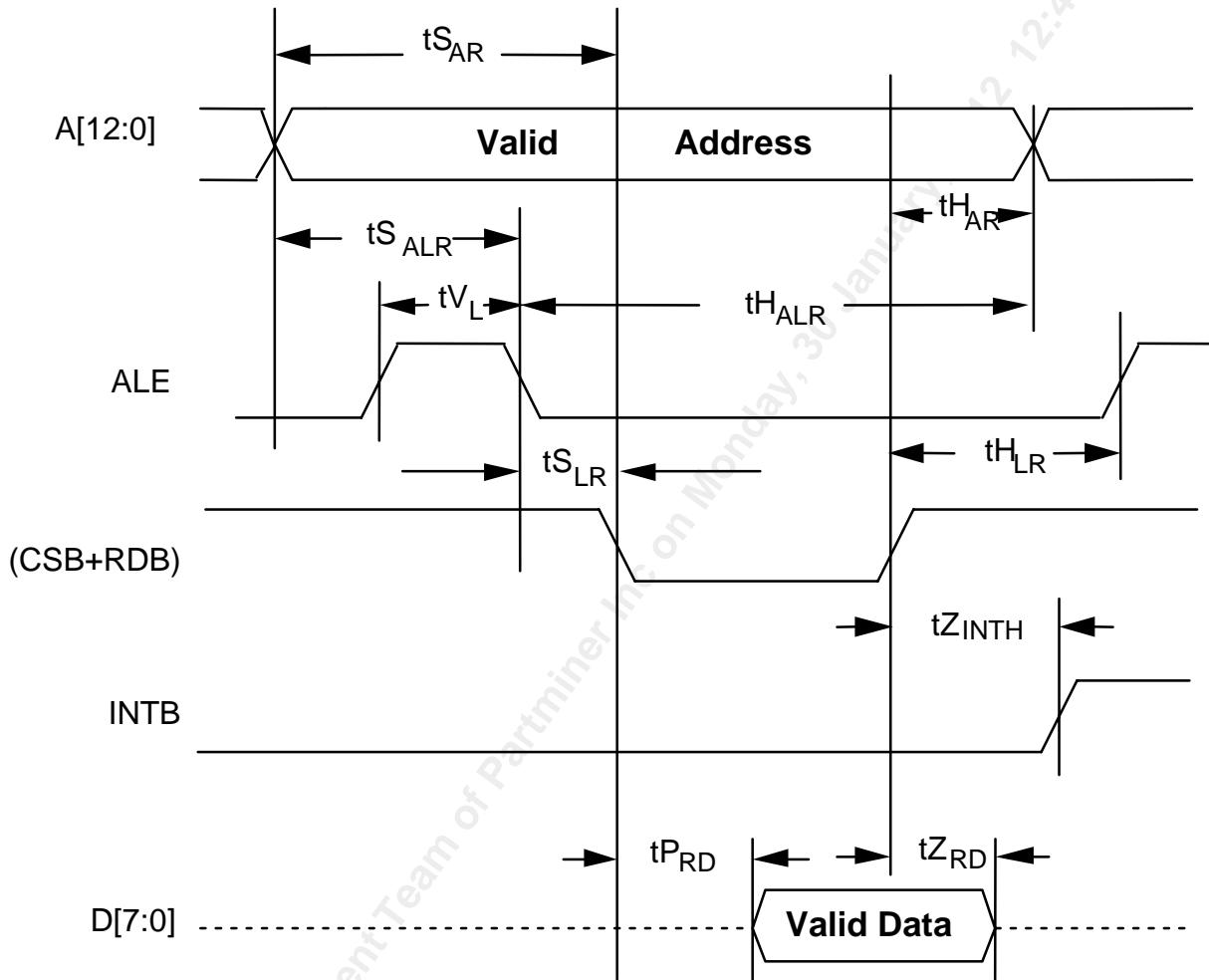


**Notes on Microprocessor Interface Read Timing:**

1.  Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2.  Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3.  A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4.  In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.

5. Parameter tHAR  is not applicable if address latching is used.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

**Table 50       - Microprocessor Interface Write Access**

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| tSAW | Address to Valid Write Set-up Time | 10 | | ns |
| tSDW | Data to Valid Write Set-up Time | 20 | | ns |
| tSALW | Address to Latch Set-up Time | 10 | | ns |
| tHALW | Address to Latch Hold Time | 10 | | ns |
| tVL | Valid Latch Pulse Width | 20 | | ns |
| tSLW | Latch to Write Set-up | 0 | | ns |
| tHLW | Latch to Write Hold | 5 | | ns |
| tHDW | Data to Valid Write Hold Time | 5 | | ns |
| tHAW | Address to Valid Write Hold Time | 5 | | ns |
| tVWR | Valid Write Pulse Width | 40 | | ns |

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**Figure 81  - Microprocessor Interface Write Timing**
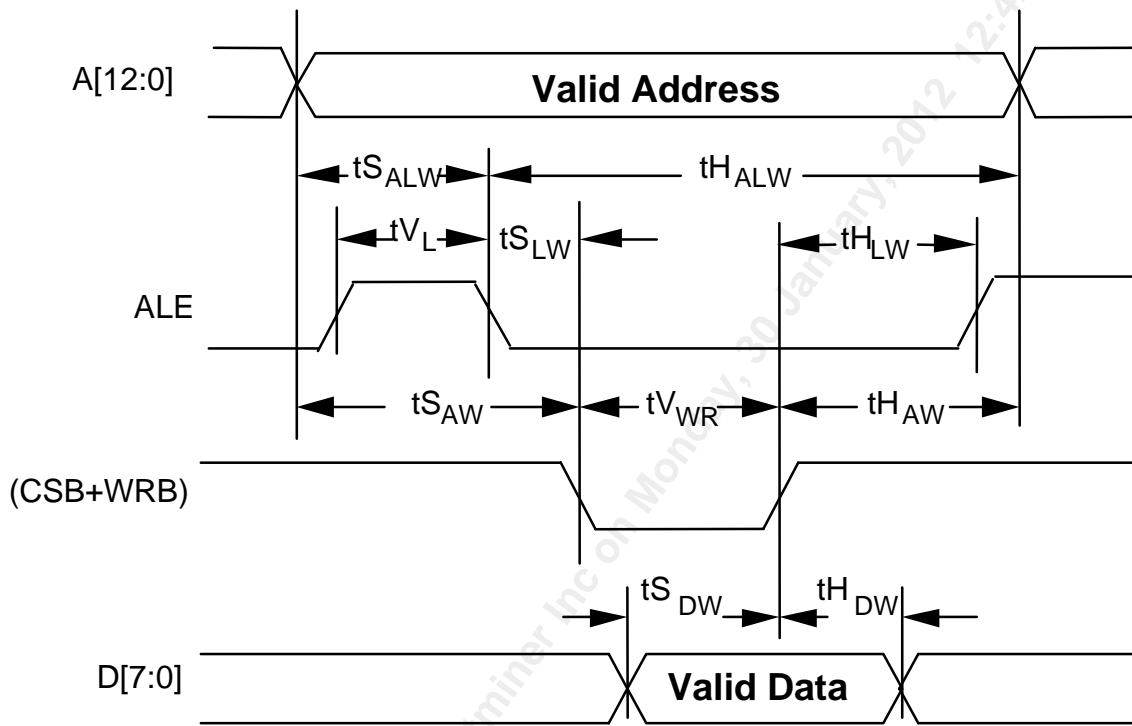


**Notes on Microprocessor Interface Write Timing:**

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW and tHLW are not applicable.

3. Parameter tHAW  is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

## 17    TEMUX 84 TIMING CHARACTERISTICS

**($T_A$ = -40°C to +85°C $V_{DD3.3}$ = 3.3V ±8%, $V_{DD1.8}$ = 1.8V ±8%)**

### Table 51    - RSTB Timing

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| tVRSTB | RSTB Pulse Width | 100 | | ns |

### Figure 82    - RSTB Timing

### Table 52    - DS3/E3 Transmit Interface Timing

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $f_{TICLK}$ | DS3 TICLK[3:1] average frequency | 44.736 -50 ppm | 44.736 +50 ppm | MHz |
| $f_{TICLK}$ | E3 TICLK[3:1] average frequency | 34.368 -50 ppm | 34.368 +50 ppm | MHz |
| $T_{TICLK}$ | Instantaneous minimum TICLK[3:1] period | 19.2 | | ns |
| $t0_{TICLK}$ | TICLK[3:1] minimum pulse width low | 7.7 | | ns |
| $t1_{TICLK}$ | TICLK[3:1] minimum pulse width high | 7.7 | | ns |
| $tS_{TFPI}$ | TFPI/TMFPI[x] to TICLK[x] Set-up Time (LOOPT=0, active TICLK edge set by TDATIFALL bit) | 5 | | ns |
| | TFPI/TMFPI[x] to RCLK[x] Set-up Time (LOOPT=1) | 5 | | |

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| tH$_{TFPI}$ | TFPI/TMFPI[x] to TICLK[x] Hold Time (LOOPT=0, active TICLK edge set by TDATIFALL bit) | 1 | | ns |
|---|---|---|---|---|
| | TFPI/TMFPI[x] to RCLK[x] Hold Time (LOOPT=1) | 1 | | |
| tS$_{TDATI}$ | TDATI[x] to TICLK[x] Set-up Time (LOOPT = 0, active TICLK edge set by TDATIFALL bit) | 5 | | ns |
| | TDATI[x] to RCLK[x] Set-up Time (LOOPT = 1) | 5 | | |
| tH$_{TDATI}$ | TDATI[x] to TICLK[x] Hold Time (LOOPT = 0, active TICLK edge set by TDATIFALL bit) | 1 | | ns |
| | TDATI[x] to RCLK[x] Hold Time (LOOPT = 1) | 1 | | |
| tP$_{TGAP}$ | TICLK[x] to TGAPCLK[x] Prop Delay (LOOPT = 0) RCLK[x] to TGAPCLK[x] Prop Delay (LOOPT = 1) | 2 2 | 10 10 | ns |
| tP$_{TFPO}$ | TICLK[x] to TFPO/TMFPO[x] Prop Delay (LOOPT = 0, active TICLK edge set by TDATIFALL bit) | 2 | 12 | ns |
| | RCLK[x] to TFPO/TMFPO[x] Prop Delay (LOOPT = 1) | 2 | 12 | |
| tS$_{TGAP}$ | TDATI[x] to TGAPCLK[x] Set-up Time | 2 | | ns |
| tH$_{TGAP}$ | TDATI[x] to TGAPCLK[x] Hold Time | 2 | | ns |
| tP$_{TCLK}$ | TICLK[x] Edge to TCLK[x] Edge Prop Delay | 2 | 13 | ns |
| tP$_{TPOS}$ | TCLK[x] Edge to TPOS/TDAT[x] Prop Delay | -1 | 4 | ns |
| tP$_{TNEG}$ | TCLK[x] Edge to TNEG/TMFP[x] Prop Delay | -1 | 4 | ns |
| tP$_{TPOS2}$ | TICLK[x] High to TPOS/TDAT[x] Prop Delay (Note 5) | 2 | 13 | ns |
| tP$_{TNEG2}$ | TICLK[x] High to TNEG/TMFP[x] Prop | 2 | 13 | ns |

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| | Delay (Note 5) | | | |
|---|---|---|---|---|

Note: The "[x]" implies the parameters for a data signal are only in relation to the associated clock.

**Figure 83      - DS3/E3 Transmit Interface Timing**

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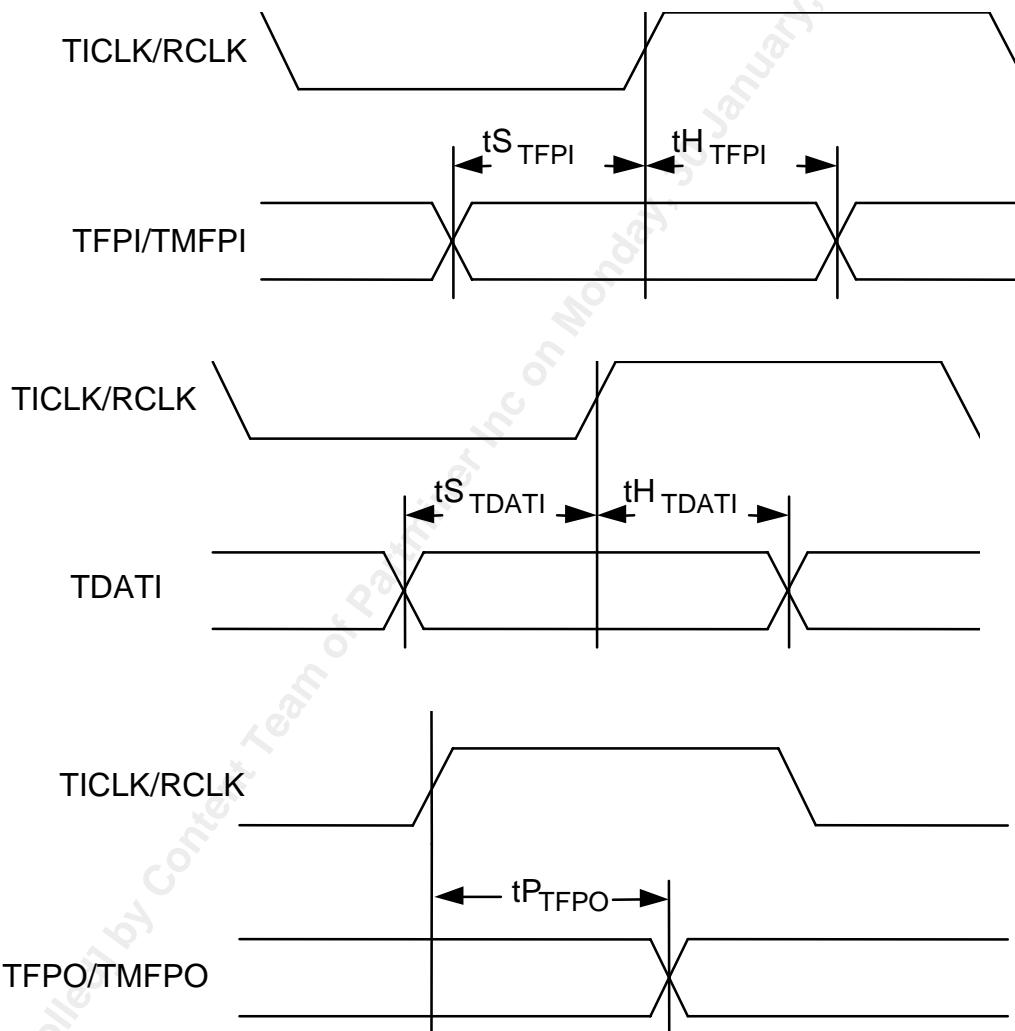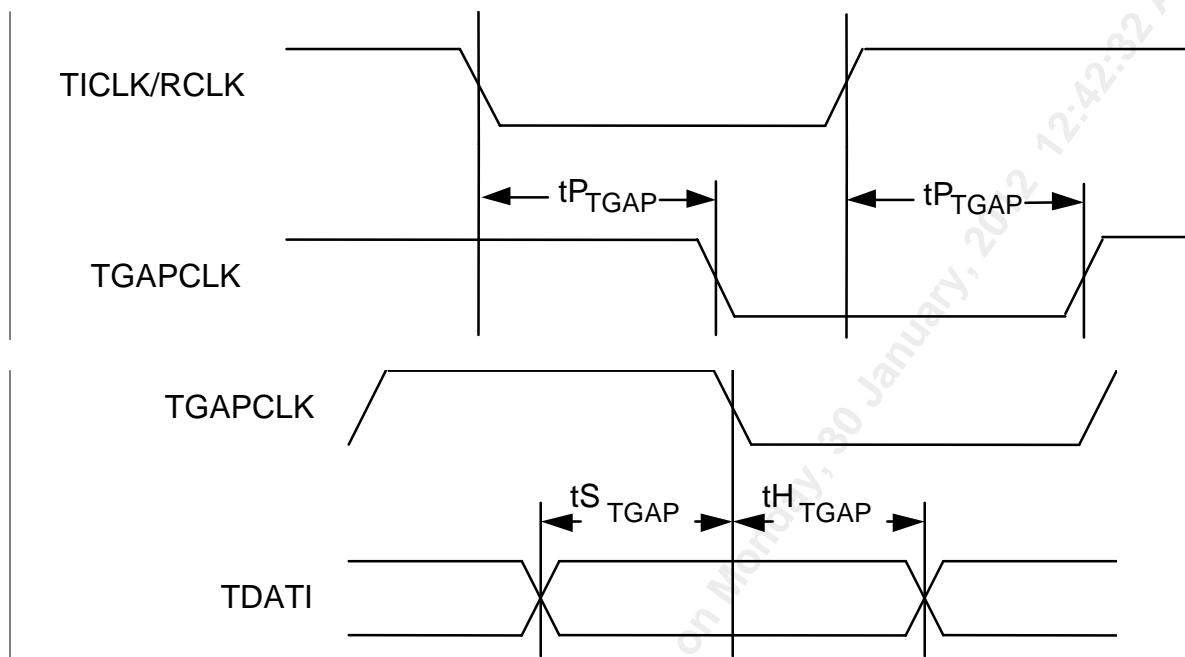
**TICLK=0, TRISE=0**    **TICLK=0, TRISE=1**
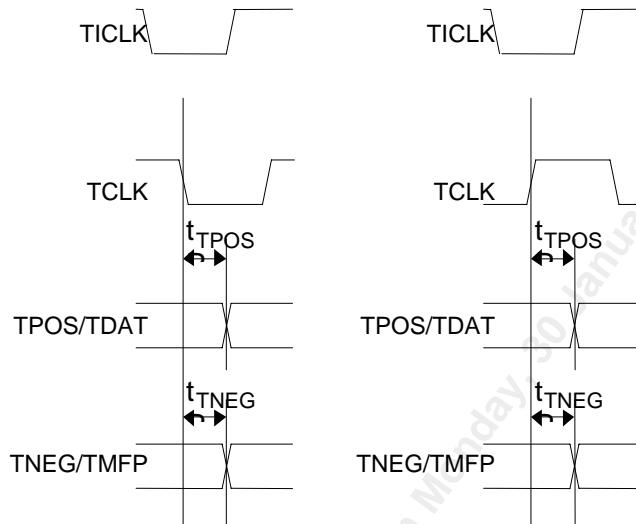


**TICLK=1, TRISE=X**
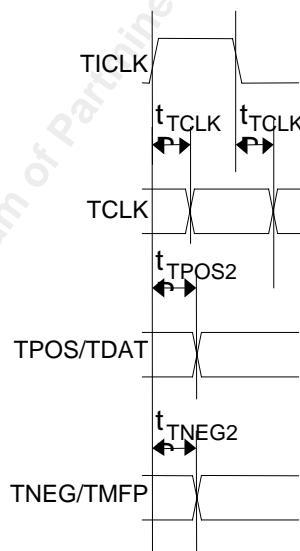


### Table 53    - DS3/E3 Receive Interface Timing

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $f_{RICLK}$ | DS3 RCLK[3:1] average frequency | 44.736 | 44.736 | MHz |

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| | | -50 ppm | +50 ppm | |
|---|---|---|---|---|
| $f_{RICLK}$ | E3 RCLK[3:1] average frequency | 34.368 -50 ppm | 34.368+ 50 ppm | MHz |
| $T_{RCLK}$ | Instantaneous minimum RCLK[3:1] period | 19.2 | | ns |
| $t0_{RCLK}$ | RCLK[3:1] minimum pulse width low | 7.7 | | ns |
| $t1_{RCLK}$ | RCLK[3:1] minimum pulse width high | 7.7 | | ns |
| $tS_{RPOS}$ | RPOS/RDAT[x] Set-up Time | 4 | | ns |
| $tH_{RPOS}$ | RPOS/RDAT[x] Hold Time | 1 | | ns |
| $tS_{RNEG}$ | RNEG/RLCV[x] Set-Up Time | 4 | | ns |
| $tH_{RNEG}$ | RNEG/RLCV[x] Hold Time | 1 | | ns |
| $tP_{RDATO}$ | RSCLK[x] Edge to RDATO[x] Prop Delay | -2 | 2 | ns |
| $tP_{RFPO}$ | RSCLK[x] Edge to RFPO/RMFPO[x] Prop Delay | -2 | 2 | ns |
| $tP_{ROVRHD}$ | RSCLK[x] Edge to ROVRHD[x] Prop Delay | -2 | 2 | ns |
| $tP_{RGAP}$ | RGAPCLK[x] Edge to RDATO[x] Prop Delay | -2 | 2 | ns |

### Figure 84      - DS3/E3 Receive Interface Timing

RSCLK

$tP_{RDATO}$

RDATO

$tP_{RFPO}$

RFPO/RMFPO

$tP_{ROVRHD}$

ROVRHD

Dashed line RSCLK represents behaviour
when RSCLKR register bit = 1.

RGAPCLK

$tP_{RGAP}$

RDATO

Dashed line RSCLK represents behaviour
when RSCLKR register bit = 1.
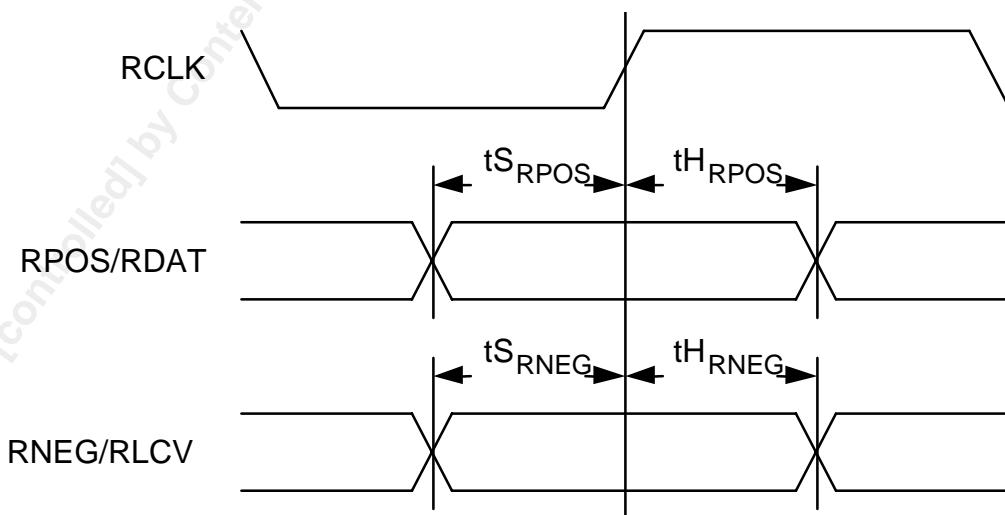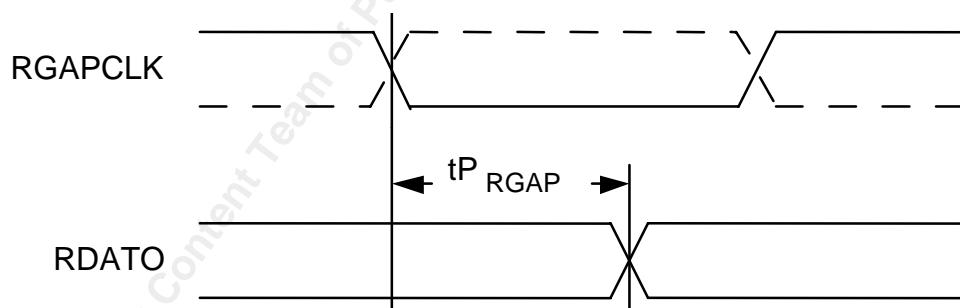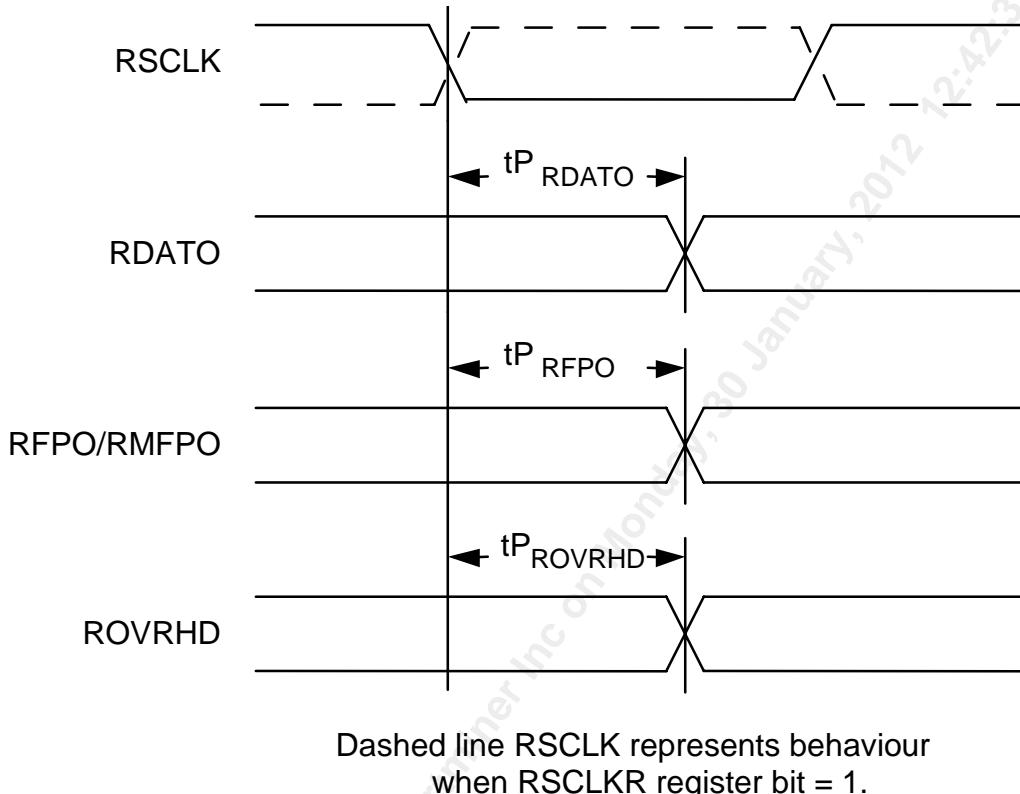
### Notes on DS3/E3 Interface Timing:

1.      When a set-up time is specified between an input and a clock, the set-up
        time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4
        Volt point of the clock.

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2.    When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3.    Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4.    Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs except the TCLK[3:1], TPOS/TDAT[3:1] and TNEG/TMFP[3:1] outputs, which have a load of 20pf.

5.    The $tP_{TPOS2}$ and $tP_{TNEG2}$ parameters are only applicable when the TICLK bit of the DS3/E3 Master Transmit Line Options register is logic 1.

**Table 54      - Line Side Telecom Bus and Line Side SBI Input Timing – 19.44 MHz (Figure 88)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
|  | LREFCLK Frequency | 19.44 -20 ppm | 19.44 +20 ppm | MHz |
|  | LREFCLK Duty Cycle | 40 | 60 | % |
|  | LREFCLK skew relative to SREFCLK | -5 | 5 | ns |
|  | CLK52M Frequency (51.84 MHz) | 51.84 -50 ppm | 51.84 +50 ppm | MHz |
|  | CLK52M Frequency (44.928 MHz) | 44.928 -50 ppm | 44.928 +50 ppm | MHz |
|  | CLK52M Duty Cycle | 40 | 60 | % |
| $tS_{TEL}$ | All Telecom BUS Inputs Set-Up Time to LREFCLK | 5 |  | ns |
| $tH_{TEL}$ | All Telecom BUS Inputs Hold Time to LREFCLK | 1 |  | ns |

**Line Side Telecom Bus Input Timing - 77.76 MHz (Figure 88)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
|  | LREFCLK Frequency | 77.76 -20 ppm | 77.76 +20 ppm | MHz |

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| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| | LREFCLK Duty Cycle | 40 | 60 | % |
| | LREFCLK skew relative to SREFCLK | -4 | 4 | ns |
| | CLK52M Frequency (51.84 MHz) | 51.84 -50 ppm | 51.84 +50 ppm | MHz |
| | CLK52M Frequency (44.928 MHz) | 44.928 -50 ppm | 44.928 +50 ppm | MHz |
| | CLK52M Duty Cycle | 40 | 60 | % |
| $tS_{TEL}$ | All Telecom BUS Inputs Set-Up Time to LREFCLK | 3 | | ns |
| $tH_{TEL}$ | All Telecom BUS Inputs Hold Time to LREFCLK | 0 | | ns |

**Notes on Telecom and Line Side SBI Input Timing:**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

**Figure 85    - Line Side Telecom BUS and Line Side SBI Input Timing**

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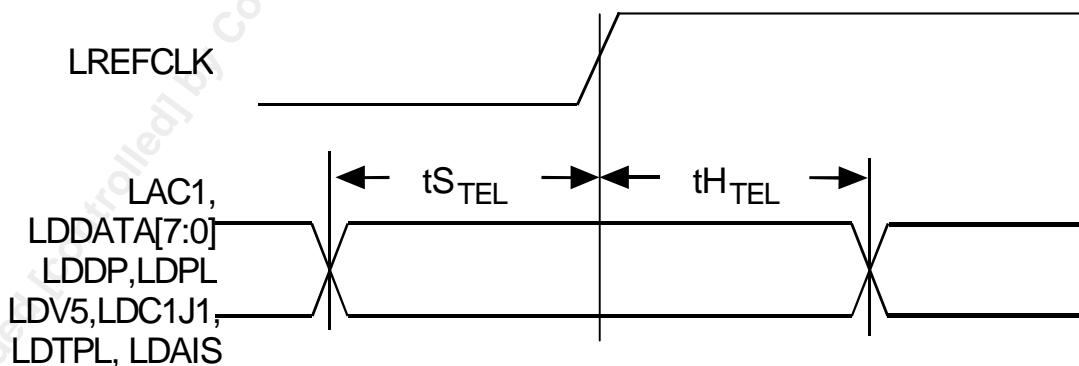
**Table 55       – Telecom Bus and Line Side SBI Output Timing - 19.44 MHz (Figure 86 and Figure 87)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $tP_{TEL}$ | LREFCLK rising to all Telecom BUS Outputs Valid | 3 | 20 | ns |
| $tZ_{TEL}$ | LREFCLK rising to all Telecom BUS tristateable Outputs going tristate | 3 | 20 | ns |
| $tP_{TELOE}$ | LREFCLK rising to all Telecom BUS tristateable Outputs going valid from tristate | 0 | 14 | ns |

**Table 56       – Telecom Bus Output Timing – 77.76 MHz (Figure 86 and Figure 87)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $tP_{TEL}$ | LREFCLK rising to LAOE and LAC1J1V1 Outputs Valid | 1 | 7 | ns |
| $tZ_{TEL}$ | LREFCLK rising to all Telecom BUS tristateable Outputs going tristate | 1 | 7 | ns |
| $tP_{TELOE}$ | LREFCLK rising to all Telecom BUS tristateable Outputs going valid from tristate | 1 | 7 | ns |

**Notes on Telecom Bus and Line Side SBI Output Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

4. The propagation delay, $tP_{TEL}$, should be used when Telecom bus outputs are always driven as configured by LADDOE in the Bus Configuration register. The propagation delays, $tP_{TELOE}$ and $tZ_{TEL}$, should be used when the

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Telecom bus outputs are multiplexed with other TEMUX 84 devices using the tristate capability of the outputs as configured by LADDOE. Note that under any specific operating condition, $tZ_{TEL}$ is guaranteed to be less than $tP_{TELOE}$.

**Figure 86      - Telecom BUS and Line Side SBI Output Timing**
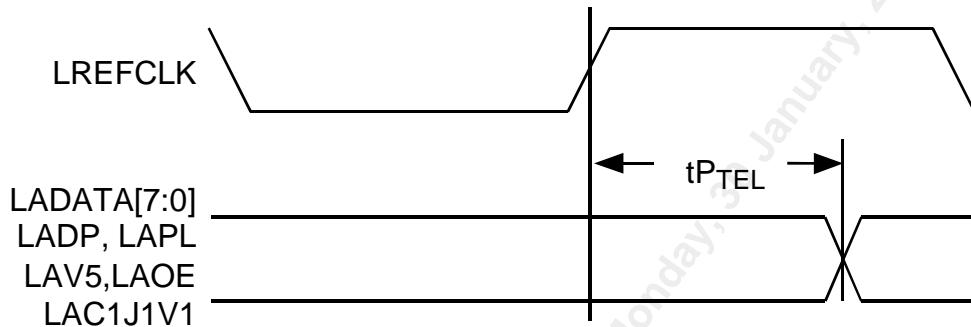


**Figure 87      - Telecom BUS and Line Side SBI Tristate Output Timing**
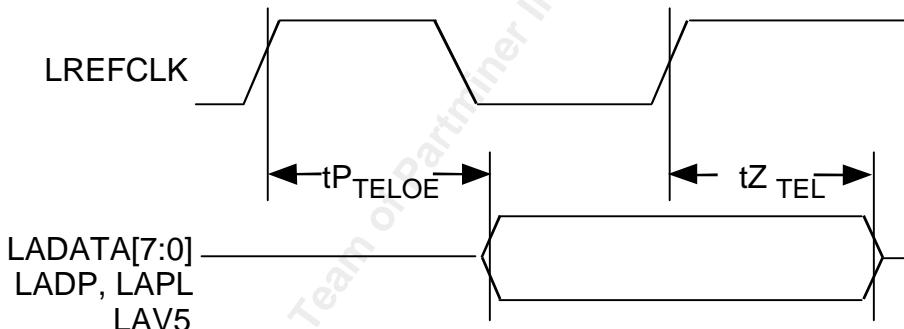


**Table 57      - System Side SBI ADD BUS Timing – 19.44 MHz (Figure 88)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| | SREFCLK Frequency | 19.44 -20 ppm | 19.44 +20 ppm | MHz |
| | SREFCLK Duty Cycle | 40 | 60 | % |
| $tS_{SBIADD}$ | All SBI ADD BUS Inputs Set-Up Time to SREFCLK | 4 | | ns |
| $tH_{SBIADD}$ | All SBI ADD BUS Inputs Hold Time to SREFCLK | 0 | | ns |
| $tP_{SBIADD}$ | SREFCLK to SAJUST_REQ Valid | 2 | 15 | ns |

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| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| tZ$_{SBIADD}$ | SREFCLK to SAJUST_REQ Tristate | 2 | 15 | ns |

**Table 58     - System Side SBI ADD BUS Timing – 77.76 MHz (Figure 88)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | SREFCLK Frequency | 77.76 -20 ppm | 77.76 +20 ppm | MHz |
| | SREFCLK Duty Cycle | 40 | 60 | % |
| tS$_{SBIADD}$ | All SBI ADD BUS Inputs Set-Up Time to SREFCLK | 2.7 | | ns |
| tH$_{SBIADD}$ | All SBI ADD BUS Inputs Hold Time to SREFCLK | 0 | | ns |
| tP$_{SBIADD}$ | SREFCLK to SAJUST_REQ Valid | 1 | 6 | ns |
| tZ$_{SBIADD}$ | SREFCLK to SAJUST_REQ Tristate | 1 | 6 | ns |

**Notes on System Side SBI Input Timing:**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

**Figure 88        - System Side SBI ADD BUS Timing**
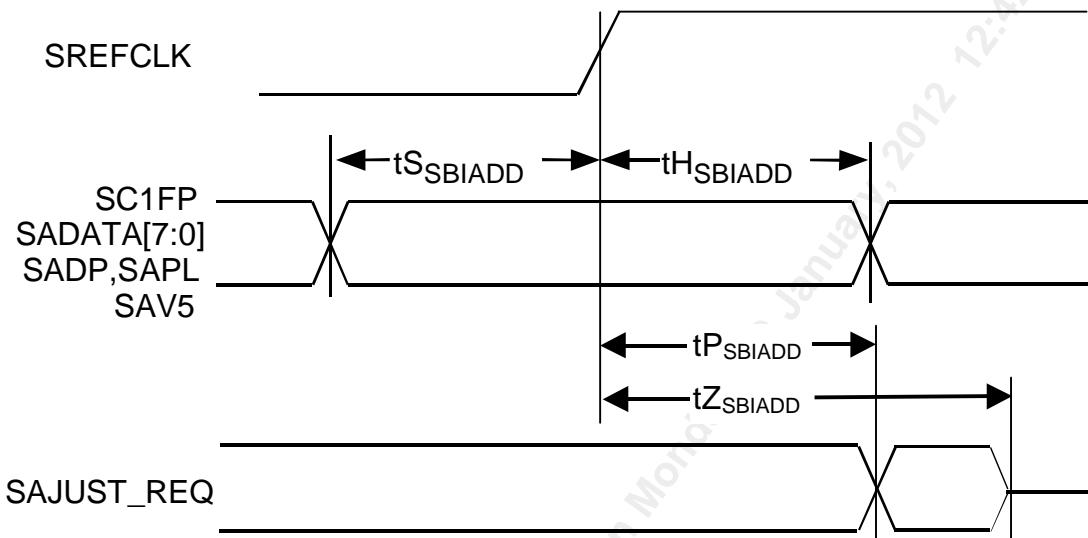


**Table 59        – System Side SBI DROP BUS Timing - 19.44 MHz (Figure 86 and Figure 89)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $tS_{SBIDROP}$ | SDC1FP Set-Up Time to SREFCLK | 4 | | ns |
| $tH_{SBIDROP}$ | SDC1FP Hold Time to SREFCLK | 0 | | ns |
| $tP_{SDC1FP}$ | SREFCLK to SDC1FP Output Valid | 2 | 17 | ns |
| $tP_{SBIDROP}$ | SREFCLK to All SBI DROP BUS Outputs except SDC1FP Valid | 2 | 17 | ns |
| $tZ_{SBIDROP}$ | SREFCLK to All SBI DROP BUS Outputs except SDC1FP Tristate | 2 | 16 | ns |
| $tP_{OUTEN}$ | SBIDET[1] and SBIDET[0] low to All SBI DROP BUS Outputs Valid | 0 | 17 | ns |
| $tZ_{OUTEN}$ | SBIDET[1] and SBIDET[0] high to All SBI DROP BUS Outputs Tristate | 0 | 16 | ns |
| $tS_{DET}$ | SBIDET[n] Set-Up Time to SREFCLK | 4 | | ns |
| $tH_{DET}$ | SBIDET[n] Hold Time to SREFCLK | 0 | | ns |

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**Table 60     – System Side SBI DROP BUS Timing - 77.76 MHz (Figure 89 to Figure 90)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| tS$_{SBIDROP}$ | SDC1FP Set-Up Time to SREFCLK | 3 | | ns |
| tH$_{SBIDROP}$ | SDC1FP Hold Time to SREFCLK | 0 | | ns |
| tP$_{SDC1FP}$ | SREFCLK to SDC1FP Output Valid | 1 | 7 | ns |
| tP$_{SBIDROP}$ | SREFCLK to All SBI DROP BUS Outputs except SDC1FP Valid | 1 | 7 | ns |
| tZ$_{SBIDROP}$ | SREFCLK to All SBI DROP BUS Outputs except SDC1FP Tristate | 1 | 7 | ns |

**Notes on System Side SBI Output Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.

3. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

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**Figure 89     - SBI System Side DROP BUS Timing**
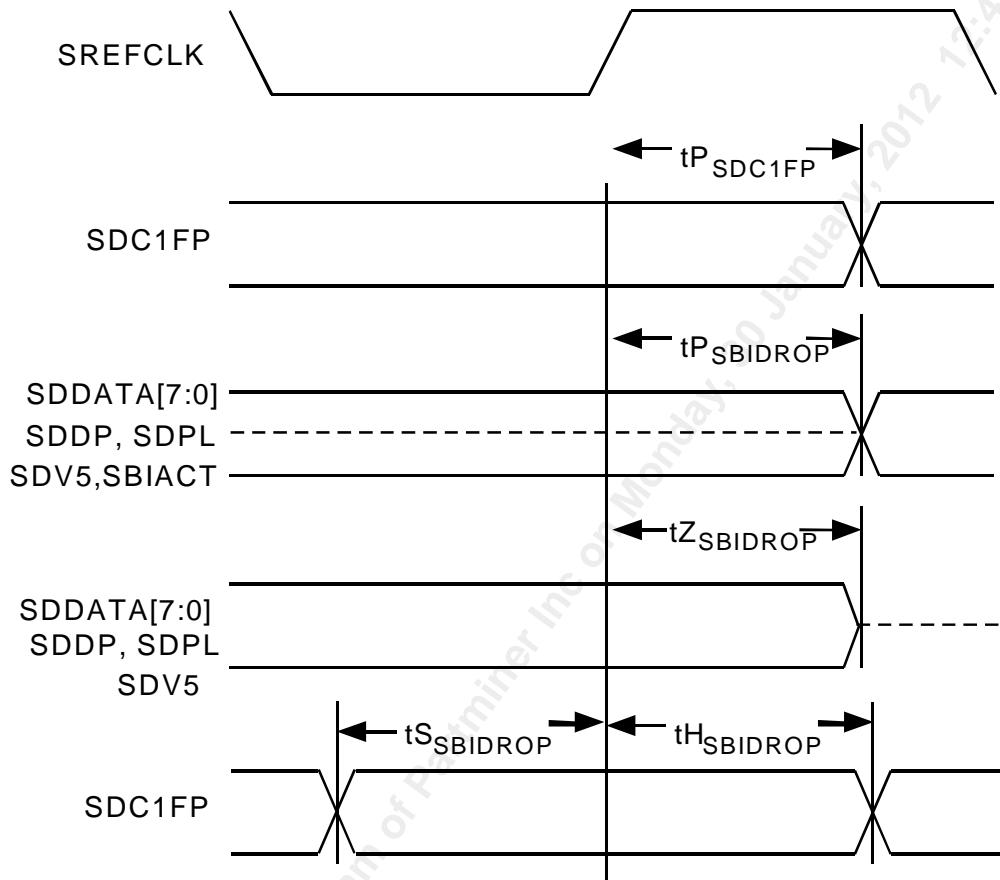


**Figure 90     - SBI System Side DROP BUS Collision Avoidance Timing**

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*INTEGRATED VT/TU MAPPER AND M13 MUX*
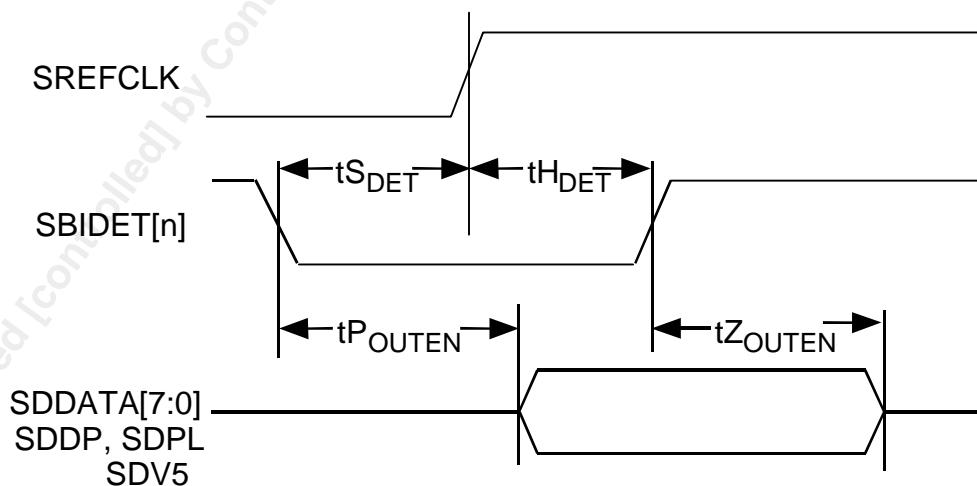
**Table 61 - Egress Flexible Bandwidth Port Timing (Figure 91)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
|  | EFBWCLK[n] Frequency | 0 | 52 | MHz |
|  | EFBWCLK[n] High Phase | 7 |  | ns |
|  | EFBWCLK[n] Low Phase | 7 |  | ns |
| $tS_{EFBW}$ | EFBWDREQ[n] Set-Up Time to EFBWCLK[n] Rising Edge | 4 |  | ns |
| $tH_{EFBW}$ | EFBWDREQ[n] Hold Time to EFBWCLK[n] Rising Edge | 0 |  | ns |
| $tP_{EFBW}$ | EFBWCLK[n] Falling Edge to EFBWDAT[n] and EFBWEN[n] Valid | 2 | 15 | ns |

**Figure 91 - Egress Flexible Bandwidth Port Timing**
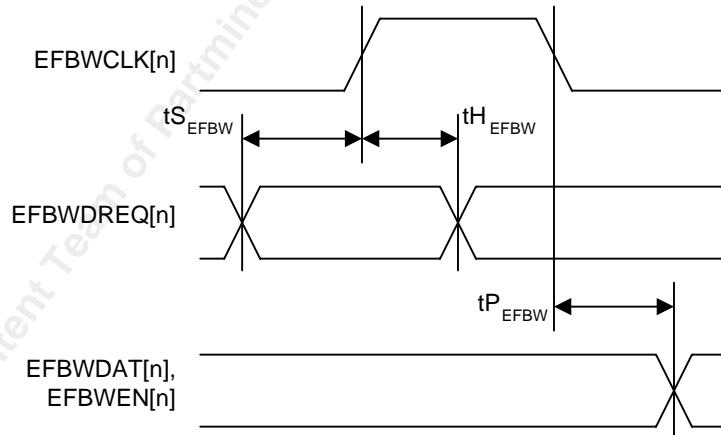


**Table 62 - Ingress Flexible Bandwidth Port Timing (Figure 92)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
|  | IFBWCLK[n] Frequency | 0 | 52 | MHz |
|  | IFBWCLK[n] High Phase | 7 |  | ns |
|  | IFBWCLK[n] Low Phase | 7 |  | ns |
| $tS_{IFBW}$ | IFBWDAT[n] and IFBWEN[n] Set-Up Time to IFBWCLK[n] Rising Edge | 4 |  | ns |

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| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| tH$_{IFBW}$ | IFBWDAT[n] and IFBWEN[n] Hold Time to IFBWCLK[n] Rising Edge | 1 | | ns |

**Figure 92     - Ingress Flexible Bandwidth Port Timing**
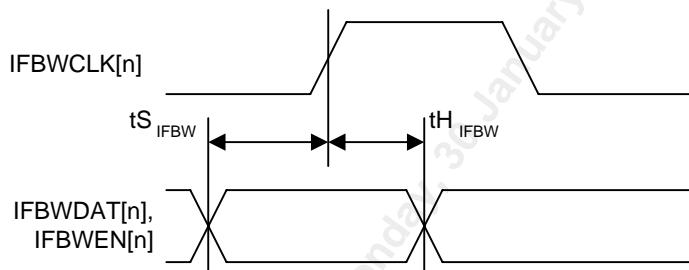


**Notes on Flexible Bandwidth Port Timing:**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs.

**Table 63     -  H-MVIP Egress Timing (Figure 93)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| | CMV8MCLK Frequency (See Note 3) | 16.384 -50 ppm | 16.384 +50 ppm | MHz |
| | CMV8MCLK Duty Cycle | 40 | 60 | % |
| | CMVFPC Frequency (See Note 4) | 4.092 | 4.100 | MHz |
| | CMVFPC Duty Cycle | 40 | 60 | % |

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| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| tP$_{MVC}$ | CMV8MCLK to CMVFPC skew | -10 | 10 | ns |
| tS$_{HMVED}$ | MVED[21:1], CASED[21:1], CCSED[3:1] Set-Up Time | 5 | | ns |
| tH$_{HMVED}$ | MVED[21:1], CASED[21:1], CCSED[3:1] Hold Time | 5 | | ns |
| tS$_{MVFPB}$ | CMVFPB Set-Up Time | 5 | | ns |
| tH$_{MVFPB}$ | CMVFPB Hold Time | 5 | | ns |

### Notes on H-MVIP Egress Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Measured between any two CMV8MCLK falling edges.

4. Measured between any two CMVFPC falling edges.

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**Figure 93      - H-MVIP Egress Data & Frame Pulse Timing**
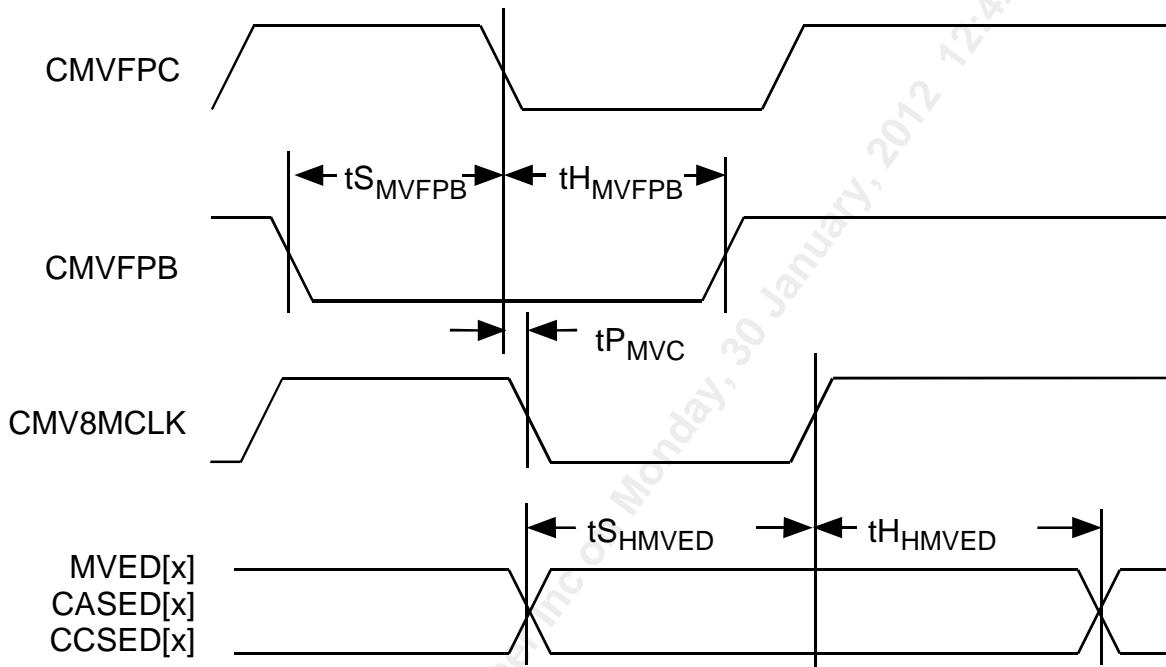


**Table 64      -  H-MVIP Ingress Timing (Figure 94)**

| Symbol | Description | Min | Max | Units |
|--------|-------------|-----|-----|-------|
| $tP_{HMVID}$ | CMV8MCLK Low to MVID[21:1], CASID[21:1], CCSID[3:1], TS0ID Valid | 4 | 25 | ns |

**Notes on H-MVIP Ingress Timing:**

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs.

3. Output propagation delays of signal outputs that are specified in relation to a reference output are measured with a 50 pF load on both the signal output and the reference output.

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**Figure 94    - H-MVIP Ingress Data Timing**
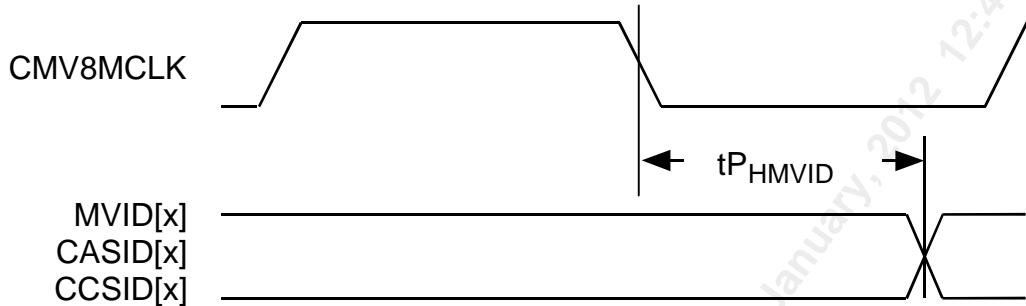


**Table 65    - XCLK Input (Figure 95)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{LXCLK}$ | XCLK_T1 and XCLK_E1 Low Pulse Width | 8 | | ns |
| $t_{HXCLK}$ | XCLK_T1 and XCLK_E1 High Pulse Width | 8 | | ns |
| $t_{XCLK}$ | XCLK_T1 and E1_XLK Period (typically 1/37.056 MHz ± 32 ppm for XCLK_T1 and 1/49.152 MHz for XCLK_E1) | 20 | | ns |

**Figure 95    - XCLK Input Timing**

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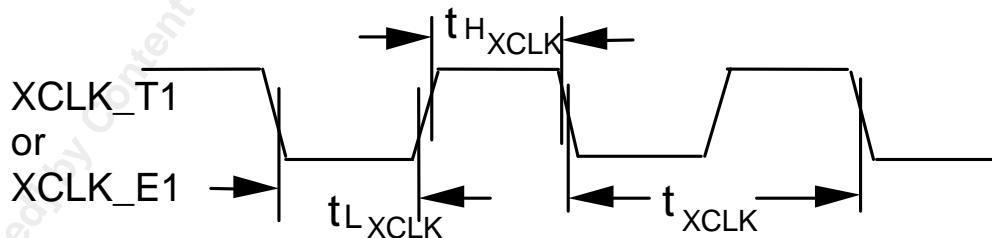
**Table 66      - Transmit Line Interface Timing (Figure 96)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | CTCLK Frequency (Must be integer multiple of 8 KHz.) | 0.008 | 2.048 | MHz |
| $t_{HCTCLK}$ | CTCLK High Duration | 60 | | ns |
| $t_{LCTCLK}$ | CTCLK Low Duration | 60 | | ns |

**Figure 96      - Transmit Line Interface Timing**
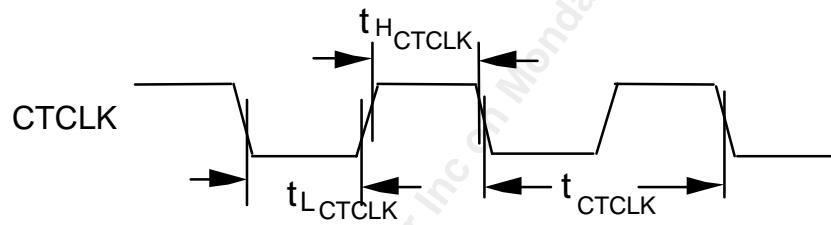


**Notes on Ingress and Egress Serial Interface Timing:**

1. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps.  Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

4. Setup, hold, and propagation delay specifications are shown relative to the default active clock edge, but are equally valid when the opposite edge is selected as the active edge.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

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6.  Output propagation delays are measured with a 50 pF load on all outputs with the exception of the high speed DS3/E3 outputs (TCLK[3:1], TPOS/TDAT[3:1], TNEG/TMFP[3:1]).  The TCLK[3:1], TPOS/TDAT[3:1], TNEG/TMFP[3:1] output propagation delays are measured with a 20 pF load.

**Table 67       - Remote Serial Alarm Port Timing**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
|  | RADEASTCK and RADWESTCK Frequency | 1.344 | 10 | MHz |
|  | RADEASTCK and RADWESTCK Duty Cycle | 40 | 60 | % |
| $t_{HRADFP}$ | RADEASTFP and RADWESTFP Hold Time | 5 |  | ns |
| $t_{SRADFP}$ | RADEASTFP and RADWESTFP Setup Time | 5 |  | ns |
| $t_{HRAD}$ | RADEAST and RADWEST Hold Time | 5 |  | ns |
| $t_{SRAD}$ | RADEAST and RADWEST Setup Time | 5 |  | ns |

**Figure 97       - Remote Serial Alarm Port Timing**
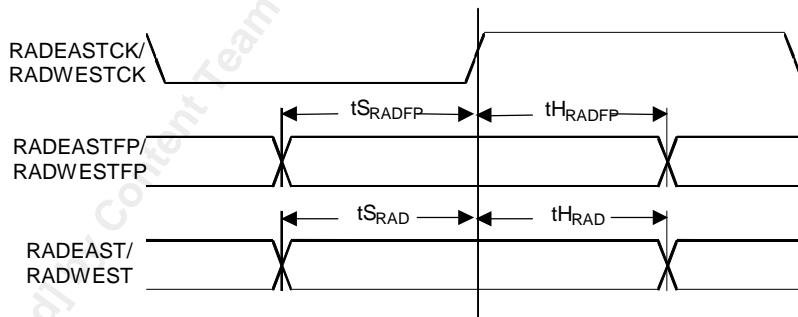
**Table 68       - JTAG Port Interface**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| | TCK Frequency | | 1 | MHz |
| | TCK Duty Cycle | 40 | 60 | % |
| $tS_{TMS}$ | TMS Set-up time to TCK | 50 | | ns |
| $tH_{TMS}$ | TMS Hold time to TCK | 50 | | ns |
| $tS_{TDI}$ | TDI Set-up time to TCK | 50 | | ns |
| $tH_{TDI}$ | TDI Hold time to TCK | 50 | | ns |
| $tP_{TDO}$ | TCK Low to TDO Valid | 2 | 50 | ns |
| $tV_{TRSTB}$ | TRSTB Pulse Width | 100 | | ns |

**Figure 98       - JTAG Port Interface Timing**

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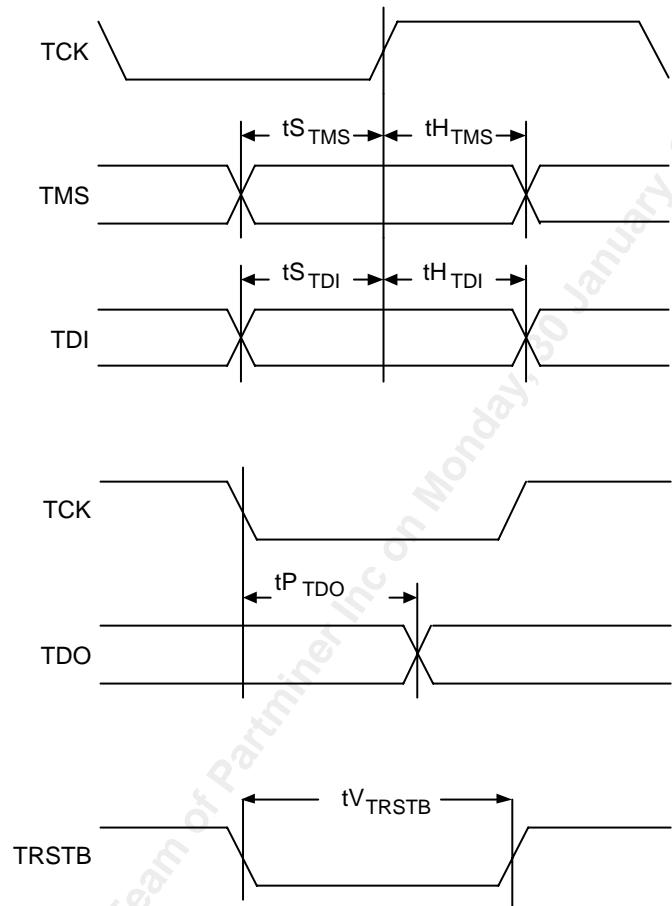
# 18    ORDERING AND THERMAL INFORMATION

### Table 69        - Ordering Information

| Part No. | Description |
|----------|-------------|
| PM8316-PI | 324-Pin Plastic Ball Grid Array (PBGA) |
| PM8316-PGI | 324-Pin PBGA, 23 x 23 x 2.28 mm, 1.00 mm BP (RoHS-Compliant) |

This product is designed to operate over a wide temperature range and is suited for industrial applications such as central office equipment or in-field locations.

| | |
|---|---|
| Maximum long-term operating junction temperature to ensure adequate long-term life | 105 $^0$C |
| Maximum junction temperature for short-term excursions with guaranteed continued functional performance.[1] This condition will typically be reached when local ambient reaches 70 Deg C. | 125 $^0$C |
| Minimum ambient temperature | -40 $^0$C |

| Thermal Resistance vs Air Flow[2] | | | |
|---|---|---|---|
| Airflow | Natural Convection | 200 LFM | 400 LFM |
| $\Theta_{JA}$ ($^0$C/W) | 18.6 | 15.2 | 12.4 |

| Device Compact Model[3] | |
|---|---|
| $\Theta_{JT}$ ($^0$C/W) | 5.6 |
| $\Theta_{JB}$ ($^0$C/W) | 11.5 |

| Operating power is dissipated in package (watts) at worst case power supply | |
|---|---|
| Power (watts) | 1.0W |

Ambient
$\Theta_{JT}$ ← Device Compact Model
Junction
$\Theta_{JB}$
Board
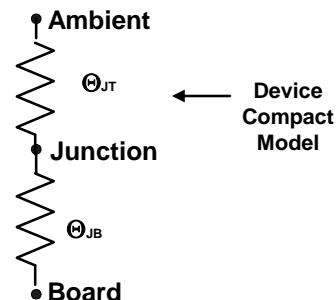
**Notes**

1.    Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core.

2.    $\Theta_{JA}$ , the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P)

3.    $\Theta_{JB}$, the junction-to-board thermal resistance and $\Theta_{JT,}$ the residual junction to ambient thermal resistance are obtained by simulating conditions described in JEDEC Standard, JESD 15-8.

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## 19    MECHANICAL INFORMATION

### Figure 99   - 324 Pin PBGA 23x23mm Body



TOP VIEW

BOTTOM VIEW

SIDE VIEW
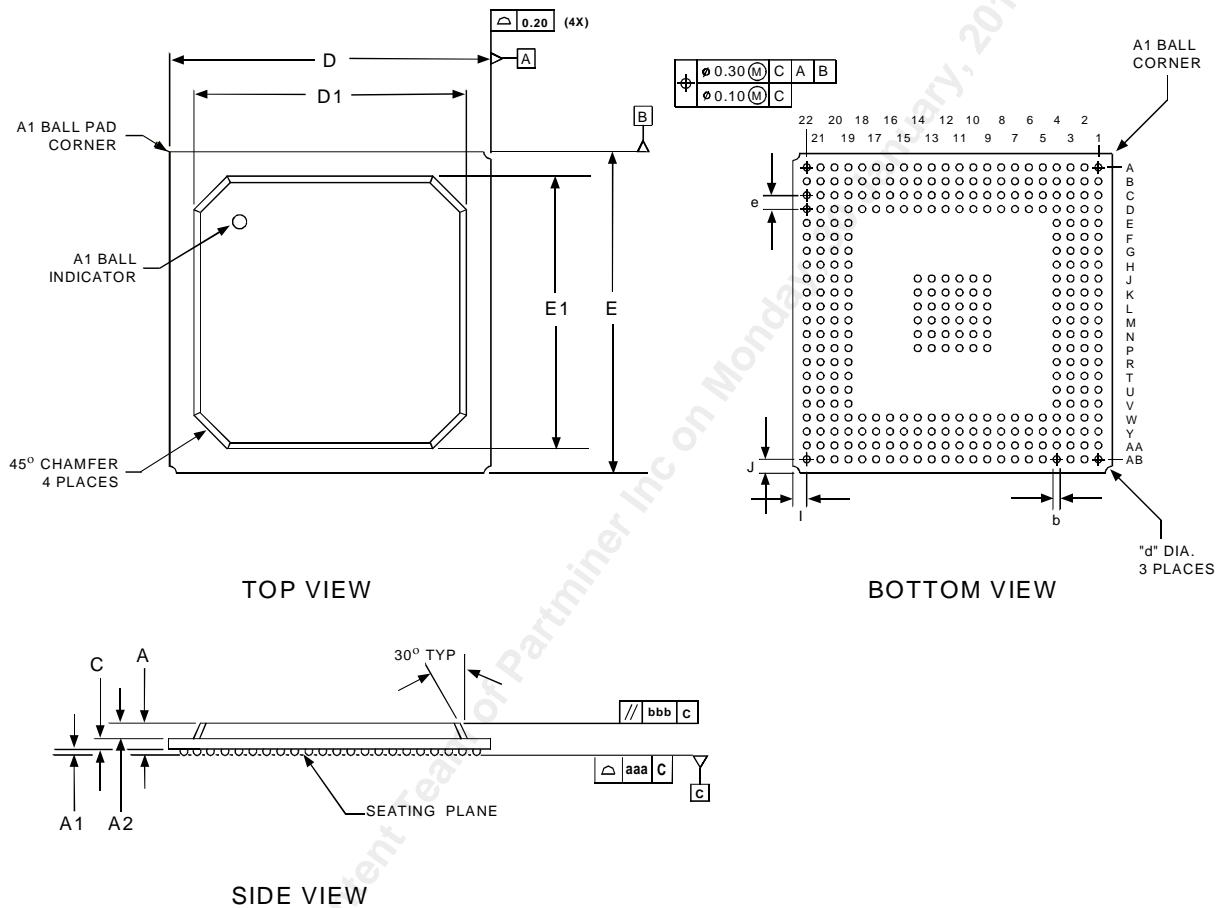
NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
       2) DIMENSION aaa DENOTES COPLANARITY.
       3) DIMENSION bbb DENOTES PARALLEL.

**PACKAGE TYPE : 324 PLASTIC BALL GRID ARRAY - PBGA**

**BODY SIZE : 23 x 23 x 2.28 MM (4 layer)**

| Dim. | A (2 layer) | A (4 layer) | A1 | A2 | D | D1 | C (2 layer) | C (4 layer) | E | E1 | I | J | b | d | e | aaa | bbb |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Min | 1.82 | 2.07 | 0.40 | 1.12 | - | 19.00 | 0.30 | 0.55 | - | 19.00 | - | - | 0.50 | - | - | - | - |
| Nom. | 2.03 | 2.28 | 0.50 | 1.17 | 23.00 | 19.50 | 0.36 | 0.61 | 23.00 | 19.50 | 1.00 | 1.00 | 0.63 | 1.00 | 1.00 | - | - |
| Max. | 2.22 | 2.49 | 0.60 | 1.22 | - | 20.20 | 0.40 | 0.67 | - | 20.20 | - | - | 0.70 | - | - | 0.15 | 0.35 |

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## <u>NOTES</u>

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