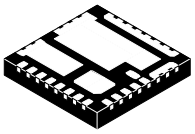
Integrated Driver and MOSFET with Over Current Limit

Product Preview

NCP303750



PQFN31 5x5, 0.5P
CASE 483BR

The NCP303750 integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.

The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NCP303750 integrated solution greatly reduces package parasitic and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 50 A
- Overcurrent Protection: 90 A Minimum
- Capable of Switching at Frequencies up to 1 MHz
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3-level PWM Inputs
- Option for Zero Cross Detection with 3-level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Low Power Shutdown Mode
- Thermal Warning Output

Typical Applications

- Desktop and AI Servers
- Graphic Cards
- Routers and Switches

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM

NNN	= Serialization Code
XX	= IC Identification
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

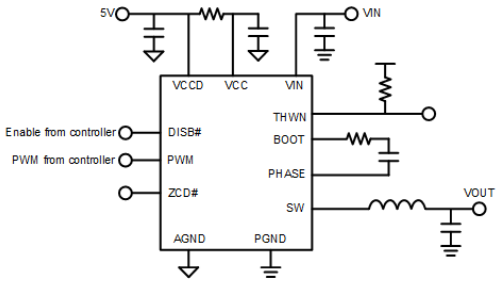


Figure 1. Application Schematic

ORDERING INFORMATION

Device	Package	Shipping†
NCP303750MNTWG	PQFN31	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

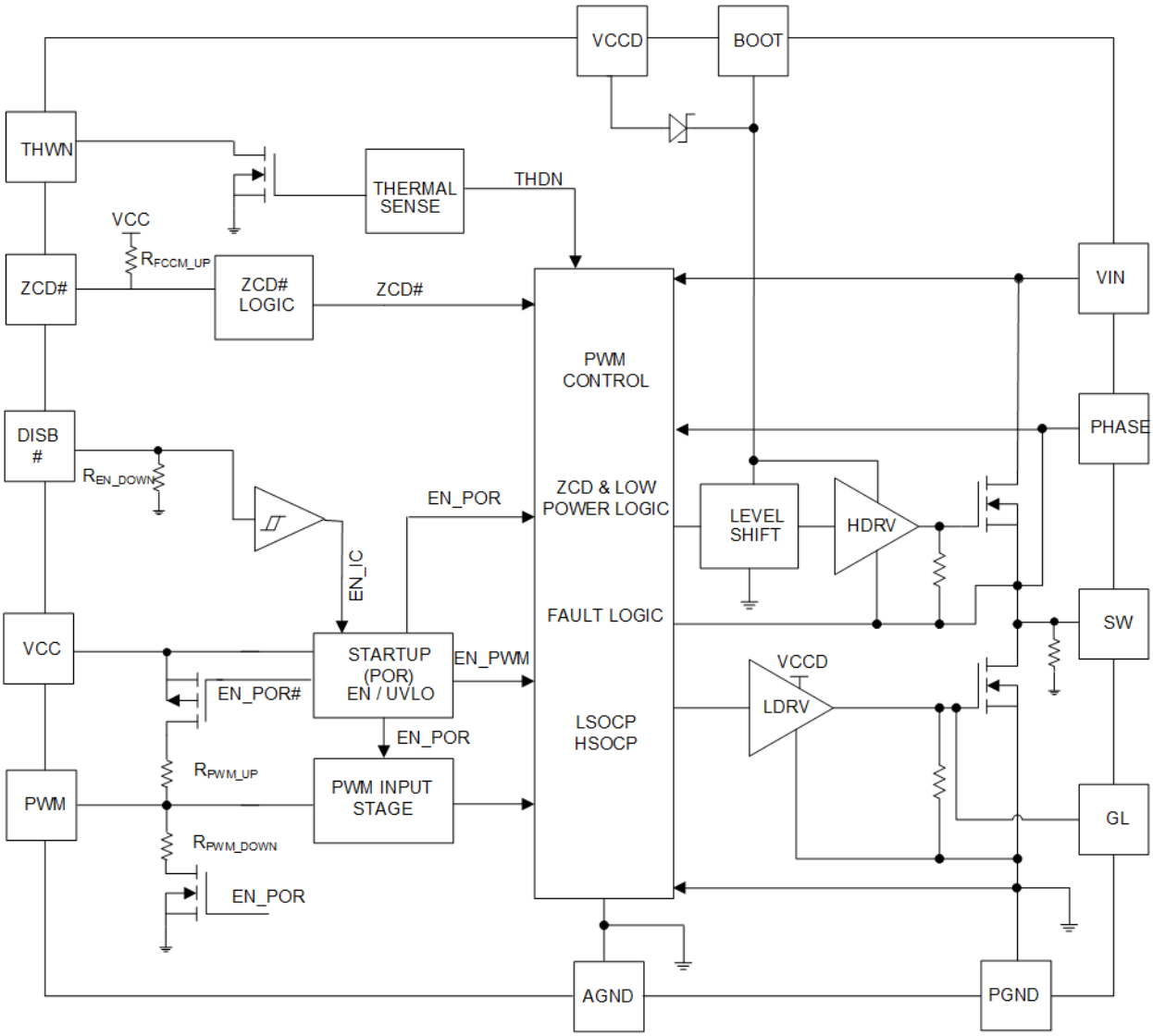


Figure 2. Block Diagram

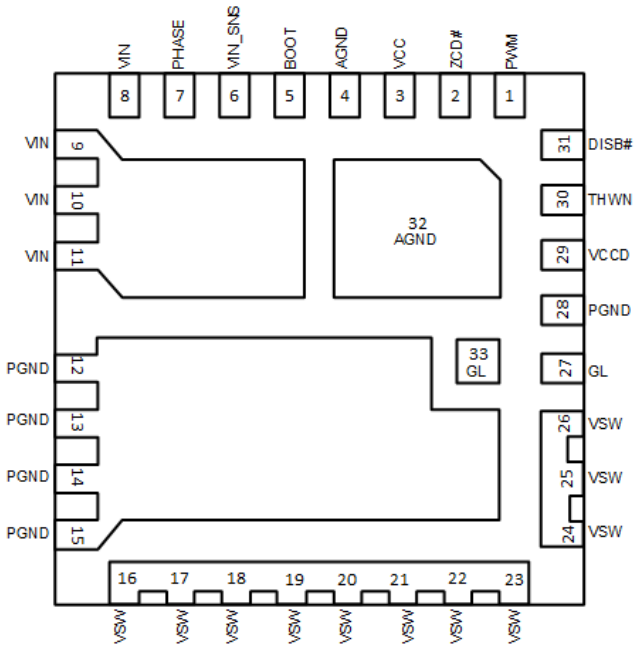


Figure 3. Pin Connections

PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	PWM	PWM Control Input and Zero Current Detection Enable PWM divider resistors connected in both states when DISB# = High PWM divider resistors disconnected in both states when DISB# = Low
2	ZCD#	ZCD / FCCM select input (see Table 1): ZCD# = High – Placing PWM into mid-state pulls GH and GL low without delay. There is an internal pull-up resistor to VCC on this pin when DISB# = High. ZCD# = Low – State of PWM determine whether the NCP303750 performs ZCD or not.
3	VCC	Control Power Supply Input
4, 32	AGND	Signal Ground (pin 4 and pad 32 are internally connected)
5	BOOT	Bootstrap Voltage
6	VIN_SNS	Input connection for overcurrent sensing. Internally tied to VIN. Pin can be floated or connected to VIN.
7	PHASE	Bootstrap Capacitor Return
8–11	VIN	Conversion Supply Power Input
12–15, 28	PGND	Power Ground
16–26	VSW	Switch Node Output
27, 33	GL	Low Side FET Gate Access (pin 27 and pad 33 are internally connected)
29	VCCD	Driver Power Supply Input
30	THWN	Thermal warning indicator. This is an open-drain output. When the temperature at the driver die reaches T_{THWN}, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull-down resistor on this pin.

ABSOLUTE MAXIMUM RATINGS (Electrical Information – all signals referenced to PGND unless noted otherwise)

Pin Name / Parameter	Min	Max	Unit
VCC, VCCD	−0.3	6	V
VIN	−0.3	30	V
VIN (< 5 ns)	–	35	V
VIN to PHASE (DC)	−0.3	30	V
VIN to PHASE (< 5 ns)	–	35	V
BOOT (DC)	−0.3	35	V
BOOT (< 2 ns)	−11.5	40	V
BOOT to PHASE (DC)	−0.3	7	V
BOOT to PHASE (< 5 ns)	–	9.0	V
VSW, PHASE (DC)	−0.3	30	V
VSW, PHASE (< 20 ns)	−7	35	V
PHASE (< 2 ns)	−18	35	V
All Other Pins	−0.3	V_{VCC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (under **onsemi** SPS Thermal Board) (Note 2)	$R_{\theta JA}$	17.1	°C/W
	$R_{\theta J-PCB}$	2.97	°C/W
	$R_{\theta JC}$	12.06	°C/W
Operating Junction Temperature Range (Note 1)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Maximum Power Dissipation		10.5	W
Moisture Sensitivity Level	MSL	1	

1. The maximum package power dissipation must be observed.
2. 70 x 70 x 1.7211 mm – 2S4P

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage	VIN		2.8	12	16	V
Continuous Output Current		F_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, T_A = 25 °C	–	–	45	A
		F_{SW} = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, T_A = 25 °C	–	–	50	A
Peak Output Current		Duration = 10 ms	–	–	80	A
		Duration = 10 μs, Period = 10 ms	90	100	110	A
Junction Temperature			−40	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

((V$_{VCC}$ = V$_{VCCD}$ = 5.0 V, V$_{VIN}$ = 12 V, V$_{DISB\#}$ = 2.0 V, C$_{VCCD}$ = C$_{VCC}$ =1.0 μF unless specified otherwise) Min/Max values are valid for the temperature range −40 °C ≤ T$_J$ ≤ 125 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC/VCCD SUPPLY CURRENT						
Normal Mode (Ivcc+Ivccd)	I_{vcc_nm}	DISB# = 5 V, PWM = 400 kHz	–	–	26	mA
Operating (No switching)	I_{vcc_op}	DISB# = 5 V	0.5	–	3.5	mA
Standby Current	I_{vcc_dis}	DISB# = GND (−40 °C ≤ T$_J$ ≤ 85 °C)	–	–	5	μA
UNDERVOLTAGE LOCKOUT						
UVLO Start Threshold	V_{uvlo}	VCC Rising	3.9	4.25	4.5	V
UVLO Hysteresis	V_{uvlo_hys}	VCC Falling	200	300	500	mV
POR to Driver Ready time	t_POR	DISB# = HIGH	10	–	100	μs
BST UVLO Rising	$V_{bst\_uvlo\_r}$	BST − SW	3.20	3.47	3.7	V
BST UVLO Falling	$V_{bst\_uvlo\_f}$	BST − SW	3.05	3.31	3.55	V
DISB# INPUT						
Rising Transition Threshold		VCC = VCCD = 5 V, PWM in operation	2	–	VCC	V
Falling Transition Threshold		VCC = VCCD = 5 V, PWM disabled	0	–	0.65	V
Passive Pull-Down Resistance	$R_{disb\#}$	DISB# to GND	100	300	500	kΩ
Enable Time	$T_{disb\#\_en}$	PWM = Low, Delay from EN from L to H to LG from L to H	1	15	30	us
Propagation Delay Time (Note 4)	Tdisb#_pdt	PWM = GND, Delay Between EN from HIGH to LOW to GL from HIGH to LOW	–	15	–	ns
ZCD# INPUT						
ZCD# Input Voltage High			1.2	–	V_{CC}	V
ZCD# Input Voltage Low			0.0	–	0.8	V
ZCD# Input Resistance	$R_{ZCD\#\_UP}$	Pull−up resistance to VCC, DISB# = High	300	500	800	kΩ
PWM INPUT						
Input Voltage High	V_{PWM_HI}		2.7	–	V_{CC}	V
Input Mid-state Voltage	V_{PWM_MID}		1.2	–	2.3	V
Input Low Voltage	V_{PWM_LO}		0	–	0.8	V
Input Resistance	R_{PWM_HIZ}	DISB# = Low	10	–	5000	MΩ
Input Resistance	RP_{WM_BIAS}	DISB# = High	7	14.6	25	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	DISB# = High	1.6	1.9	2.2	V
Non-overlap Delay, Leading Edge (Note 4)	T_{NOL_L}	GL Falling = 1 V to Gh−VSW Rising = 1 V	–	6	–	ns
Non-overlap Delay, Trailing Edge (Note 4)	T_{NOL_T}	GH−VSW Falling = 1 V to GL Rising = 1 V	–	8	–	ns
PWM Propagation Delay, Rising (Note 4)	T_{PWM,PD_R}	PWM = High to GL = 90%	–	20	–	ns
PWM Propagation Delay, Falling (Note 4)	T_{PWM,PD_F}	PWM = Low to SW = 90%	–	20	–	ns
Exiting PWM Mid-state Propagation Delay, Tri-to-Low (Note 4)	$T_{PWM\_EXIT\_L}$	PWM = Mid-to-Low to GL = 10%	–	16	–	ns
Exiting PWM Mid-state Propagation Delay, Tri-to-High (Note 4)	$T_{PWM\_EXIT\_H}$	PWM = Mid-to-High to VSW = 10%	–	17	–	ns

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} =1.0 μF unless specified otherwise) Min/Max values are valid for the temperature range −40 °C ≤ T_J ≤ 125 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ZCD FUNCTION						
Zero Cross Detect Threshold (Note 4)	V_{ZCD}		–	0	–	mV
ZCD Blanking + Debounce Time (Note 4)	t_{BLNK}		–	150	–	ns
OVERCURRENT PROTECTION (OCP)						
Positive overcurrent (HS Sensing) (Note 3)		Leading edge blanking HS = 100 ns	90	100	110	A
Positive overcurrent (LS Sensing) (Note 3)		Leading edge blanking LS = 50 ns	90	100	110	A
Negative overcurrent (Note 3)	NOCP	Leading edge blanking = 50 ns	−40	−50	−60	A
THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature (Note 4)	T_{THWN}	Temperature at driver die	–	165	–	°C
Thermal Warning Hysteresis (Note 4)	T_{THWN_HYS}		–	30	–	°C
Thermal Shutdown Temperature (Note 4)	T_{THDN}		–	190	–	°C
Thermal Shutdown Hysteresis (Note 4)	T_{THDN_HYS}		–	30	–	°C
THWN Voltage	VTHWN	500 μA Sink	100	200	400	mV
BOOTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	100	380	500	mV
LOW-SIDE DRIVER						
GL Rise Time (Note 4)	T_{R_GL}	GL = 10% to 90%, C_{LOAD} = 3.0 nF	–	12	–	ns
GL Fall Time (Note 4)	T_{F_GL}	GL = 90% to 10%, C_{LOAD} = 3.0 nF	–	7	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Min/Max values are valid for the temperature range 0 °C ≤ T_J ≤ 125 °C
4. Guaranteed by design

Table 1. TRUTH TABLE

INPUT TRUTH TABLE				
DISB#	**PWM** (Note 5)	**ZCD#**	**GH (not a pin)**	**GL**
L	X	X	L	L
H	H	X	H	L
H	L	X	L	H
H	MID	L	L	ZCD (Note 6)
H	MID	H or floating to H	L	L (Note 7)

5. PWM input is driven to mid-state with internal divider resistors when PWM input is undriven externally.
6. GL goes low following 150 ns blanking time and then SW exceeding ZCD threshold.
7. There is no delay before GL goes low.

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN} = 12 V, V_{CC} = V_{CCD} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25 °C and natural convection cooling, unless otherwise noted.)

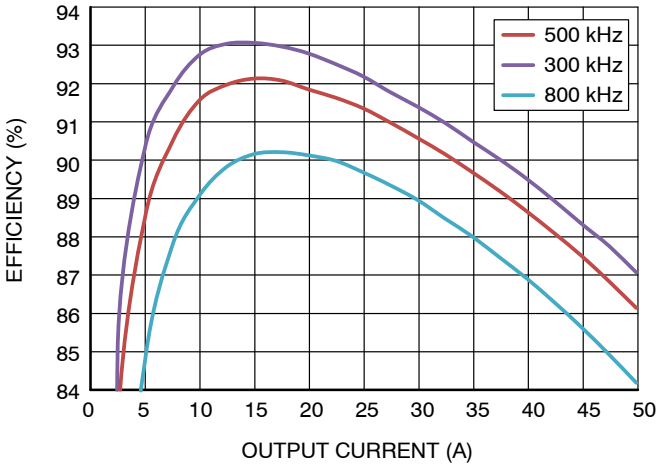


Figure 4. Efficiency – 16 V Input, 1.0 V Output

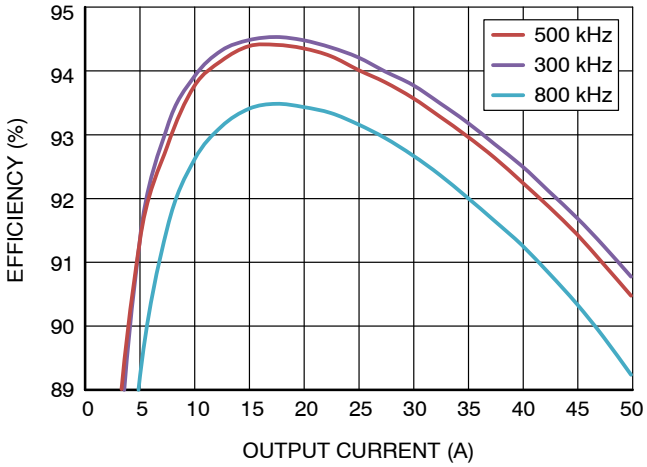


Figure 5. Efficiency – 16 V Input, 1.8 V Output

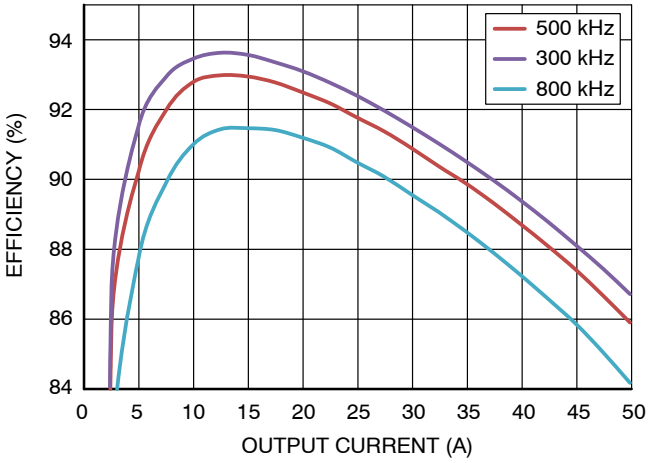


Figure 6. Efficiency – 12 V Input, 1.0 V Output

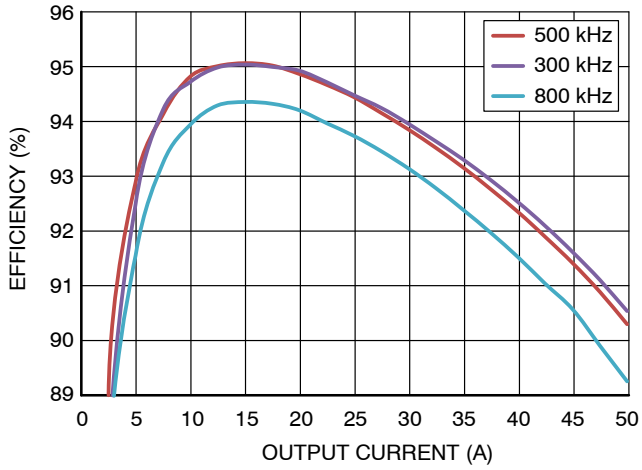


Figure 7. Efficiency – 12 V Input, 1.8 V Output

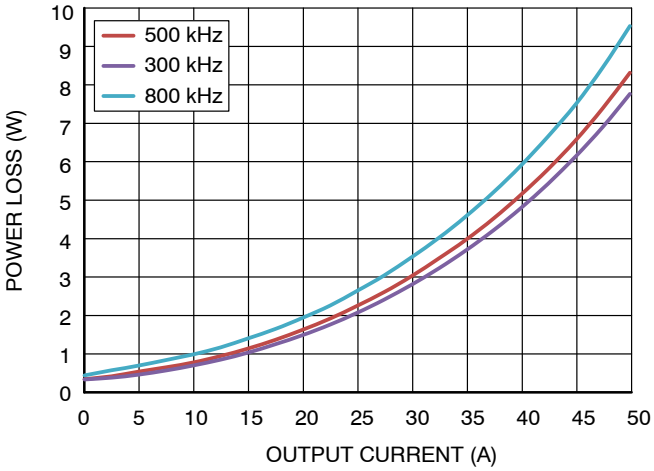


Figure 8. Power Losses vs. Output Current, 12 V Input, 1.0 V Output

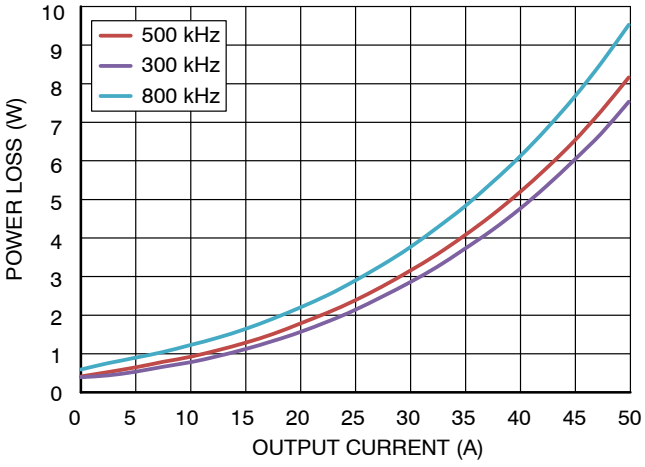


Figure 9. Power Losses vs. Output Current, 16 V Input, 1.0 V Output

TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: V_{IN} = 12 V, V_{CC} = V_{CCD} = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH, T_A = 25 °C and natural convection cooling, unless otherwise noted.)

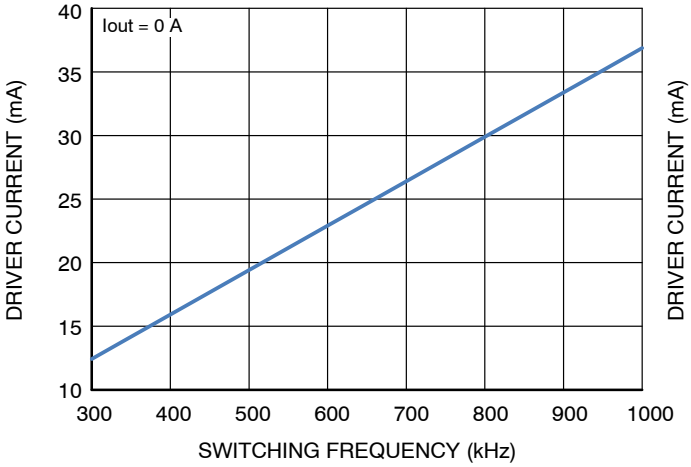


Figure 10. Driver Supply Current vs. Switching Frequency

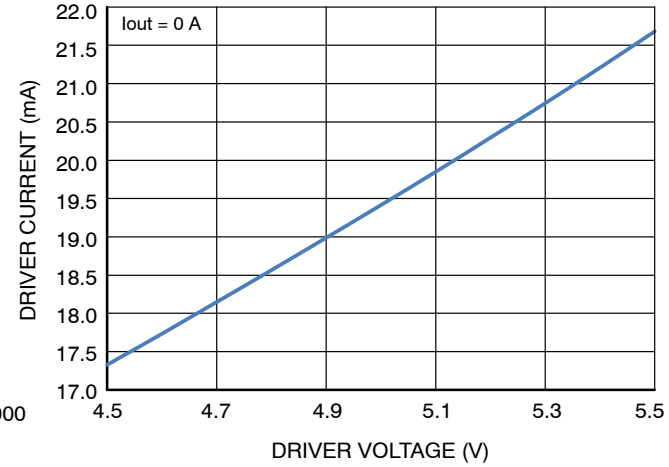


Figure 11. Driver Supply Current vs. Driver Supply Voltage

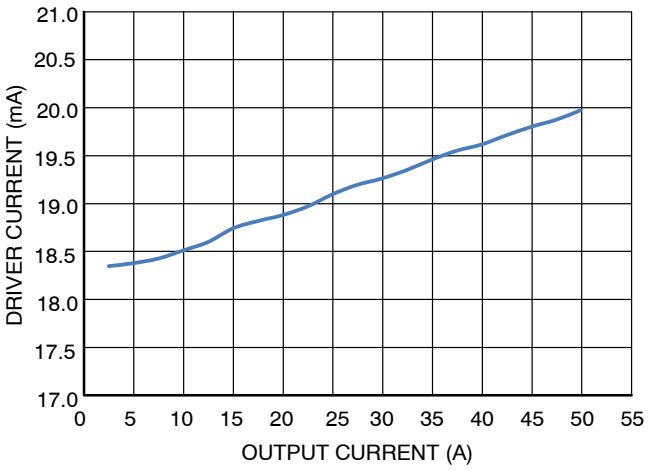


Figure 12. Driver Supply Current vs. Output Current

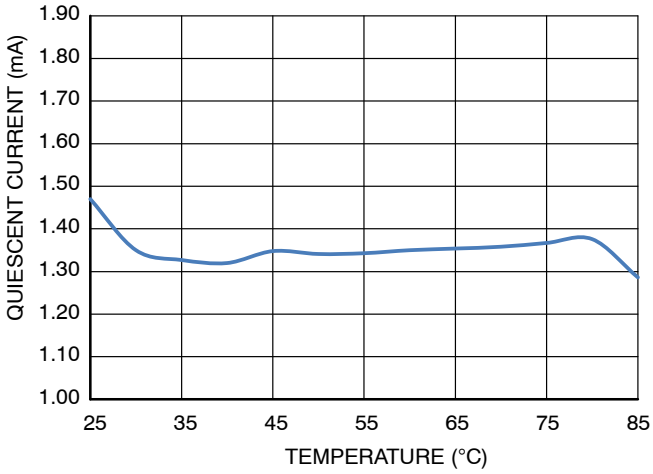


Figure 13. Driver Quiescent Current vs. Temperature

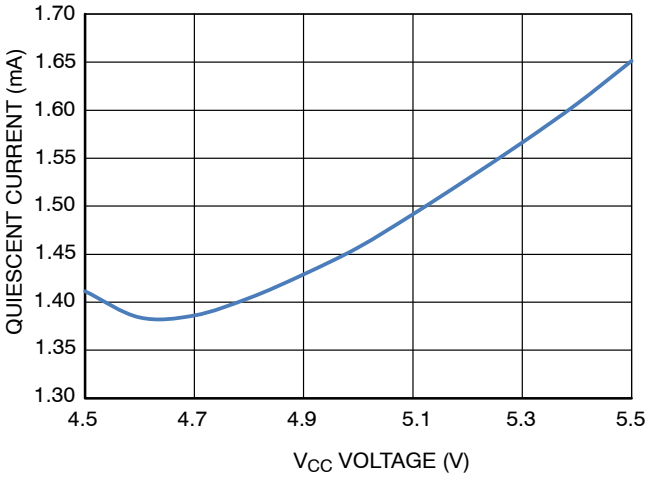


Figure 14. Driver Quiescent Current vs. Driver Voltage

The NCP303750 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP303750 supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high-side and low-side integrated MOSFETs.

Low-Side Driver

The low-side driver drives an internal, ground-referenced low-RDS(on) N-Channel MOSFET. The voltage supply for the low-side driver is internally connected to the VCCD and PGND pins.

High-Side Driver

The high-side driver drives an internal, floating low-RDS(on) N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node via the PHASE pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NCP303750 is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (See Figure 1). When the PWM input is driven high, the high-side driver turns on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the voltage at the VSW and PHASE pins rises. When the high-side MOSFET is fully turned on, the switch node settles to VIN and the BST pin settles to VIN + VCCD (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (CBST) and an integrated diode to provide current to the HS Driver. A multi-layer ceramic capacitor (MLCC) (typ. 100 nF) should be used as the bootstrap capacitor. An optional 1 to 4 Ω resistor in series with the bootstrap capacitor decreases the VSW overshoot.

Bootstrap UVLO

The BST pin is monitored by an Undervoltage Lockout Circuit (UVLO).

When VBST − VSW is below the UVLO falling threshold, the PWM signal will be ignored so that the HS FET will be turned off to protect the device.

MOSFET switching may resume when VBST − VSW is above the UVLO rising threshold.

Overlap Protection Circuit

It is important to avoid cross-conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP303750 prevents cross-conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non-overlap (NOL) time (the time between the turn-off of one MOSFET and the turn-on of the other MOSFET). When the PWM input pin is driven high, the gate of the low-side MOSFET (LSGATE) goes low after a propagation delay (tpdlGL). The time it takes for the low-side MOSFET to turn off is dependent on the total charge on the low-side MOSFET gate.

Zero Current Detect

The Zero Current Detect PWM (ZCD_PWM) mode is enabled when ZCD# is low (see Table 1).

With PWM set to > VPWM_HI, GL goes low and GH goes high after the non-overlap delay. When PWM is driven to < VPWM_HI and to > VPWM_LO, GL goes high after the non-overlap delay, and stays high for the duration of the ZCD blanking timer and a de-bounce timer for a total (TZCD_BLANK) of 145 ns.

The ZCD offset is calibrated at startup upon exiting from VCC_UVLO and cleared on POR.

PWM Input

The PWM Input pin is a tri-state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. The PWM input can work with controllers that require programming resistances to ground. These resistances can range from 10 kΩ to 300 kΩ depending on the application.

When DISB# is low, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin.

When DISB# is high, the NCP303750 has internal resistors to VCC and AGND.

PWM to SWN ON time width variation is within ± 3 ns.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High-Side FET to prevent power transfer. The pin has a pull-down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull-up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP303750.

Table 2. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table 1)
H	Open	Disabled (GH = GL = 0)

Thermal Warning Output

The THWN pin is an open drain output. When the temperature of the driver exceeds TTHWN, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops TTHWN_HYS below TTHWN, the THWN pin goes high. If the driver temperature exceeds TTHDN, the part enters thermal shutdown and turns off both MOSFETs. Once the temperature falls TTHDN_HYS below TTHDN, the part resumes normal operation.

Positive Overcurrent Protection

POCP will discontinue the GH pulse commanded by PWM on a cycle-by-cycle basis.

For every cycle-by-cycle POCP, GH is first discontinued and then GL is commanded on despite PWM being in the high state. GL will stay on, ignoring further PWM = H pulses until the end of PWM = H cycle.

Additionally, during PWM = L/M, while GL is on, LSPOCP is monitored. If LSPOCP is detected, then the subsequent PWM = H will be skipped, and GL will then be on during the PWM = H skipped cycle. If HSPOCP is detected during PWM = H then the next PWM = H will not be skipped.

After an HSPOCP, if PWM remains high for > 8 μs, the PWM will be turned back on to check for HSPOCP again. POCP is enabled by VCC > UVLO, EN high true.

Negative Overcurrent Protection

The NCP303750 can detect large negative inductor current and protect the low side MOSFET.

Once this Negative current threshold is detected the driver module takes control and truncates LS on-time pulse (LS FET is gated off regardless of PWM command).

The driver will stay in this state till one of two things happen:

- 200 ns expires in which case if the PWM pin is commanding the driver to turn on LS, the driver will respond and NOCP will again be monitored
  - ♦ After the 200 ns timer expires, NOCP will be blanked for 230 ns before a new NOCP can be detected
- PWM commands HS on in which case the driver will immediately turn on HS regardless of the 200 ns Timer.

ZCD# High Behavior

The ZCD# input pin has an internal pull-up resistance to VCC. When driven high, the ZCD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function.

PWM	ZCD#	GH (not a pin)	GL
H	H or floating	ON	OFF
M	H or floating	OFF	OFF
L	H or floating	OFF	ON

This section describes operation with controllers that are capable of three PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The NCP303750 has an internal pull-up resistor that connects to VCC that sets ZCD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP303750 to turn off the LS FET.

When the controller detects zero current, it needs to set PWM to mid-state, which causes the NCP303750 to pull both GH and GL to their off states without delay (Figure 15).

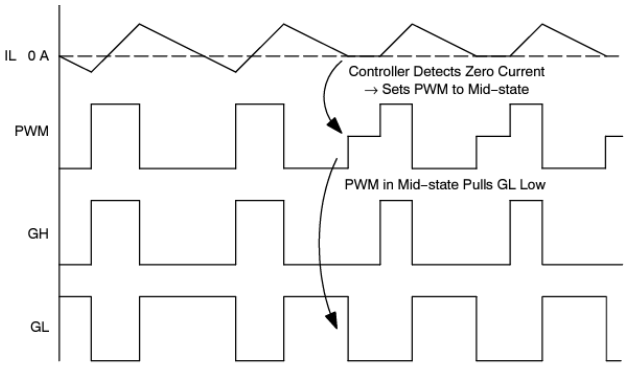


Figure 15. ZCD# High Timing Diagram

ZCD# Low Behavior

This section describes operation with controllers that are capable of three states in their PWM output and relies on the NCP303750 to conduct zero current detection during discontinuous conduction mode (DCM).

The ZCD# pin needs to be set low.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid-state.

Whenever PWM transitions to mid-state, GH turns off and GL turns on. GL stays on for the duration of the de-bounce timer and ZCD blanking timers. Once these timers expire, the NCP303750 monitors the SW voltage and turns GL off when SW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

PWM	ZCD#	GH (not a pin)	GL
H	L	ON	OFF
M	L	OFF	ZCD
L	L	OFF	ON

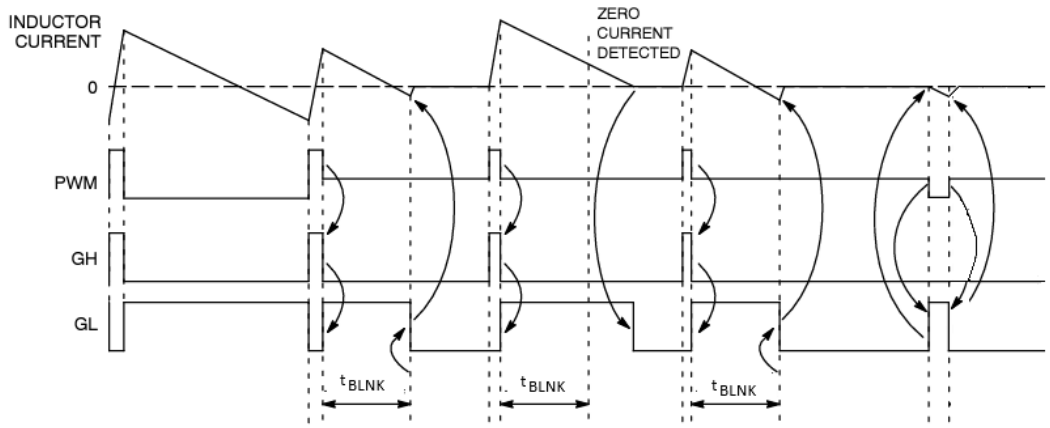


Figure 16. ZCD# Low Timing Diagram

APPLICATION INFORMATION

Power Supply Decoupling

The NCP303750 sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low-ESR capacitor should be placed near the power and ground pins. A multi-layer ceramic capacitor (MLCC) between 1 μF and 4.7 μF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 μF ceramic capacitor should be placed on this pin in close proximity to the NCP303750. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (1 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function (See Figure 1).

Decoupling Capacitor for VCCD and VCC

For the supply input (VCCD and VCC pin), local decoupling capacitors are required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68~2.2 μF / 0402~0603 / X5R~X7R multi-layer ceramic capacitors for the power rail. Keep these capacitors close to the VCCD and VCC pin and AGND copper planes. If either needs to be located on the bottom side of the board, put through-hole vias on each pad of the decoupling capacitor to connect the capacitor pad on bottom with the pins on top. Recommended value 4.7 μF.

The supply voltage range on VCCD and VCC is 4.5 V~5.5 V, typically 5 V for normal applications.

R-C Filter on VCC

The VCCD pin provides power to the gate drive of the high-side and low-side power MOSFETs. In most cases, VCCD can be connected directly to VCC, which is the pin that provides power to the analog and logic blocks of the driver. To avoid switching noise injection from VCCD into VCC, a filter resistor can be inserted between VCCD and VCC decoupling capacitors.

Recommended filter resistor value range is 0~10 Ω, typically 1 Ω for most applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}). A bootstrap capacitor of 0.1~0.22 μF / 0402~0603 / X5R~X7R is usually appropriate for most switching applications (recommended 100 nF). A series bootstrap resistor may be needed for specific applications to lower high-side MOSFET switching speed. The boot resistor is required when the DrMOS is switching above 15 V V_{IN}; when it is effective at controlling V_{SW} overshoot. R_{BOOT} value from 0.5 to 6 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high-side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

THWN Pull-up Resistor

The THWN pin is an open drain output. Recommended resistor value is 10 – 20 kΩ.

PCB LAYOUT GUIDELINES

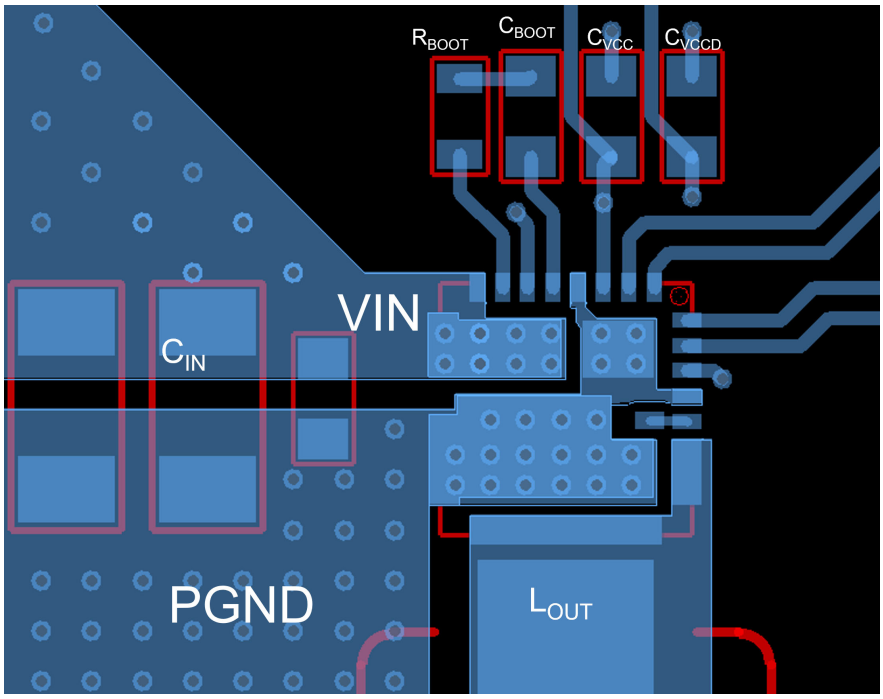


Figure 17. Top Copper Layer

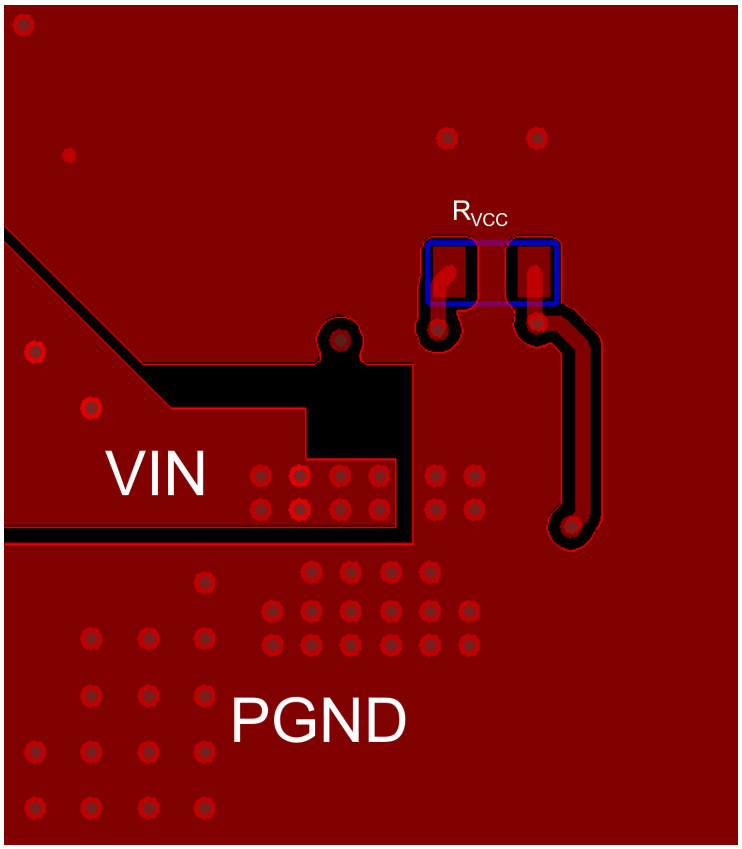


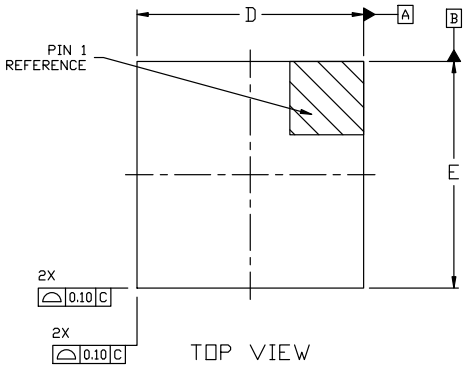
Figure 18. Bottom Copper Layer

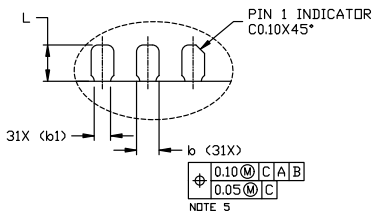
REVISION HISTORY

Revision	Description of Changes	Date
P6	Edit pin 2 description, changes to the EC table pages 4 and 5, changes to table 1 and notes, add rev history table	6/6/2025
P7	Add note to thermal resistance table, update one thermal resistance table, changes to text on page 2, 9, 10, 11.	6/24/2025

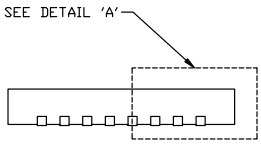
PACKAGE DIMENSIONS

PQFN31 5X5, 0.5P
CASE 483BR
ISSUE D

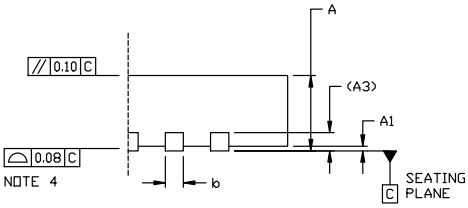




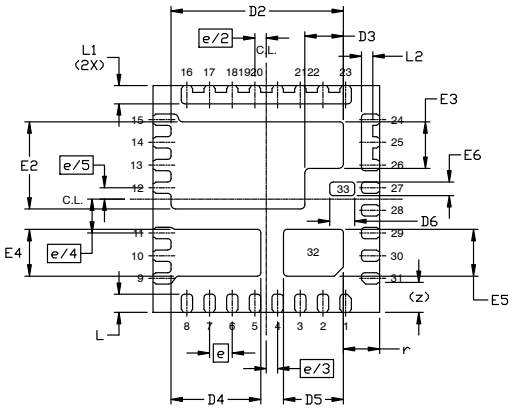
DETAIL 'B'
(SCALE 2:1)



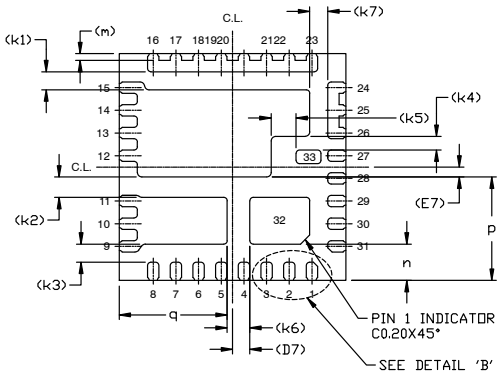
SIDE VIEW



DETAIL 'A'
(SCALE 2:1)



BOTTOM VIEW



SUPPLEMENTAL
BOTTOM VIEW

NOTES:

1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATES MAY/2005.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS
4. DIMENSIONS D2 NOT INCLUDE BURRS AND SMEAR OR MOLD FLASH.
   MOLD FLASH OR BURRS AND SMEAR DO NOT EXCEED 0.10MM.
5. DIMENSION b AND B1 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.13	0.18	0.30
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
D3	0.75	0.85	0.95
D4	1.88	1.98	2.08
D5	1.22	1.32	1.42
D6	0.45	0.55	0.65
D7	0.38 REF		
E	4.90	5.00	5.10
E2	1.82	1.92	2.02
E3	0.93	1.03	1.13
E4	0.93	1.03	1.13
E5	0.93	1.03	1.13
E6	0.20	0.30	0.40
E7	0.22 REF		
e	0.50 BSC		
e/2	0.25 BSC		
e/3	0.25 BSC		
e/4	0.75 BSC		
e/5	0.25 BSC		
k1	0.40 REF		
k2	0.45 REF		
k3	0.40 REF		
k4	0.30 REF		
k5	0.55 REF		
k6	0.50 REF		
k7	0.40 REF		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
m	0.15 REF		
n	0.80 REF		
p	2.28 REF		
q	2.38 REF		
r	0.80 REF		
z	0.625 REF		

PACKAGE DIMENSIONS

PQFN31 5X5, 0.5P
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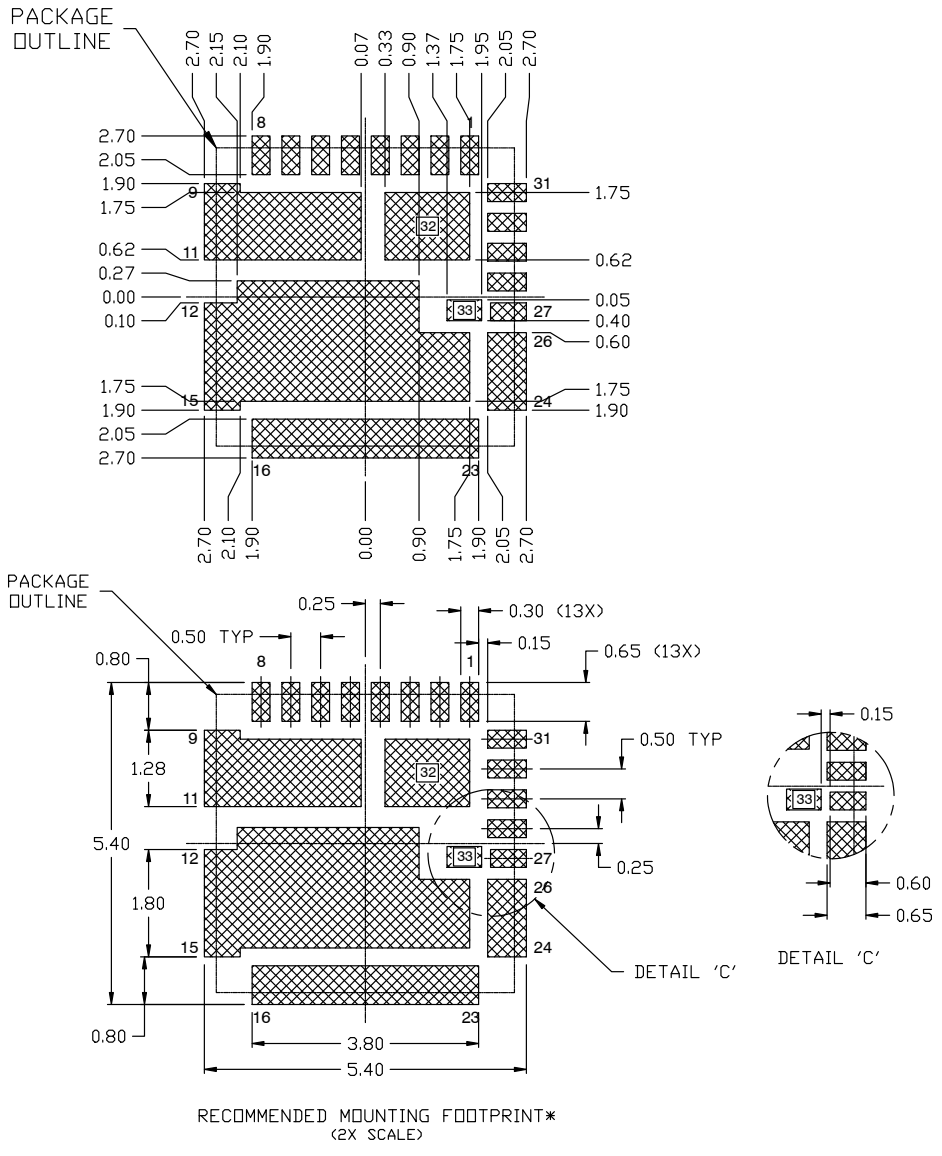
ISSUE D



* For additional information on our Pb-Free strategy and soldering details, please download the ONSEMI Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales