XR46050

Two-Step LED Current Controller

Description

The XR46050 is a two-step LED current controller for bulb application powered by an alternative current (AC) voltage source directly. It can drive an external N-channel power MOSFET to regulate the current flowing through a High Voltage (HV) LED string.

The XR46050 works as a constant current regulator to control two-step current levels for AC step driver with simplest structure. It also provides linear type Over Temperature Protection (OTP).

The PCB design can be very compact to meet various shape requirements. It is especially suitable for replacing A-series LED light bulbs and candelabra LED bulbs.

FEATURES

- Device
  - 6V to 76V chip supply voltage range
  - Over temperature protection
  - Single board LED lighting solution available
  - 2mm x 2mm TDFN-6 package
- System
  - All solid state components
  - No electrolytic capacitor required
  - Fewer component counts and simple solution for LED lighting
  - Scalable architecture allows optimization of performance vs. cost
  - Driver-on-board and chip-on-board design solution available which minimize process flow and assembly cost
  - High PF and Low THD performance
  - Flexible PCB layout options

APPLICATIONS

- A series LED bulbs
- Candelabra LED bulbs
- AC LED lighting engines

Typical Application

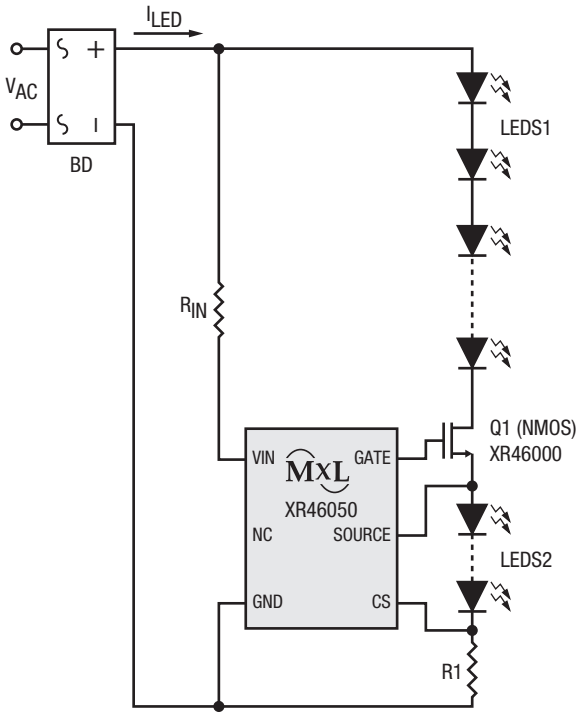


Figure 1. Typical Application

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Sustaining Voltage

- VIN, GATE, SOURCE to GND ..... -0.3V to 85V
- GATE to SOURCE ..... -0.3V to 7V
- SOURCE to CS ..... -0.3V to 70V
- CS to GND ..... -0.3V to 1V

VIN input current 3mA

SOURCE to CS current 180mA

Maximum operating junction temperature, T_J ..... 150°C

Operating temperature, T_{OPR} ..... -40°C to 85°C

Storage temperature range ..... -55°C to 150°C

Lead temperature (soldering, 10 seconds) ..... 260°C

Operating Conditions

Input Voltage, V_{IN} ..... 6V ~ 76V

Peak level current ..... 180 mA

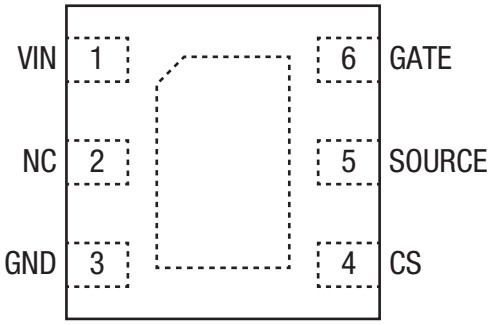
NOTES:
1. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
2. All parameters having min/max specifications are guaranteed. Typical values are for reference purpose only.
3. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN_{MIN}	Minimum VIN supply voltage		6			V
I_{IN}	VIN supply current	V_{IN} = 6V to 73V		0.3	0.5	mA
VIN_{CLAMP}	VIN over voltage clamp	When VIN > VIN_{CLAMP}, I_{IN} will increase to >1mA to clamp VIN at VIN_{CLAMP}	74	76	80	V
V_{CS}	CS voltage	VIN = 15V and 75V	310	323	336	mV
V_{REF1}/ V_{REF0}	Reference voltage ratio		85	90	95	%
V_{GATE}	GATE voltage	Gate to SOURCE		5.4		V
I_{SOURCE}	GATE source current(1)	V_{GATE} - V_{CS} = 3V		30		µA
I_{SINK}	GATE sink current(1)	V_{GATE} - V_{CS} = 3V		500		µA
T_{TP}	Thermal protection trip temperature	When T_J is higher than T_{TP}, V_{CS} decreases linearly	135	145		°C
$\Delta V_{CS}/\Delta T_J$	Thermal protection mode V_{CS} decreasing slope(1)	$T_J > T_{TP}$		-1.1		%/°C

NOTE:
1. Guarantee by design, not by production test.

Pin Configuration



2mm x 2mm TDFN-6

Pin Functions

Pin Number	Pin Name	Description
1	VIN	Power supply pin.
2	NC	No connection.
3	GND	Ground pin.
4	CS	Current sense pin. Connect a sense resistor, R_{CS}, between this pin and the GND pin. The peak current is set by $I_{OUT} = V_{CS}/R_{CS}$.
5	SOURCE	External HV NMOS SOURCE pin. The V_F of the LED segment connected between the source pin and the CS pin should not be higher than 70V.
6	GATE	External HV NMOS gate driving pin. Limited to 5.5V maximum.
Exposed thermal pad (EP)		Exposed thermal pad of the chip. Use this pad to enhance the power dissipation capability. The thermal conductivity will be improved if a copper foil on PCB is soldered with the thermal pad. It is recommended to connect the exposed thermal pad to the GND pin.

Functional Block Diagram

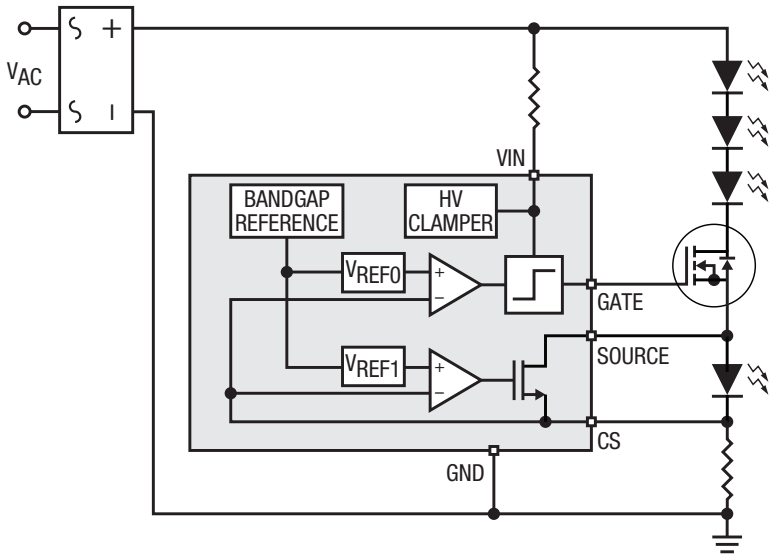


Figure 2. Functional Block Diagram

Applications Information

Typical Application

For a typical two-step driving scheme with one XR46050, the electrical performance is good enough to meet most of the requirement: the Power Factor (PF) is higher than 0.92 and the Total Harmonic Distortion (THD) is around 30%. If higher PF or lower THD is required, one more XR46083 or XR46084 can be added to make the lighting system becoming a three-step driving scheme, as shown in below. The three-step system can provide better electrical performance of PF > 0.96 and THD = ~ 20%.

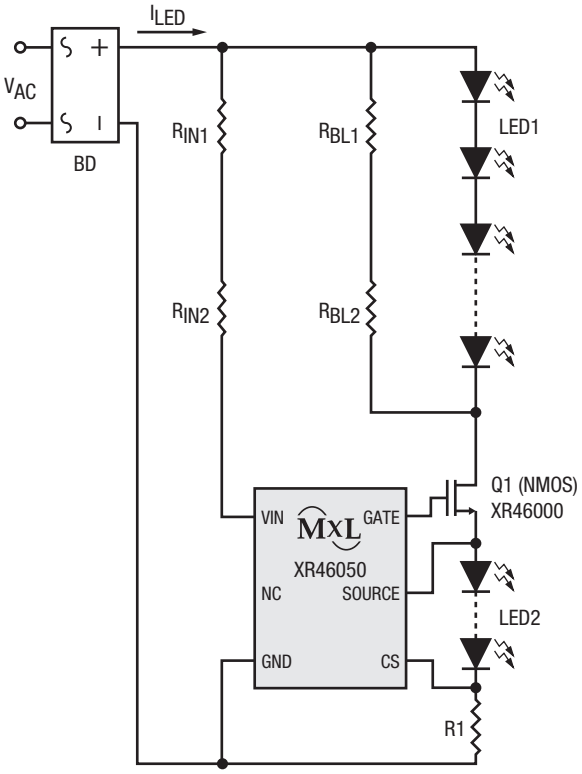


Figure 3. 2-Step (PF > 0.92, THD = ~ 30%)

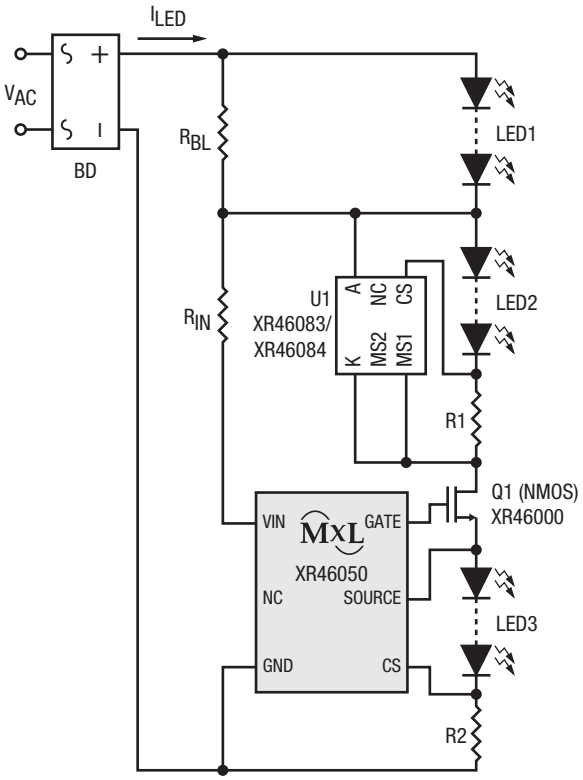


Figure 4. 3-Step (PF > 0.96, THD = ~ 20%)

Applications Information (Continued)

Linear Type Thermal Protection

When the junction temperature T_J rises up to the Thermal Protection Trip temperature T_{TP} (145°C in typical), the current sense voltage V_{CS} starts to decrease linearly at a slope of -1.1%/°C. The LED driving current decreases accordingly. The system can still work normally under the thermal protection mode with lower driving current. The power dissipation on the XR46050 chip becomes lower so the T_J will stop increasing when thermal balance is reached.

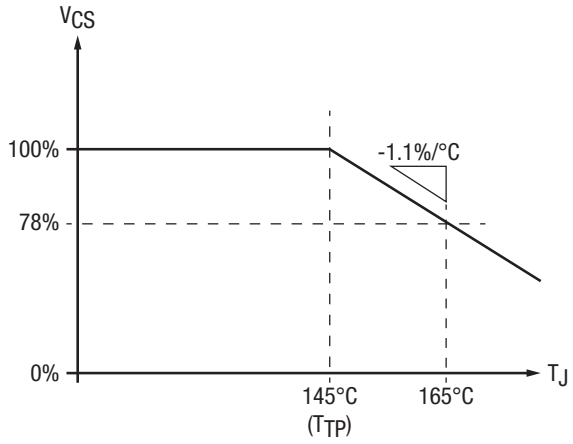


Figure 5. V_{CS} vs. T_J

Layout Suggestion

The exposed thermal pad under the chip is used to enhance the power dissipation capability. The thermal conductivity will be improved if a copper foil on PCB soldered with the thermal pad can be as large as possible. It is strongly recommended to connect the GND pin to the exposed thermal pad.

The external HV NMOS is recommended to be placed close to the chip. The pull-high resistor for the V_{IN} pin should be placed close to the chip too. The current sense resistor connected between the CS pin and GND pin should be placed as close as to the CS pin and GND pin, as the example in below.

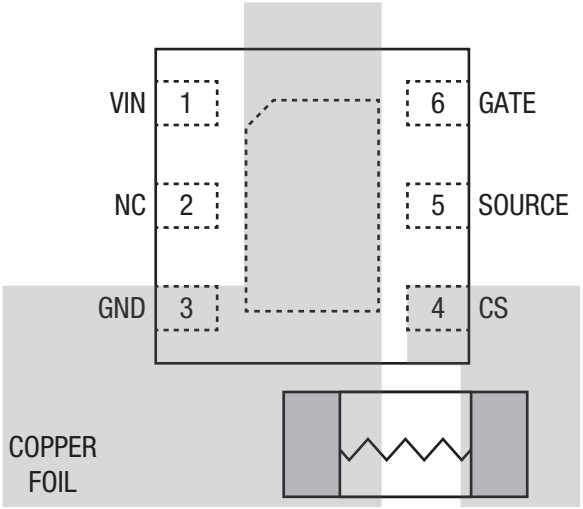
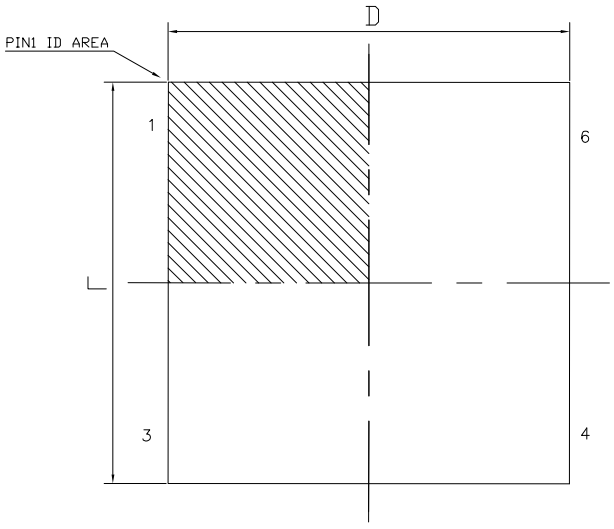
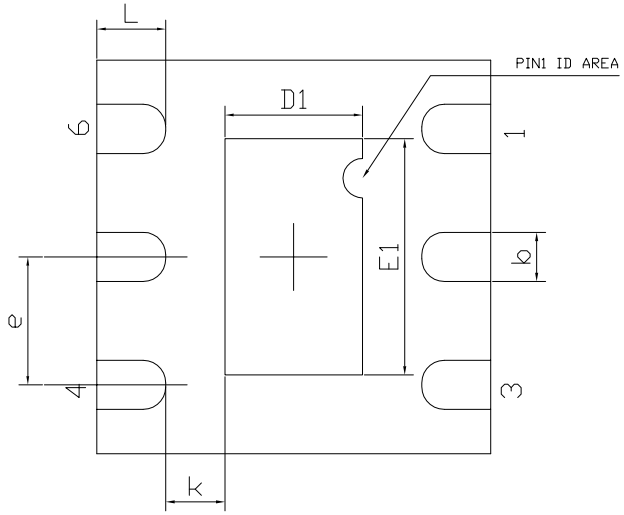


Figure 6. Foil

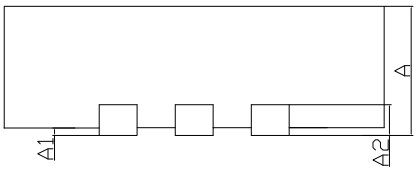
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	–	0.050
A2		0.203Ref	
b	0.200	0.250	0.300
D		2.00 BSC	
E		2.00 BSC	
e		0.650 BSC	
D1	0.600	0.700	0.800
E1	1.100	1.200	1.300
L	0.274	0.350	0.426
K	0.200	–	–
N		6	

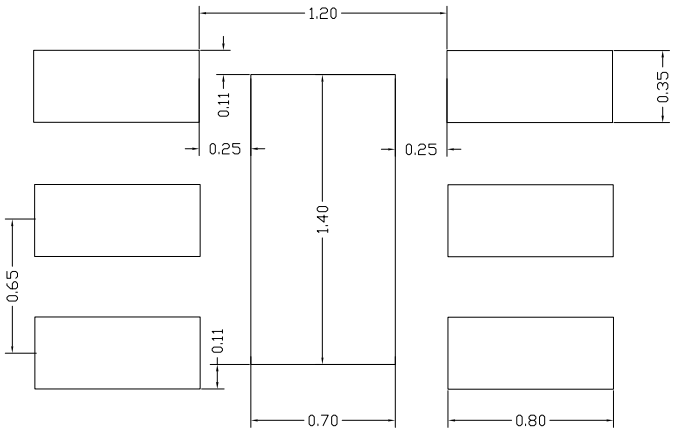
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-229.

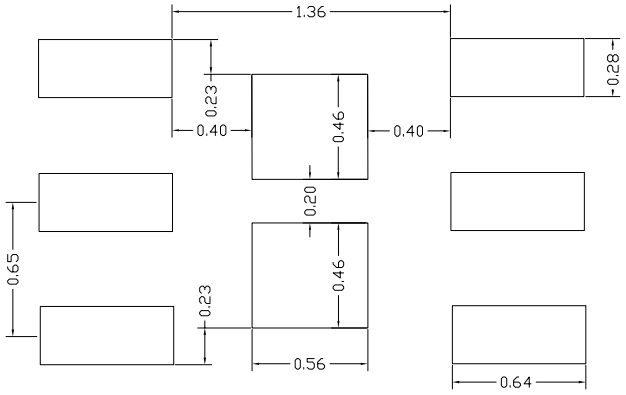
Drawing No.: POD-00000072

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000072

Revision: B

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR46050IHBTR	-40°C to 85°C	Yes[2]	TDFN6 2x2	Tape and reel

NOTE:
1. Refer to www.exar.com/XR46050 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1.0	Aug 2015	Initial release.
1A	Oct 2016	New datasheet format, update Typical Application and update Package Description.
1B	May 2018	Update to MaxLinear logo. Update format. Change Package Description to Mechanical Dimensions.

MAXLINEAR

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

High Performance Analog:
1060 Rincon Circle
San Jose, CA 95131
Tel.: +1 (669) 265-6100
Fax: +1 (669) 265-6101
www.exar.com