±15kV ESD Protected, +3.3V, 1Microamp, 250kbps, RS-232 Transmitters/Receivers

The Intersil 5962-062070xQxA devices are 3.3V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and MIL-STD 883 Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications include ruggedized portable products and remotely deployed devices exposed to extreme temperature and humidity where the low operational and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions (except for the 5962-0620703Q2A), reduce the standby supply current to a 1µA trickle. Small footprint packaging and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V-only systems.

Specifications for QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-06207. A "hot-link" is provided on our website for downloading.

Ordering Information

DESC P/N	CONFIGURATION	TEMP (°C)	PACKAGE
5962-0620701Q3A	ICL3243E 3D/5R	-55 to +125	28 Ld CLCC
5962-0620702Q3A	ICL3238E 5D/3R	-55 to +125	28 Ld CLCC
5962-0620703Q2A	ICL3232E 2D/2R	-55 to +125	20 Ld CLCC
5962-0620704Q2A	ICL3221E 1D/1R	-55 to +125	20 Ld CLCC

Features

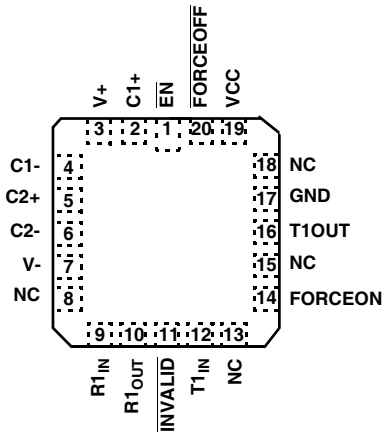
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Electrically Screened to DLA SMD#5962-06207
- QML Qualified per MIL-PRF-38535 Requirements
- SMD Compliance
- Military Temperature Range
- Latch-up Free
- Hermetic Package
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Guaranteed Mouse Driveability (ICL3243E)
- Requires Single +3.3V ±10% Power Supply
- RS-232 Compatible with V_{CC} = 2.7V
- Receiver Hysteresis for Improved Noise Immunity
- Low Power Automatic Power-down Modes (except for ICL3232E) 1µA
- Guaranteed Minimum 250kbps Data Rate
- Manual and Automatic Power-down Features
- Multiple Drivers/Receivers
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Regulated Dual Charge Pumps

Applications

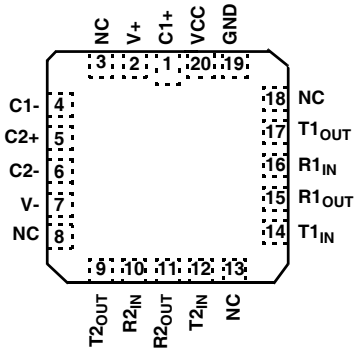
- Any Military or High-Rel System Requiring RS-232 Communication Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - Ruggedized Handheld GPS, Laptop Computers, Notebooks, Palmtops
  - Industrial Control/Shop Floor Communications
  - Field Deployed Sensors/Devices Exposed to Extreme Temperature/Humidity
  - Ruggedized Cellular/Mobile Phones

Pinouts

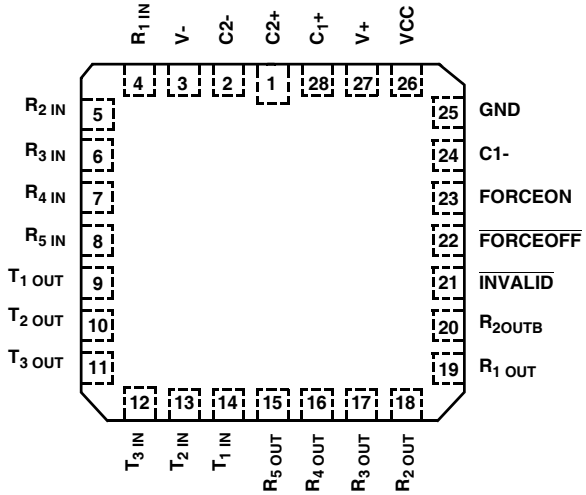
ICL3221E (CLCC)
TOP VIEW



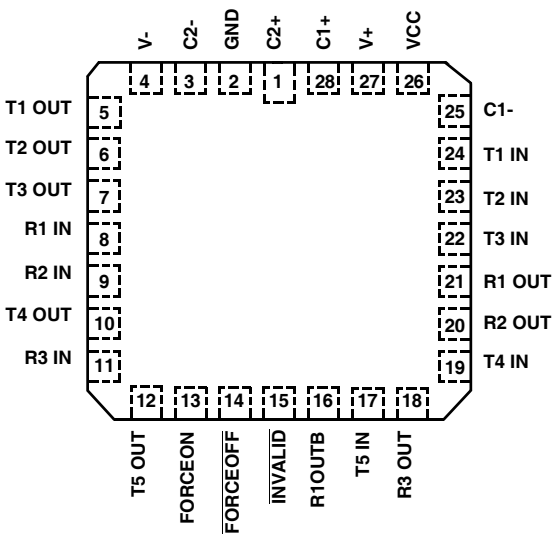
ICL3232E (CLCC)
TOP VIEW



ICL3243E (CLCC)
TOP VIEW



ICL3238E (CLCC)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V_{CC}	System power supply input (3.0V to 3.6V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs. (Note 1)
T_{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs.
R_{OUTB}	TTL/CMOS level, noninverting, always enabled receiver outputs.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
$\overline{\text{EN}}$	Active low receiver enable control; doesn't disable R_{OUTB} outputs.
$\overline{\text{FORCEOFF}}$	Active low control to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (See Tables 1 & 2, Note 1).
FORCEON	Active high input to override automatic powerdown circuitry thereby keeping transmitters active. ($\overline{\text{FORCEOFF}}$ must be high, Note 1).

NOTE:

1. The ICL3238E input pins incorporate positive feedback resistors. Once the input is driven to a valid logic level, the feedback resistor maintains that logic level until V_{CC} is removed. Unused transmitter inputs may be left unconnected by the user.

TABLE 1. POWER-DOWN LOGIC TRUTH TABLE

RCVR OR XMTR EDGE WITHIN 30 SEC?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUT	RS-232 LEVEL PRESENT AT RECEIVER INPUT?	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ICL3238E								
No	H	H	Active	Active	Active	No	L	Normal Operation (Enhanced Auto Power-down Disabled)
No	H	H	Active	Active	Active	Yes	H	
Yes	H	L	Active	Active	Active	No	L	Normal Operation (Enhanced Auto Power-down Enabled)
Yes	H	L	Active	Active	Active	Yes	H	
No	H	L	High-Z	Active	Active	No	L	Power-down Due to Enhanced Auto Power-down Logic
No	H	L	High-Z	Active	Active	Yes	H	
X	L	X	High-Z	High-Z	Active	No	L	Manual Power-down
X	L	X	High-Z	High-Z	Active	Yes	H	

TABLE 1. POWER-DOWN LOGIC TRUTH TABLE (Continued)

RCVR OR XMTR EDGE WITHIN 30 SEC?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUT	RS-232 LEVEL PRESENT AT RECEIVER INPUT?	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
$\overline{\text{INVALID}}$ DRIVING FORCEON AND $\overline{\text{FORCEOFF}}$ (EMULATES AUTOMATIC POWER-DOWN)								
X	Note 2	Note 2	Active	Active	Active	Yes	H	Normal Operation
X	Note 2	Note 2	High-Z	High-Z	Active	No	L	Forced Auto Power-down

NOTE:

2. Input is connected to $\overline{\text{INVALID}}$ Output.

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	$\overline{\text{EN}}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	(NOTE 3) R_{OUTB} OUTPUTS	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ICL3221E								
No	H	H	L	Active	Active	N.A.	L	Normal Operation (Auto Power-down Disabled)
No	H	H	H	Active	High-Z	N.A.	L	
Yes	H	L	L	Active	Active	N.A.	H	Normal Operation (Auto Power-down Enabled)
Yes	H	L	H	Active	High-Z	N.A.	H	
No	H	L	L	High-Z	Active	N.A.	L	Power-down Due to Auto Power-down Logic
No	H	L	H	High-Z	High-Z	N.A.	L	
Yes	L	X	L	High-Z	Active	N.A.	H	Manual Power-down
Yes	L	X	H	High-Z	High-Z	N.A.	H	Manual Power-down w/Rcvr. Disabled
No	L	X	L	High-Z	Active	N.A.	L	Manual Power-down
No	L	X	H	High-Z	High-Z	N.A.	L	Manual Power-down w/Rcvr. Disabled
ICL3243E								
No	H	H	N.A.	Active	Active	Active	L	Normal Operation (Auto Power-down Disabled)
Yes	H	L	N.A.	Active	Active	Active	H	Normal Operation (Auto Power-down Enabled)
No	H	L	N.A.	High-Z	Active	Active	L	Power-down Due to Auto Power-down Logic
Yes	L	X	N.A.	High-Z	High-Z	Active	H	Manual Power-down
No	L	X	N.A.	High-Z	High-Z	Active	L	Manual Power-down

NOTE:

3. Applies only to the ICL3243E.

Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground. . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$ . . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating (Receiver Input and Transmitter Output Pins) . . .±15kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
20 Ld CLCC Package	90
28 Ld CLCC Package	70

Maximum Junction Temperature (Ceramic Package) . . . . 150°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
ICL32XXE . . . . . .-55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

ICL3221E, ICL3232E, ICL3243E Test Conditions: V_{CC} = 3V to 3.6V, C1 - C4 = 0.1mF; Unless Otherwise Specified. Typicals are at T_A = 25°C, V_{CC} = 3.3V

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Current, Automatic Power-down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC} (ICL3221E, ICL3243E Only)		Full	-	1	10	µA
Supply Current, Power-down	$\overline{FORCEOFF}$ = GND (Except ICL3232E)		Full	-	1	10	µA
Supply Current, Power-up	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = V_{CC}	V_{CC} = 3.15V, ICL3221E/ICL3232E	Full	-	0.3	1.8	mA
		V_{CC} = 3.0V, ICL3243E	Full	-	0.3	1.8	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$		Full	2.0	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$		Full	-	±0.01	±10	µA
Output Leakage Current (Except ICL3232E)	$\overline{FORCEOFF}$ = GND or $\overline{EN}$ = V_{CC}		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} -0.6	V_{CC} -0.1	-	V
AUTOMATIC POWER-DOWN (ICL3221E, ICL3243E Only, FORCEON = GND, FORCEOFF = V_{CC})							
Receiver Input Thresholds to Enable Transmitters	Powers Up		Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	Powers Down		Full	-0.3	-	0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC}-0.6	-	-	V
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low			Full	0.6	1.2	-	V
Input Threshold High			Full	-	1.5	2.4	V
Input Resistance			Full	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kW to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω

Electrical Specifications **ICL3221E, ICL3232E, ICL3243E** Test Conditions: V_{CC} = 3V to 3.6V, C1 - C4 = 0.1mF; Unless Otherwise Specified. Typicals are at T_A = 25°C, V_{CC} = 3.3V **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 3.6V (ICL3232E,V_{CC} = 0 only) Automatic Power-down or $\overline{FORCEOFF}$ = GND		Full	-	-	±25	µA
MOUSE DRIVEABILITY (ICL3243 Only)							
Transmitter Output Voltage	$T1_{IN}$ = $T2_{IN}$ = GND, $T3_{IN}$ = V_{CC}, $T3_{OUT}$ Loaded with 3kW to GND, $T1_{OUT}$ and $T2_{OUT}$ Loaded with 2.5mA Each		Full	±5	-	-	V
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kW, C_L = 1000pF, One Transmitter Switching		Full	250	500	-	kbps
Transmitter Skew	t_{PHL} - t_{PLH}		Full	-	200	1000	ns
Receiver Skew	t_{PHL} - t_{PLH}		Full	-	100	1000	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kW to 7kW, Measured From 3V to -3V or -3V to 3V	C_L = 200pF to 2500pF	Full	4	8.0	30	V/µs
		C_L = 200pF to 1000pF	Full	6	-	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model (MIL-STD 883 Method 3015)		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
All Other Pins	Human Body Model (MIL-STD 883 Method 3015)		25	-	±2	-	kV

Electrical Specifications **ICL3238E** Test Conditions: V_{CC} = 3V to 3.6V, C1 - C4 = 0.1µF, Unless Otherwise Specified. Typicals are at T_A = 25°C, V_{CC} = 3.3V

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current, Automatic Power-down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	Full	-	1	10	µA
Supply Current, Power-down	$\overline{FORCEOFF}$ = GND	Full	-	1	10	µA
Supply Current, Power-up	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = V_{CC}	Full	-	0.3	1.8	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$ Wake up Threshold	Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$ Wake up Threshold	Full	2.0	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, V_{IN} = 0V or V_{CC} (Note 4)	Full	-	±0.01	±10	µA
Output Leakage Current	$\overline{FORCEOFF}$ = GND	Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.0mA	Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA	Full	V_{CC} -0.6	V_{CC} -0.1	-	V
RECEIVER INPUTS						
Input Voltage Range		Full	-25	-	25	V
Input Threshold Low		Full	0.8	1.5	-	V
Input Threshold High		Full	-	1.8	2.4	V
Input Resistance		Full	3	5	7	kΩ

Electrical Specifications **ICL3238E** Test Conditions: V_{CC} = 3V to 3.6V, C1 - C4 = 0.1µF, Unless Otherwise Specified. Typicals are at T_A = 25°C, V_{CC} = 3.3V **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
ENHANCED AUTOMATIC POWER-DOWN (FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC})							
Receiver Input Thresholds to $\overline{\text{INVALID}}$ High	Powered Up		Full	-2.7	-	2.7	V
Receiver Input Thresholds to $\overline{\text{INVALID}}$ Low	Powered Down		Full	-0.3	-	0.3	V
$\overline{\text{INVALID}}$ Output Voltage Low	I_{OUT} = 1.0mA		Full	-	-	0.4	V
$\overline{\text{INVALID}}$ Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC}-0.6	-	-	V
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 3.6V, Automatic Power-down or $\overline{\text{FORCEOFF}}$ = GND		Full	-	-	±25	µA
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	250	500	-	kbps
Transmitter Skew	t_{PHL} - t_{PLH}		Full	-	200	1000	ns
Receiver Skew	t_{PHL} - t_{PLH}		Full	-	100	1000	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V	C_L = 150pF to 1000pF	Full	6	15	30	V/µs
		C_L = 150pF to 2500pF	Full	4	12	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
	Human Body Model (MIL-STD 883 Method 3015)		25	-	±15	-	kV
All Other Pins	Human Body Model (MIL-STD 883 Method 3015)		25	-	±2.5	-	kV

NOTE:

4. These inputs utilize a positive feedback resistor. The input current is negligible when the input is at either supply rail.

Die Characteristics

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)

Thickness: 13.0kÅ ± 1.0kÅ

Top Metallization:

Type: AlSiCu

Thickness: 10.0kÅ ± 1kÅ

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

GND

ADDITIONAL INFORMATION:

Worst Case Current Density:

$<2.0 \times 10^5$ A/cm^2

Transistor Count:

ICL3221E: 286

ICL3232E: 296

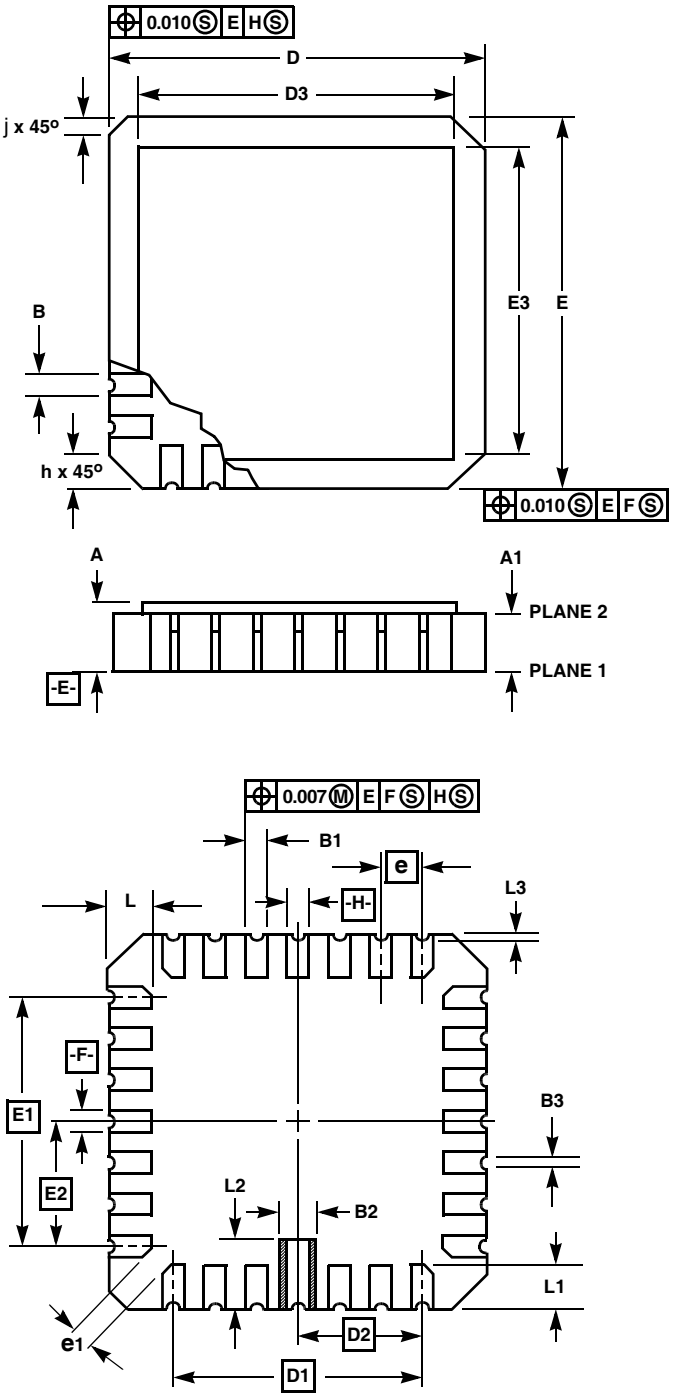
ICL3243E: 464

ICL3238E: 1235

Process:

Si Gate CMOS

Ceramic Leadless Chip Carrier Packages (CLCC)



J28.A MIL-STD-1835 CQCC1-N28 (C-4)
28 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

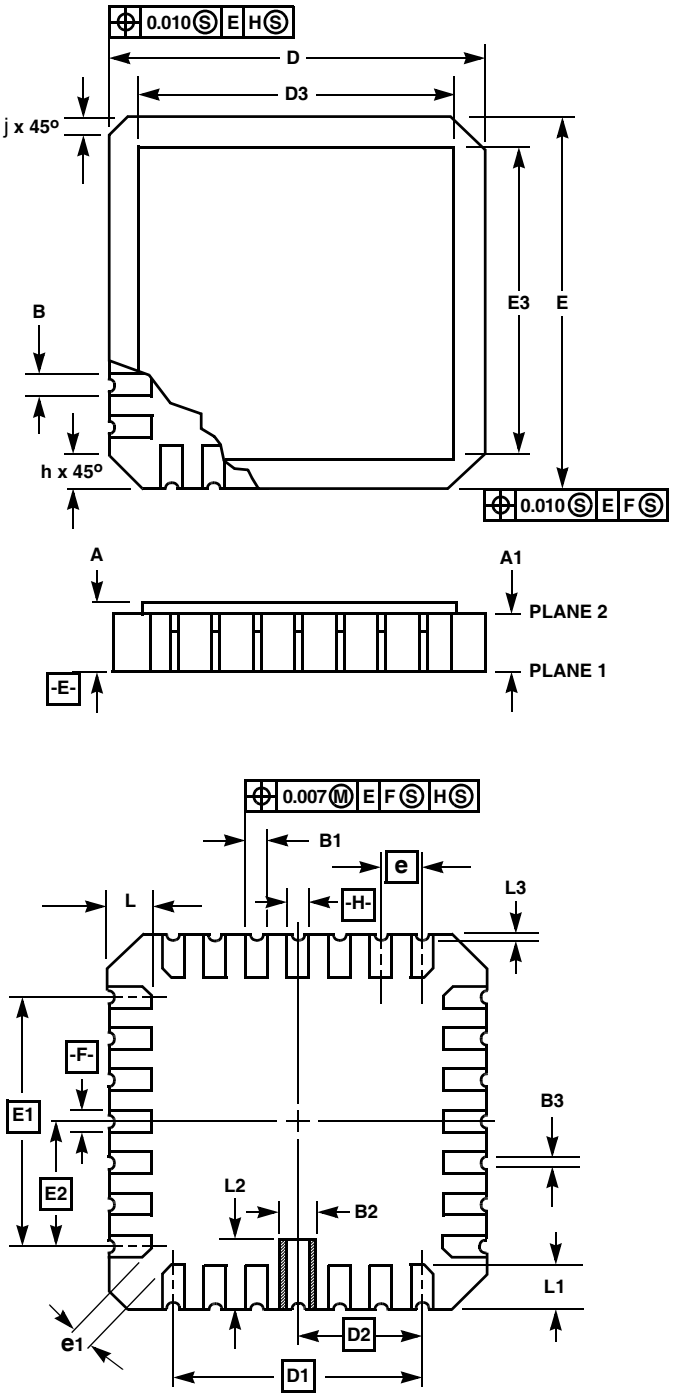
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.442	0.460	11.23	11.68	-
D1	0.300 BSC		7.62 BSC		-
D2	0.150 BSC		3.81 BSC		-
D3	-	0.460	-	11.68	2
E	0.442	0.460	11.23	11.68	-
E1	0.300 BSC		7.62 BSC		-
E2	0.150 BSC		3.81 BSC		-
E3	-	0.460	-	11.68	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.038	-
ND	7		7		3
NE	7		7		3
N	28		28		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

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NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.