iND83405, Product Brief

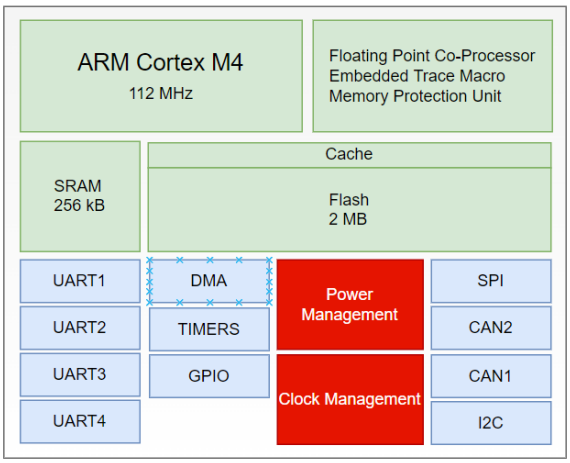
Product Brief 2530

IND83405 Features

- 32-bit ARM Cortex-M4F CPU
- Hardware Floating Point
- 112 MHz
- 256 kB embedded SRAM
- 2 MB embedded Flash
- 16 kB instruction Cache
- Four UART
- One SPI
- One I2C
- Two CAN CANbus 2.0b
- Sixteen DMA channels
- SDK provided
- Wide operating range
- T_{Jmax}=125 °C
- Single 5V supply
- SWD debugging interface
- 72-pin QFN package 10x10

Features (cont.)

- Thirteen (13) 5V IOs with 20mA sink current
- Thirty-one (31) 3.3V IOs
- Watchdog Timer (WDT)
- POR and BOR
- 8-bit SAR ADC, 80ksps, 16-channels, programable high/low voltage references.
- Tape and Reel available



Applications

- Industrial Controls
- Sensors
- Motor Controller
- Heavy Duty Equipment

General Description

iND83405 is a high-reliability general-purpose microcontroller with floating point co-processor in the OnBrD family based on ARM Cortex M4 CPU running up to 112MHz with a generous 2MB of embedded Flash memory and 256kB of SRAM. Thirty-one low-voltage 3.3V GPIO can be controlled with software or hardware in alternate peripheral modes: UART, SPI, I2C or CAN controllers. Thirteen additional robust 5V tolerant IOs with strong low-side drive are suitable for high noise environments. ECC protection on the internal flash memory ensures reliable operation, and a 16kB instruction cache allows full-speed operation up the maximum CPU frequency. IND83405 is available in 72-pin QFN package 10mm x 10mm.

About ındie Semiconductor

ındie is empowering the Autotech revolution with next generation automotive semiconductors and software platforms. We focus on EDGE sensors for Advanced Driver Assistance Systems including LiDAR, connected car, user experience and electrification applications. These technologies represent the core underpinnings of both electric and autonomous vehicles, while the advanced user interfaces transform the in-cabin experience to mirror and seamlessly connect to the mobile platforms we rely on every day. We are an approved vendor to Tier 1 partners and our solutions can be found in marquee automotive OEMs around the world. Headquartered in Aliso Viejo, CA, ındie has design centers and sales offices in Detroit, MI, Austin, TX, Boston, MA, Edinburgh, UK, Dresden, Germany and Wuxi, China.

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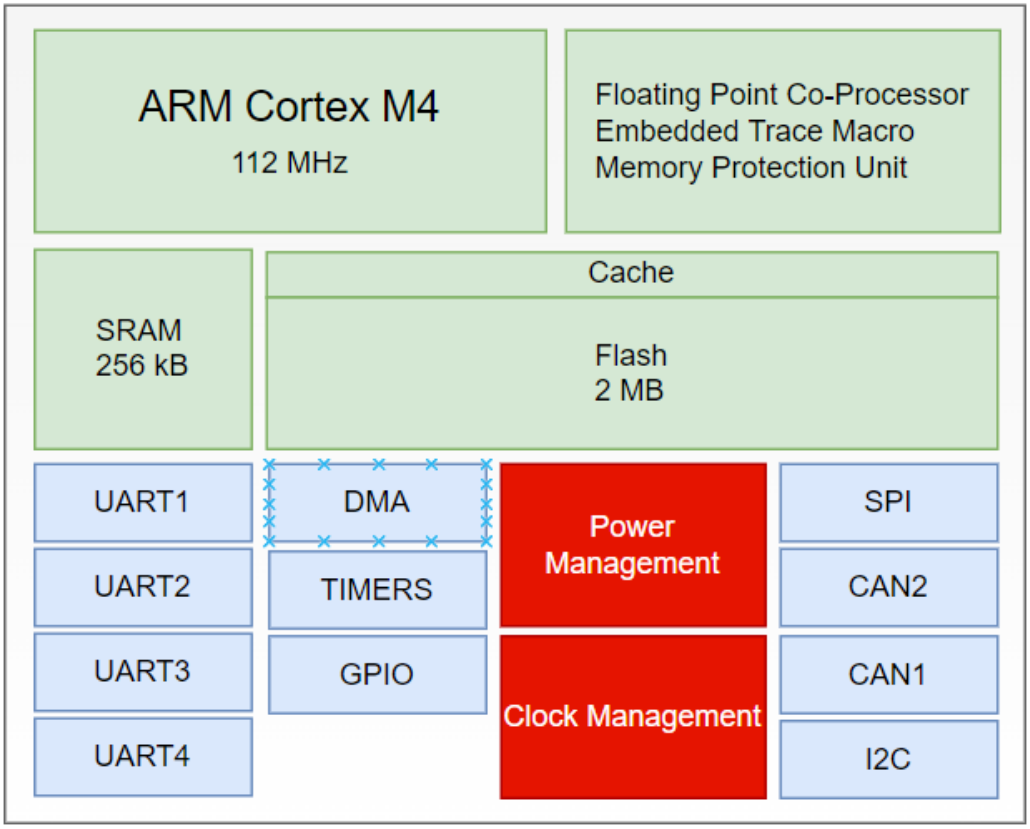
Functional Overview



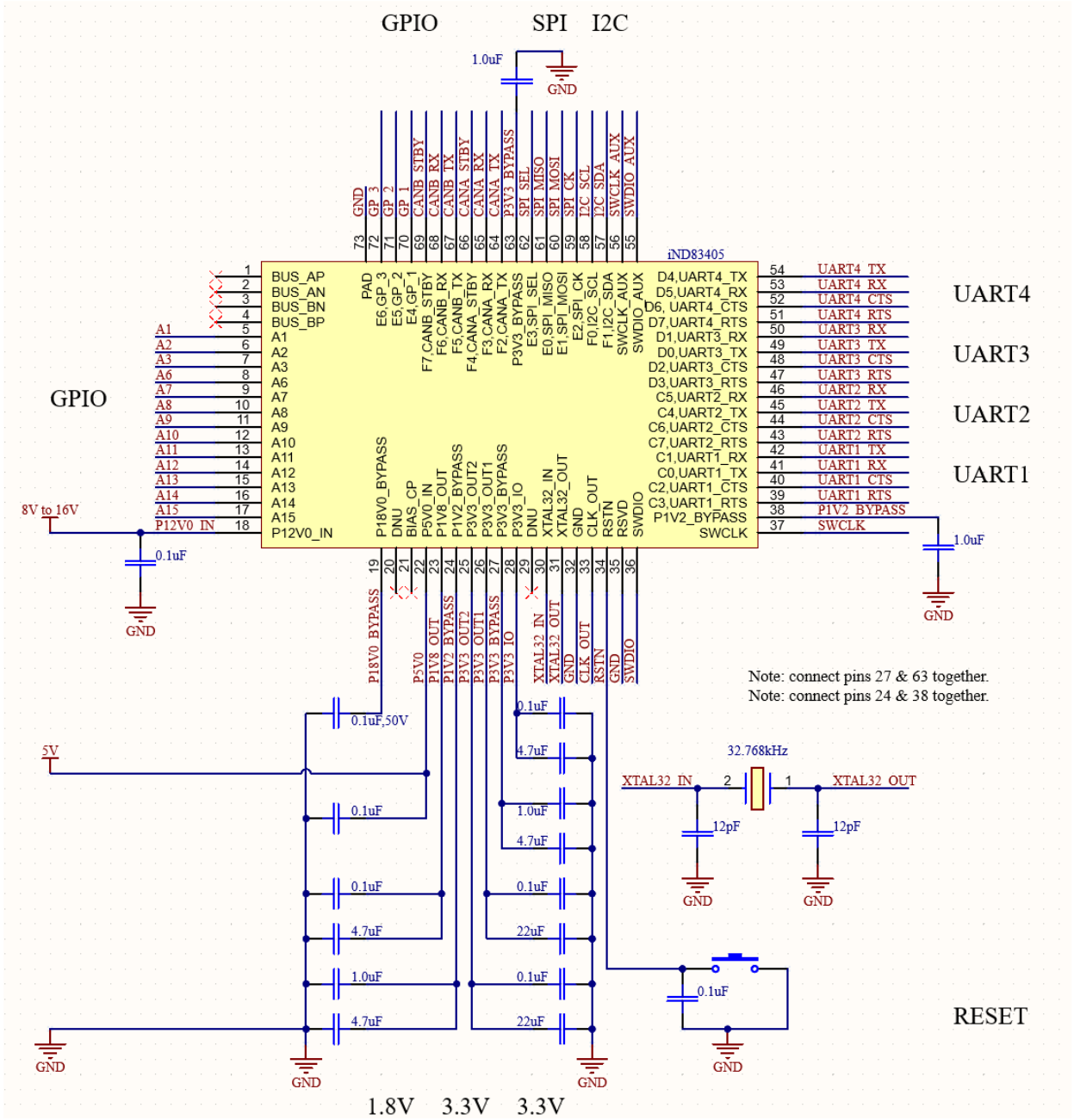
Functional Block	Description
CPU	ARM Cortex M4 112 MHz maximum speed
FPU	32-bit Floating Point Co-processor
Embedded Trace Macro Memory Protection Unit	Additional Cortex M4 Co-Processors
Non-Volatile Flash Memory	2 Megabytes of flash memory with hardware error correction (single-bit correction, two-bit detection) 40MHz maximum speed Flash organization is 2 Banks x 2 sectors x 512 pages x 8 bytes

	Banks can be operated independently. Read size is one page. Write size is one page. Supported erase sizes are one sector or one bank.
Instruction Cache	16 kilobyte SRAM-based multi-way associative cache memory for faster flash memory access
RAM Memory	256 kB zero wait-state SRAM for data and/or executable text.
TMR0	32-bit or dual-16-bit timer with optional auto-reload and interrupt
TMR1	32-bit or dual-16-bit timer with optional auto-reload and interrupt
TMR2	32-bit or dual-16-bit timer with optional auto-reload and interrupt
PLL	Fixed-frequency 32-kHz-to-28 MHz PLL
DLL	DLL clock multiplier with 1×, 2×, 3× or 4× modes The DLL provides a multiple of the system clock to the CPU, FPU RAM memory, DMA engine and Flash memory.
Crystal Oscillator	Fixed-frequency oscillator for use with external 32.768 kHz crystal
RC Oscillator	Fixed-frequency internal 11 MHz (nominal) RC oscillator
ADC	8-bit Analog-to-Digital Converter with input multiplexer
DMA Controller	16-channel DMA (Direct-memory-access) engine based on ARM PL080. Scatter-gather operation supported. Independent system bus access allows DMA to operating concurrently with CPU at full speed
GPIO Controller	A GPIO (general-purpose IO) controller with four separate interrupt channels available on all 3.3V IOs, edge detection, select-able pull-ups and pull-downs, and power management for floating inputs.
Clock Network	Configurable Clock rates for CPU and Peripherals
PMU	Power Management Unit allows granular power control for unused portions of the system. Configurable power monitors can trigger interrupts, reset the system and/or capture status flags for forensics. WIC allows use of low-power CPU modes.

Internal LDO	Internal voltage regulators power all digital/core rails and 3.3V GPIO pins from a single external 5V input. (If Ax pins are used, P12V0_IN must be supplied with 8V to 16V.)
System LDO	Two 3.3V and one 1.8V LDO are externally available for use by the system.
CAN1	CAN 2.0b controller with a large RX/TX priority frame buffers and 16 filter slots. CAN-FD mixed network tolerant.
CAN2	CAN 2.0b controller with a large RX/TX priority frame buffers and 16 filter slots. CAN-FD mixed network tolerant.
CANRXCNTR	Activity counter for CAN1_RX and CAN2_RX pins
Clock Monitor	Hardware clock fault detector
RTC	A 48-bit timer with input fixed to the 32kHz oscillator
SPIM	SPI Master with hardware FIFO and DMA capability
I2C_DMA	I2C Master with hardware FIFO and DMA capability
I2C_ARGON	Deprecated. Do not use
UART1	A UART (universal asynchronous Receive/Transmit) controller with DMA capability. Optional hardware flow control.
UART2	A UART (universal asynchronous Receive/Transmit) controller with DMA capability. Optional hardware flow control.
UART3	A UART (universal asynchronous Receive/Transmit) controller with DMA capability. Optional hardware flow control.
UART4	A UART (universal asynchronous Receive/Transmit) controller with DMA capability. Optional hardware flow control.
WDT	An internal watchdog timer with configurable timeout, warning interrupt and reset behavior

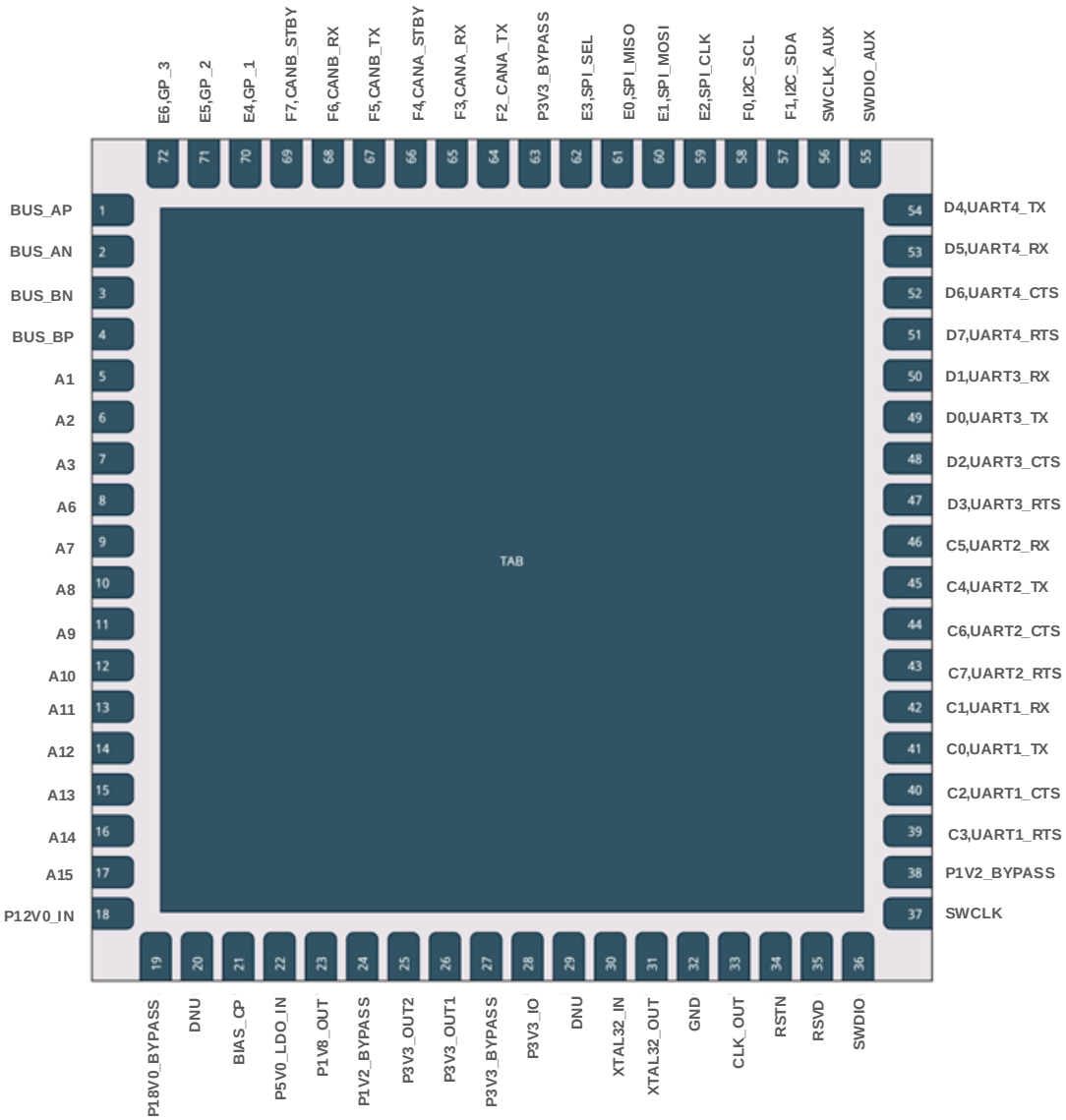
Table 2

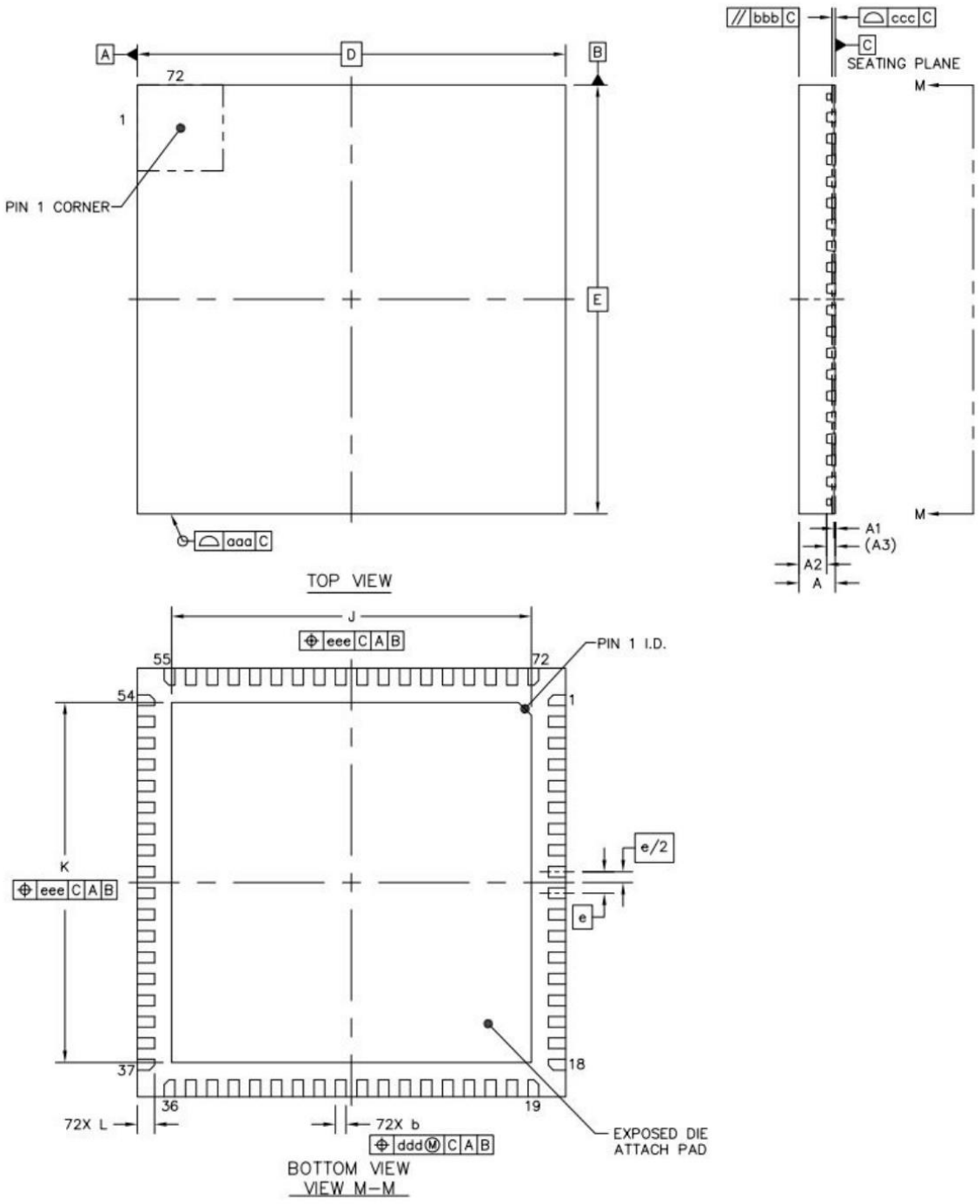
Minimal Application Circuit



Pinout and Packaging

iND83405 is available in trays of 72-Pin QFN ceramic lead frame package.
QFN72 10mm × 10mm, 0.5mm pitch, 72-pins with thermal pad. View from Top




A
D
B
72
1
PIN 1 CORNER
E
aaa C
TOP VIEW
bbb C
ccc C
C
SEATING PLANE
M
M
A1
(A3)
A2
A
J
eee C A B
55
72
PIN 1 I.D.
54
1
K
eee C A B
e/2
e
37
18
36
19
72X L
72X b
ddd M C A B
EXPOSED DIE
ATTACH PAD
BOTTOM VIEW
VIEW M–M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	8.3	8.4	8.5
	Y	K	8.3	8.4	8.5
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Detailed Pin Description

Name	Port	Pin	Dir	Description
BUS_AP BUS_AN BUS_BP BUS_BN		1 2 4 3	-	Do not use. Leave disconnected.
A1 A2 A3 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15		5 6 7 8 9 10 11 12 13 14 15 16 17	IO	5V tolerant Drive Low or Tri-state Input threshold: ~2.5V Analog input capable
P12V0_IN		18	-	If pins A1-A15 are not used, connect this pin to P5V0_IN If A1-A15 are used, then this pin must be supplied between 8V and 16V to meet pin functional specifications.
P5V0_IN		22	-	Main power input. This pin supplies power to all regulators Apply 5V (between 4.5V to 5.5V) Bypass with 0.1uF or larger.
P18V0_BYPASS		19	-	Bypass to GND with 0.1uF, **50V** capacitor. Do not connect to any other circuit.
P3V3_BYPASS P3V3_BYPASS		27 63	-	Connect these pins together and bypass to GND with 47uF capacitor, rated 6.3V or higher. Do not connect to any other circuit.
P1V2_BYPASS P1V2_BYPASS		38 24	-	Connect these pins together and bypass to GND with 4.7uF capacitor, rated 4V or greater. Do not connect to any other circuit.

DNU DNU		20 29	-	Do not use. Leave disconnected.
RSVD		35	-	Connect to GND. Do not leave disconnected.
BIAS_CP		21	-	Do not use. Leave disconnected.
P1V8_OUT		23	O	1.8V LDO output for system use. Bypass with 1uF capacitor, plus 1uF additional for every mA of output current required up to a maximum of 40mA.
P3V3_OUT1		26	O	3.3V LDO output for system use. Bypass with 1uF capacitor, plus 1uF additional for every mA of output current required up to a maximum of 40mA.
P3V3_OUT2		25	O	3.3V LDO output for system use. Bypass with 1uF capacitor, plus 1uF additional for every mA of output current required up to a maximum of 40mA.
P3V3_IO		28	O	Used internally for GPIO as a reference voltage. Bypass with 22uF capacitor with a rating of at least 6.3V. May be used externally as a system reference voltage.
XTAL32_IN XTAL32_OUT		30 31	-	Connect to 32 kHz crystal. 12pF recommended. Uninterrupted ground shield is required between crystal traces and any digital IO.
GND TAB (PAD)		32 TAB		Connect to GND
CLK_OUT		33	O	32kHz reference output. Requires an external pull-up resistor (open-drain). 3.3V Tolerant
RSTN		34	I	Hold this pin low to reset. This pin contains an internal pull-up to P3V3_IO. A small capacitor is recommended.
SWDIO SWCLK		36 37	IO I	Serial-Wire Debug interface for Cortex M4. Weak internal pull-up to P3V3_IO.
SWDIO_AUX SWCLK_AUX		55 56	IO I	Serial-Wire Debug interface for initial firmware load. This interface is **required** when programming a blank/unused device. Typically, only used once during factory programming to set values into non-volatile retention memory which enable SWDIO&SWCLK. Weak internal pull-up to P3V3_IO.

UART1_TX UART1_RX UART1_RTS UART1_CTS	C1 C0 C3 C2	41 42 39 40	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: UART1. In UART mode _TX & _RTS are output & _RX and _CTS are input.
UART2_TX UART2_RX UART2_RTS UART2_CTS	C4 C5 C7 C6	45 46 43 44	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: UART2. In UART mode _TX & _RTS are output & _RX and _CTS are input.
UART3_TX UART3_RX UART3_RTS UART3_CTS	D0 D1 D3 D2	49 50 47 48	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: UART3. In UART mode _TX & _RTS are output & _RX and _CTS are input.
UART4_TX UART4_RX UART4_RTS UART4_CTS	D4 D5 D7 D6	54 53 51 52	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: UART4. In UART mode _TX & _RTS are output & _RX and _CTS are input.
I2C_SDA I2C_SCL	F1 F0	57 58	IO	Software-controlled 3.3V GPIO with interrupt capability. Alternate mode: I2C. Optional pull-up to 3.3V with selectable resistance: none, 1kΩ,10kΩ,100kΩ (nom.)
SPI_CLK SPI_MOSI SPI_MISO SPI_SEL	E2 E1 E0 E3	59 60 61 62	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: SPI Master. In SPIM mode _CLK, _MOSI, & _SEL are output and _MISO is input.
CANA_TX CANA_RX CANA_STBY	F2 F3 F4	64 65 66	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: CAN1 Transceiver. In CAN mode _TX & _STBY are output and _RX are input.
CANB_TX CANB_RX CANB_STBY	F5 F6 F7	67 68 69	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Alternate mode: CAN2 Transceiver. In CAN mode _TX & _STBY are output and _RX are input.
GP_1 GP_2 GP_3	E4 E5 E6	70 71 72	IO	Software-controlled 3.3V GPIO with interrupt capability. Optional internal pull-up and pull-down resistors. Analog input capable.

Table 4

Environmental Ratings

Limiting Values

Exposure beyond the conditions below may cause damage to the device. Functional operation of the device at conditions beyond the recommended operating conditions is not implied. Exposure to absolute maximum conditions for extended periods of time will affect device reliability. Unless otherwise noted, voltage ranges are to be measured with respect to GND

Voltages Referenced to GND unless otherwise specified

Symbol	Condition	Min	Max	Unit
V_{IN}	All Pins	-0.3		V
	BIAS_CP		P5V0_IN	V
	A1, A2, A3, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15	-0.3	P12V_IN	V
	XTAL32_IN, XTAL32_OUT	-0.3	3.6	V
	CLK_OUT, RSTN, SWDIO, SWDCLK, SWDIO_AUX, SWCLK_AUX, UART1_TX, UART1_RX, UART1_RTS, UART1_CTS UART2_TX, UART2_RX, UART2_RTS, UART2_CTS, UART3_TX, UART3_RX, UART3_RTS, UART3_CTS, UART4_TX, UART4_RX, UART4_RTS, UART4_CTS, I2C_SDA, I2C_SCL, SPI_CK, SPI_MOSI, SPI_MISO, SPI_SEL, CANA_TX, CANA_RX, CANA_STBY, CANB_TX, CANB_RX, CANB_STBY, GP_1, GP_2, GP_3	-0.3	P3V3_IO + 0.3	V

DC Characteristics

Power

Symbol	Description	Condition	Min	Max	Unit
V_{P5V0_IN}	Operating range P5V0_IN		4.5	5.5	V

V_{P12V0_IN}	Operating range P12V0_IN	A_X Pins available	8	16	V
V_{P12V0_IN}	Operating range P12V0_IN	A_X Pins disconnected	4.5	5.5	V

LDO Output

This table applies to pins P3V3_OUT1, P3V3_OUT2 and P1V8_OUT
P_{5V0_IN} between 4.5V and 5.5V, T_J between -40°C and 100°C (unless otherwise specified)

Symbol	Description	Condition	Min	Max	Unit
LDO3P3VoutDCAcc	P3V3_OUT1, P3V3_OUT2, and P1V8_OUT Output Voltage DC accuracy		-5	+5	%

AGPIO

P12V0_IN between 8V and 16V, Tj between -40°C and 100°C, P5V0_IN=5.0V (unless otherwise specified)

Symbol	Description	Condition	Min	Typ	Max	Unit
$R_{IN,ADC}$(1)	AGPIO Input impedance	ADC enabled Tj = 25 °C	1			MΩ
V_{OL_DrvGnd}	AGPIO Output impedance driving low	Pad held at 2.0V	100			mA

Low Voltage IO

Unless otherwise specified, measured at device pins GP_*, UART*, I2C_*, SPI_*, SW*, RSTN, CLKOUT

Symbol	Description	Condition	Min	Typ	Max	Unit
R_{PU}	Pull up Resistors	Excludes CLK_OUT, I2C_SDA and I2C_SCL	7		14.2	kΩ
R_{PD}	Pull down resistors	Excludes I2C_SDA, I2C_SCL, RSTN, SW*, CLK_OUT	7		13.9	kΩ
R_{I2C}	Pull-up Resistor	I2C_SDA and I2C_SCL only.	7		13.9	kΩ

		Configured to 10K mode		
$V_{IH,33}$	Input high level		2.0	V
$V_{IL,33}$	Input low level		0.8	V
$V_{HYST,33}$	Input hysteresis		0.86	V

ADC

P5V0_IN = 4.5V to 5.5V, T_J = -40°C to 125°C unless otherwise noted

Symbol	Description	Condition	Min	Max	Unit
f_{ADC}	Maximum ADC clock			1	MHz
Resolution			8		bits

Current Power & Thermal

Unless otherwise specified, Tj = 0°C to 125°C

Symbol	Description	Condition	Min	Typ	Max	Unit
$T_{J,EXT}$	Junction Temperature, Extended operating range	f_{CPU} = 1.375 MHz f_{SYS} = 1.375 MHz LDO I_{OUT} = 0mA AGPIO in HiZ mode	-40		125	°C
MaxPow	Maximum power dissipation	Continuous			726	mW
MaxPowInst	Peak Maximum power dissipation	t ≤ 1 second			1.6	W
T_{JC}	Package Thermal Resistance	Case measured at QFN pad		25		C°/W
$I_{P5V0,LPM}$	Current on P5V0_IN	I_{P3V3_OUT}, I_{P1V8_OUT} = 0mA f_{SYS} = f_{CPU} = 3.75MHz			5.5	mA

AC Characteristics

Cortex M4

Symbol	Description	Condition	Max	Unit
f_{CPU}	Maximum CPU Frequency	Sysclk = 28 MHz DLL = 4 Flash Delay = 2	112	MHz
f_{Flash}	Maximum Flash Read	f_{CPU} = 40 MHz RDSTALL = 0x00	40	MHz
f_{SWD}	Maximum SWCLK	Measured at package pin	10	MHz
f_{SYS}	Maximum SYSCLK	by design only	28	MHz

Clocks

Test crystal is Abracon ABS06 32.768 KHz crystal, 12pF

Symbol	Description	Condition	Min	Typ	Max	Unit
XTALStartUp	Oscillator Start Time				500	ms
XTALFTol	Total frequency tolerance		-20		20	ppm
XTALQ	Minimum Crystal ESR		9000			Ω
XTALDrive	Maximum Drive				0.5	µW
XTALCl	Load Capacitor			12.5		pF
RC11Fout	Output frequency		10.7		11.3	MHz
$PLLF_{OUT}$	Output frequency			28		MHz

SPI

Unless otherwise specified, Tj between -20°C and +100°C

Symbol	Description	Conditions	Min	Max	Unit
$t_{PD,SYSCLK-SPI\_CLK}$(2)	Output Delay	C_{LOAD} = 10pF SPIDIV=1(1)	4.005	9.497	ns

$t_{PD,SYSCLK-SPI\_SEL}$[2]	Output Delay	C_{LOAD} = 10pF SPIDIV=1[1]	5.060	11.605	ns
$t_{PD,SYSCLK-SPI\_MOSI}$[2]	Output Delay	C_{LOAD} = 10pF SPIDIV=1[1]	4.980	11.947	ns
$t_{PD,SPI\_MISO-SYSCLK}$[2]	Input Setup Delay	SPIDIV=1[1]		9.508	ns
$t_{H,SPI\_MISO-SYSCLK}$[2]	Input Hold		-0.42		ns

(1) For SPIDIV settings above 1, all output delays and setup times are increased by one SYSCLK period.
(2) Guaranteed by design, not production tested

Functional Block Details

DMA Controller

iND83405 contains a powerful DMA engine with 16 independent DMA channels. Each channel has a programmable priority and can be controlled in either direction by I2C Master, SPI Master, any of the four UARTs, or via software. The DMA engine has a dedicated data path to SRAM and peripherals, allowing DMA activity without stalling the CPU.

Each DMA channel supports descriptor chaining allowing for continuous operation without the need to implement DMA control in peripheral drivers, and without implicit real time requirements. The DMA engine dynamically sizes AHB bus transactions to execute transfers using the minimum possible number of bus cycles.

See documentation for ARM PL080
https://developer.arm.com/documentation/ddi0196/g/

DMA-enabled peripherals allow peripherals to function without any CPU intervention by directly triggering DMA transfers when an event occurs. These supported events include:
- UART data received (4 devices)
- UART ready transmit (4 devices)
- SPI data received
- SPI ready to transmit
- I2C data read
- I2C ready to transmit write data

Because the DMA controller has 16 channels, all IO devices can use DMA simultaneously and continuously without interrupting the CPU. The remaining two channels can be used to offload memory-to-memory transfer from the CPU.

The DMA controller allows scatter-gather operation. The DMA engine follows a linked-list of transfer descriptors which can be circular, allowing for continuous operation with zero CPU intervention.

Bursts are not supported.

Internal Flash

iND83405 includes a 2 megabyte internal flash memory for code or data. The memory organization is 2 Banks * 256 sectors * 512 pages * 8 (+1) bytes. Due to asynchronous bus communication between the core and flash, care must be taken to avoid read operations while a program operation is pending on the selected bank; the NV0BUSY:NV0BUSY flag is provided to indicate when a non-volatile memory operation is in progress. In-field replacement of boot firmware is possible using a ping-pong mode of operation which swaps the logical address space between banks. This allows execution to continue from one 1MB bank while the other 1MB bank is programmed or data is stored.

Erase size is 1 sector and program size is 1 page. Pages can only be programmed one at a time.

The Flash memory is mapped to addresses 0x0000_0000 to 0x0010_0000 from the perspective of the CPU.

Each page represents 64-bits of data, but internally contains an additional 8-bit ECC code which is automatically generated. The code can detect up to 2-bit errors and correct 1-bit error. When accessed through the address map, bit errors in data are automatically corrected, dramatically increasing the reliability and lifetime of the Flash. Optionally, an interrupt can be enabled to monitor the number of single bit errors that have been corrected, and another interrupt allows recovery in the case of two-bit errors. The ECC feature can be optionally disabled.

The flash memory runs at a maximum of 40MHz. A selectable wait-state clock divider is provided to allow the CPU to run faster than the Flash memory. The Flash memory has a 16 kB multi-way associative shared data/instruction cache memory. The cache runs at the full CPU frequency. The associativity is run-time selectable so that the total cache memory size can be adjusted to match the required workload. The cache can be manually cleared or disabled.

Crystal Oscillator

The integrated crystal oscillator driver operates at a fixed frequency of 32.768 kHz. The oscillator must be enabled by software after boot time and requires up to 500ms to stabilize depending on the crystal used. There is no lock detection.

RTC

RTC is a 48-bit timer with an adjustable periodic interrupt feature and adjustable pre-divider.

Timers

Three 32-bit count-down timers are provided. The timers have an optional pre-scalar, expiry interrupt, and optional auto-reload.

Each timer can optionally fracture into two 16-bit timers for a total of six system timers (in addition to the RTC, WDT, and SysTick (part of the Cortex M4)).

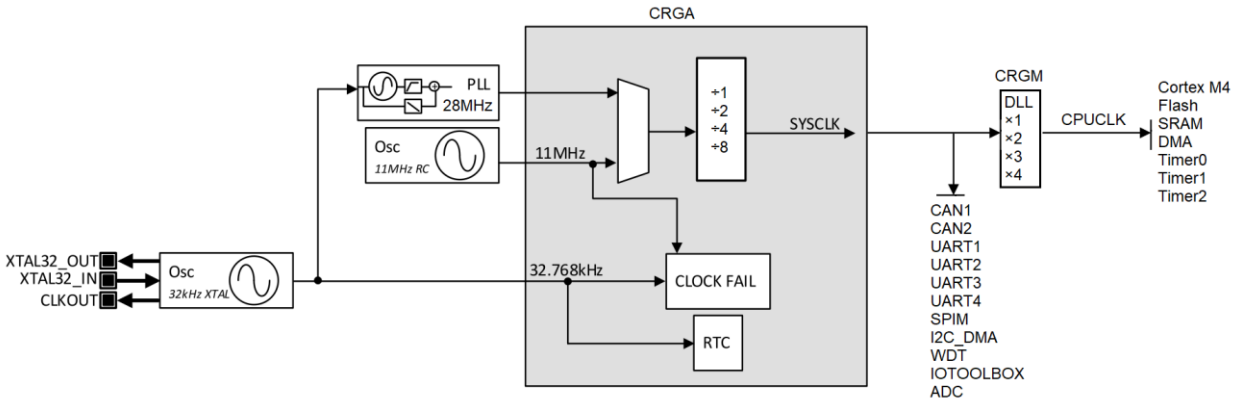
CLK_OUT

The CLK_OUT pin can output a copy of the crystal frequency. The output is open-drain, allowing the output voltage and slew rate to be set with an external resistor.

Clock Network

The iND83405 uses and internal RC oscillator and a crystal driven, fixed PLL as the source for the internal clock network. The fixed-frequency system PLL multiplies the 32.768 kHz crystal oscillator frequency by 854 to 28 MHz. The PLL can be used to source the system clock, SYSCLK, allowing frequencies of 28, 14, 7, and 3.5 MHz. The internal RC oscillator generates a *nominal* 11 MHz frequency which allows SYSCLK to be 11, 5.5, 2.75, or 1.375 MHz. The RC oscillator can also be adjusted from approximately 6MHz to 22MHz by setting RCO_11MHZ_CTRL.CAL bits from 0 to 255, resulting in additional clock choices. Neither the crystal oscillator nor the RC oscillator can be disabled in software, so power savings can only be achieved by selection of the RC oscillator which has been adjusted to run below the nominal frequency.

The RC oscillator has a wide frequency variation, so is not suitable for CAN, UART or applications which require critical timing across temperature range. At boot time the system clock is always sourced by the RC oscillator at the 11MHz nominal frequency; the PLL must be selected through software.



Regardless of the RC or PLL selection, the clock signal will enter a divider with divide-by settings of 1, 2, 4 or 8. This divider is adjusted using the CLK_CTRL.CLK_DIV. The output of this divider is the system clock, SYSCLK.

Each IO peripheral, such as UART or CAN, have additional dividers to further reduce the clock speed as needed and/or set by software.

The CPU Clock is derived from SYSCLK after being multiplied by 1, 2, 3, or 4 by a DLL using the CRGM_DLLCTRL.MULT. Using nominal frequencies, CPU clock rates between 1.375 MHz and 112MHz are possible. SRAM, Flash memory, and Timers derive their clock source from CPU clock as well. Whenever the SYSCLK frequency is changed, the DLL must first be disabled by setting the multiply-by to 1 ($f_{SYS} = f_{CPU}$). After the clock has changed the DLL can be readjusted.

Source	Post	DLL	f_{SYS} (MHz)	f_{CPU} (MHz)
PLL	÷1	×4	28	112
PLL	÷2	×4	14	56
PLL	÷4	×4	7	28
RC	÷1	×4	11	44
RC	÷8	×4	3.75	11
RC	÷8	×1	3.75	3.75

Suggested Clock Network Settings

The maximum frequency of the flash memory is 40 MHz. When CPU clock is set to frequencies above 40 MHz, a wait-state must be implemented in software to meet Flash timing requirements. This is done simply by adjusting the RDSTALL register bits as described in the table below.

CPUCLK Frequency	RDSTALL
0 – 40 MHz	**0**
41 – 79 MHz	**1**

80 – 112 MHz	**2**

Flash Wait-state Register Settings

Peripheral Functions

System LDOs

Three LDOs are provided for system use: two 3.3V LDOs and one 1.8V LDO. These are available on pins P3V3_OUT1, P3V3_OUT2 and P1V8_OUT respectively and receive their input from the P5V0_IN pin. Each LDO can be enabled independently through software using the PMUCTRL register. It is important to add sufficient capacitance to each pin to prevent (startup) instability and retain tight output tolerance. In additions to a 1uF capacitor, it is recommended that 1uF be added for each milliamp of current the LDO is expected to source. If the any LDO will not be used it can be disabled, with capacitor(s) omitted, and the pin left disconnected.

Control registers are listed and described in the PMUA_MAP.html file.

UART

Four UARTs are provided. Each supports optional hardware flow-control, internal loop-back, 16-byte hardware FIFOs, break detection, selectable bit-width, selectable parity type, selectable stop-width, two oversample modes and a build-in independent baud-rate generator.

Interrupt events include RX data available, TX complete, and break detection. Interrupt generation can be set to a counter or watermark mode to reduce overhead.

All UARTs can be used with DMA in linear or circular mode to operate continuously at very high baud rates without CPU intervention. In this way, mega-bit baud rates are easily achievable.

Upon reset UART pins default to GPIO mode. UART operation is enabled using bits in the PINMODE register which are described in the IOCTRLA_MAP.HTML file. UART control registers are listed and described in the UARTx_MAP.html files.

CAN Controller

The iND83405 has two CAN (controller-area network) 2.0b controllers. Each controller has 8 priority transmit and16 receive slots and 16 acceptance filters. CAN FD is not supported. Each controller has an independent baud rate generator.

Events with interrupt support include RX data, Error (various types), and TX slot available.

Upon reset CAN pins default to GPIO mode. CAN operation is enabled using bits in the PINMODE register which are described in the IOCTRLA_MAP.HTML file. CAN control registers are listed and described in the CANCTRLx_MAP.html files and CANRXCNTRL_MAP.html file.

SPI Master Controller

One SPI master controller is provided. It features two 16-byte FIFOs and DMA support in both the transmit and receive directions, allowing for very high throughput without CPU intervention. Standard SPI IO modes are supported. SPI has and independent baud rate generator.

Events with interrupt support include TX FIFO Overflow, RX FIFO Underflow, and TX Complete (count).

Upon reset SPI pins default to GPIO mode. SPI operation is enabled using bits in the PINMODE register which are described in the IOCTRLA_MAP.HTML file. SPI control registers are listed and described in the SPIM_ARGON_MAP.html files.

I2C Controller

One I2C controller is provided. The controller supports both master and slave modes and 7-bit or 10-bit addresses. The I2C controller is capable of using DMA for transmit and receive for any I2C transactions with a known number of write bytes followed by a known number of read bytes. In this way, peripherals like accelerometers can be read continuously without any CPU intervention.

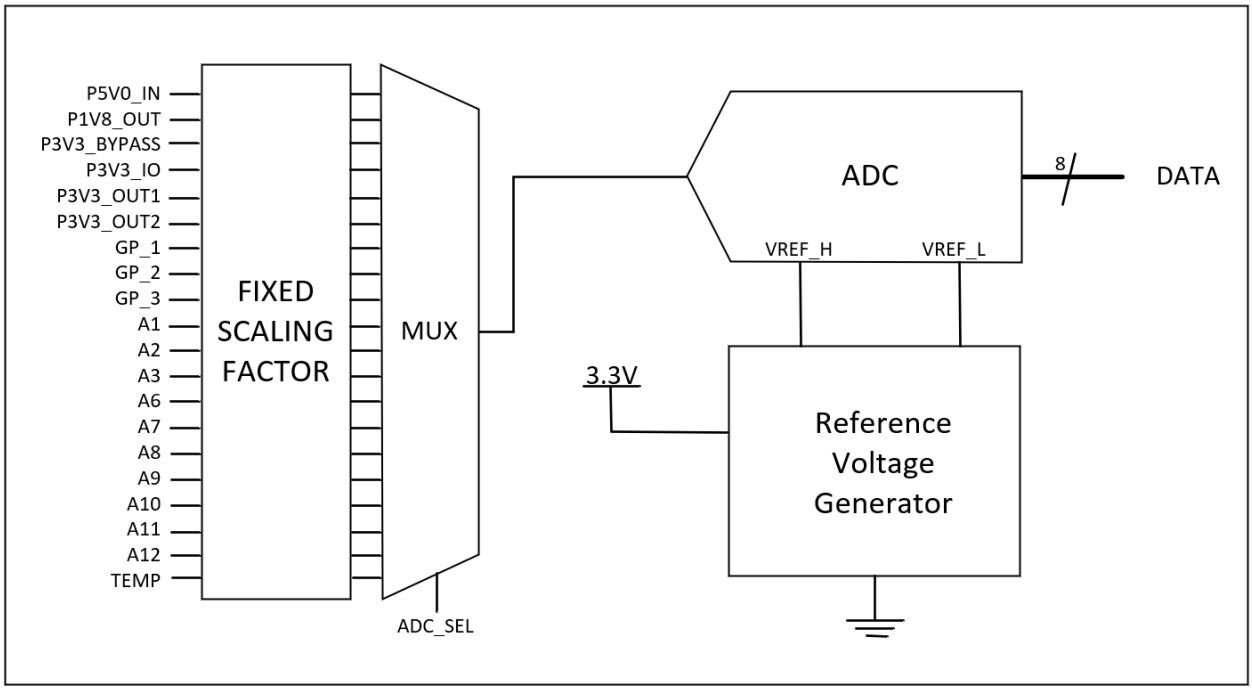
A receive interrupt is triggered by a falling edge on SDA pin.

Upon reset I2C pins default to GPIO mode. I2C operation is enabled using bits in the PINMODE register which are described in the IOCTRLA_MAP.HTML file. I2C control registers are listed and described in the I2C_MAP.html file.

ADC

One 8-bit SAR ADC can be connected to some external pins and internal power rails as well as measure die temperature. The ADC can generate up to 80,000 samples per second and is temperature compensated. A maskable interrupt is available to signal when a conversion has completed. Analog values can be measured on: GP_1, GP_2, CP_3, all 13 Ax pins, all internal power rails including both input power pins: V5P0_LDO_IN, V12P0_IN, and internal die temperature sensor.

The ADC module features adjustable voltage references. By adjusting the high and low reference voltages, the measurement range can be reduced. Since the ADC always has 256 steps, a reduced range results in better measurement precision (smaller LSB). In this way, the effective number of bits is increased. The ADC has three modes of operation as set by the GPADCMODE register bits: OFF, Single-shot, and Continuous.



The ADC is powered from V3P3_BYPASS voltage, therefor its input and references must not exceed the 3.3V value. Signal inputs are scaled down prior to the MUX to prevent clipping. The final ADC result value must be multiplied by the fixed scaling factor to compute the actual signal voltage. Similarly, the voltages on VREF_H and VREF_L must not be set such that they exceeded the 3.3V limit. Additionally, input voltages are limited by the allowable voltage range specified for the channel selected. For example, Ax pins are limited to about 12V; large voltage

reference spans, VREFH – VREFL, will have theoretical results which correspond to input pin voltages greater than the pin limit which cannot be realized.

Input Channel	Fixed Scaling Factor
GP_x	1
V5P0_LDO_IN	0.5
V12P0_IN	0.12
P1V8_OUT	1
P3V3_OUTx, P3V3_IO	0.67
Ax	~0.188

VREF_H and VREF_L voltages are created by scaling the ADC's source. This scaling factor is controlled through the adjustment of two 4-bit registers as described below.

Reference Source: 3.3V Supply

HKADDCTRL:GPADCFULLRG = 1

$$VREF\_H = 3.300V \times \frac{GPADCSELHIGH}{15}$$

$$VREF\_L = 3.300V \times \frac{GPADCSELLOW}{15}$$

$$3.3V \geq VREF\_H > VREF\_L$$

$$V\_LSB, in\ mV = 1000 \times \frac{1}{INPUT\_SCALE} \times \frac{(VREF\_H - VREF\_L)}{255}$$

$$V\_RESULT = \frac{1}{INPUT\_SCALE}\left(VREF\_L + \frac{ADC\ CODE \times (VREF\_H - VREF\_L)}{255}\right)$$

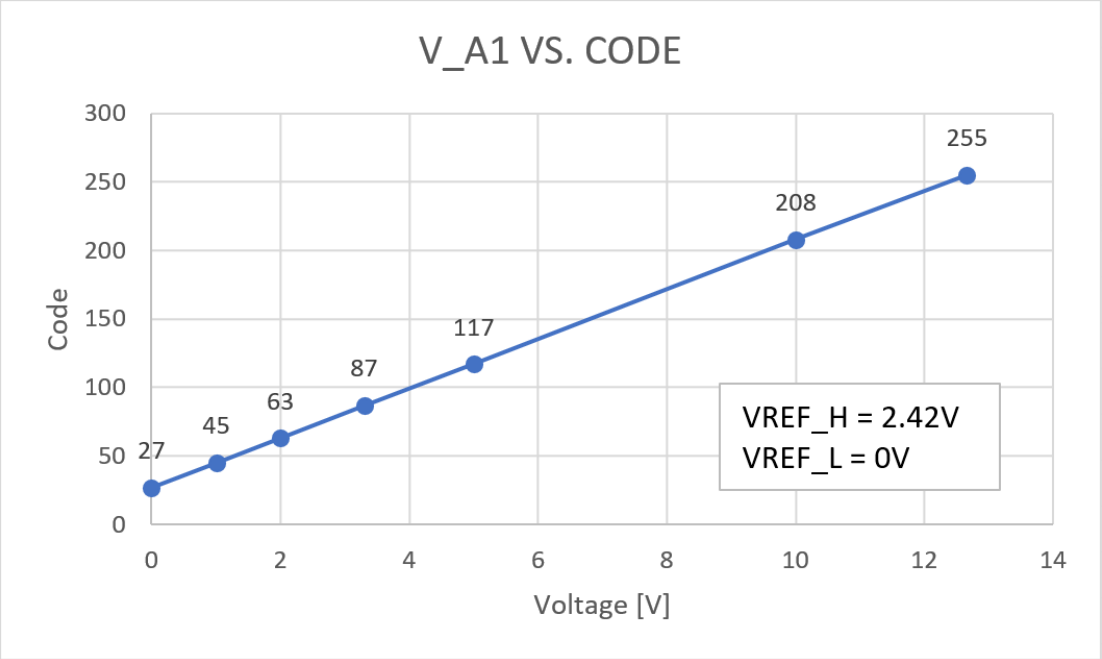
$$V\_TEMP = 24mV \times T_{°C} - 654.5mV$$

The ADC sample rate is based on the system clock, SYSCLK, with programable divider options of 8, 16, 32, or 64 by the ADCLKDIV register bits. The sample time is adjustable with the 3-bit GPADCSAMPCYC register bits. Sample time is equal to GPADCSAMPCYC X T_{SYSCLK}.

Die temperature can be measured by selecting the TEMP channel and measuring the sensor's output voltage. Use the transfer function in the figure above to compute the result in degrees Celsius.

Several other control bits are shown in the register description. These bits must be set as follows:

GPADCFULLRG = 1
GPADCRSTN = 1
GPADCGNDOFF = 0
GPADCENFORCE = 0
GPADCCAL = 0
GPADCSELGAIN = 15



The figure above shows analog voltage measurement operation with voltage on pin A1. ADC references (GPADCSELLOW = 0 and GPADCSELHIGH = 11) are set to measure the largest input pin voltage span while preserving 256 bits of resolution. In this measurement scenario, Increasing GPADCSELHIGH above 11, is not useful because the some of the ADC measurement range is above the voltage limit of the pin.

Ax pins require additional setup when used with the ADC. Due to the higher pin voltage range a charge pump and bias circuit need to be enabled; this is done by setting the ENCP and

RCOMPBIASA bits in AGPIOCTRL register. Additionally, RCOMPENA and RENA5V bits must be set in A_XCTRL registers to allow Ax pins signals to connect with the ADC.

Since multiple channels with different input scale attenuators are multiplexed to the same ADC, for simplicity it is recommended that the ADC module be used with VREF_L set to 0V, VREF_H set to 3.3V, sample time set to maximum, and with the lowest sample rate possible to meet the application requirements.

ASIC_INFO & Retention Memory

The device contains a small peripheral memory block which contains a product ID code and silicon revision, 64-bytes of retention memory, and control bits which enable and disable the CPU SWD interface.

WDT

A 32-bit count-down timer with an optional system reset trigger is provided for Watch Dog Timer use. Register access to the WDT are protected by 32-bit command words to prevent accidental triggering or resetting. The timer is based off of the system clock with a selectable strobe period set by the TIMEOUTSEL bits. By default, the WDT is disabled, but can be enabled by writing any value to the STOP register other than the special “stop” code. It can also be disabled by writing the “stop” code, 0x6DA475C3, to the STOP register. The WDT is cleared by writing to0x3C570001 then, 0x007f4AD6 to the CLEAR register in sequence with no intervening register accesses. The WDT count value can also be read using the CNTVAL register.

Upon power cycle and reset, the system clock is always derived from the internal RC timer. Software should enable the watchdog prior to switching the clock source to the external crystal. If the crystal fails to start the watchdog will reset the device.

AGPIO Pins

There are thirteen robust AGPIOs pins, A_{XX}, which are 5V tolerant. These pins can only be used if V12P0_IN is supplied with 8V or greater. They can be set low by writing 0x1 to A_{XX}CTRL:POL bit, otherwise the pin is tristate. The logic state on each pin can be read using the AGPIOREAD:A_{XX} bit. The nominal threshold for logic read values is 2.5V when the A_XCTRL:RENA5V bit is set. AGPIO pins can also be connected to the ADC using the mux as described in the ADC section.

Logic control of A1 pin differs slightly from the rest of the AGPIO pins. To set this pin low, both the A_{01}CTRL:POL bit and the AGPIODEBUG:A1REG bit must be set.

Upon reset AGPIO pins default to GPIO mode. IO operations are described in the IOCTRLA_MAP.HTML file. ADC control registers are listed and described in the ADC_MAP.html file.

Low-Voltage IO Pins

iND83405 contains thirty-one 3.3V IO pin which can be used for software controlled GPIO. Each IO supports input and output mode, and have optional pull-up and pull-down resistors, as well as edge-detection interrupts. Pins I2C_SCL and I2C_SDA have no available pull-down resistor capability but have a selectable pull-up strength with shared control bits.

Upon reset low-voltage GPIO pins default to GPIO mode. IO operations are described in the IOCTRLA_MAP.HTML and GPIO_MAP.HTML files. GP_1, GP_2, GP_3 can be connected to the ADC; ADC control registers are listed and described in the ADC_MAP.html file.

SWD Debugging Interface

SWD (Single-Wire Debug) is an interface which provides debug access to the CPU, the internal memory, and memory-mapped peripherals. The iND83405 has two sets SWD pin interfaces. The first interface uses SWCLK and SWDIO pins to communicate with the arm CPU core for debugging and programming. The second interface uses the SWCLK_AUX and SWDIO_AUX pins for the special purpose of enabling the SWCLK and SWDIO pin interface. Both interfaces operate at 3.3V. The pins contain weak pull-up resistors which are suitable for keeping the interface inactive while not in connected, however for best performance, external resistors are recommended. SWD debugging has been tested with Segger JLink and GDB.

After a system reset, the SWCLK and SWDIO pins are not configured for SWD mode, and therefore the CPU and memory cannot be accessed. SWCLK and SWDIO pins are enabled by writing command values into the ASIC_INFO registers located in the retention memory. Devices which are new from the factory or with unprogrammed Flash require SWD_AUX pin communication to enable SWD pins for programing or debugging. The SWD_AUX interface is always enabled after a system reset, but has limited access to core and memory, and can only be used to write the special command codes into ASIC_INFO registers. System firmware should initialization the ASIC_INFO registers to enable SWD pins so that the SWD_AUX pins are no longer needed.

To program blank parts, access to both the CPU and AUX SWD interfaces is required. Once programmed with a bootloader that contains the necessary code to enable the CPU/SWD interface, the AUX interface is no longer required. If a device internal flash memory is erased, the AUX interface will be required to recover the device.

Document Revision History

Date	Revision
2022-SEP-22	Initial Public Release

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