iND83215
Datasheet
Rev 0.36

1 REVISION HISTORY

Table 1 Revision History

Rev #	Date	Action
0.1	11/07/2022	First Release. (Merged from Rev 1.4 of iND83209 and Rev 0.7 of iND83212)
0.2	12/16/2022	Update Block Diagram
0.3	1/13/2023	Update Package and IO description Update iND83215 QFN24 package
0.31	3/6/2023	Update part number
0.32	3/9/2023	Update ordering code
0.33	5/16/2023	Update EC Table and Register Map Update Block Diagram Remove 48MHz OSC
0.34	8/10/2023	Fix figure and table numbering
0.35	11/02/2023	Update 8.2.14.11 SARCFG
0.36	11/22/2023	1. Updated 9.1.1 Power on sequence 2. Changed Tj from 125C to 150C

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5 ORDERING INFORMATION

Part number	Ordering Code	Package	Shipping
iND83215	iND83215-Q20	QFN20	4000pcs/Tape&Reel
	iND83215-Q24	QFN24	4000pcs/Tape&Reel

6 SYSTEM OVERVIEW

"iND83215" IC is an automotive LED lighting integrated device that combines together a 32bit MCU (Cortex M0) with a power management unit capable of handling 45V Load dump from the car battery, 3 high voltage constant current open drain IOs with PWM, a LIN slave transceiver supporting LIN auto-addressing, a LIN master transceiver for extension, an integrated 12-bit ADC for monitoring, aging and temperature compensation purpose.

- Full automotive qualification AEC-Q100 Grade1
- Functional Safety Enhancements:
    - Hardware LIN TX monitor to prevent a dominant bus caused by internal malfunction
    - LIN Bus Idle timeout monitor
        - Always active, even the chip is in hibernate mode
        - For preventing a fast discharge of the car battery, if a short to ground is detected, the following options are available
            - Automatically switch off LIN slave's pullup.
        - Auto-recovery if the failure condition disappears
- CPU architecture:
    - ARM Cortex-M0 processor
    - SysTick Timer (24bits, interruptible)
    - Serial Wire Debug port (SWD)
    - Built-in Nested Vectored Interrupt Controller (NVIC)
    - Programmable Watch-Dog Timer
    - 3 programmable timers
- Memory:
    - 48kBytes of Flash Program Memory, 10 years retention in automotive environment
    - 8kBytes of SRAM with ECC
- Peripherals/Digital Features
    - Clock and Reset Manager
        - Two internal clock resources:

- Trimmable 256kHz Auxiliary ROSC mode supports more flexible/accurate LIN wakeup filtering. Auxiliary system clock frequency is 256kHz/16.
- Trimmable 16MHz ROSC with SSC support

▪ Reset Sources:

- POR and BOR (no external reset)
- SW Triggers: Hard/Soft

o Power Management

▪ Active Mode

▪ CPU Sleep Mode

- Triggered by Cortex-M0 WFI instruction
- Wakeup Resources: Interrupts/Exceptions

▪ DeepSleep Mode

- ASIC power-on
- MCU power-off
- Wakeup Resources: GPIOs/LINS/LINM/SWD/Wakeup Timer

▪ Hibernate Mode

- ASIC 5V domain power-on
- ASIC 1.5V domain power-off
- MCU power-off
- Wakeup Resources: Only LINS/LINM

o One SAE J2602/LIN2.2 LIN Slave Controller and Transceiver

▪ Supports LIN auto-addressing through an internal LIN switch.

o One LIN Master Controller and Transceiver

▪ Only available when the internal LIN switch is not used.

▪ Only supports auto-baudrate LIN Slaves.

o Watch dog timer (ASIC side) with window mode support

o 3x16-bit PWM required to control LED current driver:

▪ Common prescaler and 16bit timer

▪ Support power balance with independent rise/fall timing configuration

- General Purpose IOs x 6(QFN20, IND83215), IOs x 10(QFN24, IND83215A)
  - SPI mater x1
  - UART x1
  - Dual edges detection interrupt supported
  - PWM mode supported
  - Input capture supported
  - External LIN Transceiver interconnection capability
    - LINM RxD/TxD: PA[3]/PA[2] or PB[1]/PB[0]
    - LINS RxD/TxD: PA[1]/PA[0] or PA[7]/PA[6]

- Peripherals/Analog Features
  - 3 Programmable 60mA max constant current / high voltage IO open drain
  - PN voltage measurement for temp compensation
    - Integrated a dedicated 2.5mA current source
    - Fully differential measurement
  - Temperature Sensor/Monitor with ADC
  - Battery voltage detection and monitoring
  - Hardware over temperature protection
  - 12-bit SAR ADC with 26channels
    - Bandgap Reference
    - Accurate VBAT Channel
    - Junction Temperature
    - Analog Input from PA/PB Pad
    - Analog Input from LED x 3
    - Forward Voltage of External LED x 3
    - VDD1V5/VDD3V3/VDDPRE5V
  - Integrated voltage regulators
    - LDO 3.3V
      - Output
      - ASIC Core and IO supply
      - MCU I/O

- LDO 1.5V（capless）
  - Output
  - MCU core

6.1 BLOCK DIAGRAM

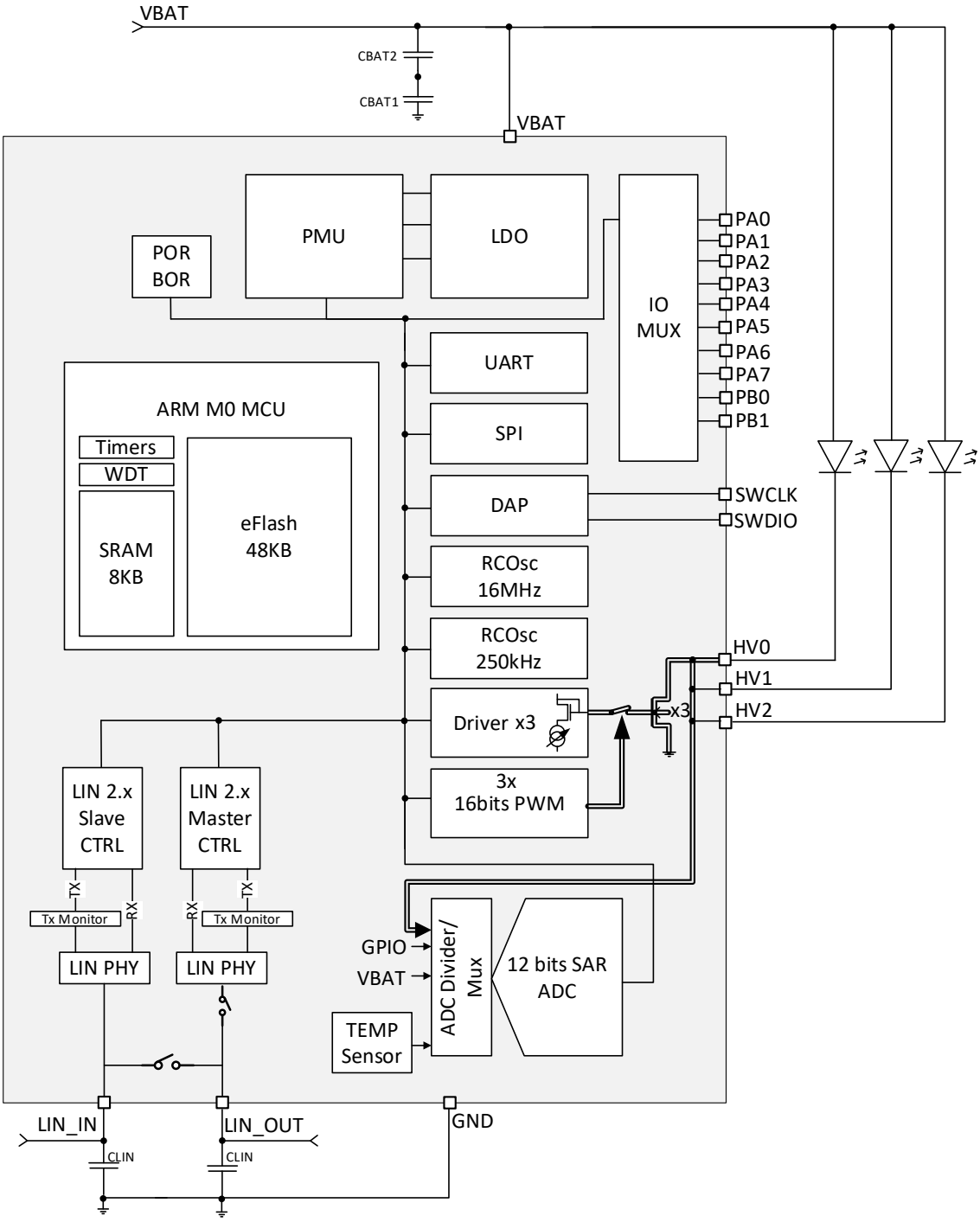


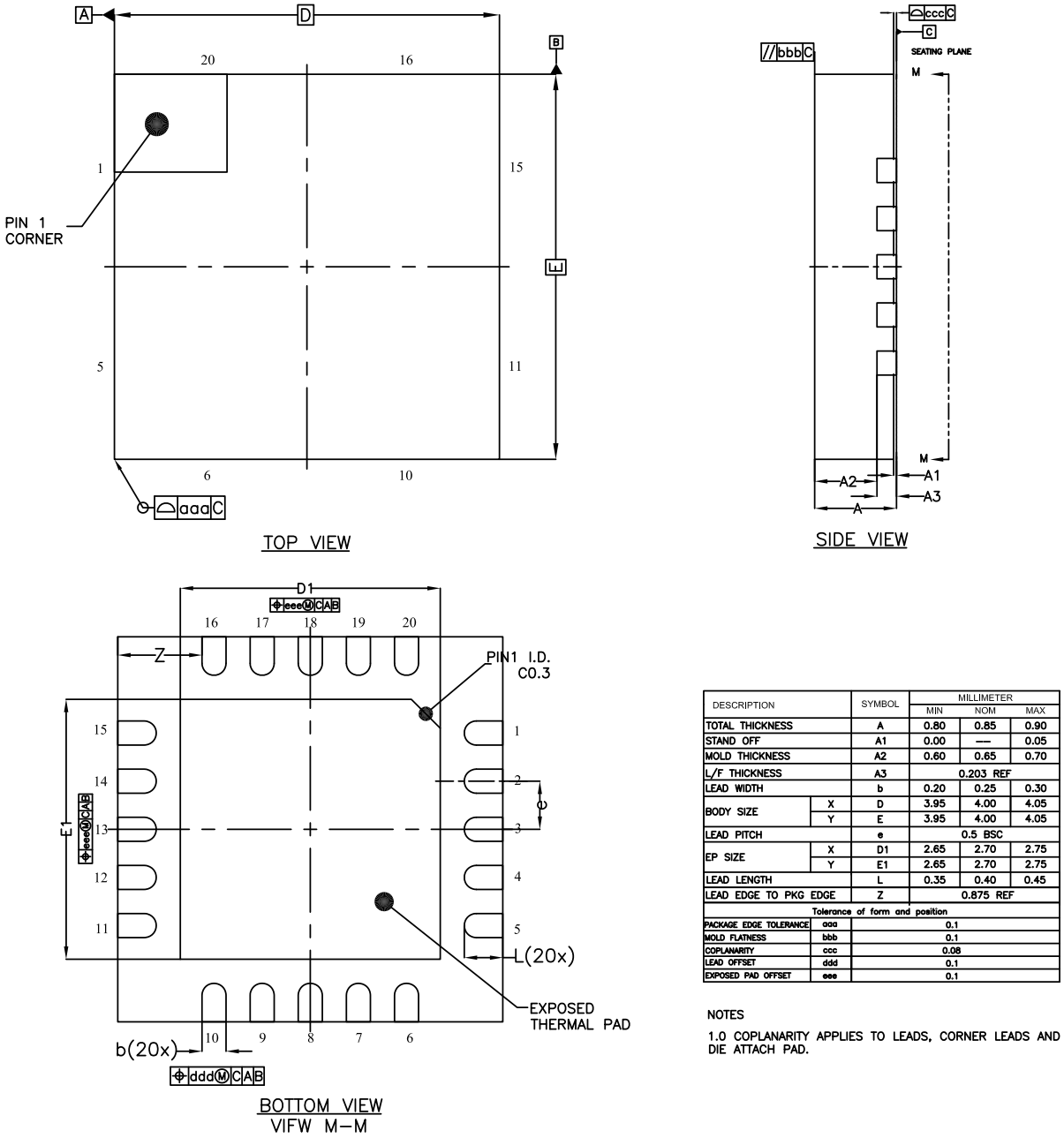
Figure 1 IC block diagram

Note: The application block diagram does not include components used to qualify the system against ISO7637-2/-3.

6.2 PACKAGE OVERVIEW AND PIN DESCRIPTIONS

6.2.1 Package Outline

iND83215-Q20, QFN20, 4x4 mm body size, 0.5 mm lead pitch.



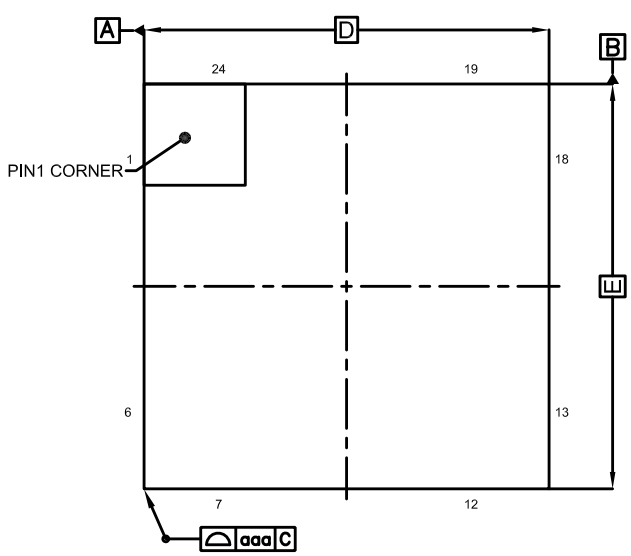
DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.20	0.25	0.30
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
LEAD LENGTH		L	0.35	0.40	0.45
LEAD EDGE TO PKG EDGE		Z	0.875 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa		0.1		
MOLD FLATNESS	bbb		0.1		
COPLANARITY	ccc		0.08		
LEAD OFFSET	ddd		0.1		
EXPOSED PAD OFFSET	eee		0.1		

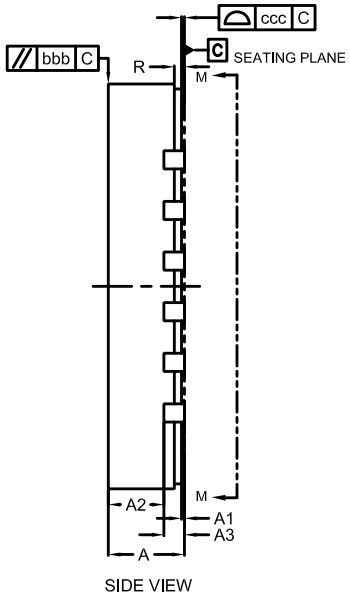
NOTES

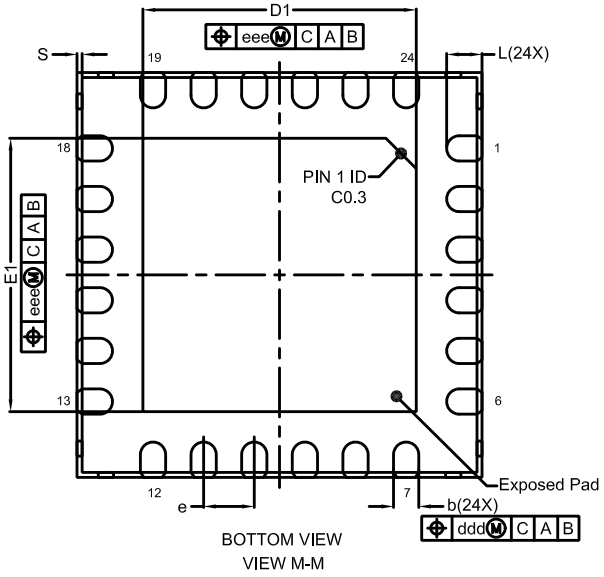
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 2 iND83215-Q20 Package Outline Dimension

iND83215-Q24, QFN24, 4x4 mm body size, 0.5 mm lead pitch.







DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.50 BSC		
LEAD WIDTH		b	0.20	0.25	0.30
LEAD LENGTH		L	0.30	0.35	0.40
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
STEP CUT WIDTH		S	0.001	0.05	0.09
STEP CUT HEIGHT		R	0.05	0.10	0.15
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.05		
MOLD FLATNESS		bbb	0.10		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.10		
EXPOSED PAD OFFSET		eee	0.10		

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 3 iND83215-Q24 Package Outline Dimension

6.2.2 Package Marking

Ordering Code: iND83215-Q20 (QFN-20)

Package Branding:

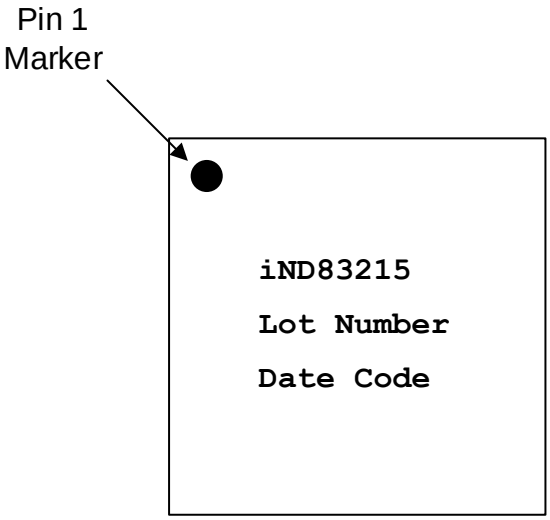


Figure 4 Package Branding(iND83215-Q20)

Ordering Code: iND83215-Q24 (QFN-24)

Package Branding:

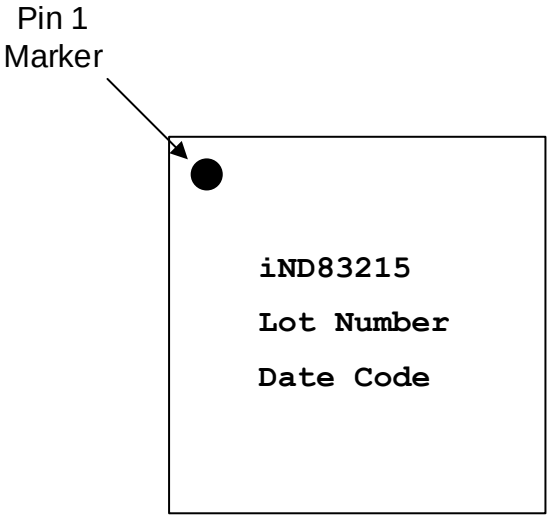


Figure 5 Package Branding(iND83215-Q24)

6.2.3 Pin Descriptions

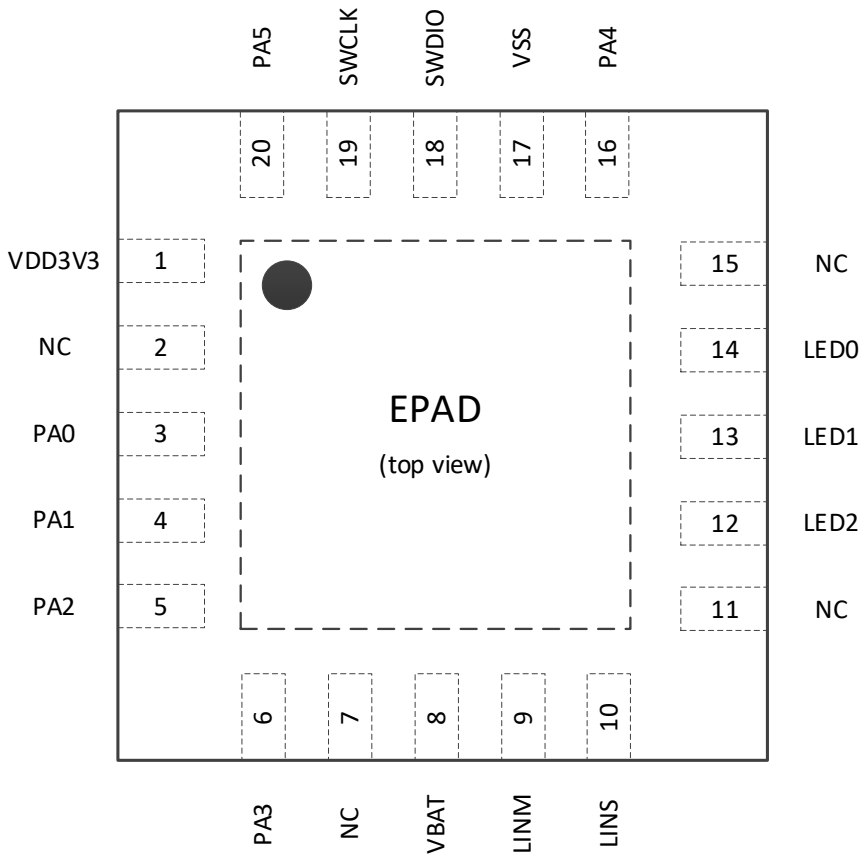


Figure 6 Pin Configuration (iND83215-Q20, QFN20)

Table 2 Pin List (iND83215-Q20, QFN20)

# QFN20	Pin Name	Type	Voltage	Direction	Description
1	VDD3V3	Supply	VDD3V3	n/a	Connect to the external 4.7uF capacitor. Also used for debugger detection.
2	NC	-	-	-	-
3	PA0	GPIO	VDD3V3	I/O	General purpose IO/ LINS TxD/SPI SS
4	PA1	GPIO	VDD3V3	I/O	General purpose IO/ LINS RxD/SPI Clock

# QFN20	Pin Name	Type	Voltage	Direction	Description
5	PA2	GPIO	VDD3V3	I/O	General purpose IO/ LINM TxD/SPI SS
6	PA3	GPIO	VDD3V3	I/O	General purpose IO/ LINM RxD/SPI MISO
7	NC	-	-	-	-
8	VBAT	Supply	Vehicle Power	n/a	-
9	LINM	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
10	LINS	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
11	NC	-	-	-	-
12	LED2	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
13	LED1	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
14	LED0	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
15	NC	-	-	-	-
16	PA4	GPIO	VDD3V3	I/O	General purpose IO/ UART TxD/SPI MOSI
17	VSS	Supply	GND	Analog	Bonding with ground plane
18	SWDIO	GPIO	VDD3V3	I/O	ARM debugger data. Integrated weak pull up.

# QFN20	Pin Name	Type	Voltage	Direction	Description
19	SWCLK	GPIO	VDD3V3	Input	ARM debugger clk. Integrated weak pull down.
20	PA5	GPIO	VDD3V3	I/O	General purpose IO/ UART RxD/SPI MISO
*	EPAD	Supply	GND	n/a	Ground

*GND pin is the thermally significant pin

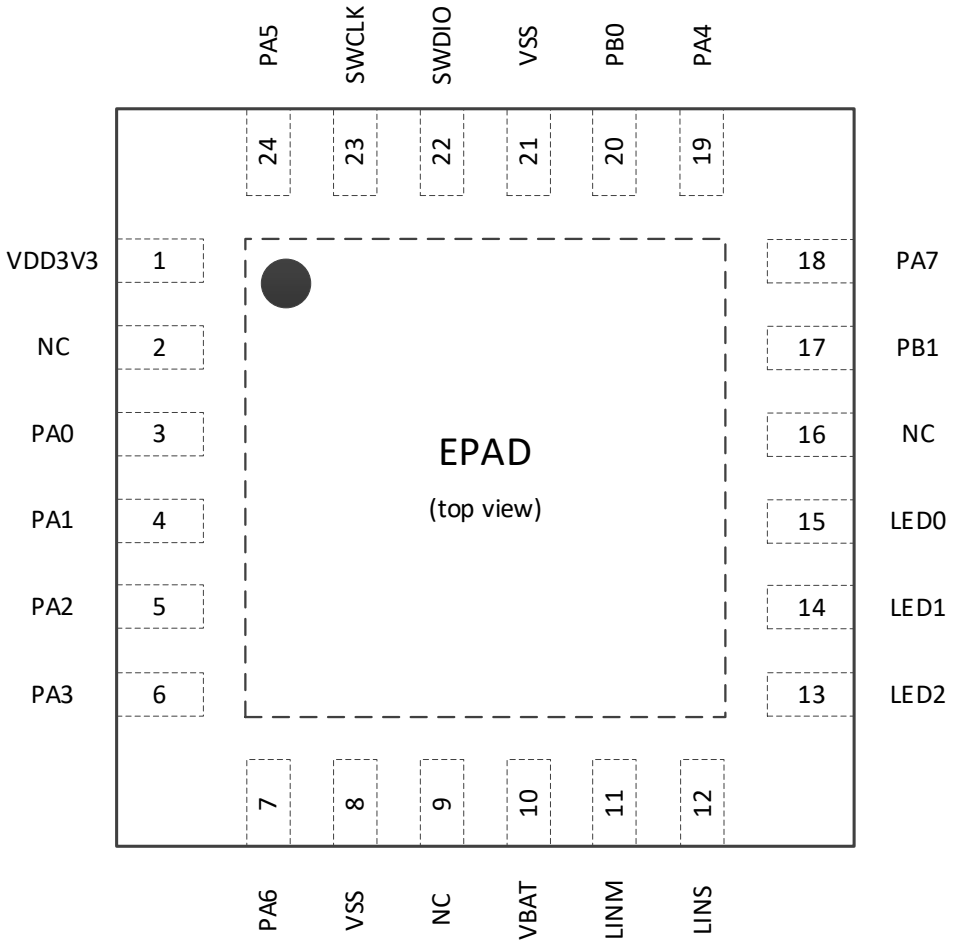


Figure 7 Pin Configuration (iND83215-Q24, QFN24)

Table 3 Pin List (iND83215-Q24, QFN24)

# QFN24	Pin Name	Type	Voltage	Direction	Description
1	VDD3V3	Supply	VDD3V3	n/a	Connect to the external 4.7uF capacitor. Also used for debugger detection.
2	NC	-	-	-	-
3	PA0	GPIO	VDD3V3	I/O	General purpose IO/ LINS TxD/SPI SS
4	PA1	GPIO	VDD3V3	I/O	General purpose IO/ LINS RxD/SPI Clock
5	PA2	GPIO	VDD3V3	I/O	General purpose IO/ LINM TxD/SPI SS
6	PA3	GPIO	VDD3V3	I/O	General purpose IO/ LINM RxD/SPI MISO
7	PA6	GPIO	VDD3V3	I/O	General purpose IO/ LINS TxD/UART TxD
8	VSS	Supply	GND	Analog	Bonding with ground plane
9	NC	-	-	-	-
10	VBAT	Supply	Vehicle Power	n/a	-
11	LINM	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
12	LINS	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
13	LED2	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
14	LED1	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current

# QFN24	Pin Name	Type	Voltage	Direction	Description
15	LED0	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
16	NC	-	-	-	-
17	PB1	GPIO	VDD3V3	I/O	General purpose IO/ LINM RxD/UART RxD
18	PA7	GPIO	VDD3V3	I/O	General purpose IO/ LINS RxD/UART RxD
19	PA4	GPIO	VDD3V3	I/O	General purpose IO/ UART TxD/SPI MOSI
20	PB0	GPIO	VDD3V3	I/O	General purpose IO/ LINM TxD/UART TxD
21	VSS	Supply	GND	Analog	Bonding with ground plane
22	SWDIO	GPIO	VDD3V3	I/O	ARM debugger data. Integrated weak pull up.
23	SWCLK	GPIO	VDD3V3	Input	ARM debugger clk. Integrated weak pull down.
24	PA5	GPIO	VDD3V3	I/O	General purpose IO/ UART RxD/SPI MISO
*	EPAD	Supply	GND	n/a	Ground

*GND pin is the thermally significant pin

6.2.3.1 Pin state upon Power-on Reset

- Unless otherwise noted, all pins default to tristate/Isolation mode (Hi-Z) upon power-on reset.

7 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Table 4 Absolute Maximum Ratings, Voltages Referenced to ground

Names	Conditions	Min.	Max.	Unit
VBAT	No damage, t<500ms	-0.3	+45	V
VBAT	No damage, t<5min	-0.3	+28	V
VBAT	No damage, t<5ms	-1.1		V
VBAT	No damage, t<20ns	-4.0		V
VBAT	No damage, ISO 7637-2 pulse 1, VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-100		V
VBAT	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+50	V
VBAT	No damage, accept ISO 7637-2 pulses 3A, 3B, VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-150	+100	V
VBAT	No damage, ISO 7637-2 pulses 5b VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+45	V
LIN	No damage, t<500ms	-40	+40	V
LIN	No damage, ISO 7637-3 pulse 1 VBAT=13.5V, TA=23°+/-5C, test pulse applied to LIN via 1nF capacitor	-100		V
LIN	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied via 1nF capacitor		+50	V

LIN	No damage, ISO 7637-2 pulses 3A, 3B VBAT=13.5V, TA= (23+/-5) °C, test pulse applied via 1nF capacitor	-150	+100	V
LEDx	No damage, t<500ms	-0.3	+45	V
LEDx	No damage, t<5min	-0.3	+28	V
LEDx	No damage, t<5ms, voltage applied on the anode side of the LED, current sink open (LED Off)	-1.1		V
LEDx	No damage, t<20ns, voltage applied on the anode side of the LED, current sink open (LED Off)	-4		V
PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PB0, PB1, PA0, PA1, SWCLK, SWDIO		-0.3	3.6	V
Storage Temp		-55	+150	℃

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. The absolute maximum ratings provided in the table above are limiting values that do not lead to a permanent damage of the part. But functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

Table 5 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operation Conditions					
Operating ambient Temperature		-40	25	125	°C
Operating Junction Temperature		-40	25	150	°C
Package Thermal Resistance	Junction to Ambient (ThetaJA)		30		K/W
VBAT		6	13.5	18	V
IO Supply (VDD3P3)		3.0	3.3	3.6	V
ASIC Core Supply (VDD3P3)		3.0	3.3	3.6	V
MCU Core Supply	MCU Core Supply including SRAM and Flash	1.35	1.5	1.65	V
Flash Memory					
Sector Endurance		20k			cycles
Data Retention	@25degC	100			Years
Data Retention	@85degC	25			Years
Data Retention	@125degC	10			Years
SRAM					
Min Retention Voltage	Minimum Retention Voltage below which SRAM data are not guaranteed.	1.08			V
Clocks					
System 16MHz RC Oscillator Frequency	16MHz		16		MHz

Parameter	Conditions	Min.	Typ.	Max.	Unit
System 16MHz RC Oscillator Accuracy	16MHz	-4		4	%
System 16MHz RC Oscillator start up time	16MHz		10		us
Auxiliary system clock	Used in sleep mode		256		kHz
Auxiliary system clock Accuracy		-6		6	%
POR/BOR					
POR (VDD3P3)		1.8		2.1	V
BOR VDD3P3	200mV window, steps every 100mV (2.3 to 3.2V)	2.1		3.2	V
BOR VDD1P5	Max Value at which system resume operation		1.35		V
Battery Monitor					
Under Voltage Threshold	Analog Comparator Generates interrupt to MCU except in Hibernate mode	4.5	5.0	5.5	V
		5.5	6.0	6.5	V
		6.5	7.0	7.5	V
		7.5	8.0	8.5	V
		8.5	9.0	9.5	V
Under Voltage hysteresis	Programmable, UVHYS=0	2.5	4.0	6.0	%
	Programmable, UVHYS=1	4.0	6.0	9.5	%
	Programmable, UVHYS=2	5.0	8.5	14.0	%
	Programmable, UVHYS=3	6.0	10.5	19.0	%
Under Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
Over Voltage Threshold	Analog Comparator, generates interrupt to MCU except in Hibernate mode	14		19	V
Over Voltage Hysteresis	Programmable, OVHYS=0	1.5	2.5	3.0	%
	Programmable, OVHYS=1	3.0	5.5	8.0	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
	Programmable, OVHYS=2	5.0	9.0	13.0	%
	Programmable, OVHYS=3	8.0	12.0	16.0	%
Over Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
LED Current Source HVIO					
HVIO voltage	minimum voltage to ensure current regulation	1.6			V
Sink Current	VBAT>6V	0.12		60	mA
Sink Current step size			120		uA
Sink Current Error	Ta=25degC	-7		+7	%
Temperature Drift			-0.025		%/K
HVIO switch resistance	Guaranteed by design	53			Ω
Over Temperature Monitor					
Overtemp Threshold	Analog Comparator, generates interrupt or reset to MCU.	90		165	degC
Overtemp hysteresis		-10			degC
Temperature Sensor					
Temperature range	The MCU is in charge to pull the ADC related data from temperature sensor.	-40		150	degC
Temperature Accuracy		-10		+10	degC
Active current			20		uA
Differential Amplifier for LED VFW measurement					
Input Voltage Range (Vin)	>4V @Gain=1/4	VBAT-4		VBAT	V
	>4V @Gain=1/8	VBAT-8		VBAT	V
Output Voltage Range	Internal output range of LED Sense	0	Vin*Gain	Vref (ADC)	ms
Output Voltage Relative Error				1	%
Gain	Programmable		1/2		

Parameter	Conditions	Min.	Typ.	Max.	Unit
			or 1/4		
Wake Up					
TWAKEUP	LIN_IN/LIN_OUT, programmable	30	150	200	us
Wake Up Timer	Wakeup Time = 2^(WUT_TAPSEL)/16kHz clock WUT_SEL=0 to 15, default 0	0.0625		2048	ms
ASIC Watchdog timer					
Timeout	Programmable	0.128		16.384	s
SAR ADC					
Resolution			12		bits
Conversion Speed	16 cycles per conversion			250	ks/s
ADC Clock	System clock			4	MHz
INL	Guaranteed by design	-1		1	LSB
DNL	Guaranteed by design	-1		1	LSB
LIN EC specified with VBAT=8V to 16V – refer to LIN 2.x specification, VBUS=LIN pin/line					
Supply Voltage	supply voltage range	6	13.5	18	V
IBUS_LIM	Current Limitation for Driver dominant state driver on VBUS = VBAT=16V	40		200	mA
Rslave	Lin Slave Pullup	20	30	60	kΩ
Rmaster	Lin Master Pullup	900	1000	1100	Ω
IBUS_PAS_dom	Input Leakage Current at the Receiver including Pull-Up Resistor driver off VBUS = 0V VBAT= 12V	-1			mA
IBUS_PAS_rec	Driver off, VBUS>VBAT 8V<VBAT<16V 8V<VBUS<16V			20	uA

Parameter	Conditions	Min.	Typ.	Max.	Unit
IBUS_no_GND	Control unit disconnected from ground GND Device = VSUP 0V<VBUS<16V VBAT = 12V Loss of local ground must not affect communication in the residual network. **LIN 2.2A**	-1		+1	mA
Device Bus Leakage Current Ground Disconnected	VBAT= VGND=12V, 0V<VBUS<18V **J2602**	-100		100	uA
IBUS_no_BAT	VBAT disconnected 0<VBUS<16V, VBAT=0V **LIN 2.2A** Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.			100	uA
Device Bus Leakage current VBAT disconnected	0V<VBUS<18V, VBAT=VGND=0V **J2602**	-23		23	uA
BUS_VOL Transmitter dominant voltage	Load 500Ohms, driver open drain active	0.0		0.2	VSUP
BUS_VOH Transmitter recessive voltage	Driver open drain high impedance	0.8		1.0	VSUP
CSLAVE	LIN pin input capacitance Note that LIN 2.2A spec 220pF typ, 250pF max as total node capacitance at the connector including the physical bus driver and all other components including C_{LIN}			35	pF
VBUSdom	Receiver dominant state			0.4	VSUP
VBUSrec	Receiver recessive state	0.6			VSUP
VBUS_CNT	Center point Receiver	0.475	0.5	0.525	VSUP

Parameter	Conditions	Min.	Typ.	Max.	Unit
	VBUS_CNT =(Vth_dom+ Vth_rec)/2				
Vhys	Receiver hysteresis VHYS = Vth_rec -Vth_dom			0.175	VSUP
Trx_pd	propagation delay of receiver C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode) minimum slew rate for the LIN rising and falling edges is 50V/us			6	us
Trx_sym	symmetry of receiver propagation delay rising edge w.r.t. falling edge C_{RXD} load 20pF C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode)	-2		+2	us
LIN Timing parameters (CBUS ; RBUS): (1nF; 1kΩ) / (6.8nF;660Ω) / (10nF;500Ω)					
D1 Duty Cycle (20kbits/s)	THRec(max) = 0.744 x VSUP; THDom(max) = 0.581 x VSUP; VSUP = 7.0V...16V; tBit = 50µs; D1 = tBus_rec(min) / (2 x tBit)	0.396			-
D2 Duty Cycle (20kbits/s)	THRec(min) = 0.422 x VSUP; THDom(min) = 0.284 x VSUP; VSUP = 7.6V...16V; tBit = 50µs; D2 = tBus_rec(max) / (2 x tBit)			0.581	-
D3 Duty Cycle (10.4kbits/s)	THRec(max) = 0.778 x VSUP; THDom(max) = 0.616 x VSUP; VSUP = 7.0V...16V; tBit = 96µs; D3 = tBus_rec(min) / (2 x tBit)	0.417			-
D4 Duty Cycle (10.4kbits/s)	THRec(min) = 0.389 x VSUP; THDom(min) = 0.251 x VSUP; VSUP = 7.6V...16V; tBit = 96µs; D4 = tBus_rec(max) / (2 x tBit)			0.590	-

Parameter	Conditions	Min.	Typ.	Max.	Unit
tBus_rec(max)- tBus_dom(min)	Δt3, 10.4kbs operation, low speed mode, **J2602**			15.9	us
tBus_dom(max)- tBus_rec(min)	Δt4, 10.4kbs operation, low speed mode, **J2602**			17.28	us
GPIOs					
GPIOVIL	Input Low Voltage			0.3* VDD3P 3	V
GPIOVIH	Input High Voltage	0.7* VDDD3 P3			V
GPIOIOL	Max load current with output voltage=VOL			10	mA
GPIOIOH	Max load current with output voltage=VOLH			10	mA
GPIOVOL	Output Low Voltage			0.4	V
GPIOVOH	Output High Voltage	2.4			V
GPIOPU	Pull Up Resistance			110	kOhm
GPIOPD	Pull Down Resistance			110	kOhm
SWDCLK, SWDIO					
SWDVIL				0.8	V
SWDVIH		2			V
SWDCLKIOL	SWCLK, Max load current with output voltage=VOL			4	mA
SWDCLKIOH	SWCLK, Max load current with output voltage=VOH			4	mA
SWDIOIOL	SWDIO, Max load current with output voltage=VOL			8	mA
SWDIOIOH	SWDIO, Max load current with output voltage=VOH			8	mA
SWDVOL				0.4	V

Parameter	Conditions	Min.	Typ.	Max.	Unit
SWDVOH		2.4			V
SWDPU (SWDIO IO)	Pull Up Resistance	22		110	kOhm
SWDPD (SWDCLK IO)	Pull Down Resistance	22		110	kOhm
SWDVIL				0.8	V

Electrical Characteristics are valid over the full temperature range of Tj = -40°C to +125°C and a supply range of 6V ≤ VBAT ≤ 18V unless otherwise noted.

The figure below shows the relation between the propagation delay, the TX thresholds and associated receiver duty cycles. Refer to D1 to D4 duty cycles in the table above for THRec and THDom threshold levels.

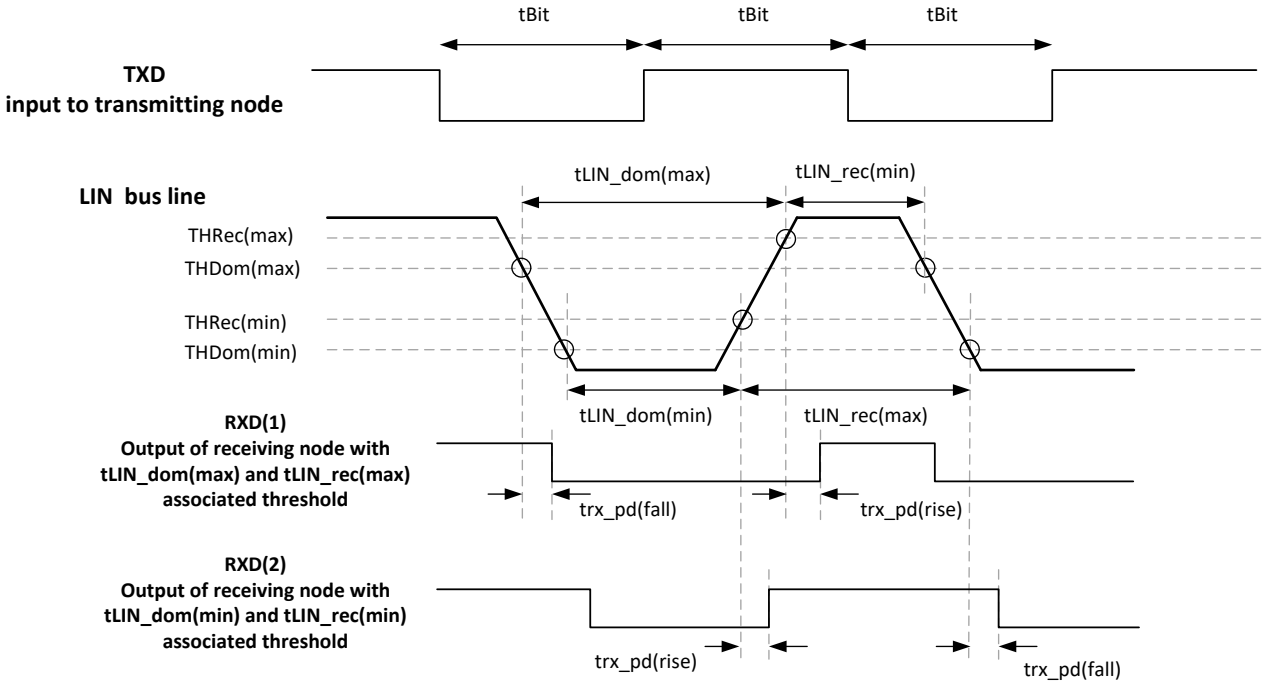


Figure 8 LIN timing Diagram

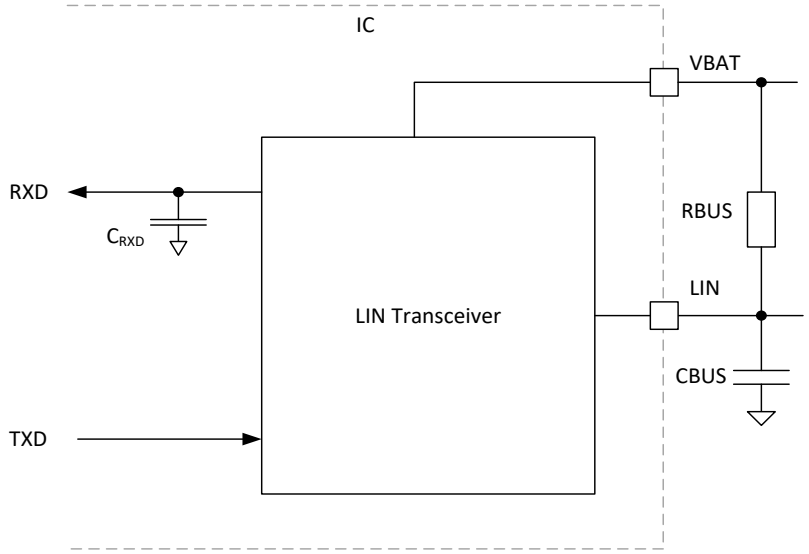


Figure 9 LIN AC Test Circuit

7.3 CURRENT CONSUMPTION (TBD)

Table 6 Current Consumption

Mode	Conditions	Min.	Typ.	Max.	Unit
Normal	Ta=85C, VBAT=18V, RCO=16MHz, full functionality: MCU running, no flash write, LED OFF, ADC ON, VBAT and TEMP monitor ON, WDT ON.			1.71	mA
DeepSleep	All regulators (5V, 3.3V,1.5V) ON, 1.5V regulator is in low power mode, MCU OFF, Load dump protection active. Ta=85degC max, VBAT=13.5V Overvoltage/Undervoltage detection, PWM, LED driver, Tempsensor and ADC are OFF except one LIN RX on and GPIO toggling and wake up timer.	45	52	60	uA
Hibernate	Main regulator (5V) ON, 3.3V/1.5V regulators OFF, IO Voltage regulator & Core Voltage regulater off, Load dump protection active. Ta=85degC max, VBAT=13.5V VBAT Overvoltage/Undervoltage detection, Only LIN Wakeup monitor active.	35	40	45	uA

8 MEMORY/REGISTER DESCRIPTION

8.1 TOP LEVEL MEMORY MAP

The chip uses a unified memory model with a linear address space (Von Neumann architecture) including Flash and RAM memories as well as registers address space. The implementation of the Cortex M0 core uses a high density 48KB Flash cell along with 8KB of SRAM.

Table 7 Top Level Memory Map

Address	**Memory**	**Description**
0x00000000–0x0000BFFF	Flash	48Kbytes of Flash Memory, user programmable.
0x0000C000 – 0x1FFFFFFF	N/A	Reserved
0x20000000 – 0x20001FFF	SRAM	8 Kbytes of SRAM
0x20002000 – 0x4FFFFFFF	N/A	Reserved
0x50000000 - 0x500003FF	CRGA	Clock & Reset Generator
0x50000400 - 0x500007FF	PMUA	Power Management Unit
0x50000800 - 0x500008FF	SYSCTRLA	System configuration and retention memory
0x50000900 - 0x500009FF	TRIMHV	Trim bits & Control bits in 5V power domain
0x50000C00 - 0x50000FFF	IOCTRLA	I/O configuration and DFT pin control
0x50001000 - 0x500013FF	WICA	WakeUp Interrupt Controller
0x50001400 - 0x500017FF	WDTA	Watchdog Timer Registers
0x50004400 - 0x500047FF	GPIO	GPIO bit control and configuration

0x50010000 - 0x500107FF	PWM	Control (and status) registers for the pulse width modulation waveform generator.
0x50010800 - 0x50010BFF	PWM_AUX	Control (and status) registers for the pulse width modulation waveform generator.
0x50010C00 - 0x50010FFF	LINM	LIN master interface registers
0x50011C00 - 0x50011FFF	LINS	LIN slave interface registers
0x50013000 - 0x500133FF	EVTHOLD	Event Hold Control
0x50013400 - 0x500137FF	SAR_CTRL	SAR ADC Interface registers
0x50015000 - 0x500153FF	SPI	SPIM Interface registers
0x50015400 - 0x500157FF	UART0	UART Interface registers
0x50020000 - 0x50020FFF	SYSCFG	System Configuration Located in Power Down Domain.
0x50021000 - 0x50021FFF	FLASH	Control (and status) registers for FMC
0x50022000 - 0x50022007	TIMER0	General purpose timer 0 registers
0x50022008 - 0x5002200F	TIMER1	General purpose timer 1 registers
0x50022010 - 0x50022017	TIMER2	General purpose timer 2 registers
0x50022018 - 0x5002201F	WDT1	The watchdog timer that is local to VERNE MCU
0x50022100 - 0x5002210F	CRC	CRC32 Registers.
0x50022110 – 0xDFFFFFFF	N/A	Reserved
0xE0000000 – 0xE00FFFFF	Private peripheral bus	ARM peripherals
0xE0100000 – 0xEFFFFFFF	N/A	Reserved
0xF0000000 – 0xF0001FFF	System ROM tables	ARM core IDs

0xF0002000 – 0xFFFFFFFF	N/A	Reserved

8.2 REGISTER MAP

Peripherals List		
Address	**Peripheral**	**Description**
0x50000000 - 0x500003FF	CRGA	Clock & Reset Generator
0x50000400 - 0x500007FF	PMUA	Power Management Unit
0x50000800 - 0x500008FF	SYSCTRLA	System configuration and retention memory
0x50000900 - 0x500009FF	TRIMHV	Trim bits & Control bits in 5V power domain
0x50000C00 - 0x50000FFF	IOCTRLA	I/O configuration and DFT pin control
0x50001000 - 0x500013FF	WICA	WakeUp Interrupt Controller
0x50001400 - 0x500017FF	WDTA	Watchdog Timer Registers
0x50004400 - 0x500047FF	GPIO	GPIO bit control and configuration
0x50010000 - 0x500107FF	PWM	Control (and status) registers for the pulse width modulation waveform generator.
0x50010800 - 0x50010BFF	PWM_AUX	Control (and status) registers for the pulse width modulation waveform generator.
0x50010C00 - 0x50010FFF	LINM	LIN master interface registers
0x50011C00 - 0x50011FFF	LINS	LIN slave interface registers
0x50013000 - 0x500133FF	EVTHOLD	Event Hold Control
0x50013400 - 0x500137FF	SAR_CTRL	SAR ADC Interface registers
0x50015000 - 0x500153FF	SPI	SPIM Interface registers
0x50015400 - 0x500157FF	UART0	UART Interface registers
0x50020000 - 0x50020FFF	SYSCFG	System Configuration Located in Power Down Domain.
0x50021000 - 0x50021FFF	FLASH	Control (and status) registers for FMC
0x50022000 - 0x50022007	TIMER0	General purpose timer 0 registers
0x50022008 - 0x5002200F	TIMER1	General purpose timer 1 registers
0x50022010 - 0x50022017	TIMER2	General purpose timer 2 registers
0x50022018 - 0x5002201F	WDT1	The watchdog timer that is local to VERNE MCU
0x50022100 - 0x5002210F	CRC	CRC32 Registers.

8.2.1 CRGA

CRGA		
Address	**Register**	**Description**
0x50000000	LFCLKCTRL	Low frequency clock control
0x50000004	SYSCLKCTRL	System clock control
0x50000008	RESETCTRL	Reset control
0x5000000C	MODUCLKSTOP	Module Clock Stop
0x50000010	MODUSLEEPEN	Module Clock Enable in CPU Sleep Mode
0x50000014	MODUDEEPSLEEPEN	Module Clock Enable in CPU Deep Sleep Mode
0x50000018	MODULERST	Module Reset control
0x5000001C	WDTACTION	Watchdog action
0x50000020	LFCLKKILL	Low frequency clock kill
0x50000024	OVTEMPACTION	OVTEMP action

0x50000028	OVUVACTION	OVUV action
0x5000002C	SWDCTRL	Swd debug control

8.2.1.1 LFCLKCTRL

0x50000000																													
LFCLKCTRL																													
Low frequency clock control.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8				-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	DIVLFCLK	Low Frequency Clock div select. Select the divider ratio on the low Frequency clock when using slow oscillator. Divider ratio is (DIV_LFCLK + 1)	4	rw	0xF
F0	LFRCSTS	Slow oscillator status. Will be high when the Low Frequency oscillator is selected	1	ro	0x0

8.2.1.2 SYSCLKCTRL

0x50000004																													
SYSCLKCTRL																													
System clock control.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F26			-	F24	-	-	F20		-	F16			-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F26	CLKSOFTSTRTDLY	Define the duration of cycles of each divider ratio when soft starting. ***NOTE:****Fast clock must have been enabled (HF_RC_ENA) when change this field.* *0x0: 2 divided clock* *0x1: 4 divided clock* *0x2: 8 divided clock* *0x3: 16 divided clock* *0x4: 32 divided clock* *0x5: 64 divided clock* *0x6: 128 divided clock* *0x7: 256 divided clock*	3	rw	0x4
F24	CLKSOFTSTRTEN	Enable Clock Soft Starter when change SYSCLKSEL from 0 to 1 for switching to fast clock. When enabled, soft starter will start the clock divider with the maximum divider ratio. And decrease divider ratio by one after staying for predefined number of cycles defined in register field CLKSOFTSTRTDLY. This operation will stop when divider ratio is equal with DIVSYSCLK. ***NOTE:****Fast clock must have been enabled (HF_RC_ENA) when change this field.*	1	rw	0x1
F20	HF_RC_LDO_VSEL	16MHz RC OSC (HF Oscillator) LDO output select. 0x0: 1V45 Selected 0x1: 1V50 Selected 0x2: 1V55 Selected 0x3: 1V65 Selected	2	rw	0x1
F16	DIVSYSCLK	Clock div select. Select the divider ratio on the system clock when using fast oscillator. 0x0: No Division. Full Clock speed. 0x1: Div by 2. 0x2: Div by 3. 0x3: Div by 4. 0x4: Div by 5. 0x5: Div by 6. 0x6: Div by 7. 0x7: Div by 8.	3	rw	0x0

F9	SELFASTCLK	high frequency oscillator unselect, must be 0x0	1	rw	0x0
F8	SYSCLKSEL	System clock select. Used to switch between the fast and slow system clocks ***NOTE:*** *This bit will be set by hardware after normal POR.*0x0: Slow clock 0x1: Fast clock	1	rw	0x0
F1	HFRCSTS	Fast oscillator status. Will be high when High Frequency oscillator is enabled or fast clock is selected as system clock	1	ro	0x0
F0	HFRCENA	HF oscillator enable. Setting this bit when the High Frequency oscillator is not running will cause the oscillator to start (the PMU may have already started it). This bit is cleared automatically on entering DeepSleep or Hibernate mode ***NOTE1:*** *This bit will be set by hardware after normal POR.* ***NOTE2:****HF oscillator will be stable in 60us after enabled. It is recommended switch to this clock source after it is stable.*	1	rw	0x0

8.2.1.3 RESETCTRL

0x50000008								**RESETCTRL**																					
Reset control.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	F14	F13	-	F11	-	F9	F8	-	F6	F5	-	F3	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	SOFTRSTREQ	Soft reset request. Set to trigger a soft reset of chip. Reset all modules in PDLV domain and LINS module Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F16	HARDRSTREQ	Hard reset request. Set to trigger a hard reset of chip	1	wo	0x0
F14	OVTEMPFLAGCLR	OVTEMP flag clear. Set to clear the OVTEMP flag	1	wo	0x0
F13	WDTFLAGCLR	WDT flag clear. Set to clear the WDT flag	1	wo	0x0
F11	UVFLAGCLR	UV flag clear. Set to clear the UV flag	1	wo	0x0
F9	OVFLAGCLR	OV flag clear. Set to clear the OV flag	1	wo	0x0
F8	PORFLAGCLR	POR flag clear. Set to clear the POR flag	1	wo	0x0
F6	OVTEMPFLAG	Over Temp Violation flag. Set by the hardware when the over temp condition is detected.	1	ro	N/A
F5	WDTFLAG	Watchdog bark flag. Set by the hardware when the watchdog barks.	1	ro	N/A
F3	UVFLAG	Under Voltage Monitor flag. Set by the hardware when the under voltage monitor.	1	ro	N/A
F1	OVFLAG	Over Voltage Monitor flag. Set by the hardware when the over voltage monitor.	1	ro	N/A
F0	PORFLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	N/A

8.2.1.4 MODUCLKSTOP

0x5000000C								**MODUCLKSTOP**																					
Module Clock Stop.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	CRC_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid. N.A. in realplum-hp.	1	rw	0x0

F6	PWM_AUX_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F5	UART_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F4	SPI_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F3	LINS_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F2	LINM_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F1	PWM_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0
F0	ADC_STOP	Force to stop the clock of the module, 1: stop is valid; 0: stop is invalid	1	rw	0x0

8.2.1.5 MODUSLEEPEN

0x50000010		MODUSLEEPEN			
Module Clock Enable in CPU Sleep Mode.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - - - - - F15 - - - - - - - F7 F6 F5 F4 F3 F2 F1 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F15	FLASH_SLEEP_EN	Flash Clock Enable in CPU Sleep Mode. Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid. N.A. in realplum-hp.	1	rw	0x1
F7	CRC_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid. N.A. in realplum-hp.	1	rw	0x1
F6	PWM_AUX_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F5	UART_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F4	SPI_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F3	LINS_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F2	LINM_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F1	PWM_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F0	ADC_SLEEP_EN	Gate the module clock when CPU has entered sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1

8.2.1.6 MODUDEEPSLEEPEN

0x50000014		MODUDEEPSLEEPEN			
Module Clock Enable in CPU Deep Sleep Mode.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - - - - - F15 - - - - - - - F7 F6 F5 F4 F3 F2 F1 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F15	FLASH_DEEPSLEEP_EN	Flash Clock Enable in CPU Deep Sleep Mode. Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid. N.A. in realplum-hp	1	rw	0x1

F7	CRC_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid. N.A. in realplum-hp.	1	rw	0x1
F6	PWM_AUX_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F5	UART_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F4	SPI_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F3	LINS_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F2	LINM_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F1	PWM_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1
F0	ADC_DEEPSLEEP_EN	Gate the module clock when CPU has entered deep sleep, 1: gate is valid; 0: gate is invalid	1	rw	0x1

8.2.1.7 MODULERST

0x50000018	**MODULERST**				
Module Reset control.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	MODULE_RST_REQ	Module Soft reset request. Set to trigger a soft reset of module below. 0x1: ADC Soft reset request 0x2: PWM Soft reset request 0x4: LIN Master soft reset request 0x8: LIN Slave soft reset request 0x10: SPIM soft reset request 0x20: UART soft reset request 0x40: CRC soft reset request 0x80: PWM_AUX soft reset request Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	8	wo	0x0

8.2.1.8 WDTACTION

0x5000001C	**WDTACTION**				
Watchdog action.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	WDTACTION	Watchdog action. Defines the consequences of watchdog bark being detected by the hardware. 0x0: IRQ generated 0x1: Hard reset generated	1	rw	0x1

8.2.1.9 LFCLKKILL

0x50000020	**LFCLKKILL**
Low frequency clock kill.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	KEEPWDTCLKDS	Keep WDT clock in Deepsleep. Set to keep WDT clock running in deepsleep mode.	1	rw	0x0
F0	KILLLFRC	Kill slow RC oscillator. Setting this bit gates the low frequency RC oscillator input	1	rw	0x0

8.2.1.10 OVTEMPACTION

0x50000024 **OVTEMPACTION**

OVTEMP action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F31	OVTEMP_LOCK	Set Only bit. Set this bit to lock OVTEMP related bits.	1	rw	0x0
F24	OVERTEMP_EN	OverTemp Monitor Enable bit.	1	rw	0x0
F0	OVTEMP	Over Temperature action. Defines the consequences of over temp condition detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x2

8.2.1.11 OVUVACTION

0x50000028 **OVUVACTION**

OVUV action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	F27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	UV_LOCK	Set Only bit. Set this bit to lock UV_ACTION related bits.	1	rw	0x0
F27	OV_LOCK	Set Only bit. Set this bit to lock OV_ACTION related bits.	1	rw	0x0
F4	UV_ACTION	Under Voltage action. Defines the consequences of under voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1
F0	OV_ACTION	Over Voltage action. Defines the consequences of over voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1

8.2.1.12 SWDCTRL

0x5000002C **SWDCTRL**

Swd debug control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	SWDFLAGCLR	SWD Wakeup flag clear. Set to clear the SWD Wakeup flag	1	wo	0x0
F16	SWDFLAG	SWD wakeup flag. Set by the hardware when chip is awakened by SWD from deepsleep mode and clear through SWDFLAGCLR.	1	ro	N/A

F8	CRSTEXTCLR	M0 core extend reset clear. clear M0 core extend reset	1	wo	0x0
F1	CRSTEXTFLAG	M0 core extend reset flag. Set by the hardware when: 1) both CRSTEXTENA and SWDFLAG are high; or 2) SWCLK is high when power up or exit from hibernate or exit from deepsleep. Clear through CRSTEXTCLR. CPU core will hold in reset state until this bit is cleared.	1	ro	N/A
F0	CRSTEXTENA	M0 core extend reset enable. enable M0 core extented reset when chip is awakened by SWD from deepsleep mode	1	rw	0x1

8.2.2 PMUA

PMUA		
Address	**Register**	**Description**
0x50000400	CTRL	Control
0x50000404	DWELL	Dwell
0x50000408	VBATCTRL	VBAT Monitor Register
0x5000040C	VBATDBNC	VBAT Debounce Register
0x50000410	VBATDBNCTHRES	VBAT Monitor Threshold Register
0x50000414	PMUIRQ	Voltage Monitor interrupts

8.2.2.1 CTRL

0x50000400																													
CTRL																													
Control.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	DBG_OT_COMP	Enable to test the comparator of over temperature function.	1	rw	0x0
F6	DBG_IPRE	EN test IBIAS_PRE 1uA current.	1	rw	0x0
F5	DBG_1P3V	LDO_1V5 output 1.35V, Set to 1V5-LDO output 1V35.	1	rw	0x0
F3	IGNORE_CIFS	Ignore QACKs. Setting a bit in this register prevents PMUA from waiting for the assertion of the corresponding 'Quiescent State Acknowlege' signal when before transitioning towards the Hibernate state.	1	rw	0x0
F2	BG_OK	the flag of bandgap OK. the flag of bandgap OK	1	ro	N/A
F1	FASTBOOT	Fast boot. Set to enable used of the fast clock during subsequent power-up sequences (including the portion consumed by the Clough boot sequence). The set value brings the system up with the slow clock to make the initial boot and any boot after a hard reset (e.g. after a brownout) as safe as possible.	1	rw	0x1
F0	HIBERNATE	Hibernate. Set to put the chip into HIBERATE mode. Before setting this bit, ensure that wake interrupt controller HOLD bit has been set (and that a corresponding Lullaby interrupt has been received).	1	wo	0x0

8.2.2.2 DWELL

0x50000404	**DWELL**
Dwell NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY = 0x0E'.	

Minimum times spent in various PMUA states. Please Note- The STARTUP_BIAS_DWELL state timeout is hardcoded to a value of 0xC. A value of 0xC in the STARTUP_BIAS_DWELL state @ 16KHz yields a delay of 1.5 milliseconds

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F12	POWER_DOWN_MCU	Power down MCU dwell time. Defines the amount of time spent in the 'Power down MCU' state. Pausing here allows the MCU supplies to discharge (to guarantee subsequent POR)	4	rw	0x4
F8	ATTACH_3V3	Attach 3.3V dwell time. Defines the amount of time spent in the 'Attach 3V3' state. State Attaches 3.3V to MCU.	4	rw	0x4
F4	ATTACH_1V5	Attach 1.5V dwell time. Defines the amount of time spent in the 'Attach 1V5' state. State Attaches 1.5V to MCU.	4	rw	0x8
F0	ENABLE_1V5	Enable 1.5V dwell time. Defines the amount of time spent in the 'Enable 1V5' state. Allows 3v3 and 1v5 regs to settle	4	rw	0x4

8.2.2.3 VBATCTRL

0x50000408 **VBATCTRL**

VBAT Monitor Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	-	-

#	Field Name	Field Description	Width	Access	Reset
F27	HIGH_DBNC	Battery Voltage High Status after deboucing. Battery monitor over voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F26	LOW_DBNC	Battery Voltage Low Status after debouncing. Battery monitor under voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F25	HIGH	Battery Voltage High Status. RAW battery monitor over voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F24	LOW	Battery Voltage Low Status. RAW battery monitor under voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F3	OV_POL	Battery Voltage Monitor Over Voltage Interrupt Event Polarity. Flips the over voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F2	UV_POL	Battery Voltage Monitor Under Voltage Interrupt Event Polarity. Flips the under voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0

8.2.2.4 VBATDBNC

0x5000040C **VBATDBNC**

VBAT Debounce Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F5	OVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of OV event.	1	rw	0x0

F4	OVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of OV.	1	rw	0x1
F3	UVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of UV event.	1	rw	0x0
F2	UVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of UV.	1	rw	0x1
F1	OV	over voltage signal debounce enable. if set to '1, debounces the over voltage signal before going to over voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1
F0	UV	under voltage signal debounce enable. if set to '1, debounces the under voltage signal before going to under voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1

8.2.2.5 VBATDBNCTHRES

0x50000410		VBATDBNCTHRES			
VBAT Monitor Threshold Register.					
31 30 29 28 27 26 25 24		23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
F24		F16	F8	F0	
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F24	OVTHRES0	Over Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the over voltage event going from 1 to 0. It will require the ov event to stay high for the (OVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F16	UVTHRES0	Under Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the under voltage event going from 1 to 0. It will require the uv event to stay high for the (UVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F8	OVTHRES1	Over Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the over voltage event going from 0 to 1. It will require the ov event to stay high for the (OVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1
F0	UVTHRES1	Under Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the under voltage event going from 0 to 1. It will require the uv event to stay high for the (UVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1

8.2.2.6 PMUIRQ

0x50000414		PMUIRQ			
Voltage Monitor interrupts. Contains the the enable, clear, status and active flag for the Battery Voltage interrupt sources.					
31 30 29 28 27 26 25 24		23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
- - - - - - F25 F24		- - - - - - F17 F16	- - - - - - F9 F8	- - - - - - F1 F0	
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F25	OV_ACT	over voltage interrupt active.	1	ro	0x0
F24	UV_ACT	under voltage interrupt active.	1	ro	0x0
F17	OV_STS	over voltage interrupt status.	1	ro	0x0
F16	UV_STS	under voltage interrupt status.	1	ro	0x0

F9	OV_CLR	over voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	UV_CLR	under voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	OV_ENA	over voltage interrupt enable.	1	rw	0x0
F0	UV_ENA	under voltage interrupt enable.	1	rw	0x0

8.2.3 SYSCTRLA

SYSCTRLA		
Address	**Register**	**Description**
0x50000800	RETAIN1	Retained data 1
0x50000804	DEBUG_ACCESS_KEY	Debug access key
0x50000808	DEBUG_ACCESS_ENABLED	Debug access enabled
0x5000080C	TRIM_ACCESS_KEY	Trim access key
0x50000810	TRIM_ACCESS_ENABLED	Trim access enabled
0x50000814	PMU_ACCESS_KEY	PMU configure access key
0x50000818	PMU_ACCESS_ENABLED	PMU configure access enabled
0x5000081C	HF_OSC_TRIM	Trim controls for the high frequency (16MHz) oscillator
0x50000824	BIAS	Bias Control
0x50000828	TRIMLEDBIAS	LED bias current Trim
0x5000082C	TRIMLED0	High Voltage LED trim
0x50000830	TRIMLED1	High Voltage LED trim
0x50000834	TRIMLED2	High Voltage LED trim
0x50000838	TRIMVFW	VFW Current Trim
0x5000083C	DFTCODE	DFT Unlock Code
0x50000840	DFT_ACCESS_ENABLED	DFT access enabled
0x50000844	DFTTESTMODESTART	DFT Mode Start
0x50000848	NAME	ASIC name
0x5000084C	REV	Silicon Revision

8.2.3.1 RETAIN1

0x50000800								**RETAIN1**																					
Retained data 1.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN1	Firmware scratch register 1 (0x1). Contents retained in Deepsleep mode - but lost after hibernate mode and hard reset.	16	rw	0x0

8.2.3.2 DEBUG_ACCESS_KEY

0x50000804								**DEBUG_ACCESS_KEY**																					
Debug access key.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		
#	**Field Name**																								**Field Description**			**Width**	**Access**	**Reset**
F31	DEBUG_LOCK																								Set Only bit. Set this bit to lock DEBUG_CODE bits.			1	rw	0x0
F0	DEBUG_ACCESS_KEY																								Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.			4	rw	0x0

8.2.3.3 DEBUG_ACCESS_ENABLED

0x50000808													**DEBUG_ACCESS_ENABLED**																	
Debug access enabled.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0
#	**Field Name**																								**Field Description**				**Width**	**Access**	**Reset**
F0	DEBUG_ACCESS_ENABLED																								A status flag that is set when debug access is enabled				1	ro	0x0

8.2.3.4 TRIM_ACCESS_KEY

0x5000080C													**TRIM_ACCESS_KEY**																	
Trim access key.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			
#	**Field Name**																								**Field Description**				**Width**	**Access**	**Reset**
F31	TRIM_LOCK																								Set Only bit. Write 1 to this bit to lock TRIM_CODE bits.				1	rw	0x0
F0	TRIM_ACCESS_KEY																								Write the value 0xe to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.				4	rw	0x0

8.2.3.5 TRIM_ACCESS_ENABLED

0x50000810													**TRIM_ACCESS_ENABLED**																	
Trim access enabled.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0
#	**Field Name**																								**Field Description**				**Width**	**Access**	**Reset**
F0	TRIM_ACCESS_ENABLED																								A status flag that is set when trim access is enabled				1	ro	0x0

8.2.3.6 PMU_ACCESS_KEY

0x50000814													**PMU_ACCESS_KEY**																	
PMU configure access key.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			
#	**Field Name**																								**Field Description**				**Width**	**Access**	**Reset**
F31	PMU_LOCK																								Set Only bit. Set this bit to lock PMU_CODE bits.				1	rw	0x0
F0	PMU_ACCESS_KEY																								Write the value 0xA to this register to enable 1v5 domain at hibernate. Write any other value to disable the 1v5 domain at hibernate.				4	rw	0x0

8.2.3.7 PMU_ACCESS_ENABLED

0x50000818																	PMU_ACCESS_ENABLED															
PMU configure access enabled.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	PMU_ACCESS_ENABLED	A status flag that is set when pmu access is enabled	1	ro	0x0

8.2.3.8 HF_OSC_TRIM

0x5000081C																	HF_OSC_TRIM															
Trim controls for the high frequency (16MHz) oscillator.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F16								-	-	-	-	F9			F8	F0							

#	Field Name	Field Description	Width	Access	Reset
F16	SSCDIV	SSC Clock Divider. SSC Freq = SYS_FREQ/[(SSC_DIV+1)*(SSC_DEEP+1)*4].	8	rw	0x28
F9	SSCDEEP	SSC Depth Configuration.	3	rw	0x0
F8	SSCENA	SSC Enable.	1	rw	0x0
F0	TRIM_HF_RC	High Frequency RC Oscillator trim. TRIM bits will be changed if SSC is enabled. Reload the trim bits from Flash should be executed by software if SSC is disabled from enable state. Following value only used as a reference: 0x0: freq= 9MHz 0xa7: freq=16MHz 0xff: freq=35MHz	8	rw	0xA7

8.2.3.9 BIAS

0x50000824																	BIAS															
Bias Control.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F1	LEDBIASREG	High Voltage LED bias select register. If LED_BIAS_SEL is set, then LED_BIAS_REG allows override access to the LED BIAS signal.	1	rw	0x0
F0	LEDBIASSEL	High Voltage LED bias select. 0x0: The LED Bias is enabled and disabled by the pmu hardware state machine by default. 0x1: The value of the LED_BIAS_REG field is what is used to drive the LED_BIAS signal. (override mode)	1	rw	0x0

8.2.3.10 TRIMLEDBIAS

0x50000828																	TRIMLEDBIAS															
LED bias current Trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	LEDBIASTRIM	LED bias current trim. each code is about 50nA step.wirte trim key	8	rw	0x80

8.2.3.11 TRIMLED0

0x5000082C																TRIMLED0															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM0	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.3.12 TRIMLED1

0x50000830																TRIMLED1															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM1	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.3.13 TRIMLED2

0x50000834																TRIMLED2															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM2	LED trim (120uA step; max about 60mA).	9	rw	0x1F4

8.2.3.14 TRIMVFW

0x50000838																TRIMVFW															
VFW Current Trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TRIMVFW	PN Forward Voltage Current trim (10uA step max about 2.56mA).	8	rw	0xC8

8.2.3.15 DFTCODE

0x5000083C																DFTCODE															
DFT Unlock Code.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	DFT_LOCK	Set Only bit. Write 1 to this bit to lock DFT related config bits.	1	rw	0x0

F0	DFTCODE	Test Mode Unlock Enable Code. 0x1C needs to be written to this register to unlock the DFT_TESTMODE_SEL and DFT_TESTMODE_START registers.	8	wo	0x0

8.2.3.16 DFT_ACCESS_ENABLED

0x50000840								DFT_ACCESS_ENABLED																							
DFT access enabled.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DFT_ACCESS_ENABLED	A status flag that is set when DFT access is enabled.	1	ro	0x0

8.2.3.17 DFTTESTMODESTART

0x50000844								DFTTESTMODESTART																							
DFT Mode Start.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F3	SRAMBISTMODESTART	Puts chip into sram bist mode.	1	wo	0x0
F2	FLASHOSCTESTMODESTART	Puts chip into flash oscillator test mode.	1	wo	0x0
F1	FLASHTESTMODESTART	Puts chip into flash test mode.	1	wo	0x0

8.2.3.18 NAME

0x50000848								NAME																							
ASIC name.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	NAME	ASIC name. A read from this register will return the Chip name	32	ro	N/A

8.2.3.19 REV

0x5000084C								REV																							
Silicon Revision.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	REV	Silicon Revision. A read from this register will return the ASCII silicon revision (e.g. ASCII A0 is 0x4130)	16	ro	N/A

8.2.4 TRIMHV

TRIMHV		
Address	**Register**	**Description**
0x50000900	RETAIN0	Retained data 0
0x50000904	CFG_ACCESS	5V domain's configuration regs access
0x50000908	LIN_SLEEP_GF	LINS Glitch Filter Configuration in active mode.
0x5000090C	LIN_WUP	LIN Wakeup Control,
0x50000910	LINS	LIN slave Pin Control.
0x50000914	LINM	LIN Master Pin Control.
0x50000918	OVTEMP_CONFIG	OVTEMP configuration.
0x5000091C	PMU_CTRL	PMU Control.
0x50000920	PMU_TRIM	PMU Trim Register.
0x50000924	VBATTRIM	VBAT Monitor Trim Register.
0x50000928	DBGCTRL	PMU Debug Control.
0x5000092C	BOR	BOR configuration
0x50000930	BORDEGLITCH	BOR Deglitch.
0x50000934	CLK_CTRL	Clock controls for 5V(always on) domain.
0x50000938	DFT	DFT

8.2.4.1 RETAIN0

0x50000900																RETAIN0															
Retained data 0.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN0	Firmware scratch register 0. Only reset at power-on (e.g contents retained in Hibernate mode and retained despite any hard or soft resets)	16	rw	0x0

8.2.4.2 CFG_ACCESS

0x50000904																								CFG_ACCESS							
5V domain's configuration regs access.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	CFG_LOCK	Set Only bit. Write 1 to this bit to lock CFG_CODE bits.	1	rw	0x0
F4	CFG_ACCESS_ENABLED	A status flag that is set when 5V domain's configuration regs access is enabled	1	ro	0x0
F0	CFG_ACCESS_KEY	Write the value 0xB to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.	4	rw	0x0

8.2.4.3 LIN_SLEEP_GF

0x50000908	LIN_SLEEP_GF

LINS Glitch Filter Configuration in active mode.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F28				F24				-	-	-	-	-	-	-	F16	F12				F8				-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F28	LINM_SLEEP_GF_THRES1	LINM RXD glitch filter threshold for 0 to 1, detect '1' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x0
F24	LINM_SLEEP_GF_THRES0	LINM RXD glitch filter threshold for 1 to 0, detect '0' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x1
F16	LINM_RXD_HIGH_RST_ENA	Enable signal that LINs RXD glitch filter at sleep mode is asynchronous reset by high of LINs_RXD.	1	rw	0x0
F12	LINS_SLEEP_GF_THRES1	LINS RXD glitch filter threshold for 0 to 1, detect '1' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x0
F8	LINS_SLEEP_GF_THRES0	LINS RXD glitch filter threshold for 1 to 0, detect '0' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x1
F0	LINS_RXD_HIGH_RST_ENA	Enable signal that LINs RXD glitch filter at sleep mode is asynchronous reset by high of LINs_RXD.	1	rw	0x0

8.2.4.4 LIN_WUP

0x5000090C **LIN_WUP**

LIN Wakeup Control,
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F24		F18						-	-	-	-	-	-	F11	F10	F8		F2						F1	F0

#	Field Name	Field Description	Width	Access	Reset
F27	LINM_BUS_IDLE_TO_DOMN	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear this bit. LIN Master's pullup will be disabled when it is set.	1	ro	0x0
F26	LINM_BUS_DOMN_RLS_WUP_ENA	LIN Master Bus Dominant Release Wakeup Enable. Set to trigger lin wakeup if bus dominant condition is released after BUS_IDLE_TIMEOUT_DOMINANT is detected.	1	rw	0x0
F24	LINM_BUS_INACTIVE	LIN Master Bus Inactivity Time. NOTE: When the chip uses the LINs bus idle detection in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	2	rw	0x0
F18	LINM_WUP_DETECT_THRES	LIN Master Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. For instace, if target threshold is 150us@LF_CLK_PREDIV=250KHz, WUP_DETECT_THRES = 150/(1000/250)-1. NOTE: When the chip uses the LINs wakeup logic in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	6	rw	0x24
F11	LINS_BUS_IDLE_TO_DOMN	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear this bit. LIN Slave's pullup will be disabled when it is set.	1	ro	0x0
F10	LINS_BUS_DOMN_RLS_WUP_ENA	LIN Slave Bus Dominant Release Wakeup Enable. Set to trigger lin wakeup if bus dominant condition is released after BUS_IDLE_TIMEOUT_DOMINANT is detected.	1	rw	0x0
F8	LINS_BUS_INACTIVE	LIN Slave Bus Inactivity Time. NOTE: When the chip uses the LINs bus idle detection in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the	2	rw	0x0

		write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE			
F2	LINS_WUP_DETECT_THRES	LIN Slave Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. For instace, if target threshold is 150us@LF_CLK_PREDIV=250KHz, WUP_DETECT_THRES = 150/(1000/250)-1. NOTE: When the chip uses the LINs wakeup logic in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	6	rw	0x24
F1	LINM_WUP_ENA	LIN Master Wakeup Enable. it enables the detect of a wakeup signal on the LIN_OUT bus	1	rw	0x1
F0	LINS_WUP_ENA	LIN Slave Wakeup Enable. it enables the detect of a wakeup signal on the LIN_IN bus	1	rw	0x1

8.2.4.5 LINS

0x50000910 **LINS**

LIN slave Pin Control.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	F16				F13				F10				F8		-	F6	F5	F4	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	SWON_LOCK	SWON Lock Bit.	1	rw	0x0
F16	LIN_TX_S_SL	LIN Slave TX driver slew rate select. Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF. 0000 -> 1110: 1.07V/us ~ 4.71V/us, step is about 0.26V/us 1111: about 10V/us for fast LIN mode	4	rw	0x4
F13	LIN_TX_S_DT	LIN Slave duty cycle adjust. 0x0: duty cycle = 0.488 0x1: duty cycle = 0.492 0x2: duty cycle = 0.494 0x3: duty cycle = 0.495 0x4: duty cycle = 0.497 0x5: duty cycle = 0.5 0x6: duty cycle = 0.507 0x7: duty cycle = 0.529	3	rw	0x5
F10	LINS_TX_BIAS_BOOST	LIN Slave IO TX Bias select. Select LIN IO TX Pull Down Current. 0x0: ~61 mA 0x1: ~83 mA 0x2: ~105 mA 0x3: ~126 mA	3	rw	0x4
F8	LINS_RX_BIAS_BOOST	adjust rise delay from LIN_IN to Input of LINS Controller. 0x0: 2.323 us 0x1: 1.344 us 0x2: 0.968 us 0x3: 0.767 us	2	rw	0x0
F6	LINS_PUOFF_TIMEOUT	LINS Pullup Disable in dominant TimeOut condition. Set to disable LINS 30K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence.	1	rw	0x1
F5	SWOFF_TIMEOUT	Switch off in dominant TimeOut condition. Set to disconnect lin switch in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LIN Switch will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence.	1	rw	0x1

F4	SWON	LIN Dual Mode Switch On. Set to enable dual-mode lin switch. Only reset by power-on sequence. This bit can be locked by setting SWON_LOCK.	1	rw	0x1
F1	LINS_RXENA	LIN receive enable.	1	rw	0x0
F0	LINS_PU30K_ENA	LIN 30K pullup enable.	1	rw	0x1

8.2.4.6 LINM

0x50000914																														
LINM																														
LIN Master Pin Control. NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F27				F24			F21			F19		-	-	-	-	-	-	-	-	-	-	-	F7	-	-	-	F3	F2	-	-

#	Field Name	Field Description	Width	Access	Reset
F27	LIN_TX_M_SL	LIN Master TX driver slew rate select. Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF. 0000 -> 1110: 1.07V/us ~ 4.71V/us, step is about 0.26V/us 1111: about 10V/us for fast LIN mode	4	rw	0x4
F24	LIN_TX_M_DT	LIN Master duty cycle adjust. 0x0: duty cycle = 0.488 0x1: duty cycle = 0.492 0x2: duty cycle = 0.494 0x3: duty cycle = 0.495 0x4: duty cycle = 0.497 0x5: duty cycle = 0.5 0x6: duty cycle = 0.507 0x7: duty cycle = 0.529	3	rw	0x5
F21	LINM_TX_BIAS_BOOST	LIN Master IO TX Bias select. Select LIN IO TX Pull Down Current. 0x0: ~61 mA 0x1: ~83 mA 0x2: ~105 mA 0x3: ~126 mA	3	rw	0x4
F19	LINM_RX_BIAS_BOOST	adjust rise delay from LIN_OUT to Input of LINM Controller. 0x0: 2.323 us 0x1: 1.344 us 0x2: 0.968 us 0x3: 0.767 us	2	rw	0x0
F7	LINM_PUOFF_TIMEOUT	LINM 1K Pullup disable in dominant TimeOut condition. Set to disable LINM 1K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS 1K Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. If this bit is set & SWON = 1, LINM's 30K pullup will be enabled for preventing bus floating. Only reset by power-on sequence.	1	rw	0x1
F3	LINM_RXENA	LIN receive enable.	1	rw	0x0
F2	LINM_PU1K_ENA	LIN 1K pullup enable.	1	rw	0x1

8.2.4.7 OVTEMP_CONFIG

0x50000918																														
OVTEMP_CONFIG																														
OVTEMP configuration. NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset

F8	TEMPSENSE_EN	enable Temp Sensor Analog Part. Set to enable Temperature Sensor analog circuit.	1	rw	0x1
F0	VTEMP_SEL	Over Temp protect threshold temp trim. Select the OVTEMP threshold level for the monitor. 0x0: Rising: 93.13-Deg; Falling: 79.13-Deg 0x1: Rising: 98.13-Deg; Falling: 84.13-Deg 0x2: Rising: 103.6-Deg; Falling: 89.13-Deg 0x3: Rising: 109.1-Deg; Falling: 94.13-Deg 0x4: Rising: 115.1-Deg; Falling: 99.63-Deg 0x5: Rising: 121.1-Deg; Falling: 105.1-Deg 0x6: Rising: 127.1-Deg; Falling: 111.1-Deg 0x7: Rising: 133.1-Deg; Falling: 117.1-Deg 0x8: Rising: 139.6-Deg; Falling: 123.1-Deg 0x9: Rising: 146.6-Deg; Falling: 129.6-Deg 0xa: Rising: 153.6-Deg; Falling: 136.1-Deg 0xb: Rising: 160.6-Deg; Falling: 142.6-Deg 0xc: Rising: 168.1-Deg; Falling: 149.6-Deg 0xd: Rising: 176.6-Deg; Falling: 157.1-Deg 0xe: Rising: 185.1-Deg; Falling: 164.6-Deg 0xf: Rising: 195.6-Deg; Falling: 172.6-Deg	4	rw	0x6

8.2.4.8 PMU_CTRL

0x5000091C **PMU_CTRL**

PMU Control.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	VDD1V5_LDO_CHOOSE	1.5V LDO Mode selection 0x0: choose Capless LDO 0x1: choose Caps LDO	1	rw	0x0
F2	OPT_EN_LP_CAPLESS	Capless 1.5V ldo low power mode, set 1 to enter low power at Deepsleep mode.	1	rw	0x1
F1	OPT_EN_LP	Set to enable of low power mode for BG_TOP at Deepsleep Mode.	1	rw	0x1
F0	PD1V5_ENA_HIBERNATE	enable of 1V5 Power Domain at Hibernate mode. set to enable the 1V5 Power Domain at Hibernate mode, this mode is defined as DEEPSLEEP mode.	1	rw	0x0

8.2.4.9 PMU_TRIM

0x50000920 **PMU_TRIM**

PMU Trim Register.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F28				F24				-	-	F16						-	-	-	F8					-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F28	OCP_CTRL_3V3	OCP trim for 3V3 LDO(default 30mA). 0x0: 10.0 mA 0x1: 12.5 mA 0x2: 15.0 mA 0x3: 17.5 mA 0x4: 20.0 mA 0x5: 22.5 mA 0x6: 25.0 mA 0x7: 27.5 mA 0x8: 30.0 mA (default)	4	rw	0x8

		0x9: 32.5 mA 0xa: 35.0 mA 0xb: 37.5 mA 0xc: 40.0 mA 0xd: 42.5 mA 0xe: 45.0 mA 0xf: 47.5 mA			
F24	OCP_CTRL_1V5	OCP trim for 1.5V LDO(default 30mA). 0x0: 20.0 mA 0x1: 22.5 mA 0x2: 25.0 mA 0x3: 27.5 mA 0x4: 30.0 mA (default) 0x5: 32.5 mA 0x6: 35.0 mA 0x7: 37.5 mA 0x8: 40.0 mA 0x9: 42.5 mA 0xa: 45.0 mA 0xb: 47.5 mA 0xc: 50.0 mA 0xd: 52.5 mA 0xe: 55.0 mA 0xf: 57.5 mA	4	rw	0x4
F16	TRIM_BG	Trim the BG core 1.21415V output voltage (1) The voltage range before trimming is 1.16797V ~ 1.26337V. (2) The trim ratio 1/1.4811. (3) The voltage is 1.21455V while TRIM_BG == 0x0. at PMU debug mode	6	rw	0x0
F8	TRIM_VREF_BUF	Trim the buffer refernce voltage include VREF_1/VREF_1P1/VREF_0P75/VREF_0P6. (1) The voltage range before trimming is 1.19825V ~ 1.237V. (2) The step is 1.25mV, and the precision of trimming is +- 0.625mV. (3) The voltage is 1.217V while TRIM_VREF_BUF == 0x0. at PMU debug mode	5	rw	0x0
F4	VDD3V3_LDO_TRIM	3.3V LDO output trim. at PMU debug mode 0x0: 3.37 V(default) 0x1: 2.98 V 0x2: 3.07 V 0x3: 3.16 V 0x4: 3.26 V 0x5: 3.49 V 0x6: 3.62 V 0x7: 3.78 V	3	rw	0x0
F0	VDD1V5_LDO_TRIM	1.5V LDO Capless output trim. at PMU debug mode 0x0: 1.452 V 0x1: 1.479 V 0x2: 1.509 V 0x3: 1.543 V(default) 0x4: 1.572 V 0x5: 1.604 V 0x6: 1.639 V 0x7: 1.679 V	3	rw	0x3

8.2.4.10 VBATTRIM

0x50000924								VBATTRIM																							
VBAT Monitor Trim Register. NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	-	-	-	-	F24		-	-	-	-	F16				-	-	-	-	-	-	F8		-	-	F0					
#	Field Name							Field Description																Width		Access			Reset		

F31	BAT_OV_EN	Battery Over Voltage Monitor Enable. Set to enable the vbat over voltage monitor analog comparator circuit.	1	rw	0x0
F30	BAT_UV_EN	Battery Under Voltage Monitor Enable. Set to enable the vbat under voltage monitor analog comparator circuit.	1	rw	0x0
F24	OVHYS	Battery Voltage Monitor Over Voltage Hysterisis Select. Selects the hysterisis level for the Over Voltage monitor. 0x0: 0.359V 0x1: 0.720V 0x2: 1.080V 0x3: 1.440V	2	rw	0x1
F16	OVLEVEL	Battery Voltage Monitor Over Voltage Select. Selects the reference level for the Over Voltage monitor to output one-hot Configuration to Analog Module.(If OVLEVEL>9, the actual analog trim value is the same as default value:OVLEVEL=0x07) 0x0: Over Voltage Threshold- 10'h001: 14.75V 0x1: Over Voltage Threshold- 10'h002: 15.18V 0x2: Over Voltage Threshold- 10'h004: 15.65V 0x3: Over Voltage Threshold- 10'h008: 16.37V 0x4: Over Voltage Threshold- 10'h010: 16.85V 0x5: Over Voltage Threshold- 10'h020: 17.57V 0x6: Over Voltage Threshold- 10'h040: 18.30V 0x7: Over Voltage Threshold- 10'h080: 19.00V 0x8: Over Voltage Threshold- 10'h100: 19.97V 0x9: Over Voltage Threshold- 10'h200: 20.70V	4	rw	0x7
F8	UVHYS	Battery Voltage Monitor Under Voltage Hysterisis Select. Selects the hysterisis level for the Under Voltage monitor. 0x0: 0.475V 0x1: 0.835V 0x2: 1.225V 0x3: 1.635V	2	rw	0x1
F0	UVLEVEL	Battery Voltage Monitor Under Voltage Select. Selects the reference level for the Under Voltage monitor. If UVLEVEL[5:3]>0x04, the actual analog trim value is the same as UVLEVEL=0x0A. The UVLEVEL threshold is mononically increased with the setting. 0x0: Vf: 4.615V 0x1: Vf: 4.685V 0x7: Vf: 5.135V 0x8: Vf: 5.225V 0x9: Vf: 5.135V 0xa: Vf: 5.405V 0xf: Vf: 5.895V 0x10: Vf: 6.015V 0x11: Vf: 6.125V 0x17: Vf: 6.925V 0x18: Vf: 7.075V 0x19: Vf: 7.235V 0x1f: Vf: 8.385V 0x20: Vf: 8.605V 0x21: Vf: 8.845V 0x27: Vf:10.610V	6	rw	0xA

8.2.4.11 DBGCTRL

0x50000928 **DBGCTRL**

PMU Debug Control.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F26				-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F31	DBG_LOCK	Set Only bit. Set this bit to lock DBG_CODE bits.	1	rw	0x0
F30	DBG_ACCESS_ENABLED	A status flag that is set when debug access is enabled	1	ro	0x0

F26	DBG_ACCESS_KEY	Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.	4	rw	0x0
F10	DBG_DIS_CP	Set 1, Shut down PRE5V ChargePump, PRE5V=Vzener-Vgs. Only take effect at Debug mode(DBG_TEST = 1) at PMU debug mode	1	rw	0x0
F9	DBG_DISCHARGE_3V3	3V3 LDO Debug Mode: a. Set '0' to test 3V3-LDO function; b. Set '1' to test 3V3-LDO Discharge Circuit.	1	rw	0x0
F8	DBG_DISCHARGE_1V5	1V5 LDO Debug Mode: a. Set '0' to test 1V5-LDO function; b. Set '1' to test 1V5-LDO Discharge Circuit.	1	rw	0x0
F7	DBG_DIS_BOR_1V5	Debug Contrl of dis_bor_1v5 at PMU debug mode	1	rw	0x0
F6	DBG_DIS_BOR_3V3	Debug Contrl of dis_bor_3v3 at PMU debug mode	1	rw	0x0
F5	DBG_DIS_LDO_1V5	Debug Contrl of dis_ldo_1v5 at PMU debug mode.	1	rw	0x0
F4	DBG_DIS_LDO_3V3	NOTE:Don't use.Debug Contrl of dis_ldo_3v3 at PMU debug mode	1	rw	0x0
F3	DBG_EN_LP_CAPLESS	1.5V ldo low power mode, set 1 to enter low power at PMU debug mode	1	rw	0x0
F2	DBG_DIS_BG_UVLO	Set to disable of low power mode for UVLO in BG_TOP at PMU debug mode	1	rw	0x0
F1	DBG_EN_LOWIQ	Set to enable of low power mode for BG_TOP at PMU debug mode	1	rw	0x0

8.2.4.12 BOR

0x5000092C **BOR**

BOR configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F15	F14	F13	F12	-	-	F9	F8	F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F31	BOR_LOCK	Set Only bit. Set this bit to lock BOR_ACTION & S_BOR bits.	1	rw	0x0
F30	EN_BOR_TESTMODE	BOR Testmode Enable. 0x0: BOR Testmode Disabled: Reference Voltage for BOR is from Band Gap (Functional Mode) 0x1: BOR Testmode Enabled: Reference Voltage for BOR is from gpio1_anaOut (Test Mode	1	rw	0x0
F15	BOR_1V5_FLAG_CLR	BOR 1v5 clear. Set to clear the 1.5V brownout detected flag	1	wo	0x0
F14	BOR_3V3_FLAG_CLR	BOR 3v3 clear. Set to clear the 3.3V brownout detected flag	1	wo	0x0
F13	BOR_1V5_FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	0x0
F12	BOR_3V3_FLAG	BOR 3v3 flag. Set by the hardware when a brownout of the 3.3V supply is detected.	1	ro	0x0
F9	BOR_1V5_ACTION	BOR 1v5 action. Defines the consequences of brown-out condition on the 1v5 supply being detected by the hardware. NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0
F8	BOR_3V3_ACTION	BOR 3v3 action. Defines the consequences of brown-out condition on the 3v3 supply being detected by the hardware. NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0
F4	S_BOR_1P5V	BOR 1v5 threshold. Select the BOR threshold voltage level for the 1v5 regulator. Following typical value can be used as reference: NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x0: Vr: 1.243 V, Vf: 1.218 V, 0x1: Vr: 1.273 V, Vf: 1.243 V, 0x2: Vr: 1.298 V, Vf: 1.273 V,	4	rw	0x3

		0x3: Vr: 1.328 V, Vf: 1.298 V, 0x4: Vr: 1.358 V, Vf: 1.328 V, 0x5: Vr: 1.393 V, Vf: 1.363 V, 0x6: Vr: 1.428 V, Vf: 1.393 V, 0x7: Vr: 1.463 V, Vf: 1.428 V, 0x8: Vr: 1.498 V, Vf: 1.468 V, 0x9: Vr: 1.538 V, Vf: 1.503 V, 0xa: Vr: 1.583 V, Vf: 1.548 V, 0xb: Vr: 1.623 V, Vf: 1.588 V, 0xc: Vr: 1.673 V, Vf: 1.633 V, 0xd: Vr: 1.718 V, Vf: 1.683 V, 0xe: Vr: 1.773 V, Vf: 1.733 V, 0xf: Vr: 1.828 V, Vf: 1.788 V,			
F0	S_BOR_3P3V	BOR 3v3 threshold. Select the BOR threshold voltage level for the 3v3 regulator, Following typical value can be used as reference: NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x0: Vr: 2.223 V, Vf: 2.163 V, 0x1: Vr: 2.288 V, Vf: 2.228 V, 0x2: Vr: 2.358 V, Vf: 2.293 V, 0x3: Vr: 2.428 V, Vf: 2.363 V, 0x4: Vr: 2.503 V, Vf: 2.433 V, 0x5: Vr: 2.583 V, Vf: 2.513 V, 0x6: Vr: 2.668 V, Vf: 2.598 V, 0x7: Vr: 2.763 V, Vf: 2.688 V, 0x8: Vr: 2.858 V, Vf: 2.783 V, 0x9: Vr: 2.968 V, Vf: 2.883 V, 0xa: Vr: 3.078 V, Vf: 2.998 V, 0xb: Vr: 3.203 V, Vf: 3.118 V, 0xc: Vr: 3.338 V, Vf: 3.248 V, 0xd: Vr: 3.483 V, Vf: 3.388 V, 0xe: Vr: 3.638 V, Vf: 3.543 V, 0xf: Vr: 3.813 V, Vf: 3.708 V,	4	rw	0xA

8.2.4.13 BORDEGLITCH

0x50000930 **BORDEGLITCH**

BOR Deglitch.
NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14		F12		-	-	-	F8	F6		F4		-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F14	SEL_BOR3V3_POS_DEGLITCH	select the deglitch width of BOR3V3 posedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x3
F12	SEL_BOR3V3_NEG_DEGLITCH	select the deglitch width of BOR3V3 negedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x0
F8	ENA_BOR3V3_DEGLITCH	enable of BOR3V3 deglitch.	1	rw	0x0
F6	SEL_BOR1V5_POS_DEGLITCH	select the deglitch width of BOR1V5 posedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x3
F4	SEL_BOR1V5_NEG_DEGLITCH	select the deglitch width of BOR1V5 negedge. 0x0: 16us Selected 0x1: 32us Selected	2	rw	0x0

		0x2: 64us Selected 0x3: 128us Selected			
F0	ENA_BOR1V5_DEGLITCH	enable of BOR1V5 deglitch.	1	rw	0x0

8.2.4.14 CLK_CTRL

0x50000934																CLK_CTRL															
Clock controls for 5V(always on) domain. NOTE:The write operation of this field register takes effect by configuring 'TRIM_HV->CFG.CFG_ACCESS_KEY = 0xB'.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8								-	-	-	F4	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F8	TRIM_LF_RC	LF RC oscillator trim. Following value only used as a reference:(the trim freq is non-linear) 0x0: freq(250k)=141.1Khz 0xa2: freq(250k)=250.0Khz 0xa4: freq(250k)=256.0Khz 0xff: freq(250k)=441.7Khz	8	rw	0xA0
F4	EN_HIGH_BW_LF_RC	set to enable to increase internal comparator bandwidth	1	rw	0x0

8.2.4.15 DFT

0x50000938																				DFT											
DFT.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F11	F10	F9	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F11	DFT_TESTMODE_START	Puts the ASIC into DFT testmode. Once the start bit is set, the I/O configuration will switch from Application mode to DFT Test Mode. The General Purpose I/Os will be configured as a JTAG interface. Once Test Mode is enabled, the ASIC will be boundary terminated and the processor will lose the ability to communicate with any ASIC peripherals. A chip power cycle is required to get out of the DFT test mode. Test Mode Enable state.	1	wo	0x0
F10	DFT_ACCESS_ENABLED	A status flag that is set when DFT access is enabled.	1	ro	0x0
F9	DFT_LOCK	Set Only bit. Write 1 to this bit to lock DFT_CODE config bits.	1	rw	0x0
F0	DFT_CODE	Write the value 0x1C to this register to Unlock 'Scan Test Mode'.	8	wo	0x0

8.2.5 IOCTRLA

IOCTRLA		
Address	**Register**	**Description**
0x50000C00	PAMUX	Port A Function Configuration
0x50000C04	PBMUX	Port B Function Configuration
0x50000C08	PACTRL	PORTA Control
0x50000C0C	PBCTRL	PORTB Control
0x50000C10	LIN	LIN Pin Control
0x50000C14	TESTMUXA	Test mux select of group A
0x50000C18	TESTMUXB	Test mux select of group B
0x50000C1C	TESTMUXC	Test mux select of group C

0x50000C20	LINSGFCONF	LINS Glitch Filter Configuration in active mode
0x50000C24	LINSGFCONF1	LINS Glitch Filter Configuration in active mode
0x50000C28	LINMGFCONF	LINM Glitch Filter Configuration in active mode
0x50000C2C	LINMGFCONF1	LINM Glitch Filter Configuration in active mode
0x50000C30	LINTXDMONITOR	LIN TXD Dominant Timeout
0x50000C34	LED	LED Pin Control
0x50000C38	ANALOGTESTMUXOVERRIDE	Analog Testmux Override
0x50000C3C	IRQ	IOCTRLA LINS/LINM TXD Dominant Monitor interrupts
0x50000C40	FILT_ACCESS	Glitch Filter access key

8.2.5.1 PAMUX

0x50000C00 **PAMUX**

Port A Function Configuration. Each port has 3bits configuration bits and the maximum number of IO functional modes are 8. If the reserved mode is selected, the port will behave as the default mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	F20			-	F16			-	F12			-	F8			-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F28	PA7MODE	0x0: GPA[7]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: LINM_Txd is driven by GPIO instead of internal LIN Core 0x2: UART Signle wire mode.NOTE:need to enable the Pullup. 0x3: UART Rxd. 0x4: Output of the 1st stage Glitch filter of LINS_Rxd. 0x5: TEST_MUX7. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x6: External LinPhy, Input LINS Rxd from GPIO. 0x7: PWM Mode. PWM Aux Channel 2 writes data to the GPIO.	3	rw	0x0
F24	PA6MODE	0x0: GPA[6]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: LINS_Txd is driven by GPIO instead of internal LIN Core 0x2: UART Signle wire mode.NOTE:need to enable the Pullup. 0x3: UART Txd. 0x4: Input of the 1st stage Glitch filter from Internal LIN Slave Phy. 0x5: TEST_MUX6. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x6: LINS_Core Txd output to GPIO(connect to External LinPhy) instead of internal LIN PHY. 0x7: PWM Mode. PWM Aux Channel 1 writes data to the GPIO.	3	rw	0x0
F20	PA5MODE	0x0: GPA[5]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: Input of LINS core Rxd. 0x2: UART Rxd from GPIO. 0x3: SPI MISO. 0x4: Input of LINM core Rxd. 0x5: Output of the 1st stage Glitch filter of LINM_Rxd. 0x6: TEST_MUX5. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x7: PWM Mode. PWM Aux Channel 0 writes data to the GPIO.	3	rw	0x0
F16	PA4MODE	0x0: GPA[4]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit.	3	rw	0x0

		Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: Output of the 3rd stage Glitch filter of LINS_Rxd. 0x2: UART Txd to GPIO. 0x3: SPI MOSI. 0x4: Output of the 3rd stage Glitch filter of LINM_Rxd. 0x5: Input of the 1st stage Glitch filter from Internal LIN Master Phy. 0x6: TEST_MUX4. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x7: PWM Mode. PWM Aux Channel 4 writes data to the GPIO.			
F12	PA3MODE	0x0: GPA[3]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: Output of the 2nd stage Glitch filter of LINS_Rxd. 0x2: SPI MISO. 0x3: TEST_MUX3. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x4: Output of the 2rd stage Glitch filter of LINM_Rxd. 0x5: Output of the 3rd stage Glitch filter of LINS_Rxd. 0x6: External LinPhy, Input LINM Rxd from GPIO. 0x7: PWM Mode, PWM Aux Channel 3 writes data to the GPIO.	3	rw	0x0
F8	PA2MODE	0x0: GPA[2]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: Output of the 1st stage Glitch filter of LINS_Rxd. 0x2: SPI MOSI. 0x3: SPI Master Slave Select Mode. 0x4: TEST_MUX2. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x5: Output of the 2nd stage Glitch filter of LINS_Rxd. 0x6: LINM_Core Txd output to GPIO(connect to External LinPhy) instead of internal LIN PHY. 0x7: PWM Mode, PWM Aux Channel 2 writes data to the GPIO.	3	rw	0x0
F4	PA1MODE	0x0: GPA[1]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: TEST_MUX1. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x2: SPI Clock. 0x3: SPI Clock. 0x4: Output of the 1st stage Glitch filter of LINM_Rxd. 0x5: Output of the 1st stage Glitch filter of LINS_Rxd. 0x6: External LinPhy, Input LINS Rxd from GPIO. 0x7: PWM Mode, PWM Aux Channel 1 writes data to the GPIO.	3	rw	0x0
F0	PA0MODE	0x0: GPA[0]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: Input of the 1st stage Glitch filter from Internal LIN Slave Phy. 0x2: SPI Master Slave Select Mode. 0x3: TEST_MUX0. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x4: Input of the 1st stage Glitch filter from Internal LIN Master Phy. 0x5: Input of the 1st stage Glitch filter from Internal LIN Slave Phy. 0x6: LINS_Core Txd output to GPIO(connect to External LinPhy) instead of internal LIN PHY. 0x7: PWM Mode. PWM Aux Channel 0 writes data to the GPIO.	3	rw	0x0

8.2.5.2 PBMUX

0x50000C04																															
PBMUX																															
Port B Function Configuration. Each port has 3bits configuration bits and the maximum number of IO functional modes are 8. If the reserved mode is selected, the port will behave as the default mode.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F20			-	F16			F15	F12			-	-	-	-	-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F20	PB5MODE	0x0: GPB[5]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: LIN Master. 0x2: LINM_Txd is driven by GPIO instead of internal LIN Core 0x3: UART Signle wire mode. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	3	rw	0x0
F16	PB4MODE	0x0: GPB[4]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: LIN Slave. 0x2: LINS_Txd is driven by GPIO instead of internal LIN Core 0x3: UART Signle wire mode. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	3	rw	0x0
F15	UARTTXDIDLEDIR	Control the direction of PAD for UART TXD Idle: 0x0: old the UART TXD Pad to output when TXD is idle. 0x1: Switch the TXD Pad to input When TXD is idle.	1	rw	0x1
F12	PB3MODE	0x0: SWD, Serial Wire Debug Data. 0x1: GPB[3]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: PWM Mode. PWM Aux Channel 4 writes data to the GPIO.	3	rw	0x0
F4	PB1MODE	0x0: GPB[1]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in IOCTRLA. 0x1: LINM Single wire mode, LINM PHY RXD/LINM PHY TXD, Open-drain output. 0x2: UART Rxd. 0x3: UART Signle wire mode.NOTE:need to enable the Pullup 0x4: TEST_MUX9. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x5: Output of the 3rd stage Glitch filter of LINM_Rxd. 0x6: External LinPhy, Input LINM Rxd from GPIO. 0x7: PWM Mode. PWM Aux Channel 4 writes data to the GPIO.	3	rw	0x0
F0	PB0MODE	0x0: GPB[0]. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by register in	3	rw	0x0

		IOCTRLA. 0x1: LINS Single wire mode, LINS PHY RXD/LINS PHY TXD, Open-drain output. 0x2: UART Txd. 0x3: UART Signle wire mode.NOTE:need to enable the Pullup 0x4: TEST_MUX8. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x5: Output of the 2nd stage Glitch filter of LINM_Rxd. 0x6: LINM_Core Txd output to GPIO(connect to External LinPhy) instead of internal LIN PHY. 0x7: PWM Mode. PWM Aux Channel 3 writes data to the GPIO.			

8.2.5.3 PACTRL

0x50000C08		PACTRL			
PORTA Control. Controls for the pads of GPIO port A					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - F16 F8 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	RE	Read enable. Each bit in this register determines whether the read data path is enabled for a pad. Set a bit to enable input data to be the read from the pad.	8	rw	0x0
F8	PD	Pull-down enable. Each bit in this register determines whether the pull-down resistor is enabled for a pad. Set a bit to enable the resistor.	8	rw	0x0
F0	PU	Pull-up enable. Each bit in this register determines whether the pull-up resistor is enabled for a pad.	8	rw	0x0

8.2.5.4 PBCTRL

0x50000C0C		PBCTRL			
PORTB Control. Controls for the pads of GPIO port B					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - F16 - - - - F8 - - - - F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	RE	Read enable. Each bit in this register determines whether the read data path is enabled for a pad. Set a bit to enable input data to be the read from the pad.	4	rw	0x0
F8	PD	Pull-down enable. Each bit in this register determines whether the pull-down resistor is enabled for a pad. Set a bit to enable the resistor.	4	rw	0x0
F0	PU	Pull-up enable. Each bit in this register determines whether the pull-up resistor is enabled for a pad.	4	rw	0x0

8.2.5.5 LIN

0x50000C10		LIN			
LIN Pin Control.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - - - F17 F16 - - - - - F9 F8 - - - F4 - - F1 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F17	LINM_RXD_DRV_UART_ENA	Enable of LIN RXD drives UART Rxd and LIN Core simultaneously.	1	rw	0x0

F16	LINS_RXD_DRV_UART_ENA	Enable of LIN RXD drives UART Rxd and LIN Core simultaneously.	1	rw	0x0
F9	LIN_DBG	LIN DEBUG. 0x0: lin_tx_s_duty_ibg1up_tp to PA[0] analog channel 0x1: lin_tx_s_slope_ibg1up_tp to PA[0] analog channel 0x2: lin_tx_m_duty_ibg1up_tp to PA[0] analog channel 0x3: lin_tx_m_slope_ibg1up_tp to PA[0] analog channel	2	rw	0x0
F8	LIN_DBG_ENA	LIN DEBUG enable.	1	rw	0x0
F4	PMODE	LIN Power Mode. Control LINS power state in hibernate mode. 0x0: Regardless of the related enable bits, LIN TX analog parts will be shut-down in hibernate mode, unless any LIN dominant signal is detected. 0x1: LIN TX analog parts are still controlled by theirs corresponding enable bits.	1	rw	0x0
F1	LINM_TXENA	LIN transmit enable.	1	rw	0x0
F0	LINS_TXENA	LIN transmit enable.	1	rw	0x0

8.2.5.6 TESTMUXA

0x50000C14 **TESTMUXA**

Test mux select of group A.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	F16						-	-	F8						-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	TESTMUX3	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F16	TESTMUX2	Selects debug signal to be output on the port when the port is configured to TEST_MUX2 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F8	TESTMUX1	Selects debug signal to be output on the port when the port is configured to TEST_MUX1 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F0	TESTMUX0	Selects debug signal to be output on the port when the port is configured to TEST_MUX0 mode. 0x0: LIN Slave Output of 1st Stage Rxd Glitch Filter 0x1: LIN Slave Output of 2nd Stage Rxd Glitch Filter 0x2: LIN Slave Output of 3rd Stage Rxd Glitch Filter 0x3: LIN Slave PHY's Rxd Monitor 0x4: LIN Slave PHY's Txd Monitor. 0x5: LIN Slave Input of Core rxd 0x6: LIN Slave Output of Core txd 0x7: LIN Master Output of 1st Stage Rxd Glitch Filter 0x8: LIN Master Output of 2nd Stage Rxd Glitch Filter 0x9: LIN Master Output of 3rd Stage Rxd Glitch Filter 0xa: LIN Master PHY's Rxd Monitor 0xb: LIN Master PHY's Txd Monitor. 0xc: LIN Master Input of Core rxd 0xd: LIN Master Output of Core txd 0xe: PMUA (Power Management Unit Asic) QACK 0xf: PMUA (Power Management Unit Asic) Wakeup signal 0x10: PMUA (Power Management Unit Asic) snowflake 0x11: BATTERY VOLTAGE MONITOR vbat_low 0x12: BATTERY VOLTAGE MONITOR vbat_high 0x13: BATTERY VOLTAGE MONITOR vbat_low_flag 0x14: BATTERY VOLTAGE MONITOR vbat_high_flag 0x15: BATTERY VOLTAGE MONITOR vbat_low_dbnc 0x16: BATTERY VOLTAGE MONITOR vbat_high_dbnc 0x17: BOR bor_control state[0] 0x18: BOR bor_control state[1] 0x19: BOR bor_bias_ena	6	rw	0x0

		0x1a: BOR bor_bias_ena_l 0x1b: BOR CONTROL STATE MACHINE pmua_bor_bias_ena 0x1c: BOR CONTROL STATE MACHINE hf_clk_allowed 0x1d: BOR CONTROL STATE MACHINE hf_active 0x1e: BOR CONTROL STATE MACHINE pmua_bor_arm_sync 0x1f: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_clk) 0x20: CRGA (Clock Reset Generation Asic) (scan_test_mode | hf_rc_clk) 0x21: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_sts) 0x22: CRGA (Clock Reset Generation Asic) (scan_test_mode | hf_rc_sts) 0x23: CRGA (Clock Reset Generation Asic) (scan_test_mode | clk_sys_gated) 0x24: CRGA (Clock Reset Generation Asic) (a_por_n) 0x25: CRGA (Clock Reset Generation Asic) (bor_3v3_n) 0x26: CRGA (Clock Reset Generation Asic) (ovtemp_flag) 0x27: CRGA (Clock Reset Generation Asic) (bor_1v5_n) 0x28: CRGA (Clock Reset Generation Asic) (wdt_bark) 0x29: ADC Controller sar_ana_clk 0x2a: ADC Controller adc_start_del 0x2b: ADC Controller sar_smp_vcm 0x2c: Flash Controller 4Mhz OSCw 0x2d: Flash Controller flash TDO 0x2e: Flash Controller flash TDI 0x2f: Flash Controller flash CLK			

8.2.5.7 TESTMUXB

0x50000C18			TESTMUXB																											
Test mux select of group B.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F16						-	-	F8						-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F16	TESTMUX6	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F8	TESTMUX5	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F0	TESTMUX4	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0

8.2.5.8 TESTMUXC

0x50000C1C			TESTMUXC																											
Test mux select of group C.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F16						-	-	F8						-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F16	TESTMUX9	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0
F8	TESTMUX8	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0

F0	TESTMUX7	Selects debug signal to be output on the port when the port is configured to TEST_MUX3 mode. Refer to TEST_MUX0 for signal selection	6	rw	0x0

8.2.5.9 LINSGFCONF

0x50000C20								LINSGFCONF																					
LINS Glitch Filter Configuration in active mode.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	F8							-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F16	LINS_DBNC_THRES1_1ST	1st Stage LINS Debounce Threshold for 0 to 1. 1st Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us].	7	rw	0x0
F8	LINS_DBNC_THRES0_1ST	1st Stage LINS Debounce Threshold for 1 to 0. 1st Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us].	7	rw	0x8
F0	LINS_RX_GF_ENA	LINS RXD Glitch Filter enables. bit-0: Enable LINS Glitch Filter 1st stage; bit-1: Enable LINS Glitch Filter 2nd stage; bit-2: Enable LINS Glitch Filter 3rd stage; NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	3	rw	0x7

8.2.5.10 LINSGFCONF1

0x50000C24								LINSGFCONF1																					
LINS Glitch Filter Configuration in active mode.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_DBNC_THRES1_3RD	3rd Stage LINS Debounce Threshold for 0 to 1. 3rd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F16	LINS_DBNC_THRES0_3RD	3rd Stage LINS Debounce Threshold for 1 to 0. 3rd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F8	LINS_DBNC_THRES1_2ND	2nd Stage LINS Debounce Threshold for 0 to 1. 2nd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us].	7	rw	0x20
F0	LINS_DBNC_THRES0_2ND	2nd Stage LINS Debounce Threshold for 1 to 0. 2nd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us].	7	rw	0x10

8.2.5.11 LINMGFCONF

0x50000C28								LINMGFCONF																					
LINM Glitch Filter Configuration in active mode.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	F8							-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset

F16	LINM_DBNC_THRES1_1ST	LINM Debounce Threshold for 0 to 1. 1st Stage LINM Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us].	7	rw	0x0
F8	LINM_DBNC_THRES0_1ST	LINM Debounce Threshold for 1 to 0. 1st Stage LINM Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us].	7	rw	0x8
F0	LINM_RX_GF_ENA	LINM RXD Glitch Filter enables. bit-0: Enable LINM Glitch Filter 1st stage; bit-1: Enable LINM Glitch Filter 2nd stage; bit-2: Enable LINM Glitch Filter 3rd stage; NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	3	rw	0x7

8.2.5.12 LINMGFCONF1

0x50000C2C **LINMGFCONF1**

LINM Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINM_DBNC_THRES1_3RD	3rd Stage LINM Debounce Threshold for 0 to 1. 3rd Stage LINM Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F16	LINM_DBNC_THRES0_3RD	3rd Stage LINM Debounce Threshold for 1 to 0. 3rd Stage LINM Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F8	LINM_DBNC_THRES1_2ND	2nd Stage LINM Debounce Threshold for 0 to 1. 2nd Stage LINM Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us].	7	rw	0x20
F0	LINM_DBNC_THRES0_2ND	2nd Stage LINM Debounce Threshold for 1 to 0. 2nd Stage LINM Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us].	7	rw	0x10

8.2.5.13 LINTXDMONITOR

0x50000C30 **LINTXDMONITOR**

LIN TXD Dominant Timeout.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F16											-	F4											F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	LINM_TXD_TO_DOM_THRES	LINS TxD monitor Threshold to detect LIN bus dominant '0' width of (T_clksys*resetvalue = 62.5us*1024 = 64[ms].	11	rw	0x400
F4	LINS_TXD_TO_DOM_THRES	LINS TxD monitor Threshold to detect LIN bus dominant '0' width of (T_clksys*resetvalue = 62.5us*1024 = 64[ms].	11	rw	0x400
F3	LINMTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINM TxD monitor if LINM's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0
F2	LINSTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINS TxD monitor if LINS's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0
F1	LINMTXDMONITORENA	LINM TxD Monitor enable.	1	rw	0x1

F0	LINSTXDMONITORENA	LINS TxD Monitor enable.	1	rw	0x1

8.2.5.14 LED

0x50000C34 **LED**

LED Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F24			F22		F19			F17		F16	F15	-	-	-	F9			F8	-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	LED_PULLUP_EN	LED PULLUP ENABLE. LED PAD Pullup enable, ONE HOT code. 0x1: LED0 PAD pullup to PRE5V through a diode and a 50K resistor 0x2: LED1 PAD pullup to PRE5V through a diode and a 50K resistor 0x4: LED2 PAD pullup to PRE5V through a diode and a 50K resistor	3	rw	0x0
F22	OP_GBW_SEL	LED SENSE OP GBW SEL. PN detect fully differential Op GBW choose 00: 3M 01: 5M 10: 8M 11: 10M	2	rw	0x1
F19	OP_CHOOSE_R	LED SENSE OP CHOOSE R. choose nulling resistor to do frequency compensation. Which denpends on the bandwidth of the OP. R R GBW(CL=3pF) 000 0.5K 11(10M) 001 2.5K 10(8M) 01(5M) 010 4.5K 011 6.5K 11(3M) 100 8.5K 101 10.5K 110 12.5K 111 14.5K	3	rw	0x1
F17	PN_OP_START_BIAS_BOOST	PN OP START BIAS BOOST. PN diff OP start bias current 00: 250nA 01: 500nA 10: 750nA 11: 1uA	2	rw	0x0
F16	GAIN_SEL	LED Sense AFE gain select. V_ADC = (vbat-vled)*GAIN , where V_ADC is voltage to ADC LED channle, and GAIN is selected by GAIN_SEL as following(typical value): 0x0: GAIN = 1/2 0x1: GAIN = 1/4	1	rw	0x0
F15	VFW_ENA	LED Forward Voltage Current Enable. Set to enable the independent LED VFW current source(maximum=5mA). When ADC CH2 measurement is active, the LED channel selected by CH2_SEL will be driven by LED_VFW current source.	1	rw	0x0
F9	SENSE_CTRL	LED. LED Sense Control bits for override control/debug.	3	rw	0x0
F8	SENSE_ENA	LED Forward Voltage Sense Enable. Set to enable LED forward voltage sense module. After setting this bit, it's recommended to wait ~40us before ADC conversion for LED_SENSE to settle down.	1	rw	0x1
F4	DATA	LED Data Out. When the LED hardware mode is disabled, then the data in this register bit is used to drive the LED driver. Each bit controls the corresonding LED Channel respectively.	3	rw	0x0
F0	HWMODE	LED hardware mode. LED Hardware Mode Enable. Each bit controls the corresponding LED Channel respectively. 0x0: Hardware Mode Disabled. LED_DATA register drives the LED Data Output pin. Read is not available on this pin. 0x1: Hardware Mode Enabled. PWM_BARIUM peripheral drives the LED Data Output pin. Read is not available on this pin.	3	rw	0x0

8.2.5.15 ANALOGTESTMUXOVERRIDE

0x50000C38 **ANALOGTESTMUXOVERRIDE**

Analog Testmux Override. This register controls the multiplexers for analog signals.
The select bit allows firmware to control the corresponding select field (in other words, firmware control).
The following table is intended to be a helpful guide in what data should be written to this register in order to connect a source and target together.
Note- Care should be taken to write zero to this register between connection changes. This ensures a clean break between selections.

Data to write at ANALOG_TESTMUX_OVERRIDE to enable connection

Source Description	Target Description	Data to write to connect Source to Target
3.3V Digital Supply * 1/2	PA0	0x0000_0107
1.5V Digital Supply	PA0	0x0000_0207
VDD_PRE5v * 1/4	PA0	0x0000_0407
VBG_1P2V	PA1	0x0000_0807
VBG_BUF	PA1	0x0000_1007
VREF_1P1	PA1	0x0000_2007
Temperature Sensor	PA1	0x0000_4007
ADC_REFP	PA1	0x0000_8007
BOR_REF	PA1	0x0001_0007

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F20												F17			F8									-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F20	ADCSELREG	Firmware Debug Value. need to be configured TOGETHER WITH GPIO_CON_REG to enable PA PAD output. (ADC_SEL_SEL also need to be set to 1) 0x1: Enable PA[0] analog connection to ADC 0x2: Enable PA[1] analog connection to ADC 0x4: Enable PA[2] analog connection to ADC 0x8: Enable PA[3] analog connection to ADC 0x10: Enable PA[4] analog connection to ADC 0x20: Enable PA[5] analog connection to ADC 0x40: Enable PA[6] analog connection to ADC 0x80: Enable PA[7] analog connection to ADC 0x100: Enable PB[0] analog connection to ADC 0x200: Enable PB[1] analog connection to ADC 0x400: Reserved 0x800: Enable PB[3] analog connection to ADC	12	rw	0x0
F17	LEDSEL	Firmware Debug Value. 0x1: Enable LED0 analog connection for short to gnd detecting 0x2: Enable LED1 analog connection for short to gnd detecting 0x4: Enable LED2 analog connection for short to gnd detecting	3	rw	0x0
F8	GPIOCONREG	Firmware Debug Value. GPIO test MUX select 0x1: Select VDD3V3 to PA0 0x2: Select VDD1V5 to PA0 0x4: Select VDD_PRE5V*1/4 to PA0 0x8: Select VBG_1P2V to PA1 0x10: Select VBG_BUF to PA1 0x20: Select VREF_1P1 to PA1 0x40: Select tempsensor to PA1 0x80: Select ADC_REFP to PA1 0x100: Select BOR_REF from PA1, for BOR trig point test	9	rw	0x0
F4	ADCCONREG	Firmware Debug Value. Contains the output value when the ADC_CON_SEL firmware select bit is set 0x1: Select LED0 Forward Voltage for measurement 0x2: Select LED1 Forward Voltage for measurement 0x4: Select LED2 Forward Voltage for measurement	3	rw	0x0
F2	ADCSELSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: ADC_SEL_REG controls output.	1	rw	0x0

F1	ADCCONSEL	ADC CON SEL. 0x0: Hardware Controlled. 0x1: ADC_CON_REG controls output.	1	rw	0x0
F0	GPIOCONSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: GPIO_CON_REG controls output.	1	rw	0x0

8.2.5.16 IRQ

0x50000C3C																													
IRQ																													
IOCTRLA LINS/LINM TXD Dominant Monitor interrupts. Contains the the enable, clear, status and active flag for the LINS/LINM TXD Dominant Monitor interrupt sources.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	INT_LINM_TXD_DOM_ACT	LINM TXD Dominant Monitor interrupt active.	1	ro	0x0
F24	INT_LINS_TXD_DOM_ACT	LINS TXD Dominant Monitor interrupt active.	1	ro	0x0
F17	INT_LINM_TXD_DOM_STS	LINM TXD Dominant Monitor interrupt status.	1	ro	0x0
F16	INT_LINS_TXD_DOM_STS	LINS TXD Dominant Monitor interrupt status.	1	ro	0x0
F9	INT_LINM_TXD_DOM_CLR	LINM TXD Dominant Monitor interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	INT_LINS_TXD_DOM_CLR	LINS TXD Dominant Monitor interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	INT_LINM_TXD_DOM_ENA	LINM TXD Dominant Monitor interrupt enable.	1	rw	0x0
F0	INT_LINS_TXD_DOM_ENA	LINS TXD Dominant Monitor interrupt enable.	1	rw	0x0

8.2.5.17 FILT_ACCESS

0x50000C40																													
FILT_ACCESS																													
Glitch Filter access key.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F31	FILT_UNLOCK	Set Only bit. Write 1 to this bit to un-lock FILT_CODE bits.	1	rw	0x0

8.2.6 WICA

WICA		
Address	**Register**	**Description**
0x50001000	CTRL	Wakeup Control Register
0x50001004	STATUS	Wakeup Status Register

8.2.6.1 CTRL

0x50001000	CTRL

Wakeup Control Register. This is the control register for wakeup via gpio or lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F22	F21	F20	-	F18	F17	F16	-	-	-	-	F8				-	-	-	-	-	F2	-	-

#	Field Name	Field Description	Width	Access	Reset
F22	TIMER_IRQCLR	clear the wutimer_irq. writting a '1 to this register will clear the wutimer_irq	1	wo	0x0
F21	LINM_IRQCLR	clear the wulinm_irq. writting a '1 to this register will clear the wulinm_irq	1	wo	0x0
F20	LINS_IRQCLR	clear the wulins_irq. writting a '1 to this register will clear the wulins_irq	1	wo	0x0
F18	TIMER_IRQENA	Timer Wakeup Interrupt Enable. if set, wutimer_irq is asserted if wakeup timer matches the tapsel	1	rw	0x1
F17	LINM_IRQENA	LIN Master Wakeup Interrupt Enable. if set, wulin_irq is asserted if a wakeup signal is detected on the LIN_OUT bus	1	rw	0x1
F16	LINS_IRQENA	LIN Slave Wakeup Interrupt Enable. if set, wulin_irq is asserted if a wakeup signal is detected on the LIN_IN bus	1	rw	0x1
F8	TIMER_TAPSEL	WakeUp Timer Tap Select. Wakeup Time = 2^(WUT_TAPSEL) x Tlfclk(62.5us)	4	rw	0x4
F2	TIMER_ENA	Wakeup Timer Enable. it enables the wakeup timer	1	rw	0x0

8.2.6.2 STATUS

0x50001004 **STATUS**

Wakeup Status Register. This is the status register for wakeup via gpio or lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TIMERCNT	Wakeup Timer Counter Value. Counter Value of the Wakeup Timer	16	ro	0x0
F2	TIMER	Wakeup Timer Status. This gets set if a wakeup timer is enabled and the count matches the tapsel setting during hibernate, CLRIRQ clears this Register	1	ro	0x0
F1	LINM	LIN Master Wakeup Status. This gets set if a wakeup signal is detected on the LIN_OUT bus when LINM SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0
F0	LINS	LIN Slave Wakeup Status. This gets set if a wakeup signal is detected on the LIN_IN bus when LINS SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0

8.2.7 WDTA

WDTA

Address	Register	Description
0x50001400	CTRL	Control
0x50001404	STOPR	Stop
0x50001408	CLEAR	Clear
0x5000140C	CNTVAL	Counter value
0x50001410	INT	WDTA Interrupts

8.2.7.1 CTRL

0x50001400																	CTRL													
Control.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14	F12		F11	F8			-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F14	WINOPENFLAG	Window open flag. A flag that indicates when the watchdog window is open. It only can be cleared by Reg CLEAR! 0x0: Window is Closed 0x1: Window is Open	1	ro	0x0
F12	WINOPENSEL	Window Mode open select. Defines the time of beginning of watchdog window open (the time between the watchdog start and the window open). 0x0: 1/2 * WDT timeout 0x1: 1/4 * WDT timeout 0x2: 1/8 * WDT timeout 0x3: 1/16* WDT timeout	2	rw	0x0
F11	WINOPENENA	Window Mode Enable. Enables Window Mode. 1'b1: Enable the Window mode of Watchdog, if the WDT is cleared before the time window opens, the WDT will issue a system reset. 1'b0: Disable the Window mode of Watchdog.	1	rw	0x0
F8	TIMEOUTSEL	Timeout select. Defines the watchdog timeout period (the time between a clear operation and the next timeout). 0x0: 2^11 * 64us ~= 131 ms 0x1: 2^12 * 64us ~= 262 ms 0x2: 2^13 * 64us ~= 524 ms 0x3: 2^14 * 64us ~= 1.05 s 0x4: 2^15 * 64us ~= 2.10 s 0x5: 2^16 * 64us ~= 4.19 s 0x6: 2^17 * 64us ~= 8.38 s 0x7: 2^18 * 64us ~= 16.77 s	3	rw	0x7
F1	RUNNING	Running status. A flag that indicates when the watchdog timer is enabled. 0x0: Watchdog timer is stopped and cleared 0x1: Watchdog timer is running	1	ro	0x0
F0	UPDATE	Window Mode Enable. Set to update Analog-Watchdog Configurations. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0

8.2.7.2 STOPR

0x50001404																														
Stop.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	STOP_LOCK	Set Only bit. Set this bit to lock STOP bits.	1	rw	0x0
F0	STOP	Stop. Write the *stop* code (0xc3) to this register to reset the timer and disable the watchdog (e.g. during debug). If any other value is written to this register the watchdog will be enabled.	8	rw	0x55

8.2.7.3 CLEAR

0x50001408		CLEAR			
Clear.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CLEAR	Clear. Write the value 0x3c574ad6 (as a single word access) to reset the watchdog timer. Periodically performing this action is the expected method of preventing the watchdog from timing out (and resetting the MCU).	32	wo	0x0

8.2.7.4 CNTVAL

0x5000140C		CNTVAL			
Counter value.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CNTVAL	Counter value. The instantaneous value of watchdog timeout counter ***NOTE:****This register should read three times and discard the one that is neither not the same with nor adjacent to the other two.*	32	ro	0x0

8.2.7.5 INT

0x50001410		INT			
WDTA Interrupts. Contains the ENABLE, CLEAR, STATUS and IRQ for the UART interrupt sources.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - F25 F24 - - - - - - F17 F16 - - - - - - F9 F8 - - - - - - F1 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F25	INTWINOPENIRQ	Window Open Interrupt.	1	ro	0x0
F24	INTWDTAIRQ	WDTA timeout Interrupt.	1	ro	0x0
F17	INTWINOPENSTS	Window Open Status. Set by WDTA window open	1	ro	0x0
F16	INTWDTASTS	WDTA timeout Status. Set by WDTA timeout	1	ro	0x0
F9	INTWINOPENCLR	Window Open Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	INTWDTACLR	WDTA timeout Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	INTWINOPENENA	Window Open Interrupt Enable.	1	rw	0x0
F0	INTWDTAENA	WDTA timeout Interrupt Enable.	1	rw	0x0

8.2.8 GPIO

GPIO		
Address	**Register**	**Description**
0x50004400	GPACTRL	GPIO Port A Control Registers
0x50004404	GPBCTRL	GPIO Port B Control Registers

0x50004408	GPAP03	GPIO Port A Pin 0-3 Control
0x5000440C	GPAP47	GPIO Port A Pin 4-7 Control
0x50004410	GPBP03	GPIO Port B Pin 0-3 Control(PB3-SWD)
0x50004414	GPBP47	GPIO Port B Pin 4-7 Control(PB4-LIN_IN,PB5-LIN_OUT)
0x50004418	GPENA	GPIO Port Enables

8.2.8.1 GPACTRL

0x50004400 **GPACTRL**

GPIO Port A Control Registers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F24	GPADATACLR	Write-only register. Write 1 to clr the corresponding GPIO output data. Write 0 has no effects.	8	wo	0x0
F16	GPADATASET	Write-only register. Write 1 to set the corresponding GPIO output data. Write 0 has no effects.	8	wo	0x0
F0	GPADATA	Port A data. Read feedbacks the status of PORTs. Write to control the GPIO's output data.	8	dual	0x0

8.2.8.2 GPBCTRL

0x50004404 **GPBCTRL**

GPIO Port B Control Registers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	F16						-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	GPBDATACLR	Write-only register. Write 1 to clr the corresponding GPIO output data. Write 0 has no effects.	6	wo	0x0
F16	GPBDATASET	Write-only register. Write 1 to set the corresponding GPIO output data. Write 0 has no effects.	6	wo	0x0
F0	GPBDATA	Port B data. Read feedbacks the status of PORTs. Write to control the GPIO's output data.	6	dual	0x30

8.2.8.3 GPAP03

0x50004408 **GPAP03**

GPIO Port A Pin 0-3 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	GPAACTDETFE[3]	PIN 3 activity fall status.	1	ro	N/A
F30	GPAACTDETRE[3]	PIN 3 activity rise status.	1	ro	N/A
F29	GPAACTDET[3]	Pin 3 activity interrupt.	1	ro	N/A
F28	GPACLR[3]	Pin 3 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[3]	Pin 3 falling edge enable.	1	rw	0x0
F26	GPARE[3]	Pin 3 rising edge enable.	1	rw	0x0

F25	GPAIE[3]	Pin 3 interrupt mask.	1	rw	0x0
F24	GPADIR[3]	Pin 3 output enable.	1	rw	0x0
F23	GPAACTDETFE[2]	PIN 2 activity fall status.	1	ro	N/A
F22	GPAACTDETRE[2]	PIN 2 activity rise status.	1	ro	N/A
F21	GPAACTDET[2]	Pin 2 activity interrupt.	1	ro	N/A
F20	GPACLR[2]	Pin 2 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[2]	Pin 2 falling edge enable.	1	rw	0x0
F18	GPARE[2]	Pin 2 rising edge enable.	1	rw	0x0
F17	GPAIE[2]	Pin 2 interrupt mask.	1	rw	0x0
F16	GPADIR[2]	Pin 2 output enable.	1	rw	0x0
F15	GPAACTDETFE[1]	PIN 1 activity fall status.	1	ro	N/A
F14	GPAACTDETRE[1]	PIN 1 activity rise status.	1	ro	N/A
F13	GPAACTDET[1]	Pin 1 activity interrupt.	1	ro	N/A
F12	GPACLR[1]	Pin 1 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[1]	Pin 1 falling edge enable.	1	rw	0x0
F10	GPARE[1]	Pin 1 rising edge enable.	1	rw	0x0
F9	GPAIE[1]	Pin 1 interrupt mask.	1	rw	0x0
F8	GPADIR[1]	Pin 1 output enable.	1	rw	0x0
F7	GPAACTDETFE[0]	PIN 0 activity fall status.	1	ro	N/A
F6	GPAACTDETRE[0]	PIN 0 activity rise status.	1	ro	N/A
F5	GPAACTDET[0]	Pin 0 activity interrupt.	1	ro	N/A
F4	GPACLR[0]	Pin 0 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[0]	Pin 0 falling edge enable.	1	rw	0x0
F2	GPARE[0]	Pin 0 rising edge enable.	1	rw	0x0
F1	GPAIE[0]	Pin 0 interrupt mask.	1	rw	0x0
F0	GPADIR[0]	Pin 0 output enable.	1	rw	0x0

8.2.8.4 GPAP47

0x5000440C		**GPAP47**			
GPIO Port A Pin 4-7 Control.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F31 F30 F29 F28 F27 F26 F25 F24 F23 F22 F21 F20 F19 F18 F17 F16 F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 F3 F2 F1 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F31	GPAACTDETFE[7]	PIN 7 activity fall status.	1	ro	N/A
F30	GPAACTDETRE[7]	PIN 7 activity rise status.	1	ro	N/A
F29	GPAACTDET[7]	Pin 7 activity interrupt.	1	ro	N/A
F28	GPACLR[7]	Pin 7 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[7]	Pin 7 falling edge enable.	1	rw	0x0
F26	GPARE[7]	Pin 7 rising edge enable.	1	rw	0x0

F25	GPAIE[7]	Pin 7 interrupt mask.	1	rw	0x0
F24	GPADIR[7]	Pin 7 output enable.	1	rw	0x0
F23	GPAACTDETFE[6]	PIN 6 activity fall status.	1	ro	N/A
F22	GPAACTDETRE[6]	PIN 6 activity rise status.	1	ro	N/A
F21	GPAACTDET[6]	Pin 6 activity interrupt.	1	ro	N/A
F20	GPACLR[6]	Pin 6 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[6]	Pin 6 falling edge enable.	1	rw	0x0
F18	GPARE[6]	Pin 6 rising edge enable.	1	rw	0x0
F17	GPAIE[6]	Pin 6 interrupt mask.	1	rw	0x0
F16	GPADIR[6]	Pin 6 output enable.	1	rw	0x0
F15	GPAACTDETFE[5]	PIN 5 activity fall status.	1	ro	N/A
F14	GPAACTDETRE[5]	PIN 5 activity rise status.	1	ro	N/A
F13	GPAACTDET[5]	Pin 5 activity interrupt.	1	ro	N/A
F12	GPACLR[5]	Pin 5 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[5]	Pin 5 falling edge enable.	1	rw	0x0
F10	GPARE[5]	Pin 5 rising edge enable.	1	rw	0x0
F9	GPAIE[5]	Pin 5 interrupt mask.	1	rw	0x0
F8	GPADIR[5]	Pin 5 output enable.	1	rw	0x0
F7	GPAACTDETFE[4]	PIN 4 activity fall status.	1	ro	N/A
F6	GPAACTDETRE[4]	PIN 4 activity rise status.	1	ro	N/A
F5	GPAACTDET[4]	Pin 4 activity interrupt.	1	ro	N/A
F4	GPACLR[4]	Pin 4 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[4]	Pin 4 falling edge enable.	1	rw	0x0
F2	GPARE[4]	Pin 4 rising edge enable.	1	rw	0x0
F1	GPAIE[4]	Pin 4 interrupt mask.	1	rw	0x0
F0	GPADIR[4]	Pin 4 output enable.	1	rw	0x0

8.2.8.5 GPBP03

0x50004410																													
GPBP03																													
GPIO Port B Pin 0-3 Control(PB3-SWD).																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	GPBACTDETFE[3]	PIN 3 activity fall status.	1	ro	N/A
F30	GPBACTDETRE[3]	PIN 3 activity rise status.	1	ro	N/A
F29	GPBACTDET[3]	Pin 3 activity interrupt.	1	ro	N/A
F28	GPBCLR[3]	Pin 3 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPBFE[3]	Pin 3 falling edge enable.	1	rw	0x0
F26	GPBRE[3]	Pin 3 rising edge enable.	1	rw	0x0

F25	GPBIE[3]	Pin 3 interrupt mask.	1	rw	0x0
F24	GPBDIR[3]	Pin 3 output enable.	1	rw	0x0
F23	GPBACTDETFE[2]	PIN 2 activity fall status.	1	ro	N/A
F22	GPBACTDETRE[2]	PIN 2 activity rise status.	1	ro	N/A
F21	GPBACTDET[2]	Pin 2 activity interrupt.	1	ro	N/A
F20	GPBCLR[2]	Pin 2 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPBFE[2]	Pin 2 falling edge enable.	1	rw	0x0
F18	GPBRE[2]	Pin 2 rising edge enable.	1	rw	0x0
F17	GPBIE[2]	Pin 2 interrupt mask.	1	rw	0x0
F16	GPBDIR[2]	Pin 2 output enable.	1	rw	0x0
F15	GPBACTDETFE[1]	PIN 1 activity fall status.	1	ro	N/A
F14	GPBACTDETRE[1]	PIN 1 activity rise status.	1	ro	N/A
F13	GPBACTDET[1]	Pin 1 activity interrupt.	1	ro	N/A
F12	GPBCLR[1]	Pin 1 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPBFE[1]	Pin 1 falling edge enable.	1	rw	0x0
F10	GPBRE[1]	Pin 1 rising edge enable.	1	rw	0x0
F9	GPBIE[1]	Pin 1 interrupt mask.	1	rw	0x0
F8	GPBDIR[1]	Pin 1 output enable.	1	rw	0x0
F7	GPBACTDETFE[0]	PIN 0 activity fall status.	1	ro	N/A
F6	GPBACTDETRE[0]	PIN 0 activity rise status.	1	ro	N/A
F5	GPBACTDET[0]	Pin 0 activity interrupt.	1	ro	N/A
F4	GPBCLR[0]	Pin 0 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPBFE[0]	Pin 0 falling edge enable.	1	rw	0x0
F2	GPBRE[0]	Pin 0 rising edge enable.	1	rw	0x0
F1	GPBIE[0]	Pin 0 interrupt mask.	1	rw	0x0
F0	GPBDIR[0]	Pin 0 output enable.	1	rw	0x0

8.2.8.6 GPBP47

0x50004414 **GPBP47**

GPIO Port B Pin 4-7 Control(PB4-LIN_IN,PB5-LIN_OUT).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F15	GPBACTDETFE[5]	PIN 5 activity fall status.	1	ro	N/A
F14	GPBACTDETRE[5]	PIN 5 activity rise status.	1	ro	N/A
F13	GPBACTDET[5]	Pin 5 activity interrupt.	1	ro	N/A
F12	GPBCLR[5]	Pin 5 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPBFE[5]	Pin 5 falling edge enable.	1	rw	0x0
F10	GPBRE[5]	Pin 5 rising edge enable.	1	rw	0x0

F9	GPBIE[5]	Pin 5 interrupt mask.	1	rw	0x0
F8	GPBDIR[5]	Pin 5 output enable.	1	rw	0x0
F7	GPBACTDETFE[4]	PIN 4 activity fall status.	1	ro	N/A
F6	GPBACTDETRE[4]	PIN 4 activity rise status.	1	ro	N/A
F5	GPBACTDET[4]	Pin 4 activity interrupt.	1	ro	N/A
F4	GPBCLR[4]	Pin 4 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPBFE[4]	Pin 4 falling edge enable.	1	rw	0x0
F2	GPBRE[4]	Pin 4 rising edge enable.	1	rw	0x0
F1	GPBIE[4]	Pin 4 interrupt mask.	1	rw	0x0
F0	GPBDIR[4]	Pin 4 output enable.	1	rw	0x0

8.2.8.7 GPENA

0x50004418																													
GPENA																													
GPIO Port Enables.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F1	GPBENA		1	rw	0x1
F0	GPAENA		1	rw	0x1

8.2.9 PWM

PWM		
Address	**Register**	**Description**
0x50010000	BASE	Base functions
0x50010004	PWMCNT	PWM Count Value
0x50010008	ENAREQ	Enable request
0x5001000C	ENASTS	Enable status
0x50010010	INIT	Intial State of Outputs
0x50010014	INV	Invert
0x50010018	UPDATE	Update
0x5001001C	PULSE0	PWM0 pulse setup
0x50010020	PULSE1	PWM1 pulse setup
0x50010024	PULSE2	PWM2 pulse setup
0x50010028	INTPOSEDGENA	PWM posedge interrupt enable
0x5001002C	INTNEGEDGENA	PWM negedge interrupt enable
0x50010030	INTPOSEDGCLR	PWM posedge interrupt control
0x50010034	INTNEGEDGCLR	PWM negedge interrupt control
0x50010038	INTPOSEDGSTS	PWM posedge interrupt status
0x5001003C	INTNEGEDGSTS	PWM negedge interrupt status
0x50010040	INTPOSEDGIRQ	PWM posedge interrupt active
0x50010044	INTNEGEDGIRQ	PWM negedge interrupt active
0x50010048	INTPWM	PWM interrupt control

8.2.9.1 BASE

0x50010000																BASE															
Base functions.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.9.2 PWMCNT

0x50010004																PWMCNT															
PWM Count Value.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT	PWM counter value to give a sense about the current period	16	dual	0x0

8.2.9.3 ENAREQ

0x50010008																ENAREQ															
Enable request.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	3	rw	0x0

8.2.9.4 ENASTS

0x5001000C																ENASTS															
Enable status.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	3	ro	0x0

8.2.9.5 INIT

0x50010010																															
Intial State of Outputs.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	3	rw	0x0

8.2.9.6 INV

0x50010014																															
Invert.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	3	rw	0x0

8.2.9.7 UPDATE

0x50010018																															
Update.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	1	dual	0x0

8.2.9.8 PULSE0

0x5001001C																															
PWM0 pulse setup.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.9 PULSE1

0x50010020	PULSE1
PWM1 pulse setup.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.10 PULSE2

0x50010024	PULSE2

PWM2 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.9.11 INTPOSEDGENA

0x50010028	INTPOSEDGENA

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[2:0]: posedge interrupt enable.	3	rw	0x0

8.2.9.12 INTNEGEDGENA

0x5001002C	INTNEGEDGENA

PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[2:0]: negedge interrupt enable.	3	rw	0x0

8.2.9.13 INTPOSEDGCLR

0x50010030	INTPOSEDGCLR

PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset

F0	INTPOSEDGCLR	Interrupt clear. bit[2:0] : posedge interrupt clear.	3	wo	0x0

8.2.9.14 INTNEGEDGCLR

0x50010034																														
INTNEGEDGCLR																														
PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[2:0] : negedge interrupt clear.	3	wo	0x0

8.2.9.15 INTPOSEDGSTS

0x50010038																														
INTPOSEDGSTS																														
PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[2:0] : posedge interrupt status.	3	ro	N/A

8.2.9.16 INTNEGEDGSTS

0x5001003C																														
INTNEGEDGSTS																														
PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[2:0] : negedge interrupt status.	3	ro	N/A

8.2.9.17 INTPOSEDGIRQ

0x50010040																														
INTPOSEDGIRQ																														
PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[2:0] : posedge interrupt active.	3	ro	N/A

8.2.9.18 INTNEGEDGIRQ

0x50010044																														
INTNEGEDGIRQ																														
PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[2:0] : negedge interrupt active.	3	ro	N/A

8.2.9.19 INTPWM

0x50010048															INTPWM															
PWM interrupt control. Contains the enable, clear, status and active for the PWM period & updated interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	INT_UPD_IRQ	Updated Interrupt active.	1	ro	N/A
F24	INT_PERIOD_IRQ	Period Interrupt active.	1	ro	N/A
F17	INT_UPD_STS	Updated Interrupt status.	1	ro	N/A
F16	INT_PERIOD_STS	Period Interrupt status.	1	ro	N/A
F9	INT_UPD_CLR	Updated Interrupt clear.	1	wo	0x0
F8	INT_PERIOD_CLR	Period Interrupt clear.	1	wo	0x0
F1	INT_UPD_ENA	Updated Interrupt enable.	1	rw	0x0
F0	INT_PERIOD_ENA	Period Interrupt enable.	1	rw	0x0

8.2.10 PWM_AUX

PWM_AUX		
Address	**Register**	**Description**
0x50010800	BASE0	Base 0 functions
0x50010804	PWMCNT0	PWM Count Value
0x50010808	BASE1	Base 1 functions
0x5001080C	PWMCNT1	PWM Count Value
0x50010810	BASESEL	Base Timer Select for individual Channels
0x50010814	ENAREQ	Enable request
0x50010818	ENASTS	Enable status
0x5001081C	INIT	Intial State of Outputs
0x50010820	INV	Invert
0x50010824	UPDATE	Update
0x50010828	PULSE0	PWM0 pulse setup
0x5001082C	PULSE1	PWM1 pulse setup
0x50010830	PULSE2	PWM2 pulse setup
0x50010834	PULSE3	PWM3 pulse setup
0x50010838	PULSE4	PWM4 pulse setup
0x5001083C	INTPOSEDGENA	PWM posedge interrupt enable
0x50010840	INTNEGEDGENA	PWM negedge interrupt enable
0x50010844	INTPOSEDGCLR	PWM posedge interrupt control
0x50010848	INTNEGEDGCLR	PWM negedge interrupt control
0x5001084C	INTPOSEDGSTS	PWM posedge interrupt status
0x50010850	INTNEGEDGSTS	PWM negedge interrupt status
0x50010854	INTPOSEDGIRQ	PWM posedge interrupt active
0x50010858	INTNEGEDGIRQ	PWM negedge interrupt active
0x5001085C	INTPERIOD	PWM Period interrupt control
0x50010860	INTUPDATED	PWM Updated interrupt control

8.2.10.1 BASE0

0x50010800	BASE0
Base 0 functions.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD0	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL0	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.10.2 PWMCNT0

0x50010804	PWMCNT0
PWM Count Value.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT0	PWM counter value to give a sense about the current period	16	ro	0x0

8.2.10.3 BASE1

0x50010808	BASE1
Base 1 functions.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD1	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL1	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.10.4 PWMCNT1

0x5001080C	PWMCNT1
PWM Count Value.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT1	PWM counter value to give a sense about the current period	16	ro	0x0

8.2.10.5 BASESEL

0x50010810	BASESEL

Base Timer Select for individual Channels.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	BASE_SEL	Base Timer Selects:1=Select BASE1, 0=Select BASE0.	5	rw	0x0

8.2.10.6 ENAREQ

0x50010814	ENAREQ

Enable request.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	5	rw	0x0

8.2.10.7 ENASTS

0x50010818	ENASTS

Enable status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	5	ro	0x0

8.2.10.8 INIT

0x5001081C	INIT

Intial State of Outputs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	5	rw	0x0

8.2.10.9 INV

0x50010820																													
Invert.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	5	rw	0x0

8.2.10.10 UPDATE

0x50010824																													
Update.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	2	dual	0x0

8.2.10.11 PULSE0

0x50010828																													
PWM0 pulse setup.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.10.12 PULSE1

0x5001082C																													
PWM1 pulse setup.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.10.13 PULSE2

0x50010830	PULSE2
PWM2 pulse setup.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.10.14 PULSE3

0x50010834	PULSE3
PWM3 pulse setup.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE3	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL3	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.10.15 PULSE4

0x50010838	PULSE4
PWM4 pulse setup.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE4	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL4	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.10.16 INTPOSEDGENA

0x5001083C	INTPOSEDGENA
PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[4:0]: posedge interrupt enable.	5	rw	0x0

8.2.10.17 INTNEGEDGENA

0x50010840																														
INTNEGEDGENA																														
PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[4:0]: negedge interrupt enable.	5	rw	0x0

8.2.10.18 INTPOSEDGCLR

0x50010844																														
INTPOSEDGCLR																														
PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGCLR	Interrupt clear. bit[4:0] : posedge interrupt clear.	5	wo	0x0

8.2.10.19 INTNEGEDGCLR

0x50010848																														
INTNEGEDGCLR																														
PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[4:0] : negedge interrupt clear.	5	wo	0x0

8.2.10.20 INTPOSEDGSTS

0x5001084C																														
INTPOSEDGSTS																														
PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[4:0] : posedge interrupt status.	5	ro	N/A

8.2.10.21 INTNEGEDGSTS

0x50010850																														
INTNEGEDGSTS																														
PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[4:0] : negedge interrupt status.	5	ro	N/A

8.2.10.22 INTPOSEDGIRQ

0x50010854																															
INTPOSEDGIRQ																															
PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[4:0] : posedge interrupt active.	5	ro	N/A

8.2.10.23 INTNEGEDGIRQ

0x50010858																															
INTNEGEDGIRQ																															
PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[4:0] : negedge interrupt active.	5	ro	N/A

8.2.10.24 INTPERIOD

0x5001085C																															
INTPERIOD																															
PWM Period interrupt control. Contains the enable, clear, status and active for the PWM period interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	INT_PERIOD_IRQ	Period Interrupt active.	2	ro	N/A
F16	INT_PERIOD_STS	Period Interrupt status.	2	ro	N/A
F8	INT_PERIOD_CLR	Period Interrupt clear.	2	wo	0x0
F0	INT_PERIOD_ENA	Period Interrupt enable.	2	rw	0x0

8.2.10.25 INTUPDATED

0x50010860																															
INTUPDATED																															
PWM Updated interrupt control. Contains the enable, clear, status and active for the PWM updated interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	INT_UPD_IRQ	Updated Interrupt active.	2	ro	N/A
F16	INT_UPD_STS	Updated Interrupt status.	2	ro	N/A
F8	INT_UPD_CLR	Updated Interrupt clear.	2	wo	0x0
F0	INT_UPD_ENA	Updated Interrupt enable.	2	rw	0x0

8.2.11 LINM

LINM		
Address	**Register**	**Description**

0x50010C00	DATABYTE1	Data Byte 1
0x50010C04	DATABYTE2	Data Byte 2
0x50010C08	DATABYTE3	Data Byte 3
0x50010C0C	DATABYTE4	Data Byte 4
0x50010C10	DATABYTE5	Data Byte 5
0x50010C14	DATABYTE6	Data Byte 6
0x50010C18	DATABYTE7	Data Byte 7
0x50010C1C	DATABYTE8	Data Byte 8
0x50010C20	CTRL	Control Register
0x50010C24	STATUS	Status
0x50010C28	ERROR	Error Register
0x50010C2C	DL	DATA Length Register
0x50010C30	BTDIV07	Bit time Divider Register
0x50010C34	BITTIME	Control Settings
0x50010C38	ID	ID Register
0x50010C3C	BUSTIME	Lin Bus Timing Register
0x50010C40	STATUSEXT	Extended Status
0x50010C48	CONF	Extended Configuration Register for compatibility issue

8.2.11.1 DATABYTE1

0x50010C00	**DATABYTE1**

Data Byte 1. DATA_BUF1~4 could be read/written through one word access to this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF4SHADOW	Data Buffer 4 Shadow. Shadow register of 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF3SHADOW	Data Buffer 3 Shadow. Shadow register of 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF2SHADOW	Data Buffer 2 Shadow. Shadow register of 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.2 DATABYTE2

0x50010C04	**DATABYTE2**

Data Byte 2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.3 DATABYTE3

0x50010C08	**DATABYTE3**

Data Byte 3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.4 DATABYTE4

0x50010C0C	DATABYTE4

Data Byte 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.5 DATABYTE5

0x50010C10	DATABYTE5

Data Byte 5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF8SHADOW	Data Buffer 8 Shadow. Shadow register of 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF7SHADOW	Data Buffer 7 Shadow. Shadow register of 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF6SHADOW	Data Buffer 6 Shadow. Shadow register of 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.6 DATABYTE6

0x50010C14	DATABYTE6

Data Byte 6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.7 DATABYTE7

0x50010C18	DATABYTE7

Data Byte 7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset

F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.8 DATABYTE8

0x50010C1C																													
DATABYTE8																													
Data Byte 8.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.11.9 CTRL

0x50010C20																													
CTRL																													
Control Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can not make use of the frame content with the received identifier(e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0 Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame. If DIS_AUTOSLEEP = 0, the bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected.	1	rw	0x1
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0
F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0
F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0
F0	STARTREQ	Start Request. The bit has to be set by the host controller of a LIN master to start the LIN transmission after loading identifier,data length and data buffer. The bit will be reset by the LIN core after the transmission is finished or an error is occurred.	1	rw	0x0

8.2.11.10 STATUS

0x50010C24																								STATUS							
Status.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active	1	ro	0x0
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register. The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence	1	ro	0x0
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

8.2.11.11 ERROR

0x50010C28																								ERROR							
Error Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F7	F6	F5	F4	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F8	BITMONDATA	Bit Monitor Error occurred in Start or Data Bits. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the start or data bits.	1	ro	0x0

F7	BITMONSTOP	Bit Monitor Error occurred in Stop Bit. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the stop bit. In SAE2602, the error belongs to framing error.	1	ro	0x0
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value, bit monitor error will trigger an interrupt	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.	1	ro	0x0
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

8.2.11.12 DL

0x50010C2C **DL**

DATA Length Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F5	DISAUTOSLEEP	Disable Auto Sleep. Set to Disable auto sleep.	1	rw	0x0
F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8).	4	rw	0x0

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

8.2.11.13 BTDIV07

0x50010C30																							BTDIV07							
Bit time Divider Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

8.2.11.14 BITTIME

0x50010C34																							BITTIME							
Control Settings.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		F1					F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F1	BTMULT	Bt Div Most Significant bit. Bit time multiplier [4:0]	5	rw	0x1
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

8.2.11.15 ID

0x50010C38																							ID							
ID Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

8.2.11.16 BUSTIME

0x50010C3C	BUSTIME

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)
0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F2	BUSINACTIVE	Bus Inactivity Time.	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

8.2.11.17 STATUSEXT

0x50010C40		STATUSEXT																													
Extended Status.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled & LIN Master's pullup will be reduced to 30K when BIT[1] is set.	2	ro	0x0
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

8.2.11.18 CONF

0x50010C48		CONF																													
Extended Configuration Register for compatibility issue.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F8	BITMONMODE	BIT Monitor Mode. Control the exit timing when bit monitor error occured. Only writable when the transaction is idle. 0x0: Default. The transmission finished immediately if bit_mon is detected. 0x1: Even bit_mon is detected, the transmission will not be finished until the byte transfer is completed.	1	rw	0x0
F0	INTERBYTECNT	Inter-Byte Space Bit Count. Bit count of inter-byte space. >= 1bit inter-byte space is required by some legacy LIN devices. Only writable when the transaction is idle.	2	rw	0x1

8.2.12 LINS

LINS		
Address	**Register**	**Description**
0x50011C00	DATABYTE1	Data Byte 1
0x50011C04	DATABYTE2	Data Byte 2
0x50011C08	DATABYTE3	Data Byte 3
0x50011C0C	DATABYTE4	Data Byte 4
0x50011C10	DATABYTE5	Data Byte 5
0x50011C14	DATABYTE6	Data Byte 6
0x50011C18	DATABYTE7	Data Byte 7
0x50011C1C	DATABYTE8	Data Byte 8

0x50011C20	CTRL	Control Register
0x50011C24	STATUS	Status
0x50011C28	ERROR	Error Register
0x50011C2C	DL	DATA Length Register
0x50011C30	BTDIV07	Bit time Divider Register
0x50011C34	BITTIME	Control Settings
0x50011C38	ID	ID Register
0x50011C3C	BUSTIME	Lin Bus Timing Register
0x50011C40	STATUSEXT	Extended Status
0x50011C48	CONF	Extended Configuration Register for compatibility issue
0x50011C4C	BAUDCTRL	BaudRate Control

8.2.12.1 DATABYTE1

0x50011C00	**DATABYTE1**				
Data Byte 1. DATA_BUF1~4 could be read/written through one word access to this register.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
F24	F16	F8	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F24	DATABUF4SHADOW	Data Buffer 4 Shadow. Shadow register of 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF3SHADOW	Data Buffer 3 Shadow. Shadow register of 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF2SHADOW	Data Buffer 2 Shadow. Shadow register of 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.2 DATABYTE2

0x50011C04	**DATABYTE2**				
Data Byte 2.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.3 DATABYTE3

0x50011C08	**DATABYTE3**				
Data Byte 3.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.4 DATABYTE4

0x50011C0C	DATABYTE4

Data Byte 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.5 DATABYTE5

0x50011C10	DATABYTE5

Data Byte 5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF8SHADOW	Data Buffer 8 Shadow. Shadow register of 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF7SHADOW	Data Buffer 7 Shadow. Shadow register of 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF6SHADOW	Data Buffer 6 Shadow. Shadow register of 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.6 DATABYTE6

0x50011C14	DATABYTE6

Data Byte 6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.7 DATABYTE7

0x50011C18	DATABYTE7

Data Byte 7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.8 DATABYTE8

0x50011C1C	DATABYTE8

Data Byte 8.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

8.2.12.9 CTRL

0x50011C20	CTRL
Control Register.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can not make use of the frame content with the received identifier(e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0 Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame. If DIS_AUTOSLEEP = 0, the bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected.	1	rw	0x1
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0
F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0
F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0

8.2.12.10 STATUS

0x50011C24	STATUS
Status.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct	1	ro	0x0

		SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active			
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register. The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence	1	ro	0x0
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

8.2.12.11 ERROR

0x50011C28								**ERROR**																					
Error Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F8	BITMONDATA	Bit Monitor Error occurred in Start or Data Bits. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the start or data bits.	1	ro	0x0
F7	BITMONSTOP	Bit Monitor Error occurred in Stop Bit. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the stop bit. In SAE2602, the error belongs to framing error.	1	ro	0x0
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value, bit monitor error will trigger an interrupt	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from	1	ro	0x0

		the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.			
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

8.2.12.12 DL

0x50011C2C																								DL							
DATA Length Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F5	DISAUTOSLEEP	Disable Auto Sleep. Set to Disable auto sleep.	1	rw	0x0
F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8).	4	rw	0x0

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

8.2.12.13 BTDIV07

0x50011C30																								BTDIV07							
Bit time Divider Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

8.2.12.14 BITTIME

0x50011C34	BITTIME
Control Settings.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

8.2.12.15 ID

0x50011C38	ID
ID Register.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

8.2.12.16 BUSTIME

0x50011C3C	BUSTIME

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)
0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F2	BUSINACTIVE	Bus Inactivity Time.	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

8.2.12.17 STATUSEXT

0x50011C40	STATUSEXT
Extended Status.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by	2	ro	0x0

		the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled & LIN Master's pullup will be reduced to 30K when BIT[1] is set.			
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

8.2.12.18 CONF

0x50011C48 **CONF**

Extended Configuration Register for compatibility issue.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F18	F17	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F18	DISBIT2CHECK	Disable Two Bits Width Check. Set to disable two bits width check for sync field. 0x0: Default.If the width mismatch is >25% between any two close bits and the 1st two bits, the byte will not be taken as a sync field. 0x1: Disabled. Recommended for the fast mode case that its baud rate is >=250KHz.	1	rw	0x0
F17	DUTYMAXSEL	Maximum Duty Select. Select the maximum duty constraint for sync field check. 0x0: Default. Check will fail if Duty > 68.75%. 0x1: Check will fail if Duty > 62.5%.	1	rw	0x0
F16	DUTYMINSEL	Minimum Duty Select. Select the minimum duty constraint for sync field check. 0x0: Default. Check will fail if Duty < 31.25%. 0x1: Check will fail if Duty < 37.5%.	1	rw	0x0
F8	BITMONMODE	BIT Monitor Mode. Control the exit timing when bit monitor error occured. Only writable when the transaction is idle. 0x0: Default. The transmission finished immediately if bit_mon is detected. 0x1: Even bit_mon is detected, the transmission will not be finished until the byte transfer is completed.	1	rw	0x0
F0	INTERBYTECNT	Inter-Byte Space Bit Count. Bit count of inter-byte space. >= 1bit inter-byte space is required by some legacy LIN devices. Only writable when the transaction is idle.	2	rw	0x1

8.2.12.19 BAUDCTRL

0x50011C4C **BAUDCTRL**

BaudRate Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0														

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIVSYNC	Bit BaudRate Divider. Bit BaudRate = Fsys/(2**PRESCL)/BT_DIV_SYNC. The register is automatically updated once a legal sync field is received.	15	rw	0x7FFF

8.2.13 EVTHOLD

EVTHOLD		
Address	**Register**	**Description**
0x50013000	HOLD	Hold

8.2.13.1 HOLD

0x50013000	**HOLD**
Hold.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	HOLD	Hold. Set to prevent serialisation of new non-wakeup events in prepartion for hibernate mode. At the point of becoming set, a request to send the lullaby interrupt is automatically generated. The lullaby handler can then safely assert the PMUA->CTRL.HIBERNATE bit in order to put the device into hibernate mode.	1	wo	0x0

8.2.14 SAR_CTRL

SAR_CTRL		
Address	**Register**	**Description**
0x50013400	DATA1	Data Out of CH1,
0x50013404	DATA2	Data Out of CH2,
0x50013408	DATA3	Data Out of CH3,
0x5001340C	DATA4	Data Out of CH4,
0x50013410	DATA5	Data Out of CH5,
0x50013414	DATA6	Data Out of CH6,
0x50013418	DATA7	Data Out of CH7,
0x5001341C	DATA8	Data Out of CH8,
0x50013420	DATA9	Data Out of CH9,
0x50013424	DATA10	Data Out of CH10,
0x50013428	SARCFG	SAR Configuration Register
0x5001342C	AFECTRL	SAR AFE Control
0x50013430	SARCTRL	SAR ADC Control
0x50013434	ADCCHCONF	ADC Channel Configuration
0x50013438	ADCCHSELR	ADC Channel Selection Register
0x5001343C	ADCCHCTRL0R	ADC Channel Control0 Register
0x50013440	ADCCHCTRL1R	ADC Channel Control1 Register
0x50013444	ADCCHCTRL2R	ADC Channel Control2 Register
0x50013448	SARINT	SAR Interrupts
0x5001344C	SARCLKDIV	SAR CLOCK DIVIDE

8.2.14.1 DATA1

0x50013400	**DATA1**
Data Out of CH1,.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA1	The result of ADC conversion of CH1(in 2's-complement)	16	ro	0x0

8.2.14.2 DATA2

0x50013404	DATA2

Data Out of CH2,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA2	The result of ADC conversion of CH2(in 2's-complement)	16	ro	0x0

8.2.14.3 DATA3

0x50013408	DATA3

Data Out of CH3,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA3	The result of ADC conversion of CH3(in 2's-complement)	16	ro	0x0

8.2.14.4 DATA4

0x5001340C	DATA4

Data Out of CH4,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA4	The result of ADC conversion of CH4(in 2's-complement)	16	ro	0x0

8.2.14.5 DATA5

0x50013410	DATA5

Data Out of CH5,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA5	The result of ADC conversion of CH5(in 2's-complement)	16	ro	0x0

8.2.14.6 DATA6

0x50013414	DATA6

Data Out of CH6,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA6	The result of ADC conversion of CH6(in 2's-complement)	16	ro	0x0

8.2.14.7 DATA7

0x50013418								DATA7																							
Data Out of CH7,.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA7	The result of ADC conversion of CH7(in 2's-complement)	16	ro	0x0

8.2.14.8 DATA8

0x5001341C								DATA8																							
Data Out of CH8,.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA8	The result of ADC conversion of CH8(in 2's-complement)	16	ro	0x0

8.2.14.9 DATA9

0x50013420								DATA9																							
Data Out of CH9,.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA9	The result of ADC conversion of CH9(in 2's-complement)	16	ro	0x0

8.2.14.10 DATA10

0x50013424								DATA10																							
Data Out of CH10,.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA10	The result of ADC conversion of CH10(in 2's-complement)	16	ro	0x0

8.2.14.11 SARCFG

0x50013428								SARCFG																							
SAR Configuration Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F24				-	-	-	-	-	-	F16		-	F12			F8				F7	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F24	TRIGDLY	trigger delay. setting trigger delay time from 0 to 15 sar clock cycles. For PN-detect, trigger delay MUST >= 2us.	4	rw	0x8
F16	PWMSEL1	PWM Period Trigger Signal Selects. Selects the PWM Period trigger Source. 0x0: Triggered by PWM Period 0x1: Triggered by PWM Aux counter0 Period 0x2: Triggered by PWM Aux counter1 Period	2	rw	0x0
F12	PWMSEL	PWM Edge Trigger Signal Selects. Selects the PWM Edge trigger Source. 0x0: Triggered by PWM0 edge 0x1: Triggered by PWM1 edge 0x2: Triggered by PWM2 edge 0x3: Triggered by PWM AUX0 edge 0x4: Triggered by PWM AUX1 edge 0x5: Triggered by PWM AUX2 edge 0x6: Triggered by PWM AUX3 edge 0x7: Triggered by PWM AUX4 edge	3	rw	0x0
F8	TRIGSEL	SAR Converion Trigger Selects. Selects the trigger condition of SAR ADC. Don't change the bits during an ADC conversion sequence is ongoing. 0x1: Triggered through writing 1 to conversion bit. 0x2: Triggered by PWM posedge. 0x4: Triggered by PWM negedge. 0x8: Triggered by PWM period.	4	rw	0x0
F7	ROUND	ADC round enable. Enable ADC round. 0x0: No round. 0x1: Negative code+1	1	rw	0x1

8.2.14.12 AFECTRL

0x5001342C **AFECTRL**

SAR AFE Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F7	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	SARPREAMPEN	adc pre-amp enable. 0:disable, 1:enable	1	rw	0x0
F7	SARAFEEN	ADC AFE Enable. adc afe enable. If vinp, vinn and vin vcm all choose external, adc afe should be disabled: adc_adc_en=0, otherwise, adc afe must be enabled: adc_afe_en=1.	1	rw	0x0
F0	ADCSELVINVCMEXT	Select External Inputs to ADC. choose ADC input common voltage. 0: choose internal vin_vcm, equals to (vinp+vinn)/2; 1: choose external vin_vcm, for PN detect.	1	rw	0x0

8.2.14.13 SARCTRL

0x50013430 **SARCTRL**

SAR ADC Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F18	-	F16	-	-	-	-	-	F10	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F18	CONT	Continuous Conversion Enable. If this bit has been set before an ADC conversion sequence trigged by CONVERT bit or PWM signals, the	1	rw	0x0

		sequence will be treated as a sequential conversion, rather than a single conversion.			
F16	CONVERT	ADC START/STATUS Register. If SOFTWARE trigger source is selected, set to start a conversion, If HARDWARE trigger source is selected, write to this field will be ignored. Read 1 indicates ADC conversion is active; Read 0 indicates ADC is in idle state.	1	dual	0x0
F10	DIGRESET	SAR Digital Part Reset. Resets SAR digital parts. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	SARENAREQ	SAR ADC Enable. Set to enable the SAR analog & digital part	1	rw	0x0

8.2.14.14 ADCCHCONF

0x50013434																															
ADCCHCONF																															
ADC Channel Configuration.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	F24					-	-	-	F16					-	F10					F5					-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	TESTBATTERYGAINCHOOSE	VBAT Gain Select. 0: gain=1/14, vbat max 30V/14=2.14v, under ADC vref=2.4v 1: gain=1/28, vbat max 30V/28=1.07v, under ADC vref=1.2v	1	rw	0x0
F24	CH4SEL	Channel4 Selection. Refer to Channel1 Selects.	5	rw	0x0
F16	CH3SEL	Channel3 Selection. Refer to Channel1 Selects.	5	rw	0x0
F10	CH2SEL	Channel2 Selection. Refer to Channel1 Selects.	5	rw	0x0
F5	CH1SEL	Channel1 Selection. Channel1 Selects. 0x1: adc_vinp=adc_refp , adc_vinn=adc_refp (all shot to adc_ref(2.4V) for adc channel offset K) 0x2: adc_vinp=adc_refp , adc_vinn=vref_gnd (for adc channel +gain error K) 0x3: adc_vinp=vref_gnd , adc_vinn=adc_refp (for adc channel -gain error K) 0x4: adc_vinp=TempSensor , adc_vinn=vref_gnd 0x5: adc_vinp=VDD_1V5 , adc_vinn=vref_gnd 0x6: adc_vinp=VDD_3V3 , adc_vinn=vref_gnd. If IOCTRL.GPIOCONSEL is set when measuring this channel, IOCTRL.GPIOCONREG[0] must also set. 0x7: adc_vinp=VDD_PRE5V (1/4) , adc_vinn=vref_gnd. If IOCTRL.GPIOCONSEL is set when measuring this channel, IOCTRL.GPIOCONREG[2] must also set. 0x8: adc_vinp=VBAT ACCURATE (gain selected by TEST_BATTERY_GAIN_CHOOSE), adc_vinn=vref_gnd 0x9: adc_vinp=LED0 , adc_vinn=vref_gnd.(for short gnd detecting) 0xa: adc_vinp=LED1 , adc_vinn=vref_gnd.(for short gnd detecting) 0xb: adc_vinp=LED2 , adc_vinn=vref_gnd.(for short gnd detecting) 0xc: adc_vinp=PA0 , adc_vinn=vref_gnd 0xd: adc_vinp=PA1 , adc_vinn=vref_gnd 0xe: adc_vinp=PA2 , adc_vinn=vref_gnd 0xf: adc_vinp=PA3 , adc_vinn=vref_gnd 0x10: adc_vinp=PA4 , adc_vinn=vref_gnd 0x11: adc_vinp=PA5 , adc_vinn=vref_gnd 0x12: adc_vinp=PA6 , adc_vinn=vref_gnd 0x13: adc_vinp=PA7 , adc_vinn=vref_gnd 0x14: adc_vinp=PB0 , adc_vinn=vref_gnd 0x15: adc_vinp=PB1 , adc_vinn=vref_gnd 0x16: Reserved 0x17: adc_vinp=PB3 , adc_vinn=vref_gnd 0x18: adc_vinp=VBAT , adc_vinn=LED0 0x19: adc_vinp=VBAT , adc_vinn=LED1 0x1a: adc_vinp=VBAT , adc_vinn=LED2	5	rw	0x0

F0	SEQCNT	Channel Sequence count. Selects the sequence of channels to be converted 0x1: CH1 only 0x2: CH1->CH2 0x3: CH1->CH2->CH3 0x4: CH1->CH2->CH3->CH4 0x5: CH1 to CH5 sequentially 0x6: CH1 to CH6 sequentially 0x7: CH1 to CH7 sequentially 0x8: CH1 to CH8 sequentially 0x9: CH1 to CH9 sequentially 0xa: CH1 to CH10 sequentially	4	rw	0x0

8.2.14.15 ADCCHSELR

0x50013438 **ADCCHSELR**

ADC Channel Selection Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F25						F20				F15					F10					F5							F0		

#	Field Name	Field Description	Width	Access	Reset
F25	CH10SEL	Channel10 Selection. Refer to Channel1 Selects.	5	rw	0x0
F20	CH9SEL	Channel9 Selection. Refer to Channel1 Selects.	5	rw	0x0
F15	CH8SEL	Channel8 Selection. Refer to Channel1 Selects.	5	rw	0x0
F10	CH7SEL	Channel7 Selection. Refer to Channel1 Selects.	5	rw	0x0
F5	CH6SEL	Channel6 Selection. Refer to Channel1 Selects.	5	rw	0x0
F0	CH5SEL	Channel5 Selection. Refer to Channel1 Selects.	5	rw	0x0

8.2.14.16 ADCCHCTRL0R

0x5001343C **ADCCHCTRL0R**

ADC Channel Control0 Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F18		F16		F14		F12		F10		F8		F6		F4		F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F29	SARINPUTGAINCH10	ADC Channel10 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F28	SARINPUTGAINCH9	ADC Channel9 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F27	SARINPUTGAINCH8	ADC Channel8 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F26	SARINPUTGAINCH7	ADC Channel7 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F25	SARINPUTGAINCH6	ADC Channel6 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F24	SARINPUTGAINCH5	ADC Channel5 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1

F23	SARINPUTGAINCH4	ADC Channel4 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F22	SARINPUTGAINCH3	ADC Channel3 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F21	SARINPUTGAINCH2	ADC Channel2 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F20	SARINPUTGAINCH1	ADC Channel1 input gain. 0x0: 22/32 0x1: 31/32	1	rw	0x1
F18	SAR_INPUT_MODE_CH10	CH10 AFE Input Modes. ADC AFE Input Modes for Channel10.	2	rw	0x3
F16	SAR_INPUT_MODE_CH9	CH9 AFE Input Modes. ADC AFE Input Modes for Channel9.	2	rw	0x3
F14	SAR_INPUT_MODE_CH8	CH8 AFE Input Modes. ADC AFE Input Modes for Channel8.	2	rw	0x3
F12	SAR_INPUT_MODE_CH7	CH7 AFE Input Modes. ADC AFE Input Modes for Channel7.	2	rw	0x3
F10	SAR_INPUT_MODE_CH6	CH6 AFE Input Modes. ADC AFE Input Modes for Channel6.	2	rw	0x3
F8	SAR_INPUT_MODE_CH5	CH5 AFE Input Modes. ADC AFE Input Modes for Channel5.	2	rw	0x3
F6	SAR_INPUT_MODE_CH4	CH4 AFE Input Modes. ADC AFE Input Modes for Channel4.	2	rw	0x3
F4	SAR_INPUT_MODE_CH3	CH3 AFE Input Modes. ADC AFE Input Modes for Channel3.	2	rw	0x3
F2	SAR_INPUT_MODE_CH2	CH2 AFE Input Modes. ADC AFE Input Modes for Channel2.	2	rw	0x3
F0	SAR_INPUT_MODE_CH1	CH1 AFE Input Modes. ADC AFE Input Modes for Channel1. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x3

8.2.14.17 ADCCHCTRL1R

0x50013440 **ADCCHCTRL1R**

ADC Channel Control1 Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F28				F24				F20				F16				F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F28	SAMPCYCCH8	Channel8 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F24	SAMPCYCCH7	Channel7 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F20	SAMPCYCCH6	Channel6 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F16	SAMPCYCCH5	Channel5 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F12	SAMPCYCCH4	Channel4 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F8	SAMPCYCCH3	Channel3 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F4	SAMPCYCCH2	Channel2 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F0	SAMPCYCCH1	Channel1 Sample cycle. setting sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycles 0x2: 3 Cycles ... 0xf: 16 Cycles Note: 1. For PN Detect sample, sampcyc need to >=2.2us 2. For non-PN Detect sample, sampcyc need to >=1.2us	4	rw	0x7

8.2.14.18 ADCCHCTRL2R

0x50013444																ADCCHCTRL2R															
ADC Channel Control2 Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F26		F24		F22		F20		F18		F16		F14		F12		F10		F8		F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F26	ADCVREFSELCH10	Channel10 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F24	ADCVREFSELCH9	Channel9 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F22	ADCVREFSELCH8	Channel8 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F20	ADCVREFSELCH7	Channel7 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F18	ADCVREFSELCH6	Channel6 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F16	ADCVREFSELCH5	Channel5 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F14	ADCVREFSELCH4	Channel4 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F12	ADCVREFSELCH3	Channel3 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F10	ADCVREFSELCH2	Channel2 adc vref select. Refer to ADC_VREF_SEL_CH1.	2	rw	0x1
F8	ADCVREFSELCH1	Channel1 adc vref select. 0x0: adc_vref = vbg 0x1: adc_vref = 2*vbg 0x2: adc_vref = VDD_3V3 0x3: adc_vref = VDD_3V3	2	rw	0x1
F4	SAMPCYCCH10	Channel10 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7
F0	SAMPCYCCH9	Channel9 Sample cycle. Refer to SAMPCYC_CH1.	4	rw	0x7

8.2.14.19 SARINT

0x50013448																															
SAR Interrupts. Contains the enable, status and clear for the SAR interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	INT_TRIG_CLASH	Trigger Clash Interrupt. Set by the SAR when TRIG_CLASH is high and INT_TRIG_CLASH_ENA is set	1	ro	0x0
F24	INT_CONV_DONE	Convert Done Interrupt. Set by the SAR when an convert done occurs	1	ro	0x0
F17	TRIG_CLASH	Trigger Clash. Set by the SAR when new trigger issued when previous has not finished.	1	ro	0x0
F16	CONV_DONE	Convert Done. Set by the SAR when an conversion is done.	1	ro	0x0
F9	INT_TRIG_CLASH_CLR	Trigger Clash Interrupt Clear.	1	wo	0x0
F8	INT_CONV_DONE_CLR	Convert Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	INT_TRIG_CLASH_ENA	Trigger Clash Interrupt Enable.	1	rw	0x0
F0	INT_CONV_DONE_ENA	Convert Done Interrupt Enable.	1	rw	0x0

8.2.14.20 SARCLKDIV

0x5001344C																SARCLKDIV															
SAR CLOCK DIVIDE. sar clock divider. sar_div_clk is divided from system clock, sar_div_clk maximum frequency is 4Mhz.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	SARCLKDIV	SAR CLOCK DIVIDE. Divide ration is (SAR_CLK_DIV+1)	8	rw	0x3

8.2.15 SPI

SPI		
Address	**Register**	**Description**
0x50015000	SPIRXDATA	Serial Peripheral Rx Data Register
0x50015004	SPITXDATA	Serial Peripheral Tx Data Register
0x50015008	SPICTRL	Serial Peripheral Control Register
0x5001500C	SPISTATUS	Serial Peripheral Status Register
0x50015010	SPIINTSTATUS	SPI Interrupt Status
0x50015014	SPIINTENABLE	SPI Interrupt Enable
0x50015018	SPIINTCLEAR	SPI Interrupt Clear

8.2.15.1 SPIRXDATA

0x50015000		**SPIRXDATA**			
Serial Peripheral Rx Data Register.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	RXDATA	Rx Data buffer. Received Data Register. A read from this register will return data from current read pointer on the receive FIFO. A read from this register will increment the read pointer on the receive FIFO.	8	ro	0x0

8.2.15.2 SPITXDATA

0x50015004		**SPITXDATA**			
Serial Peripheral Tx Data Register.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	TXDATA	Tx Data buffer. Transmit Data Register. Used for data that is to be transmitted. A write to this register will place data into the transmit FIFO and increment the write pointer for the transmit FIFO.	8	wo	0x0

8.2.15.3 SPICTRL

0x50015008		**SPICTRL**			
Serial Peripheral Control Register.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - F24	- - - - - - - F16	- - - - - - F8	F6 F5 F4 F2 F1 F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**

F24	FIFOSOFTRESET	FIFO Soft Reset. FIFO Soft Reset bit (active high). Writing a one here will clear the FIFO pointers. This bit automatically clears to zero.	1	wo	0x0
F16	LPBK	Port wired-OR mode bit. 0x0: master_in = miso 0x1: master_in = mosi	1	rw	0x0
F8	ICNT	Interrupt counter bits. 0x0: Interrupt is set after every completed transfer 0x1: Interrupt is set after two completed transfers 0x2: Interrupt is set after three completed transfers 0x3: Interrupt is set after four completed transfers	2	rw	0x0
F6	SCKEXT	Extended clock divider. SPR - Standard Clock Rate Divider Select SPRE (SCKEXT) - Extended Clock Rate Select Bits {SPRE, SPR} = Clock Divide Result {00, 00}: System Clock / 2 {00, 01}: System Clock / 4 {00, 10}: System Clock / 8 {00, 11}: System Clock / 32 {01, 00}: System Clock / 64 {01, 01}: System Clock / 16 {01, 10}: System Clock / 128 {01, 11}: System Clock / 256 {10, 00}: System Clock / 512 {10, 01}: System Clock / 1024 {10, 10}: System Clock / 2048 {10, 11}: System Clock / 4096 {11, xx}: Reserved	2	rw	0x0
F5	CPOL	SPI clock polarity (Motorola SPI Frame Format). 0x0: The base value of the clock is zero 0x1: The base value of the clock is one	1	rw	0x0
F4	CPHA	SPI clock phase. 0x0: Data is captured on clock transition from base and data is propagated on the clock transition to base 0x1: Data is captured on clock transition to base and data is propagated on the clock transition from base	1	rw	0x0
F2	SPR	Standard clock divider selection. Please refer to SPRE register for system clock.	2	rw	0x0
F1	ENA_STS	SPI enable status. Status of SPI enable	1	ro	0x0
F0	ENA_REQ	SPI enable request. Enables the SPI interface. When SPI enable is deasserted the Tx and Rx FIFO's are still operable. Careful- If data is present in the Tx FIFO prior to enabling SPI, then once SPI is enabled it will begin transmitting the data present in the Tx FIFO.	1	rw	0x0

8.2.15.4 SPISTATUS

0x5001500C **SPISTATUS**

Serial Peripheral Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	F16					-	-	-	F8					-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TXFIFOCOUNT	Transmit FIFO Count. Signal indicates active number of bytes in the FIFO. Increments on Push. Decrements on Pop.	5	ro	0x0
F8	RXFIFOCOUNT	Reception FIFO Count. Signal indicates active number of bytes in the FIFO. Increments on Push. Decrements on Pop.	5	ro	0x0

F6	TXFIFOFULL	Transmit FIFO full. 0x0: FIFO is NOT full 0x1: FIFO is full	1	ro	0x0
F5	TXFIFOEMPTY	Transmit FIFO empty. 0x0: FIFO is NOT empty 0x1: FIFO is empty	1	ro	0x1
F4	RXFIFOFULL	Reception FIFO full. 0x0: FIFO is NOT full 0x1: FIFO is full	1	ro	0x0
F3	RXFIFOEMPTY	Reception FIFO empty. 0x0: FIFO is NOT empty 0x1: FIFO is empty	1	ro	0x1
F2	TXFIFOOF	Transmit FIFO overflow. 0x0: overflow inactive 0x1: overflow active	1	ro	0x0
F1	RXFIFOUF	Reception FIFO underflow. 0x0: underflow inactive 0x1: underflow active	1	ro	0x0
F0	XFERCNT	Completed Transfer Count. Signal is set after a programmable amount of completed transfer. See SPI_CTRL register field ICNT.	1	ro	0x0

8.2.15.5 SPIINTSTATUS

0x50015010	**SPIINTSTATUS**
SPI Interrupt Status. Read this register to establish the reason for an SPI interrupt. This interrupt status is reporting the status after the interrupt enable. All interrupts are OR'ed together into a single SPI IRQ signal.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOF	Transmit FIFO Overflow Interrupt. Interrupt is set when Transmit FIFO is full and a write transaction occurs. (WRITE COLLISION)	1	ro	0x0
F1	INTRXFIFOUF	Reception FIFO Underflow Interrupt. Interrupt is set when Receive FIFO is empty and a read transaction occurs. (READ COLLISION)	1	ro	0x0
F0	INTXFERCNT	SPI Transfer Count Interrupt. Interrupt is set after a programmable amount of completed transfer. See SPI_CTRL register field ICNT.	1	ro	0x0

8.2.15.6 SPIINTENABLE

0x50015014	**SPIINTENABLE**
SPI Interrupt Enable. SPI Interrupt Enable Register	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOFENA	Transmit FIFO Overflow Interrupt Enable.	1	rw	0x0
F1	INTRXFIFOUFENA	Reception FIFO Underflow Interrupt Enable.	1	rw	0x0
F0	INTXFERCNTENA	SPI Transfer Count Interrupt Enable.	1	rw	0x0

8.2.15.7 SPIINTCLEAR

0x50015018	**SPIINTCLEAR**
SPI Interrupt Clear. SPI Interrupt Clear Register	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOFCLR	Transmit FIFO Overflow Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	INTRXFIFOUFCLR	Reception FIFO Underflow Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	INTXFERCNTCLR	SPI Transfer Count Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0

8.2.16 UART0

UART0		
Address	**Register**	**Description**
0x50015400	DATA	Data
0x50015404	UARTDATARECEIVESTATUS	Data Receive Status
0x50015408	MSGCTRL	Message control
0x5001540C	UARTINT	UART Interrupts
0x50015410	UARTINT2	Extended UART Interrupts
0x50015414	UARTBAUD	UART Baud rate
0x50015418	UARTFIFO	UART FIFO interface

8.2.16.1 DATA

0x50015400	DATA

Data.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DUMMY2	Data. Used for both received data and data that is to be transmitted.	8	dual	0x0
F16	DUMMY1	Data. Used for both received data and data that is to be transmitted.	8	dual	0x0
F8	DUMMY0	Data. Used for both received data and data that is to be transmitted.	8	dual	0x0
F0	BYTE	Data. Used for both received data and data that is to be transmitted.	8	dual	0x0

8.2.16.2 UARTDATARECEIVESTATUS

0x50015404	UARTDATARECEIVESTATUS

Data Receive Status. This register contains the receive status associated with the current byte read from the UART_DATA register.
The Data Receive Status register is updated only after a read from the UART_DATA register.
Example- Read UART_DATA byte first. Then read UART_DATA_RECEIVE_STATUS register second.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BREAKERROR	Break Error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than	1	ro	0x0

		a full-word transmission time (defined as start, data, parity, and stop bits).			
F1	PARITYERROR	Parity Error. When this bit is set to 1, it indicates that the parity of the received data character has parity error.	1	ro	0x0
F0	FRAMEERROR	Framing Error. When this bit is set to 1, it indicates that the received byte did not have a valid stop bit (a valid stop bit is 1).	1	ro	0x0

8.2.16.3 MSGCTRL

0x50015408 **MSGCTRL**

Message control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F23	F22	-	-	-	-	-	-	-	-	F13	F12	F11	F10	F8		-	-	-	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F23	LOOPENA	Loopback enable. Set to enable loopback	1	rw	0x0
F22	BREAKENA	Break enable. Set to force transmission of zero (for a break condition)	1	rw	0x0
F13	STICKENA	Sticky parity enable. Set to enable sticky parity	1	rw	0x0
F12	PARODD	Odd parity. 0x0: ODD Parity 0x1: EVEN parity	1	rw	0x0
F11	PARENA	Parity enable. Set to enable parity (see PARODD for odd/even)	1	rw	0x0
F10	STOP	Stop bit control. 0x0: One stop bit 0x1: If a 5-bit transmission it selects 1.5 stop bits, otherwise 2 stop bits (6, 7 & 8 bits)	1	rw	0x0
F8	SIZE	Transmission word size. 0x0: 5-bit 0x1: 6-bit 0x2: 7-bit 0x3: 8-bit	2	rw	0x3
F4	TXXFERCNTCLR	TX Transfer Counter Clear. Clear TX Multi Transfer Counter to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	RXXFERCNTCLR	RX Transfer Counter Clear. Clear RX Multi Transfer Counter to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F2	UFIFOSOFTRESET	FIFO SOFT RESET. Resets FIFO pointers to zero and initializes FIFO contents to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	ENABLE_STS	Enable status. Status of UART enable	1	ro	0x0
F0	ENABLE	Enable. Set to enable the UART	1	rw	0x0

8.2.16.4 UARTINT

0x5001540C **UARTINT**

UART Interrupts. Contains the enable, status and clear for the UART interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	INT_TXMULTDONE_IRQ	Multiple Transmit Transactions Done Interrupt. Set by the UART when the programmed number of transmit transactions have completed. See UART_FIFO_LEVEL_CTL register.	1	ro	0x0

F30	INT_RXMULTDONE_IRQ	Multiple Receive Transactions Done Interrupt. Set by the UART when the programmed number of receive transactions have completed. See UART_FIFO_LEVEL_CTL register	1	ro	0x0
F29	INT_TXDONE_IRQ	Transmission done Interrupt. Set by the UART when the transmission is done	1	ro	0x0
F28	INT_BREAKKERR_IRQ	Break Error Interrupt. Set by the UART when a break error occurs	1	ro	0x0
F27	INT_PRTYERR_IRQ	Parity Error Interrupt. Set by the UART when a parity error occurs	1	ro	0x0
F26	INT_FRMERR_IRQ	Framing error Interrupt. Set by the UART when a framing error occurs	1	ro	0x0
F25	INT_OVRUNERR_IRQ	RX FIFO overflow error Interrupt. Set by the UART when an overrun error occurs	1	ro	0x0
F24	INT_RXDONE_IRQ	Rx Data ready Interrupt. Set by the UART when Rx data is ready	1	ro	0x0
F23	INT_TXMULTDONE_STS	Multiple Transmit Transactions Done. Set by the UART when the programmed number of transmit transactions have completed. See UART_FIFO_LEVEL_CTL register.	1	ro	0x0
F22	INT_RXMULTDONE_STS	Multiple Receive Transactions Done. Set by the UART when the programmed number of receive transactions have completed. See UART_FIFO_LEVEL_CTL register	1	ro	0x0
F21	INT_TXDONE_STS	Transmission is done. Set by the UART when the transmit is done	1	ro	0x0
F20	INT_BREAKKERR_STS	Break IRQ. Set by the UART when a break error occurs	1	ro	0x0
F19	INT_PRTYERR_STS	Parity Error. Set by the UART when a parity error occurs	1	ro	0x0
F18	INT_FRMERR_STS	Framing error. Set by the UART when a framing error occurs	1	ro	0x0
F17	INT_OVRUNERR_STS	RX FIFO overflow error. Set by the UART when an overrun error occurs	1	ro	0x0
F16	INT_RXDONE_STS	Rx Data ready. Set by the UART when Rx data is ready	1	ro	0x0
F15	INT_TXMULTDONE_CLR	Multiple Transmit Transactions Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F14	INT_RXMULTDONE_CLR	Multiple Receive Transactions Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F13	INT_TXDONE_CLR	Transmission done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F12	INT_BREAKKERR_CLR	Break Error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	INT_PRTYERR_CLR	Parity Error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F10	INT_FRMERR_CLR	Framing error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F9	INT_OVRUNERR_CLR	RX FIFO overflow error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	INT_RXDONE_CLR	Rx Data ready Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F7	INT_TXMULTDONE_ENA	Multiple Transmit Transactions Done Interrupt Enable.	1	rw	0x0
F6	INT_RXMULTDONE_ENA	Multiple Receive Transactions Done Interrupt Enable.	1	rw	0x0
F5	INT_TXDONE_ENA	Transmission done Interrupt Enable.	1	rw	0x0
F4	INT_BREAKKERR_ENA	Break Error Interrupt Enable.	1	rw	0x0
F3	INT_PRTYERR_ENA	Parity Error Interrupt Enable.	1	rw	0x0

F2	INT_FRMERR_ENA	Framing error Interrupt Enable.	1	rw	0x0
F1	INT_OVRUNERR_ENA	RX FIFO overflow error Interrupt Enable.	1	rw	0x0
F0	INT_RXDONE_ENA	Rx Data ready Interrupt Enable.	1	rw	0x0

8.2.16.5 UARTINT2

0x50015410								UARTINT2																					
Extended UART Interrupts. Contains the enable, status and clear for the extended UART interrupt sources.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	F18	F17	F16	-	-	-	-	-	F10	F9	F8	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F26	INT_OVERRUNERR_IRQ	TX FIFO overflow error Interrupt. Set by the UART when an TX FIFO overflow error interrupt occurs.	1	ro	0x0
F25	INT_UNRUNERR_IRQ	RX FIFO underflow error Interrupt. Set by the UART when an under flow error interrupt occurs.	1	ro	0x0
F24	INT_RXTOUT_IRQ	Rx Time-out Interrupt. Set by the UART when RXTOUT flag is set and RXOUT interrupt is enabled.	1	ro	0x0
F18	INT_OVERRUNERR_STS	TX FIFO overflow error. Set by the UART when an TX FIFO overflow error occurs.	1	ro	0x0
F17	INT_UNRUNERR_STS	RX FIFO underflow error. Set by the UART when an under flow error occurs.	1	ro	0x0
F16	INT_RXTOUT_STS	Rx Time-out. Set by the UART when timeout of 4 data frame times without reception, and data received(one or three bytes received,programmable)	1	ro	0x0
F10	INT_OVERRUNERR_CLR	TX FIFO overflow error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F9	INT_UNRUNERR_CLR	RX FIFO underflow error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	INT_RXTOUT_CLR	Rx Time-out Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F2	INT_OVERRUNERR_ENA	TX FIFO overflow error Interrupt Enable.	1	rw	0x0
F1	INT_UNRUNERR_ENA	RX FIFO underflow error Interrupt Enable.	1	rw	0x0
F0	INT_RXTOUT_ENA	Rx Time-out Interrupt Enable.	1	rw	0x0

8.2.16.6 UARTBAUD

0x50015414								UARTBAUD																					
UART Baud rate. The controls in this register define the relationship between the system clock and the UART baud rate. The baud rate is given by the following equation. baud_rate = Fclk/(OSR*(BAUDDIV+1+FDIV/8)) where Fclk is the frequency of the system clock, and OSR , FDIV and BAUDDIV are the fields of this register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F30	F29	F24					-	-	-	-	-	F3																F0		

#	Field Name	Field Description	Width	Access	Reset
F30	URETARD	Retard Register. Retards the sample window by 1 cycle. For Debug.	1	rw	0x0
F29	UADVANCE	Advance Register. Advances the sample window by 1 cycle. For Debug.	1	rw	0x0
F24	OSR	Over-sampling ratio. Valid OSR Range: 6 to 16.	5	rw	0x10
F3	BAUDDIV	Baud rate divider.	16	rw	0x0

F0	FDIV	Fractional divider.	3	rw	0x0

8.2.16.7 UARTFIFO

0x50015418								UARTFIFO																						
UART FIFO interface. The FIFO register is gives the current state of the Receive and Transmit FIFO's and defines the trigger points for the transmit and receive interrupts.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F24					-	-	-	F16					F11					F10	F9	-	F3					F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F24	TXMULTIPLEXFERDONECNT	Transmit Data Count Interrupt. Number of bytes transmitted from the transmit FIFO before a INT_TX_MULTIPLE_XFER_DONE interrupt is asserted. Example: A value of 4 would be used to compare to the number of completed transfers (pops from the Tx FIFO). Valid Range: 1 to 16	5	rw	0x1
F16	RXMULTIPLEXFERDONECNT	Receive Data Count Interrupt. Minimum number of bytes in the receive FIFO before a INT_RX_MULTIPLE_XFER_DONE interrupt is asserted. Example: A value of 4 would be used to compare to the number of receive transactions (pushes to the Rx FIFO). Valid Range: 1 to 16	5	rw	0x1
F11	TXCOUNT	Transmit FIFO current count.	5	ro	0x0
F10	TXFULL	Transmit FIFO full.	1	ro	0x0
F9	TXEMPTY	Transmit FIFO empty.	1	ro	0x0
F3	RXCOUNT	Reception FIFO current count.	5	ro	0x0
F2	RXFULL	Reception FIFO full.	1	ro	0x0
F1	RXEMPTY	Reception FIFO empty.	1	ro	0x0

8.2.17 SYSCFG

SYSCFG		
Address	**Register**	**Description**
0x50020000	SRAMCFGR	SRAM Configuration Register
0x50020004	SRAMRACR	SRAM Raw Access Control Register
0x50020008	SRAMWPKEYR	SRAM Write Protection Register key register
0x5002000C	SRAMWPR	SRAM Write Protection Register
0x50020010	M0IVTRKEYR	M0 Interrupt Vector Table write key register
0x50020014	M0IVTR	M0 Interrupt Vector Table Register

8.2.17.1 SRAMCFGR

0x50020000								SRAMCFGR																						
SRAM Configuration Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	F24	F23	-	-	-	-	F18	F17	F16	-	-	-	-	-	F0										

#	Field Name	Field Description	Width	Access	Reset

F31	SRAMWRECCDIS	SRAM WRITE ECC Disable bit. 0x0: SRAM WRITE ECC function enabled 0x1: SRAM WRITE ECC function disabled	1	rw	0x0
F24	SRAMRDECCDIS	SRAM READ ECC Disable bit. 0x0: SRAM READ ECC function enabled 0x1: SRAM READ ECC function disabled	1	rw	0x1
F23	SRAMECCCIE	SRAM ECC correction interrupt enable. 0x0: SRAMECCC interrupt disabled 0x1: SRAMECCC interrupt enabled	1	rw	0x0
F18	FLSECCDNMI	Flash ECC detection Indication. This bit reflect status of ECCD bit of register FLSECCR.	1	ro	0x0
F17	SRAMECCD	SRAM ECC detection. Set by hardware when two bits ECC errors has been detected and corrected when access SRAM. When this bit is set, a NMI is generated. Cleared by writing 1.	1	dual	0x0
F16	SRAMECCC	SRAM ECC correction. Set by hardware when one bit ECC error has been detected and corrected when access sram. An interrupt is generated if SRAMECCIE is set. Cleared by writing 1.	1	dual	0x0
F0	SRAMECCADDR	SRAM ECC Error Address.	11	ro	0x0

8.2.17.2 SRAMRACR

0x50020004	**SRAMRACR**

SRAM Raw Access Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F24	RD_ECC_RAW	ECC Raw Value for Read. This field store the data from SRAM bit[38:32] when SRAM_RAWACC_EN is set.	7	ro	0x0
F16	WR_ECC_RAW	ECC Raw Value for Write. This field will write to SRAM when bit[31:24] is writing and SRAM_RAWACC_EN is set.	7	rw	0x0
F0	SRAM_RAWACC_EN	SRAM Raw Access Enable. Set to enable raw access to SRAM. ***NOTE:****SRAM_ECC_DIS need to set when executing raw access.*	1	rw	0x0

8.2.17.3 SRAMWPKEYR

0x50020008	**SRAMWPKEYR**

SRAM Write Protection Register key register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	SRAMWPKEY	Write pretection key for SRAMWPR to take effect. A value of 0x26 must be written to this address to allow SRAMWPR to take effect.	8	rw	0x0

8.2.17.4 SRAMWPR

0x5002000C	**SRAMWPR**

SRAM Write Protection Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	SRAMWP	SRAM Write Protection. Each bit protect 1Kbyte SRAM area, bit0 correspondint the first 1Kbyte. This field is set only. NOTE:The write operation of this field register takes effect by configuring 'SYSCFG->SRAMWPKEYR.SRAMWPKEY = 0x26 0x0: Corresponding 1K area can be modified 0x1: Corresponding 1K area write protected	16	rw	0x0

8.2.17.5 M0IVTRKEYR

0x50020010 **M0IVTRKEYR**

M0 Interrupt Vector Table write key register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	M0IVTRKEY	Write pretection key for M0IVTR to take effect. A value of 0x53 must be written to this address to allow M0IVTR to take effect.	8	rw	0x0

8.2.17.6 M0IVTR

0x50020014 **M0IVTR**

M0 Interrupt Vector Table Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F16	IVTRAMSEL	IVT SRAM Selection. This field contains the selection of the interrupt vector table location. NOTE:The write operation of this field register takes effect by configuring 'SYSCFG->M0IVTRKEYR.M0IVTRKEY = 0x53 0x0: IVT is located in Flash 0x1: IVT is located in SRAM	1	rw	0x0
F0	IVTBADDR	Interrupt Vector Table Base Address. This field contains the base address of the interrupt vector table remapping block. IVT_BADDR will be used to replace Address[15:8] if Address[31:8] is equal to 0x0 (Access first 256 byte space). When IVTRAMSEL=0, remapped address will be {Address[31:16],IVTBADDR,Address[7:0]}; When IVTRAMSEL=1, remapped address will be {16'h2000,IVTBADDR,Address[7:0]}. NOTE:The write operation of this field register takes effect by configuring 'SYSCFG->M0IVTRKEYR.M0IVTRKEY = 0x53	8	rw	0x0

8.2.18 FLASH

FLASH		
Address	**Register**	**Description**
0x50021000	FLADDR	Destination address for flash write or erase operation
0x50021004	DATALR	Data (least-significant word)
0x50021008	DATAMR	Data (most-significant word)
0x5002100C	ECCVALR	ECC value
0x50021010	UNLBWR	Flash write unlock register
0x50021014	BWRSTRTR	Flash write start register

0x50021018	UNLERSR	Flash erase unlock register
0x5002101C	ERSSTRTR	Flash erase start register
0x50021020	FLSCPR	Flash code protection register
0x50021024	FLSWPKEYR	Flash write protection key register
0x50021028	FLSWP0R	Flash write protection 0 register
0x5002102C	FLSWP1R	Flash write protection 1 register
0x50021030	FLS_UNLOCK_CTRL_OPR	Flash Unlock Control Operation Register
0x50021034	CTRL_OPR	Flash Control Operation Register
0x50021038	FLSECCR	Flash ECC Register
0x5002103C	TRIM	Flash Trim Register
0x50021040	FLSSTATR	Flash Status Register
0x50021044	FLSOPTL0R	Flash Operation Time Length 0 Register
0x50021048	FLSOPTL1R	Flash Operation Time Length 1 Register
0x5002104C	DATAFIELDCTRL	Flash data field with optional ecc register

8.2.18.1 FLADDR

0x50021000																**FLADDR**															
Destination address for flash write or erase operation.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3													-	-	-

#	Field Name	Field Description	Width	Access	Reset
F3	FLASHADDR	Target flash line for write/erase operation. In byte writes, this is the line address of the flash to be written to. In erase modes, it is an address inside the sector to be erased. ***NOTE:****This register must be written in the correct sequence or the operation will fail.*	13	rw	0x1FFF

8.2.18.2 DATALR

0x50021004																**DATALR**															
Data (least-significant word).																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	DATAL	Data (least-significant word). The least-significant, 32-bit word of data that will be written to Flash	32	rw	0x0

8.2.18.3 DATAMR

0x50021008																**DATAMR**															
Data (most-significant word).																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	DATAM	Data (most-significant word). The most-significant, 32-bit word of data that will be written to Flash	32	rw	0x0

8.2.18.4 ECCVALR

0x5002100C	ECCVALR

ECC value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	ECCVAL	ECC value. If ECCSTREN = 1, 8bit redundant bits will be stored into ECCVAL during each flash fetch operation. ***NOTE:*** *If RDECCEN = 1, this field may be corrected by ECC algorithm.*During programming ECCVAL will be copied to the 8bit redundant bits of a Flash word. This field will update by syndrome code generated by ECC encoder when DATAM is written with 32-bit data. This field can still be updated by software after hardware update, through this method we can implement raw data program into flash 72bit line.	8	dual	0x1

8.2.18.5 UNLBWR

0x50021010	UNLBWR

Flash write unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_WRITE	Control register to unlock write. A value of 0x55555555 must be written to this address at the correct point in the write sequence or the operation will fail. Bit 0 will be set if 0x55555555 is written, and will be clear if write operation is started successfully or any other value is written the this register. Other bits read return zero.	32	dual	0x0

8.2.18.6 BWRSTRTR

0x50021014	BWRSTRTR

Flash write start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	WRITE_START	Control register to start a write. A value of 0xAAAAAAAA must be written to this address at the correct point in the write sequence or the operation will fail. Read return zero.	32	wo	0x0

8.2.18.7 UNLERSR

0x50021018	UNLERSR

Flash erase unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_ERASE	Control register to unlock a erase operation. A value of 0x66666666 must be written to this address at the correct point in the erase sequence or the operation will fail.	32	dual	0x0

		Bit 0 will be set if 0x66666666 is written, and will be clear if erase operation is started successfully or any other value is written the this register. Other bits read return zero.			

8.2.18.8 ERSSTRTR

0x5002101C		ERSSTRTR			
Flash erase start register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	ERASE_START	Control register to commit a sector erase. A value of 0x99999999 must be written to this address at the correct point in the sector erase sequence or the operation will fail. Read return zero.	32	wo	0x0

8.2.18.9 FLSCPR

0x50021020		FLSCPR			
Flash code protection register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CODE_PROT	Code Protection / SerialWire Lockout Control Write a value of 0xF2E11047 to disable the SerialWire interface. Write other values will enable it. This allows the user program to disable the SerialWire interface to prevent unauthorized debug access to the part. Bit 0 will be set if 0xF2E11047 is written, and will be clear if any other value is written the this register. Other bits read return zero. ***NOTE1:****This register does not lock the Flash Memory against read/write/erase by the applications program. Instead what it does is to disable all communications with the debug interface, therefore preventing any external attack. The application code is still able to modify the flash content.* ***NOTE2:****Upon Power-On Reset or Normal Reset the system disables the communication for a small time interval (8192 clock cycles). If the application needs to be protected it is mandatory to set this register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication.*	32	dual	0x0

8.2.18.10 FLSWPKEYR

0x50021024		FLSWPKEYR			
Flash write protection key register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	WPKEY	Flash write pretection key for FLSWPx to take effect. A value of 0x12100511 must be written to this address to allow FLSWP0 and FLSWP1 to take effect. Once FLSWPx have taken effect it will be locked for safety. Bit 0 will be set if 0x12100511 is written, and can only be cleared by system reset. Other bits read return zero.	32	dual	0x0

8.2.18.11 FLSWP0R

0x50021028		FLSWP0R			
Flash write protection 0 register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	FLSWP0	Flash write protection field protect one kilo byte by one bit. Bit0 protect the first KB, bit1 for the second KB, ... ***NOTE:****This field only take effect after correct key has been written to FLSWPKEYR. And this field can not be modified after taking effect.*	32	rw	0x0

8.2.18.12 FLSWP1R

0x5002102C		FLSWP1R			
Flash write protection 1 register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - - - - - F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	FLSWP1	Flash write protection field protect one kilo byte by one bit. Bit0 protects the 33th KB, bit1 for the 34th KB, ... ***NOTE:****This field only take effect after correct key has been written to FLSWPKEYR. And this field can not be modified after taking effect.*	16	rw	0x0

8.2.18.13 FLS_UNLOCK_CTRL_OPR

0x50021030		FLS_UNLOCK_CTRL_OPR			
Flash Unlock Control Operation Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	UNLOCK_CTRL_OP	Flash Control Operation Register Unlock value. 0xACDC_1972 needs to be written in this register to unlock the Control Operation Register access. When this register is read, it returns the state of the lock: 0: The Control Operation Register is locked. The CHIPSEL bit of FLASH_CTRL_OPR cannot be written. 1: The Control Operation Register is unlocked. The CHIPSEL bit of FLASH_CTRL_OPR can be written. ***NOTE:****After each write to the third byte of FLASH_CTRL_OPR register, the state of the lock is cleared and the pattern needs to be written again to allow a new configuration of the register.*	32	dual	0x0

8.2.18.14 CTRL_OPR

0x50021034		CTRL_OPR			
Flash Control Operation Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - F24 - - - F20 F19 F18 - F16 - - - - - - - F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**

F24	FRWS	Flash Read Wait State Number. Number of wait states used in the reading process. Each read from flash memory will take number of cycles equal to 1+FRWS to complete. ***NOTE:****FRWS = 0 is adequate for normal read. When in margin read, make sure (1 + FRWS) * Fhclk is slower than 225ns.*	2	rw	0x2
F20	ERSVREAD	Erase Margin Read Enable. Set to enable margin read for erase cell verification. ***NOTE:****After set ERSVREAD, must wait one cycle to issued new flash read to execute erase margin read.*	1	rw	0x0
F19	PROGVREAD	Program Margin Read Enable. Set to enable margin read for program cell verification. ***NOTE:****After set PROGVREAD, must wait one cycle to issued new flash read to execute program margin read.*	1	rw	0x0
F18	ECCSTREN	ECC Store Enable. When set, 8bit redundant bits will be stored into ECCVAL during every flash fetch operation.	1	rw	0x0
F16	CHIPSEL	CHIP selection bit. This bit is only used during the Erase operation. It allows the system to execute mass erase. 0: The Erase operation will only erase the sector selected by the FLASH_ADDR register value. 1: The Erase operation will erase the full main array of the flash. ***NOTE:****CHIPSEL can only be written when bit-0 of FLS_UNLOCK_CTRL_OPR is set.*	1	rw	0x0
F0	BYTESEL	Byte selection of the write operation. Set to 1 indicated the corresponding byte will be programmed. ***NOTE:****BYTESEL's set bits must be continuous, otherwise will cause unintentional chaos. ex. 9'b11100_0000, 9'b00011_1110, 9'b00000_0011, 9'b00000_1000 are valid setting, 9'b01011_1111, 9'b01001_0000 are not allowed.*	9	rw	0x0

8.2.18.15 FLSECCR

0x50021038 **FLSECCR**

Flash ECC Register.
While ECCD is set, FLSECCR is not updated if a new ECC error occurs. FLSECCR is updated only when ECCD is cleared.
While ECCC is set, FLSECCR will only be updated when a new ECC detection occurs. In this situation, ECCC flag will keep but ECCC's fail address in ADDRECC and NVRFECC will update to ECCD's fail address.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	-	-	-	-	-	F24	F23	F22	F21	F20	-	-	-	-	-	-	-	F0												

#	Field Name	Field Description	Width	Access	Reset
F31	ECCD	ECC detection. Set by hardware when two ECC errors has been detected. When this bit is set, a NMI is generated. Cleared by writing 1.	1	dual	0x0
F30	ECCC	ECC correction. Set by hardware when one ECC error has been detected and corrected. An interrupt is generated if ECCIE is set. Cleared by writing 1.	1	dual	0x0
F24	WPVIOL	Write Protection Violation. Set by hardware when flash write protection has been violated. An interrupt is generated if WPVIOLIE is set. Cleared by writing 1.	1	dual	0x0
F23	WPVIOLIE	Write Protection Violation interrupt enable. 0x0: WPVIOL interrupt disabled 0x1: WPVIOL interrupt enabled	1	rw	0x0
F22	ECCCIE	ECC correction interrupt enable. 0x0: ECCC interrupt disabled 0x1: ECCC interrupt enabled	1	rw	0x0
F21	RDECCEN	Read ECC correction and detection Enable. ECC correction and detection will only be enabled when RDECCEN is set.	1	rw	0x0

F20	NVRFECC	NVR ECC fail. This bit indicates that the ECC error correction or double ECC error detection is located in the NVR Flash memory.	1	ro	0x0
F0	ADDRECC	ECC fail double-word address offset. In case of ECC error or ECC correction detected, this bitfield contains double-word offset (multiple of 64 bits) to Main Flash memory or to NVR1.	13	ro	0x0

8.2.18.16 TRIM

0x5002103C																													
TRIM																													
Flash Trim Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	OSC_TRIM	Flash Oscillator Trim Value. This register will be automatically populated with the value stored in the least significant bits of NVR sector 1 (@0002_0000).	8	dual	0x86

8.2.18.17 FLSSTATR

0x50021040																													
FLSSTATR																													
Flash Status Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F8	OPBSY	Flash operatoin busy indication. Reading 1 indicate program/erase operation busy. ***NOTE:****In the SWD erase operation, OPBSY may be started 256 cycles later after command issued.*	1	ro	0x0

8.2.18.18 FLSOPTL0R

0x50021044																													
FLSOPTL0R																													
Flash Operation Time Length 0 Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F16						F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PGTL	Program Time Length. This register define the duration of byte program operation in number of 4M oscillator's cycles. Default duration is 6750ns	6	rw	0x1B
F0	SERTL	Sector Erase Time Length. This register define the duration of sector erase operation in number of 4M oscillator's cycles. Default duration is 4.5ms	16	rw	0x4650

8.2.18.19 FLSOPTL1R

0x50021048																													
FLSOPTL1R																													
Flash Operation Time Length 1 Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0																

#	Field Name	Field Description	Width	Access	Reset

F0	MERTL	Chip Mass Erase Time Length. This register define the duration of chip mass erase operation in number of 4M oscillator's cycles. Default duration is 30ms	17	rw	0x1D4C0

8.2.18.20 DATAFIELDCTRL

0x5002104C																															
DATAFIELDCTRL																															
Flash data field with optional ecc register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8							-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	DATAFIELDADDR	Flash data field base address. Flash data field base address. DATAFIELDADDR = 0 represent DATA field start at the first sector, DATAFIELDADDR = 95 represent DATA field start at the last sector,and ends at the end address of the 96th sector	7	rw	0x5F
F0	DATAECCDIS	0x0: ECC for data field enabled 0x1: ECC for data field disabled	1	rw	0x0

8.2.19 TIMER0

TIMER0		
Address	**Register**	**Description**
0x50022000	COUNT	Timer Counter Register
0x50022004	CFG	Timer Control Register

8.2.19.1 COUNT

0x50022000																															
COUNT																															
Timer Counter Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.19.2 CFG

0x50022004																															
CFG																															
Timer Control Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

8.2.20 TIMER1

TIMER1		
Address	**Register**	**Description**
0x50022008	COUNT	Timer Counter Register
0x5002200C	CFG	Timer Control Register

8.2.20.1 COUNT

0x50022008																															
COUNT																															
Timer Counter Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.20.2 CFG

0x5002200C																															
CFG																															
Timer Control Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

8.2.21 TIMER2

TIMER2		
Address	**Register**	**Description**
0x50022010	COUNT	Timer Counter Register
0x50022014	CFG	Timer Control Register

8.2.21.1 COUNT

0x50022010																															
COUNT																															
Timer Counter Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset

F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

8.2.21.2 CFG

0x50022014																															
CFG																															
Timer Control Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

8.2.22 WDT1

WDT1		
Address	**Register**	**Description**
0x50022018	CFG	Config
0x5002201C	KEY	Key

8.2.22.1 CFG

0x50022018																															
CFG																															
Config.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3		F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	PRESET	Preset. Defines the watchdog timeout period. It means that the WDT internal counter will count from 0 to the prescaler value at the system clock speed and trigger if not cleared. For instance, a system running from a 30MHz Crystal with WDTPRES[1I0] = 10 will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application. 0x0: 2^13 / System Clock 0x1: 2^19 / System Clock 0x2: 2^22 / System Clock 0x3: 2^32 / System Clock	2	rw	0x0
F2	RSTFLAG	Reset flag. This flag is set by the system at the initialization if the initialization was caused by a reset triggered by the WDT. The bit can be cleared by the application.	1	rw	0x0
F1	RSTEN	Reset enable. If enabled a WDT time-out will force the microcontroller to reset. This bit can be asserted but it cannot be de-asserted.	1	rw	0x0
F0	ENA	WDT Enable. This bit can be asserted but it cannot be de-asserted. It means that once the WDT is enabled it cannot be turned off until a Reset or Power-On Reset occurs.	1	rw	0x0

8.2.22.2 KEY

0x5002201C	KEY

Key. Writing the sequence CLEAR, KEY0, KEY1 to this register will clear (pet) the watchdog - preventing it from timing out and resetting the system.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	KEY	Key. To clear the WDT counting the following words must be written in this order and without any other instruction between then: 0x3C570001 0x007F4AD6	32	rw	0x0

8.2.23 CRC

CRC		
Address	**Register**	**Description**
0x50022100	CRCDR	CRC Data Register
0x50022104	CRCIR	CRC Initial Value Register
0x50022108	CRCCR	CRC Control Register

8.2.23.1 CRCDR

0x50022100	CRCDR

CRC Data Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	CRCDATA3	**CRC data bits**. This register is used to write new data to the CRC calculator. When read it returns the previous CRC calculation result or the data write to CRCINIT If the data size is less than 32 bits, only the least significant bits will be take effect. ex. byte write to field [15:8] will be ignored, half-word write to bit field [31:16] will be ignored	8	dual	0xFF
F16	CRCDATA2	**CRC data bits**. This register is used to write new data to the CRC calculator. When read it returns the previous CRC calculation result or the data write to CRCINIT If the data size is less than 32 bits, only the least significant bits will be take effect. ex. byte write to field [15:8] will be ignored, half-word write to bit field [31:16] will be ignored	8	dual	0xFF
F8	CRCDATA1	**CRC data bits**. This register is used to write new data to the CRC calculator. When read it returns the previous CRC calculation result or the data write to CRCINIT If the data size is less than 32 bits, only the least significant bits will be take effect. ex. byte write to field [15:8] will be ignored, half-word write to bit field [31:16] will be ignored	8	dual	0xFF
F0	CRCDATA0	**CRC data bits**. This register is used to write new data to the CRC calculator. When read it returns the previous CRC calculation result or the data write to CRCINIT If the data size is less than 32 bits, only the least significant bits will	8	dual	0xFF

		be take effect. ex. byte write to field [15:8] will be ignored, half-word write to bit field [31:16] will be ignored			

8.2.23.2 CRCIR

0x50022104		CRCIR			
CRC Initial Value Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CRCINIT	**CRC initial value**. This register is used to write the CRC initial value. The data write to this register will be stored in CRCDATA until it replaced by new calculated result ***NOTE:****This register can only be writen by word*	32	wo	0xFFFFFFFF

8.2.23.3 CRCCR

0x50022108		CRCCR			
CRC Control Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F2 F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F2	REVOUT	**Reverse output data**. This bit controls the reversal of the bit order of the output data. 0x0: Bit order not affected 0x1: Bit order is reversed	1	rw	0x0
F0	REVIN	**Reverse input data**. These bits control the reversal of the bit order of the input data 0x0: Bit order not affected 0x1: Bit reversal done by byte 0x2: Bit reversal done by half-word 0x3: Bit reversal done by word	2	rw	0x0

9 DEVICE FUNCTIONAL DESCRIPTION

9.1 MCU FEATURES

9.1.1 Power on sequence

Figure 10 shows the power on sequence , VDD3V3/ VDD1V5 connect to the external 4.7uF capacitor.

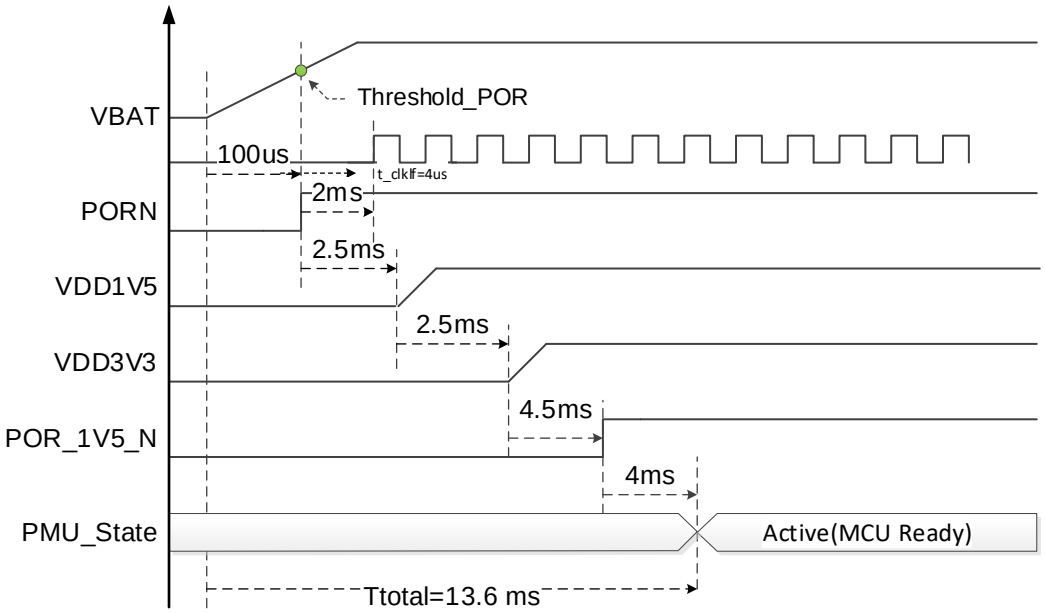


Figure 10 power on sequence

ASIC has an On-chip Brown-out Detection (BOD) circuit for monitoring the VCC level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by the BOR3V3THRESH / BOR1V5THRESH. The trigger level has a hysteresis to ensure spike free Brown-out Detection.

When the BOR ACTION is configured as hard reset, and VDD_3V3/ VDD_1V5 decreases to a value below the trigger level (Threshold_BOR_3V3/Threshold_BOR_1V5 – in Figure 11Figure 8), the Brown-out Reset(BORN) is activated. When VCC increases above the trigger level, the BORN is released.

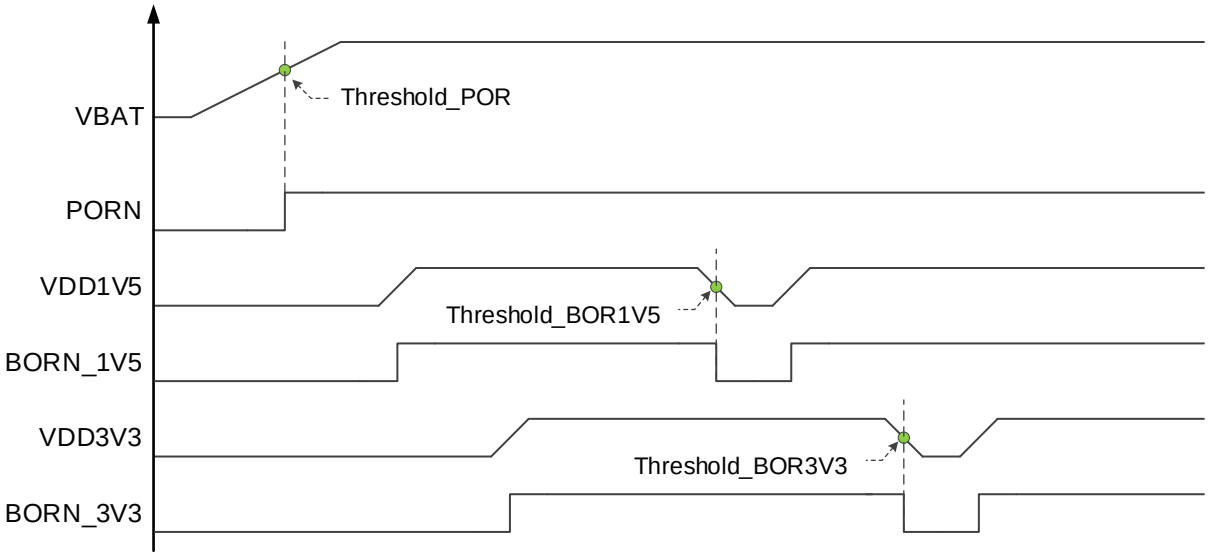


Figure 11 BORN Generation

9.1.2 MCU Core

The chip implements one ARM Cortex M0 core.

Additional documentation on ARM Cortex-M0 32 bits microcontroller can be found at

http://www.arm.com/products/processors/cortex-m/cortex-m0.php

9.1.3 System Memory (SRAM)

MCU core implements 8kbytes of SRAM. MCU can execute codes from the SRAM memories.

9.1.4 Flash Non Volatile Memory

MCU implements a Programmable Flash Memory with x72 configuration, sector and chip erase and byte program capability. It integrates five 512bytes nonvolatile registers (NVR) sectors.

In normal operation the ARM core fetches instructions (or data permanently stored) from the Flash memory but it is also possible for a program to alter the content of the flash memory. The following operations can be performed in the Flash Memory:

- Byte Write
- Sector Erase
- Block Erase
- Code Protect

For a description of the flash memory registers, please refer to the product register map. Here is a simple description of the basic features supported:

- Registers support to write/erase data to a byte, sector address
- Support programmable read wait states*
- Support system clock divider for write/erase functions
- Protection mechanism to unlock flash memory write and start flash memory byte-write
- Protection mechanism to unlock flash memory sector erase

* The design is implemented such that the timings associated with the flash macro meet the maximum speed of the system clock requirements.

9.1.5 Interrupt vectors

The first 148 bytes of Flash Memory are organized following the standard created by ARM. In this standard the Address 0x00000 contains the top-of-stack address (four bytes). The following addresses contain interrupt vectors used by the microcontroller:

Table 8 Interrupt Vector

Vector Name	Address	Comments
STACK_VALUE	0x00000	Typically set to 0x20000FFFF (Top of SRAM)
Reset_Handler	0x00004	Reset routine entry
Reserved	0x00008	Reserved. No NMI implemented.
HardFault Handler	0x0000C	
Reserved	0x00010 to 0x00028	

SVC_Handler	0x0002C	
Reserved	0x00030-0x00034	
PendSV_Handler	0x00038	
SysTick_Handler	0x0003C	
WULIN_Handler,	0x00040	Wake Up LIN Slave
IOCTRLA_Handler,	0x00044	LINS TxD Dominant Timeout
WUTIMER_Handler,	0x00048	Wake Up Timer
BOR_Handler,	0x0004C	Brown out event
WatchdogA_Handler,	0x00050	ASIC watchdog timeout
UV_Handler,	0x00054	Under voltage event
OV_Handler,	0x00058	Over voltage event
LINS_Handler,	0x0005C	LIN Slave bus event
ADC_Handler,	0x00060	ADC data ready
PWM_Handler,	0x00064	PWM event
GPIO_Handler,	0x0006C	GPIO Interrupts
OVTEMP_Handler,	0x00074	Over Temperature event
Reserved	0x00078	Reserved
Lullaby_Handler,	0x0007C	Software Interrupt
Timer0_Handler	0x00080	
Timer1_Handler	0x00084	
Timer2_Handler	0x00088	
Watchdog_Handler	0x0008C	

BTE_Handler	0x00090	Block Transfer – Contact indie to get more information.
Reserved	0x00094	

All other addresses in the flash memory can be used for the user's program.

The meanings of the standard interrupt vectors (Provided with the ARM Cortex M0 core) are defined in ARM's documentation. One of the sources of information is:

http://infocenter.arm.com/help/topic/com.arm.doc.dui0497a/DUI0497A_cortex_m0_r0p0_generic_ug.pdf

9.1.6 Interrupt Enabling/Disabling Process

Cortex-M0 implements a NVIC (**N**ested **V**ector **I**nterrupt **C**ontroller) peripheral capable of handling up to 16 peripheral's interrupts. Upon reset the microcontroller can answer only to Reset, NMI (Non-Maskable Interrupt) and Hard-Fault interrupts/exceptions. All other interrupts must be enabled. To enable and disable the interrupts the user must use access the ISER (Interrupt Set Enable Register) and ICER (Interrupt Clear Enable Interrupt) registers associated with the desired interrupt.

NOTE: Both inline functions and all parameters are defined in the product_file.h file, which must be included in the source files. Besides that the product_file.h file contains a list of available interrupts. The format of this list is as follows:

```
typedef enum IRQn
{
 //******  Cortex-M0 Processor Exceptions Numbers ***************************
 NonMaskableInt_IRQn    = -14,   // Non Maskable Interrupt
 HardFault_IRQn         = -13,   // Hard Fault Interrupt
 SVCall_IRQn            = -5,    // SV Call Interrupt
 PendSV_IRQn            = -2,    // Pend SV Interrupt
 SysTick_IRQn           = -1,    // System Tick Interrupt
```

```
//*****  CM0IKMCU Cortex-M0 specific Interrupt Numbers **********************
IRQ01_IRQn              = 0,     // Product specific
IRQ02_IRQn              = 1,     // Product specific
IRQ03_IRQn              = 2,     // Product specific
IRQ04_IRQn              = 3,     // Product specific
IRQ04_IRQn              = 4,     // Product specific
IRQ05_IRQn              = 5,     // Product Specific
IRQ06_IRQn              = 6,     // Product Specific
IRQ07_IRQn              = 7,     // Product Specific
IRQ08_IRQn              = 8,     // Product Specific
IRQ09_IRQn              = 9,     // Product Specific
IRQ10_IRQn              = 10,    // Product Specific
IRQ11_IRQn              = 11,    // Product Specific
IRQ12_IRQn              = 12,    // Product Specific
IRQ13_IRQn              = 13,    // Product Specific
IRQ14_IRQn              = 14,    // Product Specific
IRQ15_IRQn              = 15,    // Product Specific
TIMER0_IRQn             = 16,    // Timer 0
TIMER1_IRQn             = 17,    // Timer 1
TIMER2_IRQn             = 18,    // Timer 2
WATCHDOG_IRQn           = 19,    // Watchdog timer
IRQ20_IRQn              = 20,    // Product Specific
IRQ21_IRQn              = 21,    // Product Specific
IRQ22_IRQn              = 22     // Product Specific

} IRQn_Type;
```

9.1.7 Flash Code protection

The controlled access to the flash content is based on disabling all communications with the debug interface, therefore preventing any external attack. Hence, the application code is still able to modify the Flash content.

Upon Power-On Reset or Normal Reset, MCU core disables the communication with the debug interface for a small time interval (8192 system clock cycles). If the application needs to be protected it is mandatory to set the protection register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication. In other words, if during this time interval the protection register is loaded with a specific pattern, then the communication remains disabled after the end of this interval and stays disabled until this register is loaded with a different pattern. To allow for debug communication the application has only to write a different value in the lock register.

If a part is protected, the emulator can still erase and program the part, but first it will be required to erase the Flash content, therefore protecting it.

9.1.8 Systick Timer

This timer is an optional peripheral created by ARM and implemented in the Cortex M0 160/8. It is fully described in the Cortex-M0 Devices Generic User Guide (Chapter 4.4 Optional System Timer, Systick) found at:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0497a/Babieigh.html

9.1.9 Timers (0, 1 and 2)

The MCU implements three identical timers: Timer0, Timer1 and Timer2. All three timers operate using the system clock as clock source. They increment at the system clock rate starting from the loaded value in the counter until they roll over from 0xFFFFFFFF to 0x00000000. At this point an interrupt is generated if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.

9.1.10 Watch Dog Timer

The MCU implements a WDT (**W**atch **D**og **T**imer) that can operate in one of two ways:

- Interrupt Mode: In the event of a WDT rollover an interrupt will be generated.
- Reset Mode: In the event of a WDT rollover the microcontroller will reset.

The WDT supports Reset, Enable, status/flag and clear functions. It integrates a pre-scaler that can divide the system clock by 2^{13}, 2^{19}, 2^{22} or 2^{32}. It means that the WDT internal counter will count from 0 to the pre-scaler value at the system clock speed and trigger if not cleared.

For instance, a system running from a 30MHz system clock and 2^{22} pre-scaler value will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application.

9.1.11 MCU Core to ASIC interface

The ASIC die communicates with the indie Cortex M0 MCU through a proprietary interface. The interface enables any swap between ASIC die and MCU die and is transparent to software.

9.2 ASIC FEATURES

9.2.1 Clock Generation

Two clock sources are integrated in the device. The system clock is based on a RC network and will be trimmed to meet the accuracy requirements specified in the EC Table. Additionally, an auxiliary clock will be used during Hibernate/Deepsleep.

9.2.2 Reset

Both ASIC and MCU integrates Power on Reset (POR) circuitry: MCU POR monitors its input supply and generate a reset every time the MCU supply is recycled. ASIC POR monitors the main 1V5 LDO supply and generate a reset every time the LDO supply is recycled. Both POR maintain their output reset active as long as the monitored supply voltage is not above the minimum supply level to ensure safe logic operation of the Power Management Unit including the necessary analog features such as clock generator, bandgap, etc…This level is hardcoded and process technology dependent.

Additionally, the ASIC integrates Brown Out (BOR) circuit detectors that are configurable by SW (enable/disable as well as threshold programmable for the main ASIC core supply) and are actively

monitored by the ASIC power management unit (PMU). In case any BOR is triggered, the PMU can be configured to either do the following (per BOR blocks).

- trigger a system reset
- generate an interrupt to the MCU for further actions.
- do nothing

Finally, the MCU watchdog timer (if configured to do so) or a reset instruction can reset the MCU logic while on the ASIC side the watchdog timer (if configured to do so) or a reset register write can reset the ASIC system.

9.2.3 PMU and Load Dump Protect circuits

ASIC integrates battery monitoring functionality that will detect load dump events occurring at the battery supply pin. An analog comparator will detect over voltage transients after going through a load dump limitation circuit. The protection circuit can handle DC voltage up to 45V and will limit these to maximum of *Over Voltage Threshold* nominal, therefore the comparator will detect any over voltage transients at the battery pin beyond that threshold. The circuit will generate a digital output signal to be filtered and sent to the interrupt controller. The circuit will be active during normal operation mode – not during Hibernate condition.

The voltage regulators themselves are supplied by VBAT directly and sustain DC level of load dump voltages.

Meanwhile, the PMU integrated internal reference voltage and power supply, which include analog modules power supply, GPIO power supply 3.3V LDO and digital core power supply 1.5V LDO. And internal powerup state-machine guarantee PMU module to work stably.

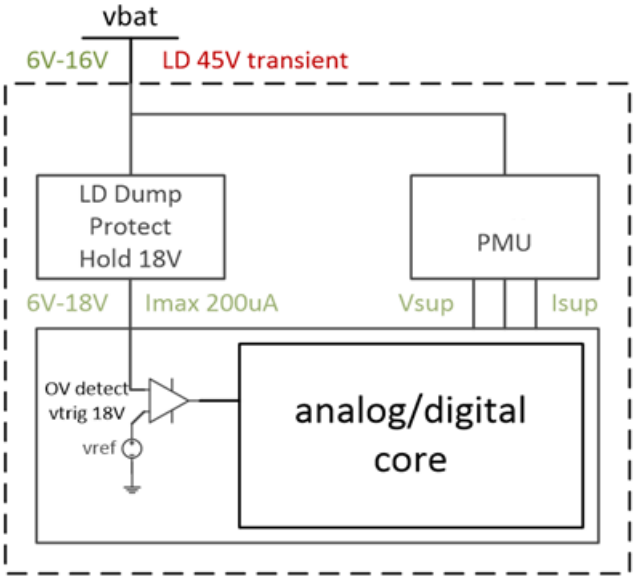


Figure 12 Load Dump Protect

9.2.4 LIN Interface

9.2.4.1 LIN Transceiver

Supports LIN Protocol Controller according to LIN 2.x and SAE J2602 (rev J2602-1_201211). The IC contains two integrated PHYs (One for Slave and the other for Master) for low speed vehicle serial data network communication using the LIN protocol.

Notice that LIN Master PHY is disconnected from LIN Master controller is the internal LIN Switch is enabled.

9.2.4.1.1 LIN RxD Debounce

For preventing RxD spikes in case of RF interferences and automotive pulses, two digital glitch filters are integrated in the data pathes of LIN RxD.

Debounce thresholds for low to high and high to low can be programmable independently.

$$T_{thres} = \left(T_{hfosc}\right) \times LINDBNCTHRESx$$

For instance, the default DBNCTHRES value is 0x30 and HFOSC freq is 16MHz.Thus the default debounce threshold is 62.5ns * 48 = 3 us.

9.2.4.1.2 LIN TxD Timeout Monitor

Two TxD Timout monitors are integrated to prevent dominant bus due to internal malfunction. LIN TX is controlled by TxD signal from LIN controller or GPA (Selected by bit LINS_HWMODE. If TxD is stuck at low over a specified TxD timeout time due to a crash of MCU/GPA/LIN Controller, the

integrated TxD monitor will switch off the LIN TX output automatically until a low to high transition of TxD.

9.2.4.1.3 Short LIN Bus to Ground

If the bus idle timeout monitor detects the bus is shorted to ground (See bit BUS_IDLE_TIMEOUT_DOMINANT, LIN Slave's 30K pullup will be automatically switched off to prevent a fast discharge of the car battery.

If enabled, the feature is always on even the chip is in hibernate mode.

9.2.4.1.4 External LIN Transceiver Mode

In this mode, the internal LIN transceiver is bypassed and LIN Slave controller's RxD/TxD can be connected with an external transceiver through GPIO3/4 or GPIO5/6; LIN Master controller's RxD/TxD can be connected with an external transceiver through GPIO1/2.

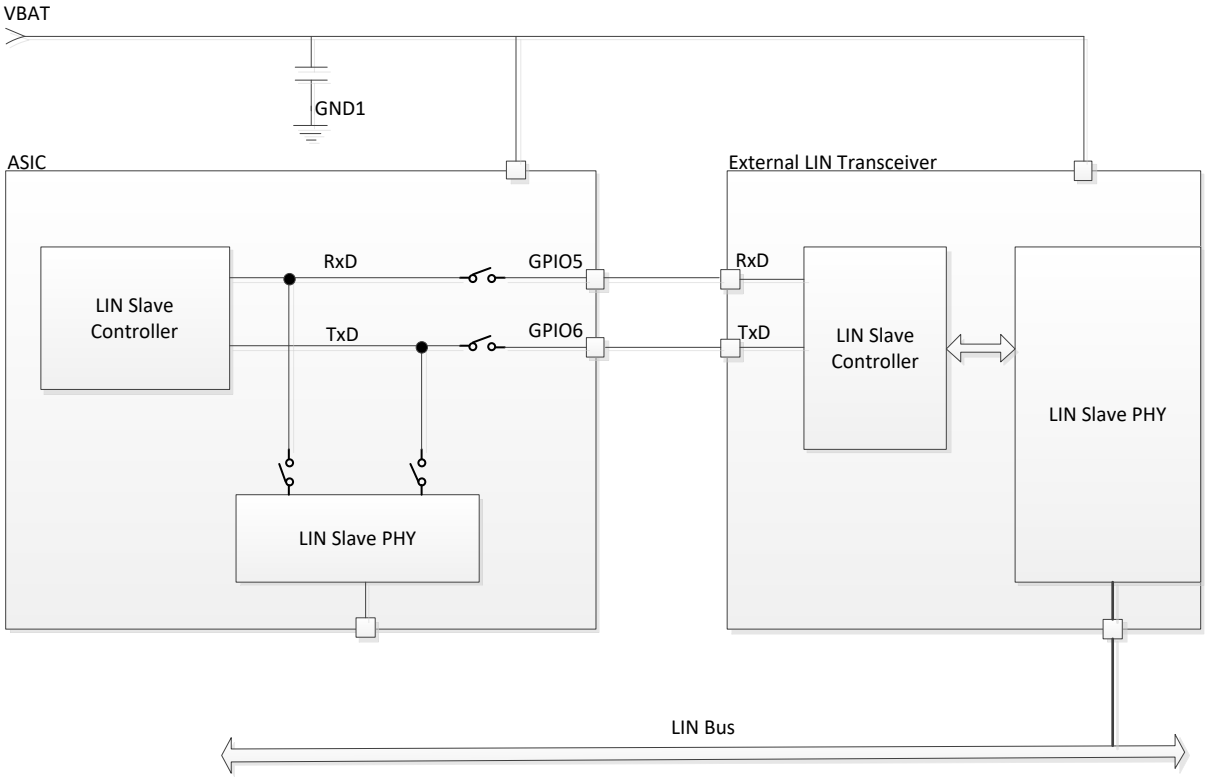


Figure 13 External LIN Transceiver Connection

9.2.4.2 LIN controller

The IC contains two LIN cores. One is for LIN Slave and the other is for LIN Master. The LIN core is a communication controller that performs serial communication. It implements the datalink layer of the LIN Protocol Specification. LIN uses a single master / multiple slave concept for the message transfer between nodes of the LIN network. The LIN controller core comprises an interface to connect

a micro controller that accesses the LIN core registers to control the transmission and reception of message frames.

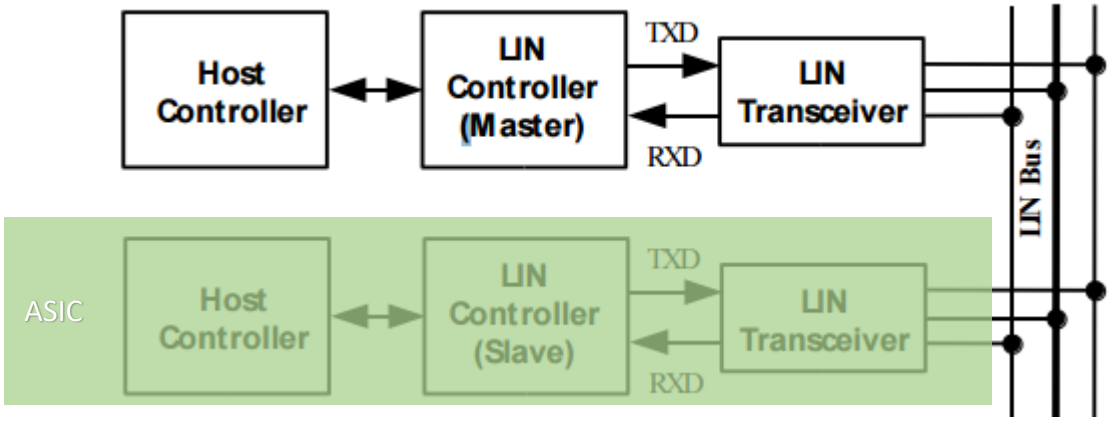


Figure 14 Lin System

Features:

- One LIN Slave Controller
  - Support of LIN specification 2.2A/SAE J2602
  - Backward compatibility to LIN 1.3
  - Supports LIN auto-addressing through an internal LIN switch.
- One LIN Master Controller
  - Only available when the internal LIN switch is not used.
  - Only supports auto-baudrate LIN Slaves.
- Programmable data rate between 1 Kbit/s and 20 Kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface
- Fully synchronous design, available in VHDL or Verilog, completely synthesizable
- Support auto addressing
  - Note: Node configuration and diagnostics implemented by the host controller

9.2.4.2.1 Data Length Register and Enhanced Checksum

The host controller has to define the length of the data field of the current LIN frame by adjusting the DATA LENGTH register. If the data length bits[3:0] are loaded with the value “1111b” the length of the data field is decoded from Bit 5 and 4 of the identifier register (ID) according to table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the DATA LENGTH register (supported values are 0...8).

Table 9 ID bits and number of bits

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

The LIN core supports classic checksum (Spec 1.3, inverted eight bit sum with carry over all data bytes) and enhanced checksum (Spec. 2.0, inverted eight bit sum with carry over all data bytes and protected identifier). The host controller has to set the checksum type used in the current frame by adjusting Bit ENCHK in the data length register (‘1’ for enhanced checksum, ‘0’ for classic checksum).

9.2.4.2.2 Timing Settings for "Wake up Repeat Time" and "Bus Inactivity Time"

The time for repeating of wake up because of no reaction on the bus and for go to sleep because of inactivity on the bus can be optionally written by the host controller to registers WUPREPEAT and BUSINACTIVE (address 0x0F).

Table 10 LIN Inactivity Time

BUSINACTIVE [1:0]	LIN Inactivity Time (sec.)
00	4*
01	6
10	8
11	10

Table 11 LIN Wake-Up Repeat Time

WUPREPEAT [1:0]	LIN Wake-Up Repeat Time (msec.)
00	180*
01	200
10	220
11	240

9.2.4.2.3 Bit Time Settings

The Bit rate of the LIN system has to be defined in the bit timing registers.

Table 12 Bit Timing Related Registers

Name	Description	Width(bits)
BTDIV	Bit time divider integer value	9
PRESCL	Clock Prescaler	2

The LIN bit rate *f*bit can be calculated from system clock *f*clk and bit timing registers according to the following general equation:

$$f_{bit} = \frac{f_{clock}}{2^{prescl} * bt\_div * (bt\_mul + 1)}$$

Note that the procedure of adjusting the bit timing registers is different between master and slave. For the slave controller, the Bit timing register adjustment of slave is the following:

The steps for adjusting the bit timing registers of the LIN slave are explained below.

Note: Register bt_mul does not exist in the slave. The LIN core slave synchronizes to any bit rate between 1 Kbit/s and 20 Kbit/s. Nevertheless, the bit timing registers have to be adjusted to adapt the LIN core to the used system clock frequency.

- Setting up the pre-scaler register depending on system clock according to the following equation; the value has to be rounded down to the next integer value:

$$prescl = \ln\left(\frac{f_{clock}}{20KHz * 200}\right) * \frac{1}{\ln 2}$$

- Adjusting the bit time divider depending on system clock and pre-scaler according to the following equation; the value has to be rounded down to the next integer value:

$$bt\_div = \frac{f_{clock}}{2^{prescl} * 20KHz}$$

Table 13 Sample value for setting up bit timing registers

System Clock	PRESCL	BTDIV
8MHz	1	200

12MHz	1	300
16MHz	2	200

9.2.4.2.4 Controlling the LIN core (slave) by a host controller

The first step before transmitting messages with the LIN core is setting up the bit rate of the LIN system. For that, the host controller has to load the bit time registers. After that, the message transfer can be started. The LIN core slave detects the header of the message frame sent by the LIN master and synchronizes its internal bit time to the master bit time. An interrupt to the host controller is requested after the reception of the IDENTIFIER FIELD, after the reception of a wakeup signal (if the slave is in sleep mode), when an error is detected or when the message transfer is completed.

The following steps have to be done by the host controller when an interrupt is requested.

1) Check bit DATAREQ in the status register (it is 1 when the IDENTIFIER FIELD has been received). Proceed with the following if DATAREQ is set else proceed with step 2.

    a. Load the identifier from the ID register and process it.
    b. Adjust the bit TRANSMIT in the control register (“1” - if the current frame is a transmit operation for the slave, “0” – if the current frame is a receive operation for the slave).
    c. Load the data length in the data LENGHT register (number of data bytes or value “1111b” if the data length should be decoded from the identifier) and set the checksum type (enhanced checksum (Bit ENHCHK = ‘1’) or classic checksum (Bit ENHCHK = ’0’)).
    d. Load the data to transmit into the data buffer (for transmit operation only).
    e. Set the bit DATAACK in the control register.

Note 1: Steps a..e have to be done during the IN-FRAME RESPONSE SPACE, if the current frame is a transmit operation for the slave; otherwise a timeout will be detected by the master. If the current frame is a receive operation for the slave, steps a..e have to be finished until the reception of the first byte after the IDENTIFIER FIELD. Otherwise, the internal receive buffer of the slave core will be overwritten and a timeout error will be detected in the slave core.

Note 2: If the host controller of the slave detects an unknown identifier (e.g. extended identifier) it has to write a ‘1’ to bit “stop” in control register instead of setting bit DATAACK (steps b .. e can be skipped). In that case the LIN core slave stops the processing of the LIN communication until the next SYNC BREAK is received.

2) Check bit ERROR in the status register. Perform error handling and proceed with step 6 if bit ERROR is set else proceed with step 3.

Note 3: Bit TIMEOUT in the error register and bit WAKEUP in the status register are set if the slave has sent a wakeup signal but the master did not respond within 150ms.

3) Check bit BUSIDLETIMEOUT in the status register and activate the sleep mode by setting bit SLEEP in the control register if BUSIDLETIMEOUT is set.
4) Check bit WAKEUP in the status register (it is set if the slave has received a wakeup signal). If WAKEUP is set proceed with step 6 else proceed with step 4.

Note 4: Bit COMPLETE in the status register is not changed when a wakeup signal is transmitted or received. Therefore, bit WAKEUP has to be checked before bit COMPLETE

5) Check bit COMPLETE in the status register (it is set if the transmission was successful). If COMPLETE is set and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
6) Set the bits RSTINT (reset interrupt) and RSTERR (reset error) in the control register to reset the interrupt request and the error flags.

9.2.4.2.5 Sleep Mode and Wakeup

To reduce the systems power consumption the LIN Protocol Specification defines a Sleep Mode. The message used to broadcast a Sleep Mode request has to be started by the host controller of the LIN core master in the same way as a normal transmit message. The host controller of the LIN core slave has to decode the Sleep Mode Frame from Identifier and data bytes. After that, it has to put the LIN slave node into the Sleep Mode by setting bit SLEEP in the control register. If bit SLEEP in the control register of the LIN core slave is not set and there is no bus activity for 4 s to 10 s (specified bus idle timeout), bit SLEEP & BUSIDLETIMOUT are set and an interrupt request is generated. After that application has to understand that the LIN bus is in Sleep Mode. The bus inactivity time which should be defined as bus idle timeout for the slave can optionally set to values 4s, 6s, 8s or 10s as possible accordingly with specification 2.2A.

After receiving a Wakeup signal from the master or any slave node a wakeup request is generated, the host controller terminates the Sleep Mode of the LIN bus by clearing bit SLEEP in the control register.

Notice that don’t enter hibernate mode when bit SLEEP = 0, because in this state dominant signal will not be taken as a wakeup request.

To send a Wakeup signal, the host controller of the LIN core has to set the bit WAKEUPREQ in the control register. After successful transmission of the wakeup signal with the LIN core master the WAKEUP bit in the status register of the sending LIN core master is set and an interrupt request is generated. The LIN core slave does not generate an interrupt request after successful transmission of the Wakeup signal but it generates an interrupt request if the master does not respond to the Wakeup signal within 150ms to 250ms. This value can be set optionally to 180ms, 200ms, 220ms or 240ms as it is possible accordingly with specification 2.2A. In that case, bit ERROR and bit TIMOUT are set**.** The host controller has to decide whether to transmit another Wakeup signal or not.

9.2.4.2.6 Error Detection and Handling

The LIN core generates an interrupt request and stops the processing of the current frame if it detects the following errors：

- BITMON: The bit value monitored on the bus is different from the sent bit value.
- Timeout caused by wakeup repeat timeout.
- BUS IDLE Timeout.

The errors detected in Break/Sync field will be ignored by LIN controller. The other errors happen in ID field/Data field will be recorded. In DataReq interrupt routine, the application has to check the type of error by processing the ERROR register. After that, it has to reset the ERROR register and the ERROR bit in status register by writing a 1 to bit RSTERR in control register. Starting a new message with the LIN core master or sending a Wakeup signal with master or slave is possible only if bit ERROR in status register is 0.

9.2.4.3 Auto Addressing (Lin Switch Mode):

While iND83215 integrates a lin switch and two LIN interface pins, LIN_IN and LIN_OUT, connecting to LIN transceiver. Software is in charge to control the lin switch through IOCTRLA LIN control registers. When SWON is set to 1, the lin switch will connect LIN_IN and LIN_OUT. At the same time, the lin master controller will lose the connection with the lin master transceiver.

With this lin switch, iND83215 can support auto addressing function. BCM connects iND83215 in a chain by connecting LIN_IN to upstream LIN bus, and connecting LIN_OUT to downstream LIN bus, as Figure 10. At the first boot of the system, every switch is on. The following is a SNPD sequence for instance:

1. Lin Master sends a diagnostic frame (ID=3C, 8 bytes data frame) to inform the slaves that SNPD sequence is started. Then the slaves disconnect downstream LIN bus by opening the internal switch. Thus, only the first one, iND83215 1, can receive message from BCM via LIN_IN pin.
2. Lin Master sends 1st NAD configure frame with NAD=”01”. Thus “01” address is assigned to iND83215 1 at first. And then iND83215 1 close its internal LIN switch, thus iND83215 2 can receive message from LIN bus.
3. Then system can assign the second address for iND83215 2 accordingly. By analogy, all iND83215s on the chain can be assigned address.

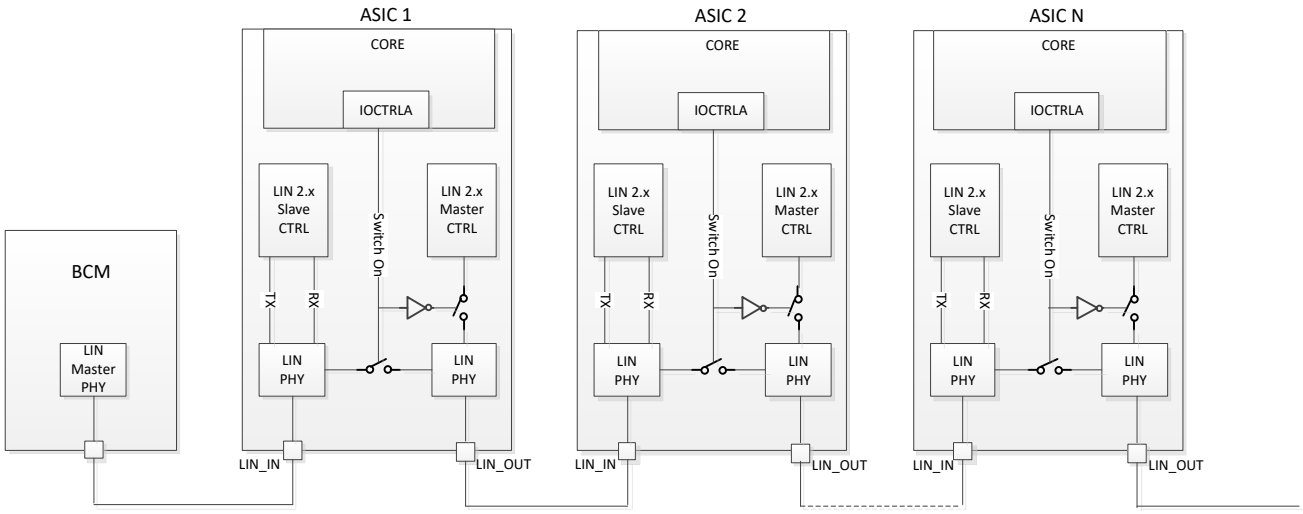


Figure 15 LIN auto addressing

Cautions:

1. LIN protocol requires inter-frame space not negative. That means any space > = 0 is acceptable. Since the internal switch is controlled by software, there are a big latency from frame complete interrupt to control the switch by interrupt routine. So a big inter-frame space is required during SNPD sequence, while this is determined by LIN master.

9.2.5 LED Driver Stage

ASIC integrates a high precision open drain LED Driver Stage that allows for LED currents in the range of 120uA to 60mA in 120uA increments. The LED bias circuit uses a precise bandgap referenced current (CurrentV2I) which is multiplied over stages to sink current via the LED which is connected to the HVIO(LED) pin. After factory test, the trim value for CurrentV2I = 30uA will be recorded and boot program is in charge of initializing the V2I trim bits correctly (refer to Register Description). The mirror stages consist of 120uA unit cells which are weighted linear to provide 120uA ~ 60mA current (CurrentLED). The desired current is provided according the formula below:

$$\mathrm{CurrentLED(mA)} = \mathrm{TRIM}[8:0] * CurrentV2I * 4 = TRIM[8:0] * 120uA$$

After delicate calibration by LED trim bits (refer to Register Description), the combination of stages allows for high accurate LED current in 120uA steps that are combined at the HVIO(LED) pad on chip (refer to Figure 16).

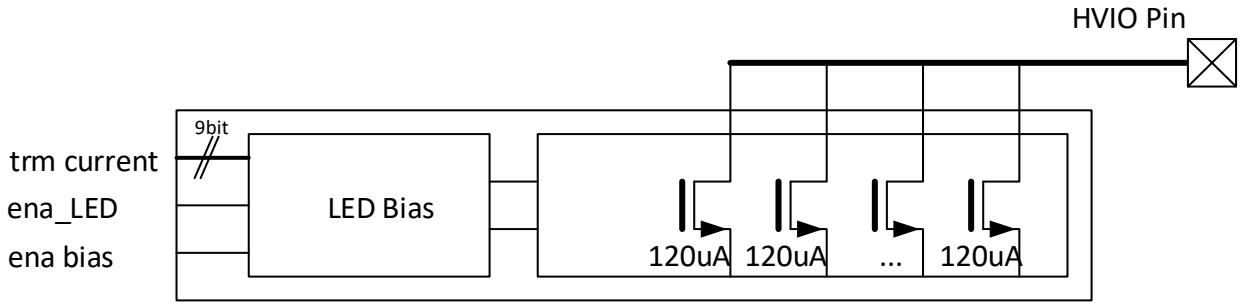


Figure 16 LED Driver Concept

The operation of the LED Driver IP requires two actions. At first the LED bias circuit needs to be enabled (ena_bias) (refer to Register Description), followed by enabling the LED (ena_LED). Latter control signal is driven by the pulse width modulator that will drive the current from the battery via the LED. The PWM signal utilizes an input signal at maximum of 250Hz and modulates its pulse width (refer to section 9.2.6 LED PWM).

9.2.6 LED PWM

LED PWMs are used to control accurately the light intensity.

Features:

- 3x16bit PWM channels with one unified period length, independent pulse rise and pulse fall timestamps.
- Frequency and duty cycle of PWM waveform support up to a maximum Resolution of 16 bits. The 16-bit resolution is only achievable if the pre-scaler from system clock is correctly chosen to have enough clock cycles depth to count up to 2^16.
- Programmable pre-scaler: system clock division (PWM_DIV)
- Programmable PWM Period (PWM_PER)

$$\text{Period} = \frac{\text{PWM\_PER} \times \text{PWM\_DIV}}{SystemClock}$$

- Programmable duty cycle 0 to 100% (PWM_PW)

$$\text{PulseWidth} = \frac{(\text{PWM}_{\text{PFALL}} - \text{PWM}_{\text{PRISE}}) \times \text{PWM\_DIV}}{SystemClock}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period.
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an UPDATE bit can be set to 1 that will trigger the activation of the new parameters

at the end of the current pulse as not to affect the pulse shape. Basically, the UPDATE bit clear is the interrupt.

- PWM Frequency range 80 - 250 Hz
- Pulse rise -> fall cases, listed in priority:
    - PRISE = 0, PFALL = PERIOD: 100% On
    - PRISE = 0, PFALL = 0: equivalent to PRISE = 0 & PFALL = 1
    - PRISE > PFALL: 100% off
    - PRISE = PFALL: 100% off
    - PRISE < PFALL: Normal case. On at PRISE, Off at PFALL.

9.2.7 House Keeping SAR ADC

- 12-bit resolution
- Differential Input
- Bandgap Voltage reference
- Used for monitoring voltages
    - Bandgap Reference
    - Accurate VBAT Channel (limited to max voltage limited by the load-dump protection circuit)
    - Junction Temperature
    - Analog Input from PA/PB Pad
    - Analog Input from LED x 3
    - Forward Voltage of External LED x 3
    - VDD1V5/VDD3V3/VDDPRE5V
- Capable of being configured for converting up to 4 channels successively
- Interrupt on conversion complete regardless of digital comparator configuration

9.2.8 Over and Under Voltage detection (VBAT)

The over and under voltage comparators are based on comparing a divided voltage from the Load Dump limiter output feeding an analog comparator with hysteresis (refer to EC Table for electrical parameters and PMU description). The Over and Under voltage events generate Interrupts to the interrupt controller.

9.2.9 Temperature monitor

The MCU is in charge to pull the ADC related data from temperature sensor and in case the measured data is too high, MCU will reduce power profile to reduce heat. Table 14 shows the tempsensor output voltage corresponding to Tj for reference. Calibration is required due to different offset per chip.

Table 14 Tempsensor Output voltage vs Junction Temp

Junction Temp (°C)	Tempsensor Output Voltage(V) @VBAT=13.5V
-40	0.50163
-30	0.521679
-20	0.544496
-10	0.566225
0	0.587857
10	0.609077
20	0.629778
30	0.650982
40	0.672195
50	0.693153
60	0.714406
70	0.735295
80	0.7564
90	0.777649
100	0.798814
110	0.819774
120	0.840907
130	0.876265
140	0.885424
150	0.905518

9.2.10 Over Temperature detection

The over temperature comparator monitors the junction temperature with hysteresis. The Over temperature event generates reset or interrupt to the interrupt controller.

9.2.11 ASIC Watchdog Timer

While it exists a watchdog timer in the MCU, the ASIC integrates another watch-dog timer that is intended to be used to recover from a situation where there may have been a software fault or other system failure where the software has ceased to operate correctly. If the timer is not reset by software periodically, it will time out, and this event can be used to reset the system or generate an interrupt (Refer to Register Description).

Features:

- Programmable timeout period (Refer to Register Description) with instantaneous access to the value of watchdog timeout counter
- Status flag, stop and clear/reset control registers
- The Watchdog timer is by default active after power up and set to its maximum duration setting (Refer to Register Description)
- Window mode supported: If enabled, WDTA can only be cleared after the watchdog window opened and before time-out period; Otherwise, WDTA will issue a system reset or an interrupt (Refer to Register Description).

9.2.12 SLEEP (Hibernate/DeepSleep) Modes

IC can enter SLEEP mode through SW request(PMUA->CTRL.HIBERNATE). The device comes out of SLEEP with either the slow auxiliary or the system clock. It's up to the SW to select which clock shall be used after a wake event is detected. The SW does't have to request to go to SLEEP with the same clock selected for wake up.

There are two major SLEEP modes:

1. Hibernate mode: In this mode, MCU and ASIC's Core(1.5V)/IO(3.3V) power domains are off. In this mode, only lin wakeup is available as the wakeup source. This mode has an extremely low current consumption.
2. Deepsleep mode: If PMUA->CTRL.PD1V5_ENA_HIBERNATE is set, ASIC's Core & IO supplies remain active after chip enters low power mode. This mode can keep IO status and supports more wakeup sources in the low power mode.

9.2.12.1 Wake up Sources

Coming out from Hibernate mode can happen through the following events:

- LIN Wakeup: After a low pulse on the LIN pin such that a dominant (low) voltage level is applied for longer than TWAKEUP time. Notice that LIN wakeup interrupts can be generated in either active or Hibernate mode when bit SLEEP = 1. This wakeup source is available in active/hibernate/deepsleep modes.

- GPIOs pin toggling either from high to low or low to high levels (VIL/VIH). This kind of wakeup sources are available in active/deepsleep modes.
- Wake up timer. Programmable range. Wake up timer has the option to be disabled. This wakeup source is available deepsleep mode.
- SWD Wakeup. This wakeup source is available deepsleep mode.

MCU can check which wake up events triggered the system through a status register read. MCU to clear the register after status check.

10 DISCLAIMERS

Product brief datasheet is an exact from full datasheet for quick reference purpose

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