AEM10941 Evaluation Kit with Dracula Technologies Flexible OPV Module User Guide

Description

The **AEM10941** is an ambient energy manager that extracts power from photovoltaic harvesters to simultaneously store energy in a rechargeable element and supply your system with two independent regulated voltages.

The **AEM10941** evaluation board with flexible photovoltaic module allows users to test the e-peas IC and the **Dracula Technologies** Organic Photo-Voltaic (OPV) module and analyse its performances in a laboratory-like setting.

It allows easy connections to the storage element and the low-voltage and high-voltage loads. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers , allowing users to configure it for any usage scenario and evaluate the relevant performances.

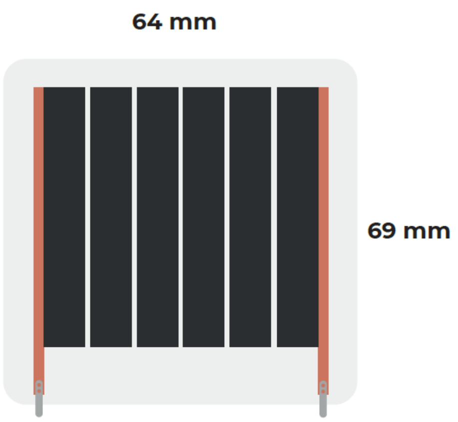
The **AEM10941** evaluation board with Dracula Technologies flexible photovoltaic module is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes, etc) for the design of a highly efficient subsystem in your target application.

Applications

OPV module harvesting	Smart home/building
Industrial applications	Environmental sensors

Device Information

Part Number	Dimensions
2AAEM10941CDR10	64 mm x 49 mm
Demokit LAYER #6	64 mm x 69 mm



Features

Two-way screw terminals

- Source of energy (**Dracula Technologies** OPV module)
- Primary battery
- HVOUT LDO output
- LVOUT LDO output

Three-way screw terminals

- Energy storage element (Battery)

3-pin headers

- Energy storage element threshold configuration (CFG[2:0])
- Low drop-out regulators (LDOs) enabling
- Dual-cell supercapacitor configuration

One 2-pin header

- Primary battery configuration

Provision for five resistors

- Custom mode configuration
- Cold start configuration
- Primary battery configuration

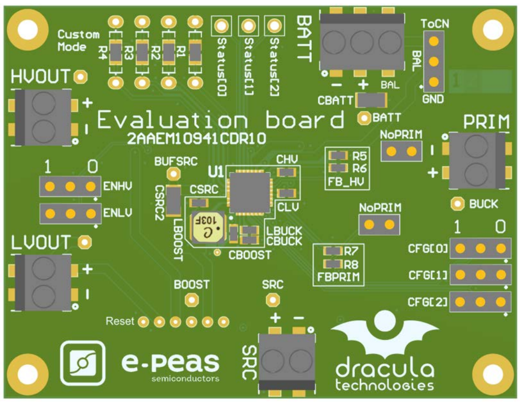
1-pin headers

- Access to status pins

Dracula Technologies OPV module

- Up to 2.9V and 200µA under 1000 lux
- 6 interconnected cells in series

Appearance



1. Connections Diagram

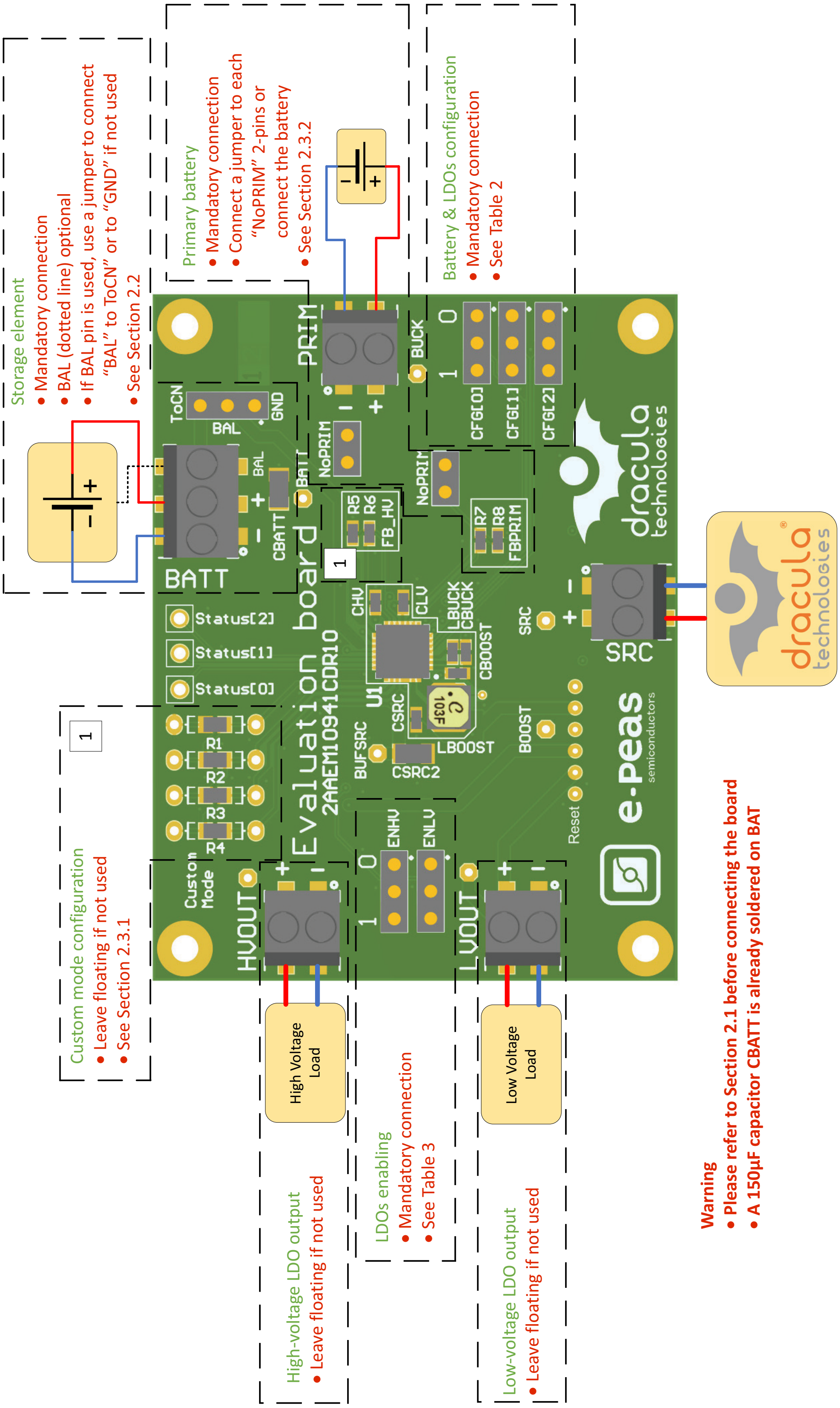


Figure 1: Connection diagram

1.1. Signals Description

NAME	FUNCTION	CONNECTION	
		If used	If not used
Power signals			
SRC	Connection to the harvested energy source.	Connect the source element.	Leave floating.
BATT	Connection to the energy storage element.	Connect the storage element in addition to CSTO (150 µF).	Do not remove CBATT
BAL	Connection to mid-point of a dual-cell supercapacitor	Connect mid-point and jumper BAL to "ToCN	Use a jumper to connect "BAL" to "GND"
PRIM	Connection to the primary battery	Connect primary battery.	Connect a jumper to each NoPRIM 2-pins.
LVOUT	Output of the low-voltage LDO regulator.	Connect a load	
HVOUT	Output of the high-voltage LDO regulator.	Connect a load	
Debug signals			
VBOOST	Output of the boost converter.		
VBUCK	Output of the buck converter.		
BUFSRC	Connection to an external capacitor buffering the boost converter input.		
Configuration signals			
CFG[2:0]	Configuration of the threshold voltages for the energy storage element.	Connect jumper (see Table 2)	Cannot be left floating (see Table 2)
FB_PRIM	Configuration of the primary battery.	Use resistors R7-R8 (see Section 2.3.2)	Connect a jumper to each NoPRIM 2-pins.
FB_HV	Configuration of the high-voltage LDO in the custom mode	Use resistor R5-R6 (see Section 2.3.1)	Leave floating.
Control signals			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3)	Cannot be left floating (see Table 3)
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3)	Cannot be left floating (see Table 3)
Status signals			
STATUS[2]	Logic output. Asserted when the AEM perfoms the MPP evaluation.		
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		

Table 1: Pin description

2. General Considerations

2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board - see "How to reset the AEM10941 evaluation board" on page 7.
2. Completely configure the PCB (jumper/resistors);
   - Battery and LDOs configuration (CFG[2:0] and, if needed, R1-R2-R3-R4-R5-R6) - see Table 2,
   - Primary battery configuration (NoPRIM or R7-R8) - see Section 2.3.2,
   - LDOs enabling (ENHV and ENLV) - see Section 2.2,
   - Balun circuit connection (BAL) - see Section 2.3.3,
3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
5. Connect the Dracula Technologies OPV modules on SRC.

To avoid damage to the board, users are urged to follow this procedure.

2.2. Basic Configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	Vovch	Vchrdy	Vovdis	Vhv	Vlv	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - see Section 2.3.1				1.8 V	

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

Table 3: LDOs enabling

2.3. Advanced Configurations

A complete description of the system constraints and configurations is available in Section 8 “System configuration” of the AEM10941 datasheet.

A reminder on how to compute the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found at the e-peas website.

2.3.1. Custom mode

In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4 and to tune the output of the high voltage LDO via resistors R5-R6.

By defining RT = R1 + R2 + R3 + R4 (1MΩ ≤ RT ≤ 100 MΩ):

- R1 = RT (1V / Vovch)
- R2 = RT (1V / Vchrdy - 1V / Vovch)
- R3 = RT (1V / Vovdis - 1V / Vchrdy)
- R4 = RT (1 - 1V / Vovdis)

By defining RV = R5 + R6 (1MΩ ≤ RV ≤ 40MΩ):

- R5 = RV (1V / Vhv)
- R6 = RV (1 - 1V / Vhv)

Make sure the protection levels satisfy the following conditions:

- Vchrdy + 0.05 V ≤ Vovch ≤ 4.5 V
- Vovdis + 0.05 V ≤ Vchrdy ≤ Vovch - 0.05 V
- 2.2 V ≤ Vovdis
- Vhv ≤ Vovdis - 0.3V

If unused, leave the resistor footprints (R1 to R6) empty.

2.3.2. Primary battery configuration

For the main storage element, the primary battery protection levels have to be defined. To do so, use resistors R7 - R8.

By defining RP = R7 + R8 (100 kΩ ≤ RP ≤ 10MΩ):

- R7 = Vprim_min / 4 x RP x 1 / 2.2 V
- R8 = RP - R7

If unused, use a jumper to short each “NoPRIM” 2pins headers.

2.3.3. Balun circuit configuration

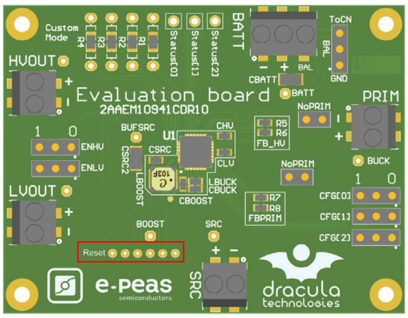
When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (BATT connector)
- Use a jumper to connect “BAL” to “ToCN”

If unused, use a jumper to connect “BAL” to “GND”.

How to reset the AEM10941 evaluation board:

To reset the board, simply disconnect the storage device and the optional primary battery and connect the 6 “Reset” connections (working from the rightmost to the left) to a GND node (i.e. the negative pin of any connector) in order to discharge the internal nodes of the system.



3. Dracula Technologies LAYER OPV modules

The LAYER® Organic Photovoltaic modules can be used in low light conditions and efficiently convert light into energy. In fact, LAYER® uses specific organic materials which harvest both natural and artificial light to generate energy from its environment.

The organic photovoltaic cells are printed on flexible substrate (PET) by inkjet printing technology. The versatility of the production process allows Dracula Technologies to create on demand module to meet customers specifications in terms of performances and design.

The LAYER Demokit#6 OPV module available in the evaluation kit is composed of 6 cells connected in series and can generate up to 2.85 V and 200 µA under 1000 lux (see datasheet below). Additional information can be found on Dracula Technologies Website (at dracula-technologies.com) .

For optimized performances please expose the OPV module labelled side to the light source.

Illuminance (lux)	Voc (V)	Isrc (µA)	Vmax (V)	Imax (µA)	Pmax (µA)
50	3.00 - 3.20	13 -15	2.35 - 2.45	10 - 11	23 - 27
100	3.25 - 3.30	30 - 35	2.55 - 2.65	24 - 27	61 - 72
200	3.40 - 3.50	55 - 65	2.70 - 2.75	45 - 55	121 - 151
300	3.55 - 3.60	75 - 85	2.80 - 2.85	65 - 75	182 - 214
400	3.60 - 3.65	100 - 110	2.85 - 2.90	85 - 95	242 - 275
500	3.65 - 3.68	130 - 140	2.85 - 2.95	105 - 115	294 - 328
1000	3.70 - 3.80	245 - 255	2.85 - 3.00	200 - 210	570 - 609

Table 4: LAYER performance between 50 -1000 lux

3.1. Operating condition

Item	Unit	Minimum	Maximum
Surface temperature	°C	0	40
Ambient humidity	%RH	1	90
Illuminance	lux	10	100 000
Atmospheric pressure	hPa	550	1100

Table 5: Operating condition

3.2. Storage condition

Item	Unit	Minimum	Maximum
Surface temperature	°C	-30	50
Ambient humidity	%RH	1	90
Illuminance	lux	-	100 000
Atmospheric pressure	hPa	550	1100

Table 6: Storage condition

4. Functional Tests

This section presents a few simple tests that allow the user to understand the functional behaviour of the AEM10941. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted make sure to properly reset the system to obtain reproducible results.

The featured functional tests were made using the following setup:

- Configuration: CFG[2:0] = HLL, ENHV = H, ENLV = H
- Storage element: Capacitor (4.7 mF + CBATT)
- Load: 10kΩ on HVOUT, LVOUT floating
- SRC: Dracula Technologies OPV module

Feel free to adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 “introduction” of AEM10941 datasheet).

4.1. Start-up

The following example allows users to observe the behavior of the AEM10941 in the wake-up mode.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.

Observations and measurements

- BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 2).
- SRC: Regulated at Vmpp, which is a voltage equal to the open-circuit voltage (Voc) times the MPP ratio of 70%. Vsrc equals Voc during MPP evaluation (see Figure 3). Note that Vsrc must be higher than 380 mV to coldstart.
- HLDO/LLDO: regulated when voltage on BATT first rises above Vchrdy (see Figure 2).
- STATUS[0]: Asserted when the LDOs are ready to be enabled (refer to Section 7.2 “Normal mode” of the AEM10941 datasheet) (see Figure 2).
- STATUS[2]: Asserted each time the AEM10941 performs a MPP evaluation (See Figure 3).

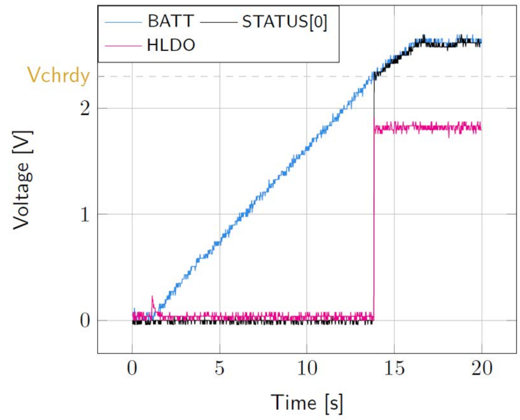


Figure 2: STATUS [0] and HLDO evolution with BATT

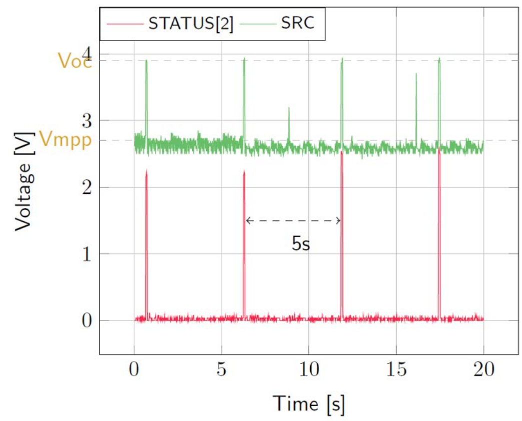


Figure 3: SRC and STATUS[2] while energy is extracted from SRC (BATT under Vovch)

4.2. Shutdown

This test allows users to observe the behaviour of the AEM10941 when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 "Safety Information". Configure the board in the desired state and start the system (see Section 4.1). Do not use a primary battery.
- Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
- Remove the Dracula Technologies OPV module and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing Vovdis (see Figure 4).
- STATUS[0]: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 4).
- STATUS[1]: Asserted for 600ms when the storage element voltage (BATT) falls below Vovdis (see Figure 4).

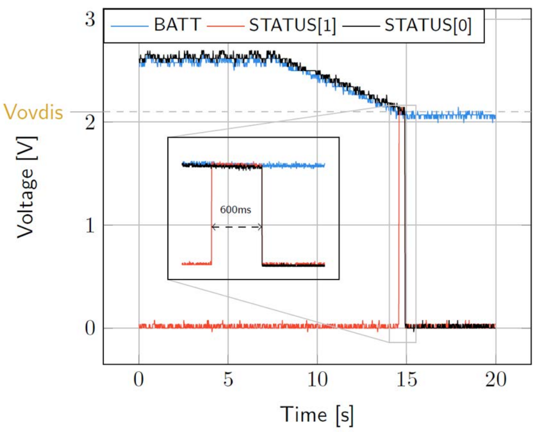


Figure 4: LDOs disabled around 600 ms after BATT reaches Vovdis

4.3. Switching on primary battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

Setup

- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 "Safety Information". Configure the board in the desired state and start the system (see Section 4.1). Connect a primary battery (example: 3.1V coil cell with protection level at 2.4V, R7 = 68kΩ and R8 = 180kΩ).
- Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
- Remove the Dracula Technologies OPV module and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches Vovdis and than rises again to Vchrdy as it is recharged from the primary battery (see Figure 5).
- STATUS[0]: Never de-asserted as the LDOs are still functional (see Figure 5).
- HLDO: Stable and not affected by switching on the primary battery (see Figure 5).

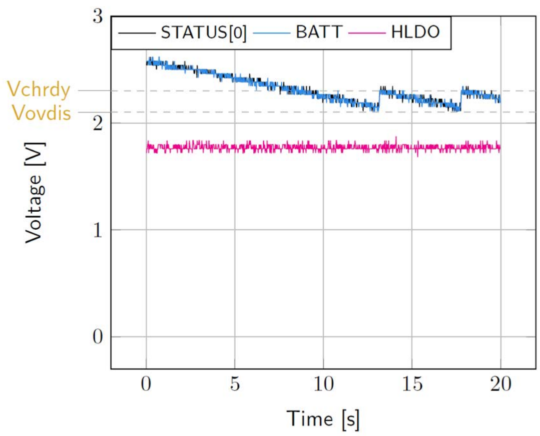


Figure 5: Switching from SRC to the primary battery

4.4. Cold start

The following test allows the user to observe the minimum voltage required to coldstart the AEM10941. To prevent leakage current induced by the probe the user should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behaviour.

Setup

- Place the probes on the nodes to be observed.

- Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.
- SRC: Connect your source element

Observations and measurements

- SRC: Equal to the cold-start voltage during the coldstart phase. Regulated at 70% of Voc when cold start is over. (See Figure 6). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- BATT: Starts to charge when the cold-start phase is over (see Figure 6).

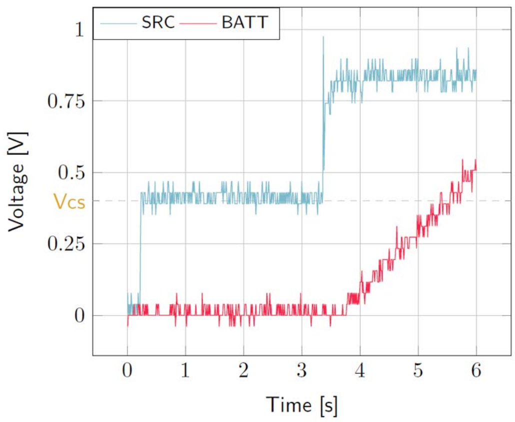


Figure 6: AEM10941 behaviour during cold start

4.5. Dual-cell supercapacitor balancing circuit

The following test allows the user to observe the balancing circuit behaviour that balances the voltage on both side of the BAL pin.

Setup

- Following steps 1 and 2 explained in section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking “BAL” to “ToCN”.
- BATT: Plug capacitor C1 between the positive (+) pin and the bal pin, and a capacitor C2 between the BAL pin and the negative (-) pin.
  - C1 & C2 > 1 mF
  - (C2 x Vchrdy) / C1 ≥ 0.9V
- SRC: Plug your source element to power up the system.

Observations and measurements

- BAL: equal to half the voltage on BATT.

Warning regarding measurements:

Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

5. Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM10941 datasheet and to understand the functionalities of the AEM10941. to be able to reproduce those tests, you will need the following:

- 1 voltage source
- 2 source measure units (SMUs)
- 1oscilloscope

To avoid damaging the board, follow the procedure in Section 2.1 "Safety information". If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see "How to reset the AEM10941 evaluation board" on page 7).

5.1. LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Figure 16 and Figure 17 of the AEM10941 datasheet).

Setup

- Referring to Figure 1, follow steps 1 and 2 explained in the section 2.1. Configure the board in the desired state and plug your storage element(s)
- VBOOST: connect SMU1. configure it to source voltage with a current compliance of 200 mA.
- HVOUT / LVOUT: connect SMU2 to the LDO you want to measure. Configure it to sink current with a voltage compliance of 5V for HVOUT or 2.5V for LVOUT.

Manipulations

- Impose a voltage between Vovch and 5V on SMU 1 to force the AEM to start.
- Sweep voltage on SMU1 from Vovdis + 50 mV to 4.5 V
- Repeat with different current levels on SMU2 (from 10µA to 80mA for HVOUT and from 10µA to 20mA for LVOUT).

Measurements

- HVOUT/LVOUT: Measure the voltage.

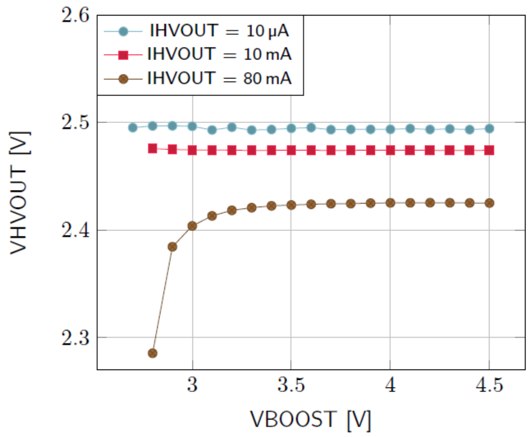


Figure 7: HVOUT at 2.5V

5.2. BOOST efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (Figure 14 of the AEM10941 datasheet).

Setup

- Following steps 1 and 2 explained in the section 2.1 and referring to Figure 1, configure the board in the desired state.
- VBUCK: Connect a 2.3 V voltage source to prevent VBUCK to sink from VBOOST.
- SRC: Connect SMU1. Configure it to source current with a voltage compliance of 0 V.
- VBOOST: Connect SMU2. Configure it to source voltage with a current compliance of 200 mV
- STATUS[2] Connect to one of the SMU to detect falling edge.

Manipulations

- Impose a voltage between Vovch and 5V on SMU 2 to force the AEM to start. When done, impose a voltage between Vovdis + 50mV and Vovch.
- Sweep voltage compliance on SMU1 from Vovdis + 50 mV to 4.5 V
- Repeat with different current levels on SMU1 (from 100µA to 100mA) and with different voltage levels on SMU2 (from Vovdis + 50 mV to Vovch).

Measurements

- STATUS[2]: Dot not make any measurements while high (boost converter is not active during MPP calculation).
- SRC: Measure the current and the voltage.

- VBOOST: Measure the current and the voltage. Repeat the measurement many times to be sure to capture the current peaks. Figure 8 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.
- Deduce input and output power (P = U x I) and efficiency (η = Pout/Pin).

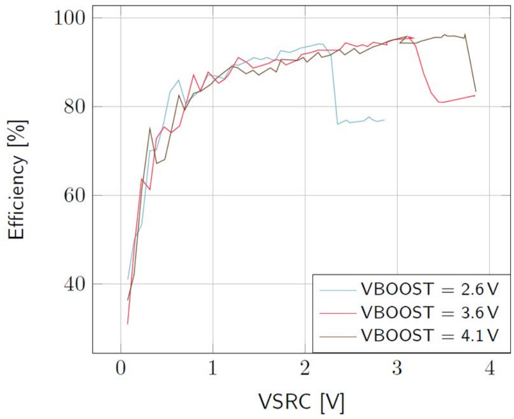


Figure 8: Boost efficiency for ISRC = 1mA

5.3. Custom mode configuration

This test allows users to measure the custom protection levels of the storage element set by resistors R1 to R6.

Setup

- Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Connect CFG[2:0] = LLL to select custom mode and choose R1 to R6 to configure the battery protection levels and HVOUT output voltage.
- Place the probes on the nodes to be observed.
- SRC: connect your source element to power up the system.

Manipulations

- Remove the source element after the voltage on BATT has reached steady state (between Vchrdy and Vovch).

Measurements

Measure the following nodes to ensure the correct behaviour of the AEM10941 with respect to the custom configuration:

- STATUS[0]: Asserted when the LDOs can be enabled (i.e. when BATT first rises above Vchrdy).
- STATUS[1]: Asserted when BATT falls below Vovdis.
- BATT: Rise up and oscillate around Vovch as long as the source element has not been removed.
- HVOUT: Equal to the value set by R5-R6