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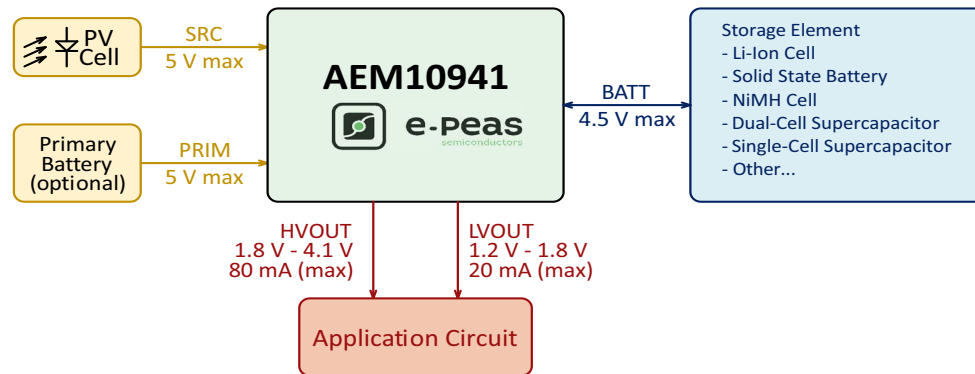


Figure 1: Simplified schematic view

1. Introduction

The AEM10941 is a full-featured energy efficient power management circuit capable of charging a storage element (battery or supercapacitor, connected to **BATT**) from an energy source (connected to **SRC**) as well as supplying loads at different operating voltages through two power supplying LDO regulators (**LVOUT** and **HVOUT**).

The heart of the AEM10941 is a cascade of two regulated switching converters, namely the boost converter and the buck converter, both with high power conversion efficiencies (See Section 12).

At first start-up, as soon as a required cold-start voltage of 380 mV and a scant amount of power of only 3 μ W are available from the harvested energy source, the AEM coldstarts. After the cold start, the AEM can extract the power available from the source as long as the input voltage is within 50 mV to 5 V range.

Through three configuration pins (**CFG[2:0]**), the user can select a specific operating mode from a range of seven modes that covers most application requirements without any dedicated external component. These operating modes define the LDO output voltages and the protection levels of the storage element. A custom mode allows the user to define arbitrary storage element protection levels and the output voltage of the high-voltage LDO (See Section 9.1).

The Maximum Power Point (MPP) ratio can be configured using two configuration pins (**SELMPP[1:0]**) (See Section 9.2).

Two logic control pins (**ENLV** and **ENHV**) allow to dynamically activate or deactivate the LDO regulators that supply the low and high voltage load. The status pin **STATUS[0]** alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the battery voltage gets depleted, **LVOUT** and **HVOUT** are power-gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin **STATUS[1]** alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected on **PRIM**, the AEM10941 automatically uses it as a source to recharge the storage element before switching back to the ambient source. This guarantees continuous operation even under the most adverse conditions (See Section 8.2.4). **STATUS[1]** is asserted when the primary battery is providing power.

The status of the MPPT controller is reported with one dedicated status pin (**STATUS[2]**). The status pin is asserted when an MPP calculation is being performed.

2. Pin Configuration and Functions

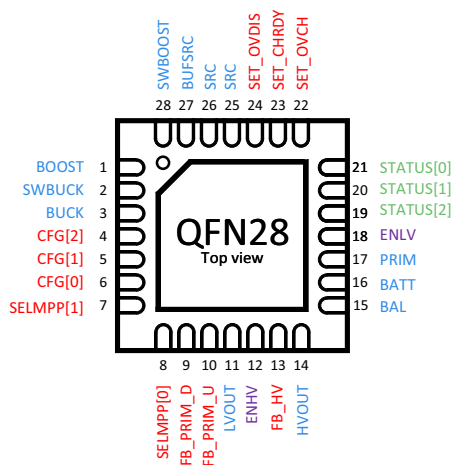


Figure 2: Pinout diagram QFN 28-pin

Name	Pin Number	Function
Power pins		
BOOST	1	Output of the boost converter.
SWBUCK	2	Switching node of the buck converter.
BUCK	3	Output of the buck converter.
LVOUT	11	Output of the low voltage LDO regulator.
HVOUT	14	Output of the high voltage LDO regulator.
BAL	15	Connection to the mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.
SRC	25, 26	Connection to the harvested energy source.
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.
SWBOOST	28	Switching node of the boost converter.
Configuration pins		
CFG[2]	4	Used for the configuration of the threshold voltages of the energy storage element and the output voltage of the LDOs.
CFG[1]	5	
CFG[0]	6	
SELMPP[1]	7	Used for the configuration of the MPP ratio.
SELMPP[0]	8	
FB_PRIM_D	9	Used for the configuration of the primary battery overdischarge voltage (optional). Must be connected to GND if not used.
FB_PRIM_U	10	
FB_HV	13	Used for the configuration of the high-voltage LDO when in custom mode (optional). Must be left floating if not used.
SET_OVCH	22	Used for the configuration of the threshold voltages for the energy storage element when in custom mode (optional). Must be connected to BUCK if not used.
SET_CHRDY	23	
SET_OVDIS	24	

Table 1: Pins description (Part 1)

Name	Pin Number	Function
Control pins		
ENHV	12	Enabling pin for the high-voltage LDO (See Table 7).
ENLV	18	Enabling pin for the low-voltage LDO (See Table 7).
Status pins		
STATUS[2]	19	Logic output. Asserted when the AEM performs a MPP evaluation.
STATUS[1]	20	Logic output. Asserted during 600 ms if the battery voltage falls below V_{OVDIS} or asserted as long as the AEM is taking energy from the primary battery.
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.
Other pins		
GND	Exposed pad	Ground connection, should be solidly tied to the PCB ground plane.

Table 1: Pins description (Part 2)

3. Absolute Maximum Ratings

Parameter	Rating
Voltage on SRC, BUFSRC, BATT, BAL, PRIM, BOOST, SWBOOST, HVOUT, ENLV	5.5 V
Voltage on BUCK, SWBUCK, LVOUT, CFG[2:0], FB_PRIM_U, FB_PRIM_D, SELMPP[1:0], SET_OVDIS, SET_CHRDY, SET_OVCH, ENHV	2.75 V
Voltage on FB_HV	2.5 V
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Table 2: Absolute maximum ratings

4. Thermal Resistance

Package	θ_{JA}	θ_{JC}	Unit
QFN 28-pin	38.3	2.183	°C/W

Table 3: Thermal data

ESD CAUTION		
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality	
	Human-body model according to Jedec JS001-2017 Charge device model according to Jedec JS002-2014	± 500 V ± 1000 V

Table 4: ESD caution



5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input voltage and input power						
P _{SRC_CS}	Source power required to coldstart.	During cold start.	3			μW
V _{SRC}	Input voltage of the energy source (maximum given by the open-circuit voltage).	During cold start.	0.38		5	V
		After cold start.	0.05 ¹		5	
I _{SRC}	Harvested current from the energy source.	L _{BOOST} = 10 μH.			110	mA
		L _{BOOST} = 22 μH.			50	
V _{MPP}	Voltage level of the Maximum Power Point.	After cold start.	0.05		4.5	V
DC-DC converters						
V _{BOOST}	Output voltage of the boost converter.	During normal operation.	2.2		4.5	V
V _{BUCK}	Output voltage of the buck converter.		2	2.2	2.5	
I _{BUCK}	Total load current supplied by the BUCK converter (including LVOUT current I _{LV}).	L _{BUCK} = 10 μH.	0		20	mA
		L _{BUCK} = 4 μH.	0		50	mA
Storage element						
V _{BATT}	Voltage on the storage element.		0 ²		4.5	V
V _{PRIM}	Voltage on the primary battery.		0.6		4.5	V
I _{PRIM}	Current from the primary battery.			20		mA
V _{FB_PRIM_U}	Feedback for defining the overdischarge voltage level on the primary battery.		0.15		1.1	V
V _{OVCH}	Maximum voltage accepted on the storage element before disabling the boost converter.	See Table 8.	2.3		4.5	V
V _{CHRDY}	Minimum voltage required on the storage element before enabling the LDO when coming from WAKE-UP MODE.	After cold start See Table 8.	2.25		4.45	V
V _{OVDIS}	Minimum voltage accepted on the storage element before switching to primary battery or entering SHUTDOWN MODE.	See Table 8.	2.2		4.4	V
I _Q	Quiescent current on BATT when the boost converter is not running.	V _{BATT} = 3 V; LDOs disabled.		400		nA
		V _{BATT} = 3 V; LDOs enabled.		600		nA
Low-Voltage LDO regulator						
V _{LV} ³	Output voltage of the low-voltage LDO.	See Table 8.	1.2		1.8	V
I _{LV}	Load current supplied by the low-voltage LDO.	L _{BUCK} = 10 μH.	0		20	mA
High-Voltage LDO regulator						
V _{HV} ⁴	Output voltage of the high-voltage LDO.	See Table 8.	1.8		V _{OVDIS} - 0.3 V	V
I _{HV}	Load current supplied by the high-voltage LDO.		0		80	mA

Table 5: Electrical characteristics (Part 1)



Symbol	Parameter	Condition	Min	Typ	Max	Unit
Timing						
$T_{MPPT,VOC}$	Time during which the AEM10941 stops pulling current on SRC to measure the harvester open circuit voltage (V_{OC}).			82		ms
$T_{MPPT,PERIOD}$	Period of the MPPT V_{OC} evaluations.			5		s
T_{CRIT}	Time before shutdown once STATUS[1] has been asserted (see Section 8.2.5 and Figure 5).		400	600	800	ms
Logic output pins						
STATUS[2:0]	Logic output levels on the status pins.	Logic HIGH (H).	$V_{BATT} - 0.1$	V_{BATT}	$V_{BATT} + 0.1$	V
		Logic LOW (L).	GND - 0.1	GND	GND + 0.1	V

Table 5: Electrical characteristics (Part 2)

1. Minimum V_{SRC} value for harvesting capabilities after coldstart.
2. To stay in NORMAL MODE, V_{BATT} minimum voltage must stay above V_{OVDIS} .
3. The variability of V_{LV} at 1 mA is 1% (typical and preliminary result from simulations).
4. The variability of V_{HV} at 1 mA is 1.3% (typical and preliminary result from simulations).



6. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External components					
C_{SRC}	BUFSRC pin decoupling capacitor.	8	10	22	μF
C_{BOOST}	Output capacitor of the boost converter.	10	22		μF
L_{BOOST}	Inductor of the boost converter.	4	10		μH
C_{BUCK}	Output capacitor of the buck converter.	8	10		μF
L_{BUCK}	Inductor of the buck converter.	4	10	25	μH
C_{LV}	Low-voltage LDO regulator decoupling capacitor.	8	10	14	μF
C_{HV}	High-voltage LDO regulator decoupling capacitor.	8	10	14	μF
C_{BATT}	Optional - Capacitor connected on BATT if no storage element is connected (see Section 9.4 and Section 9.6).	LDOs disabled.	22		μF
		LDOs enabled.	150		μF
R_T	Optional - Sum of resistors for setting battery protection threshold voltages in custom mode. $R_T = R1 + R2 + R3 + R4$ (see Section 9.1).	1	10	100	$M\Omega$
R_V	Optional - Sum of resistors for setting the output voltage of the high-voltage LDO in custom mode. $R_V = R5 + R6$ (see Section 9.1).	1	10	40	$M\Omega$
R_P	Optional - Sum of resistors used to define the primary battery minimum voltage. $R_P = R7 + R8$ (see Section 9.3).	100		500	$k\Omega$
Logic input pins					
ENHV	Enabling pin for the high-voltage LDO.	Logic HIGH (H).	Connect to BUCK.		
		Logic LOW (L).	Connect to GND.		
ENLV	Enabling pin for the low-voltage LDO.	Logic HIGH (H).	Connect to BUCK or BOOST.		
		Logic LOW (L).	Connect to GND.		
CFG[2:0]	Configuration pins for the storage element protection threshold voltages (see Table 8).	Logic HIGH (H).	Connect to BUCK.		
		Logic LOW (L).	Connect to GND.		
SELMPP[1:0]	Configuration pins for the MPPT ratio (see Table 9).	Logic HIGH (H).	Connect to BUCK.		
		Logic LOW (L).	Connect to GND.		

Table 6: Recommended operating conditions

7. Functional Block Diagram

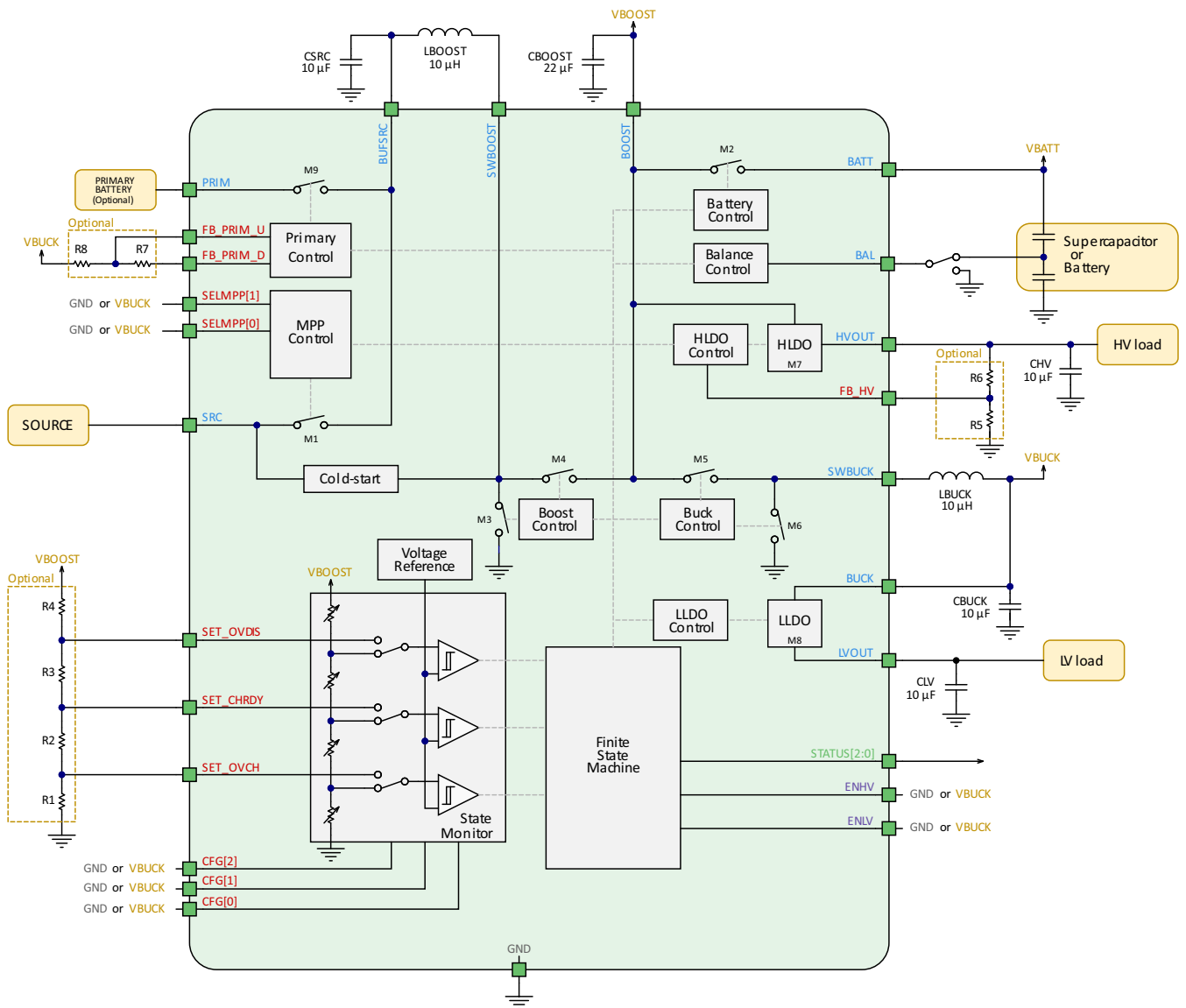


Figure 3: Functional block diagram

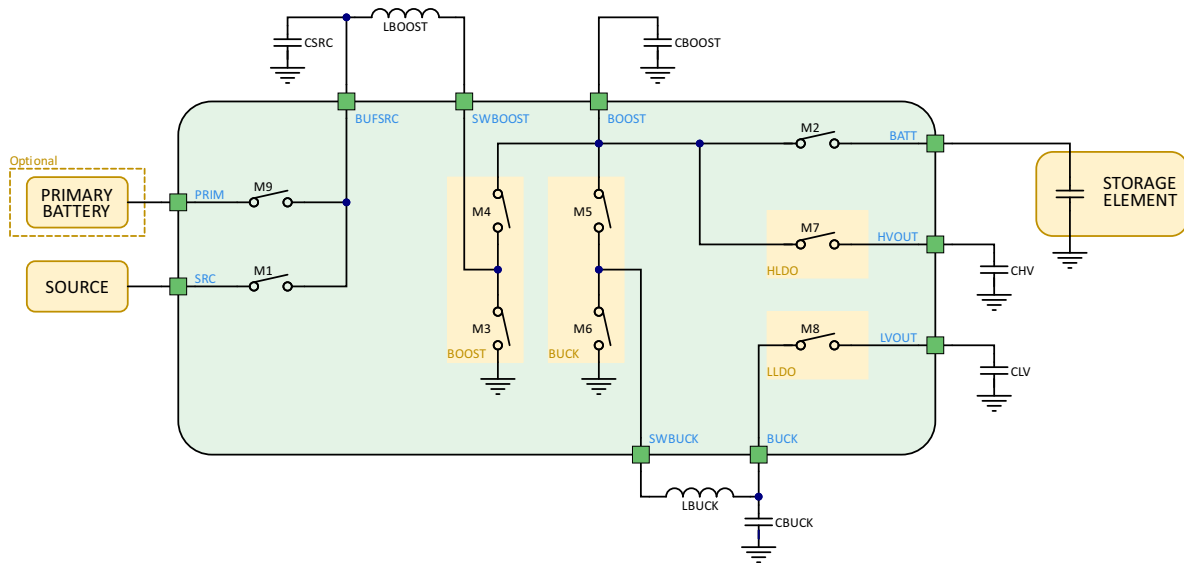


Figure 4: Simplified schematic view of the AEM10941

8. Theory of Operation

8.1. Power Converters

8.1.1. Boost Converter

The boost (or step-up) converter raises the voltage available at **BUFSRC** to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (V_{BOOST}) is available at the **BOOST** pin.

The switching transistors of the boost converter are M3 and M4, with the switching node available externally at **SWBOOST**. The reactive power components of this converter are the external inductor L_{BOOST} and the external capacitor C_{BOOST} .

The MPPT control circuit (see Section 8.3) periodically disconnects the source on **SRC** pin from the **BUFSRC** pin with the transistor M1 in order to measure the open-circuit voltage of the harvester on **SRC** and define the optimal **SRC** regulation voltage.

BUFSRC is decoupled by the capacitor C_{SRC} , which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the **BATT** pin. Its voltage is named V_{BATT} . This node is linked to **BOOST** through the transistor M2. In **NORMAL MODE** (see Section 8.2.2), this transistor effectively shorts the battery to the **BOOST** node ($V_{\text{BATT}} = V_{\text{BOOST}}$). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the LDOs. M2 is opened to disconnect the storage element when V_{BATT} reaches V_{OVDIS} . However, in such a scenario, the AEM10941 offers the possibility of connecting a primary battery to recharge V_{BATT} up to V_{CHRDY} . The transistor M9 connects **PRIM** to **BUFSRC** and the transistor M1 is opened to disconnect the **SRC** input pin as explained in the **PRIMARY BATTERY MODE** section.

More explanations about the different modes can be found in Section 8.2.

8.1.2. Buck Converter

The buck (or step-down) converter lowers the voltage from V_{BOOST} to a constant V_{BUCK} value of 2.2 V. This voltage is available at the **BUCK** pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at **SWBUCK**. The reactive power components of the buck converter are the external inductor L_{BUCK} and the external capacitor C_{BUCK} .

8.1.3. LDO Outputs

Two Low Drop-Out linear regulators are available to supply loads at different operating voltages:

- Through M7, **BOOST** supplies the high-voltage LDO that powers its load through **HVOUT**. This regulator delivers a clean voltage named V_{HV} . When using the built-in configuration modes, an output voltage of 1.8 V, 2.5 V or 3.3 V can be selected. When using the custom configuration mode, V_{HV} is adjustable between 1.8 V and $V_{OVDIS} - 0.3$ V. The output is decoupled by the external capacitor C_{HV} .
- Through M8, V_{BUCK} supplies the low-voltage LDO that powers its load through **LVOUT**. This regulator delivers a clean voltage named V_{LV} of 1.2 V or 1.8 V. The output is decoupled by the external capacitor C_{LV} .

See Table 5 for **HVOUT** and **LVOUT** maximum current values (respectively I_{HV} and I_{LV}).

Both the high-voltage and the low-voltage outputs can be dynamically enabled or disabled respectively with the logic control pins **ENHV** and **ENLV** (see Table below).

ENLV	LVOUT	ENHV	HVOUT
L	Disabled	L	Disabled
H	Enabled	H	Enabled

Table 7: LDOs configurations

8.2. Operating Modes

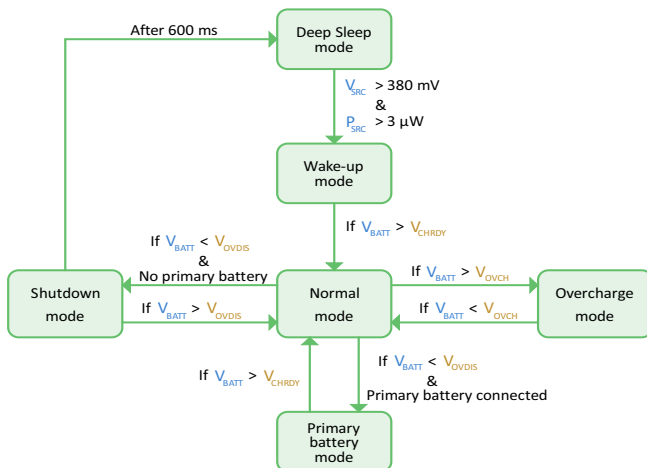


Figure 5: Diagram of the AEM10941 modes

8.2.1. Deep Sleep & Wake Up Modes

The **DEEP SLEEP MODE** is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold-start voltage of 380 mV and the required power of 3 μ W becomes available on **SRC**, the **WAKE-UP MODE** is activated. V_{BOOST} and V_{BUCK} rise up to a voltage of 2.2 V. V_{BOOST} then rises up to V_{OVCH} .

At this stage, both LDOs are internally disabled. Therefore, **STATUS[0]** is low as shown in Figure 11 and Figure 12.

When V_{BOOST} reaches V_{OVCH} , two scenarios are possible:

- In the first scenario, a supercapacitor or a capacitor having a voltage lower than V_{CHRDY} is connected to the **BATT** node (see Section 8.2.1.1).
- In the second scenario, a charged battery is connected to the **BATT** node (see Section 8.2.1.2).

8.2.1.1. Supercapacitor as a Storage Element

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges **BATT** from the input source and by modulating the conductance of M1 and M2. During the charge of the **BATT** node, both LDOs are disabled and **STATUS[0]** is set to low. When V_{BATT} reaches V_{CHRDY} , the circuit enters **NORMAL MODE**, **STATUS[0]** is asserted and the LDOs can be enabled by the user using **ENLV** and **ENHV** control pins as shown in Figure 11.

8.2.1.2. Battery as a Storage Element

If the storage element is a battery but its voltage is lower than V_{CHRDY} , the storage element first needs to be charged until it reaches V_{CHRDY} . This allows a safety margin to ensure that the storage element is able to provide the required power before enabling the outputs (LDOs).

Once V_{BATT} exceeds V_{CHRDY} , or if the battery was initially charged above V_{CHRDY} , the circuit enters **NORMAL MODE**. **STATUS[0]** is asserted and the LDOs can be dynamically enabled or disabled through **ENLV** and **ENHV** as shown in Figure 12.

8.2.2. Normal Mode

Once the AEM enters **NORMAL MODE**, it stays in this mode as long as the following condition is met:

$$V_{OVDIS} < V_{BATT} < V_{OVCH}$$

The AEM10941 will switch to another mode in the following cases:

- V_{BATT} increases above V_{OVCH} because the source provides more power than the load consumes. The circuit enters **OVERCHARGE MODE**, as explained in Section 8.2.3.
- V_{BATT} falls below V_{OVDIS} due to a lack of power from the source. In this case, either the circuit enters **SHUTDOWN MODE** as explained in Section 8.2.5, or, if a charged primary battery is connected on **PRIM**, the circuit enters **PRIMARY BATTERY MODE** as explained in Section 8.2.4.

8.2.3. Overcharge Mode

When V_{BATT} reaches V_{OVCH} , the battery charge is complete. The AEM maintains V_{BATT} around V_{OVCH} , with a hysteresis of a few mV as shown in Figure 13, to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain V_{BATT} and the LDOs are available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 4 is opened to prevent current from the source to the storage element when V_{SRC} is higher than V_{OVCH} .

8.2.4. Primary Battery Mode

When V_{BATT} drops below V_{OVDIS} , the circuit compares the voltage on **PRIM** with the voltage on **FB_PRIM_U** to determine whether a charged primary battery is connected on **PRIM**. The voltage on **FB_PRIM_U** is set thanks to two optional resistors as explained in Section 9.3.

If the following formula is true, the circuit considers the primary battery as available and the circuit enters **PRIMARY BATTERY MODE**.

$$\frac{V_{PRIM}}{4} > V_{FB_PRIM_U}$$

In that mode, transistor M1 is opened and the primary battery is connected to **BUFSRC** through transistor M9 to become the source of energy of the AEM10941. **STATUS[1]** is asserted as long as the chip is in **PRIMARY BATTERY MODE**.

The AEM remains in this mode until V_{BATT} reaches V_{CHRDY} . At that point, the circuit enters **NORMAL MODE**.

If no primary battery is used in the application, **PRIM**, **FB_PRIM_U** and **FB_PRIM_D** must be tied to GND.

8.2.5. Shutdown Mode

When V_{BATT} drops below V_{OVDIS} and no power is available from a primary battery, the circuit enters **SHUTDOWN MODE**, as shown in Figure 14, to prevent deep discharge that could damage the storage element and make the LDOs unstable. The circuit asserts **STATUS[1]** to warn the application that a shutdown may occur. Both LDO regulators remain enabled during the next 600 ms (T_{CRIT}).

If no primary battery is used, this mechanism allows the application circuit, whether it is powered on **LVOUT** or **HVOUT**, to trigger an interrupt by the low to-high transition of **STATUS[1]**, and to take all appropriate actions before **LVOUT** and **HVOUT** are disabled.

If V_{BATT} recovers to V_{OVDIS} within T_{CRIT} (about 600 ms), the AEM switches back to **NORMAL MODE**. But if, after T_{CRIT} , V_{BATT} does not reach V_{OVDIS} , the circuit enters **DEEP SLEEP MODE**. Both LDOs are disabled and **BATT** is disconnected from **BOOST** to avoid damaging the battery due to the overdischarge. From now on, the AEM must go through the wake-up procedure described in the Section 8.2.1.

8.3. Maximum Power Point Tracking

During **NORMAL MODE**, **SHUTDOWN MODE** and a part of **WAKE-UP MODE**, the boost converter is regulated thanks to an internal MPPT (Maximum Power Point Tracking) module. V_{MPP} is the voltage level of the MPP, and depends on the input power available at the source.

The MPPT module evaluates V_{MPP} as a constant fraction of the open-circuit voltage of the source V_{OC} . The ratio between V_{MPP} and V_{OC} can be configured with the **SELMPP[1:0]** pins.

The AEM10941 periodically measures V_{OC} by stopping to pull current from the source (**SRC** pin) during $T_{MPPT,VOC}$ (82 ms) every $T_{MPPT,PERIOD}$ (5 s), thus letting the source rise to its open-circuit voltage. The source target voltage V_{MPP} is then redefined as a fraction of the previously measured V_{OC} . This way, the MPPT module adapts to the harvester variations due to varying ambient conditions. The behavior of the MPPT module is shown in Figure 6.

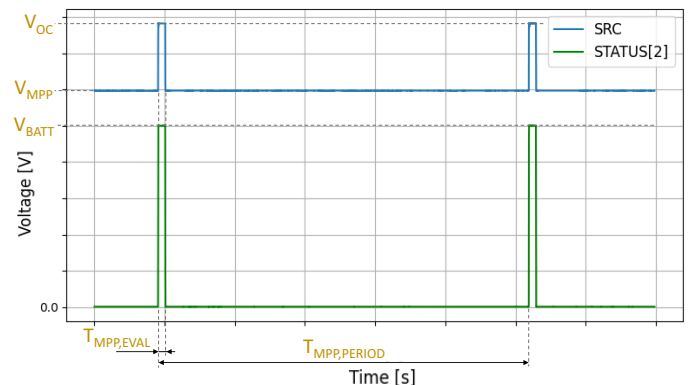


Figure 6: MPP evaluation behavior

With the exception of this sampling process, the source voltage V_{SRC} is continuously compared to V_{MPP} :

- When V_{SRC} exceeds V_{MPP} by a small hysteresis, the boost converter is switched on, extracting electric charges from the source, thus lowering its voltage.
- When V_{SRC} falls below V_{MPP} by a small hysteresis, the boost converter is switched off, allowing the harvester to accumulate new electric charges into C_{SRC} , which voltage rises.

This way, the boost converter regulates its input voltage so that the electric current (or flow of electric charges) that enters the boost converter yields the best power transfer from the harvester under any ambient conditions. The AEM10941 supports any V_{MPP} level in the range from 50 mV to 4.5 V. It offers a choice of four values for the V_{MPP} / V_{OC} ratio through the configuration pins **SELMPP[1:0]** as shown in Table 9. The status of the MPPT controller is reported through one dedicated status pins (**STATUS[2]**). This status pin is asserted when a MPPT module periodic V_{OC} evaluation is being performed.

8.4. Storage Element Balancing Circuit for Dual-cell Supercapacitor

When using a dual-cell supercapacitor, it is necessary to keep both cells at similar voltages to avoid damage due to a potential over-voltage on one cell. This is ensured by the AEM10941 storage element balancing circuit.

If a battery, a capacitor or a single-cell supercapacitor is connected on **BATT**, **BAL** is connected to **GND** and the storage element balancing circuit is disabled.

If a dual-cell supercapacitor is connected on **BATT**, **BAL** is connected to the node between the two cells of the supercapacitor. The storage element balancing circuit compensates for any mismatch of the two cells that could overcharge one of both cells. It ensures that **BAL** remains close to $V_{BATT} / 2$.

9. System Configuration

9.1. Battery and LDOs Configuration

Configurations pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V _{OVCH}	V _{CHRDY}	V _{OVDIS}	V _{HV}	V _{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell supercapacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - Programmable through R1 to R6.					1.8 V

Table 8: Usage of CFG[2:0]

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling the boost converter.
- V_{CHRDY}: minimum voltage required on the storage element after a cold start before enabling the LDOs.
- V_{OVDIS}: minimum voltage accepted on the storage element before considering the storage element as depleted.

See Section 8 for more information about the purposes of these thresholds.

The two LDOs output voltages are called V_{HV} and V_{LV} for the high and low output voltages respectively. Seven combinations of these voltage levels are hard-wired and selectable through the CFG[2:0] configuration pins, covering most application cases. For other V_{OVCH}, V_{CHRDY}, V_{OVDIS} and V_{HV} voltages combinations, a custom mode is available. In this mode, the user can define those voltages with resistors, connected to the pins named SET_OVDIS, SET_CHRDY, SET_OVCH and FB_HV.

When the custom mode is not used, SET_OVDIS, SET_CHRDY and SET_OVCH pins must be connected to V_{BUCK} and FB_HV must be left floating.

9.1.1. Custom Mode

When CFG[2:0] are tied to GND, the custom mode is selected. All six resistors, shown in Figure 7, are used to configure the custom mode as follows:

V_{OVCH}, V_{CHRDY} and V_{OVDIS} are defined thanks to R1, R2, R3 and R4. The resistors are calculated as follows:

- $R_T = R1 + R2 + R3 + R4$
- $1\text{M}\Omega \leq R_T \leq 100\text{M}\Omega$
- $R1 = R_T \cdot \frac{1\text{V}}{V_{OVCH}}$
- $R2 = R_T \cdot \left(\frac{1\text{V}}{V_{CHRDY}} - \frac{1\text{V}}{V_{OVCH}} \right)$
- $R3 = R_T \cdot \left(\frac{1\text{V}}{V_{OVDIS}} - \frac{1\text{V}}{V_{CHRDY}} \right)$
- $R4 = R_T \cdot \left(1 - \frac{1\text{V}}{V_{OVDIS}} \right)$

V_{HV} is defined thanks to R5 and R6. The resistive divider is configured as follows:

- $R_V = R5 + R6$
- $1\text{M}\Omega \leq R_V \leq 40\text{M}\Omega$
- $R5 = R_V \cdot \frac{1\text{V}}{V_{HV}}$
- $R6 = R_V \cdot \left(1 - \frac{1\text{V}}{V_{HV}} \right)$

NOTE: If ENHV = L (HVOUT is disabled), R5 and R6 are not needed, FB_HV should be left floating.

The resistors should have high values to make the current flowing through them negligible. Moreover, the following constraints must be met to ensure the functionality of the chip:

- $V_{\text{CHRDY}} + 0.05\text{V} \leq V_{\text{OVCH}} \leq 4.5\text{V}$
- $V_{\text{OVDIS}} + 0.05\text{V} \leq V_{\text{CHRDY}} \leq V_{\text{OVCH}} - 0.5\text{V}$
- $2.2\text{V} \leq V_{\text{OVDIS}}$
- $V_{\text{HV}} \leq V_{\text{OVDIS}} - 0.3\text{V}$

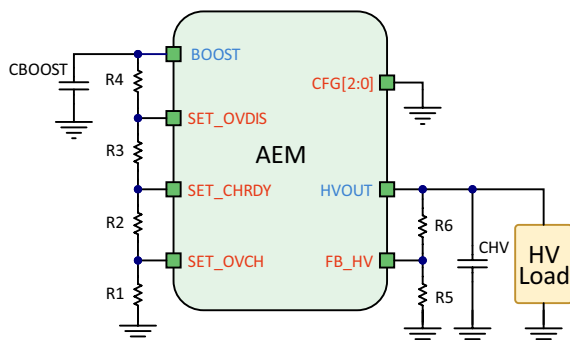


Figure 7: Custom configuration resistors

9.2. MPPT Configuration

Two dedicated configuration pins, **SELMPP[1:0]**, allow selecting the MPP tracking ratio based on the characteristic of the input power source.

SELMPP[1]	SELMPP[0]	V_{MPP} / V_{OC}
L	L	70%
L	H	75%
H	L	85%
H	H	90%

Table 9: Usage of SELMPP[1:0]

9.3. Primary Battery Configuration

To use the primary battery, it is mandatory to determine $V_{\text{PRIM,MIN}}$, the voltage at which the primary battery is considered as fully depleted. The circuit uses a resistive divider between **BUCK** and **FB_PRIM_D** to define the voltage on **FB_PRIM_U** as $V_{\text{PRIM,MIN}}$ divided by 4. During $V_{\text{PRIM,MIN}}$ evaluation, the circuit connects **FB PRIM D** to **GND**.

When $V_{\text{PRIM,MIN}}$ is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. The resistors are calculated as follows:

- $R_P = R_7 + R_8$
- $100k\Omega \leq R_P \leq 500k\Omega$
- $R_7 = \frac{V_{PRIM_MIN}}{4} \cdot R_P \cdot \frac{1}{2.2V}$
- $R_8 = R_P - R_7$

*NOTE: **FB_PRIM_U**, **FB_PRIM_D** and **PRIM** must be tied to GND if no primary battery is used.*

9.4. No-battery Configuration

If the application doesn't use a storage element, the PCB must include a capacitor on the **BATT** pin. See Section 9.6 for C_{BATT} value.

The storage element may not be necessary in the following cases:

- If the harvested energy source is permanently available and covers the application purposes.
- If the application does not need to store energy when the harvested energy source is not available.

9.5. Supplying an Application Circuit with BUCK

It is possible to supply an application circuit directly from **BUCK**, with the benefit of high **BATT** to **BUCK** efficiency, provided that the following conditions are met:

- The application circuit can be supplied from a voltage in the 2.0 V - 2.5 V range (V_{BUCK} is typically 2.2 V with ripple, see Table 5).
- The sum of the following currents must be below the maximum I_{BUCK} value (see Table 5):
 - Current of the load connected to **BUCK**.
 - Current of the load connected to **LVOUT**.
- The application circuit on **BUCK** does not pull current during the AEM10941 cold start.

To satisfy the last condition, the following circuit may be implemented:

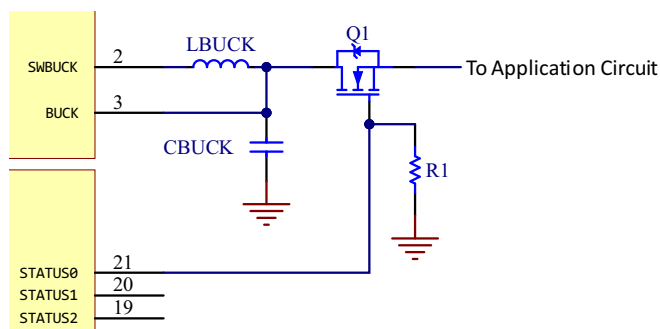


Figure 8: Schematic for supplying an application circuit with BUCK

Q1 is a N-MOSFET, whose gate is driven by **STATUS[0]** with R1 as a pull-down resistor. When the AEM10941 is in **DEEP SLEEP MODE** or in **WAKE-UP MODE**, **STATUS[0]** is LOW (see Section 8.2), ensuring that Q1 is non-conducting, and thus that the application circuit is not supplied.

When the AEM10941 switches from **WAKE-UP MODE** to **NORMAL MODE**, **STATUS[0]** is HIGH, making Q1 conducting. The application circuit is then supplied by **BUCK**, and remains so when the AEM10941 is in **NORMAL MODE**, **OVERCHARGE MODE**, **PRIMARY BATTERY MODE** and **SHUTDOWN MODE**.

Q1 must be chosen as follows:

- Low Gate-Source Leakage I_{GSS} .
- Low Zero Gate Voltage Drain Current I_{DSS} .
- Drain-Source On-State Resistance $R_{DS(on)}$ low enough to supply application circuit with an acceptable voltage drop.
- V_{GS} maximum voltage must be above V_{OVCH} (**STATUS[0]** HIGH voltage is V_{BOOST}).
- Maximum gate-source threshold voltage $V_{GS(th),MAX}$ matches the following, with $V_{BUCK,MAX}$ being V_{BUCK} maximum value stated in Table 5:

$$V_{GS(th),MAX} < V_{OVDIS} - V_{BUCK,MAX}$$

9.6. Storage Element Information

The energy storage element of the AEM10941 can be a rechargeable battery, a supercapacitor or a large capacitor. It should be chosen so that its voltage does not fall below V_{OVDIS} even during occasional peaks of the load current. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to buffer the battery by decoupling it with a capacitor.

The **BATT** pin, connecting the storage element, must never be left floating. If the application expects a disconnection of the battery (e.g., because of a user removable connector), the PCB must include a capacitor:

- If the LDOs are used, the minimum needed capacitor value is 150 μF .
- If the LDOs are not used, the minimum needed capacitor value is 22 μF .

The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the subsystem.

9.7. External Inductors Information

The AEM10941 operates with two standard miniature inductors. Switching frequency must be at least 10 MHz for both. Low equivalent series resistance (ESR) favors the power conversion efficiency of the boost and buck converters.

L_{BOOST}

The AEM10941 circuit is typically implemented with one of the following values on L_{BOOST} :

- 10 μH (peak current min. 250 mA) allows higher current from **SRC** to **BATT**.
- 22 μH (peak current min. 115 mA) allows better efficiencies, especially at low **SRC** voltages.

L_{BUCK}

The buck inductor L_{BUCK} must sustain a peak current of at least 50 mA. The recommended value is 10 μH .

9.8. External Capacitors Information

The AEM10941 operates with:

- Four identical standard miniature ceramic capacitors of 10 μF .
- One miniature ceramic capacitor of 22 μF .

The leakage current of the capacitors should be small as leakage currents directly impact the quiescent current of the subsystem.

C_{SRC}

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage fluctuations of V_{SRC} when the boost converter is switching. The recommended value is 10 μF +/- 20%.

C_{BUCK}

This capacitor acts as an energy buffer for the buck converter. It also reduces the voltage ripple induced by the current pulses inherent to the switching mode of the converter. The recommended value is 10 μF +/- 20%.

C_{BOOST}

This capacitor acts as an energy buffer for the boost converter. It also reduces the voltage ripple induced by the current pulses inherent to the switching mode of the converter. The recommended value is 22 μF +/- 20%.

C_{HV} / C_{LV}

These capacitors ensure a high-efficiency load regulation of the high-voltage and low-voltage LDO regulators. Closed-loop stability requires the value to be in the range of 8 μF to 14 μF .

10.2. Example Circuit 2

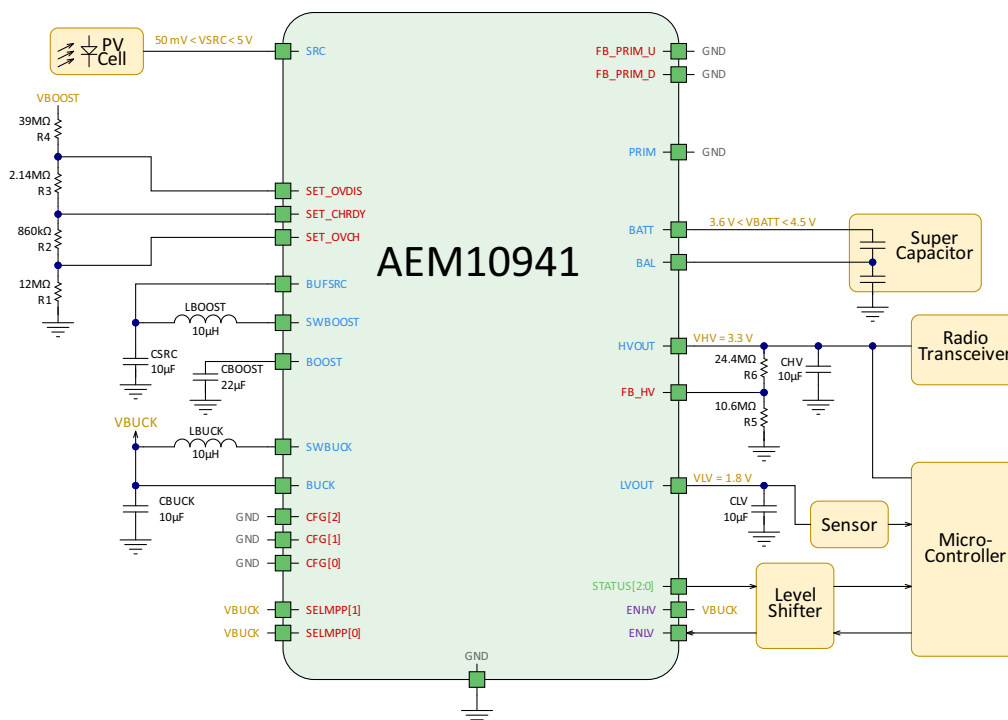


Figure 10: Typical application circuit 2

The energy source is a photovoltaic cell and the storage element is a dual-cell supercapacitor. Please note that the supercapacitor might be completely depleted during the cold start.

Moreover, BAL is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and, in that way, protect the supercapacitor.

A micro-controller acts as the application master. The operating mode pins are set as follows:

- CFG[2:0] = LLL (all to GND)

The storage element voltages are set as follows with a custom configuration:

- $V_{OVCH} = 4.5 \text{ V}$
- $V_{CHRDY} = 4.2 \text{ V}$
- $V_{OVDIS} = 3.6 \text{ V}$

R_T is set to 54 M Ω . R_1 , R_2 , R_3 and R_4 values are computed from the equations in Section 9.1.1:

- $R1 = 54\text{M}\Omega \cdot \frac{1\text{V}}{4.5\text{V}} = 12\text{M}\Omega$
- $R2 = 54\text{M}\Omega \cdot \left(\frac{1\text{V}}{4.2\text{V}} - \frac{1\text{V}}{4.5\text{V}} \right) = 860\text{k}\Omega$
- $R3 = 54\text{M}\Omega \cdot \left(\frac{1\text{V}}{3.5\text{V}} - \frac{1\text{V}}{4.2\text{V}} \right) = 2.14\text{M}\Omega$
- $R4 = 54\text{M}\Omega \cdot \left(1 - \frac{1\text{V}}{3.5\text{V}} \right) = 39\text{M}\Omega$

The LDO voltages are set as follows:

- $V_{HV} = 3.3 \text{ V}$
- $V_{IV} = 1.8 \text{ V}$

Enabling and disabling **LVOUT** is controlled by the application circuit with a micro-controller GPIO connected to **ENLV**.

ENHV is tied to BUCK so that HVOUT is always on.

R_V is set to 35 M Ω . R5 and R6 are determined by applying the equations found in Section 9.1:

- $R5 = 35\text{M}\Omega \cdot \frac{1\text{V}}{3.3\text{V}} = 10.6\text{M}\Omega$
- $R6 = 35\text{M}\Omega \cdot \left(1 - \frac{1\text{V}}{3.3\text{V}}\right) = 24.4\text{M}\Omega$

The micro-controller is supplied by **HVOUT**, which is enabled when **V_{BATT}** and **V_{BOOST}** voltages rise above **V_{CHRDY}**.

The MPP configuration pins **SELMPP[1:0]** are tied to **BUCK** (logic HIGH), thus, selecting an MPP ratio of 90%, suitable for the particular PV cell in use.

No primary battery is connected: PRIM, FB_PRIM_U and FB_PRIM_D pins are tied to GND.

11. Circuit Behavior

11.1. Cold-start Behavior

11.1.1. (Super)capacitor as a Storage Element

The following figure shows the AEM10941 behavior with a capacitor connected to **BATT** and the following settings:

- **CFG[2:0]** = LHH
- **SELMPP[1:0]** = LH (75%)
- **C_{BATT}** = 4.85 mF
- **SRC**: 1 mA current source with 3 V voltage compliance
- **ENHV** = **ENLV** = H
- 22 kΩ resistive load on **LVOUT**
- 2 kΩ resistive load on **HVOUT**

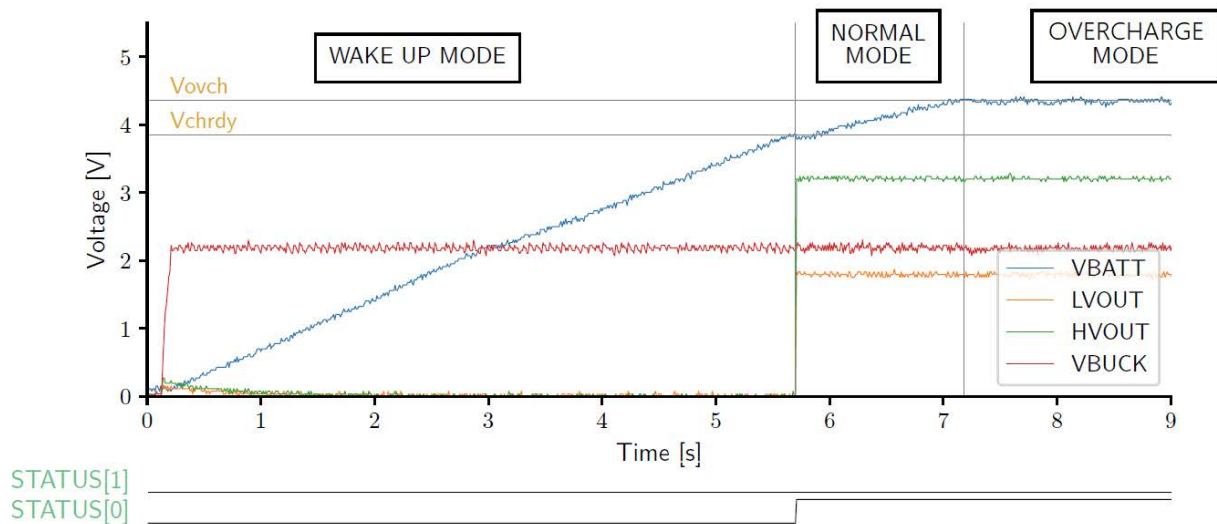


Figure 11: Cold start with a capacitor connected to BATT

11.1.2. Battery as a Storage Element

The following figure shows the AEM10941 behavior with a pre-charged capacitor (acting as a battery) connected to **BATT** and the following settings:

- **CFG[2:0]** = LHH
- **SELMPP[1:0]** = LH (75%)
- **C_{BATT}** = 4.85 mF
- **SRC**: 1 mA current source with 3 V voltage compliance
- **ENHV** = **ENLV** = H
- 22 kΩ resistive load on **LVOUT**
- 2 kΩ resistive load on **HVOUT**

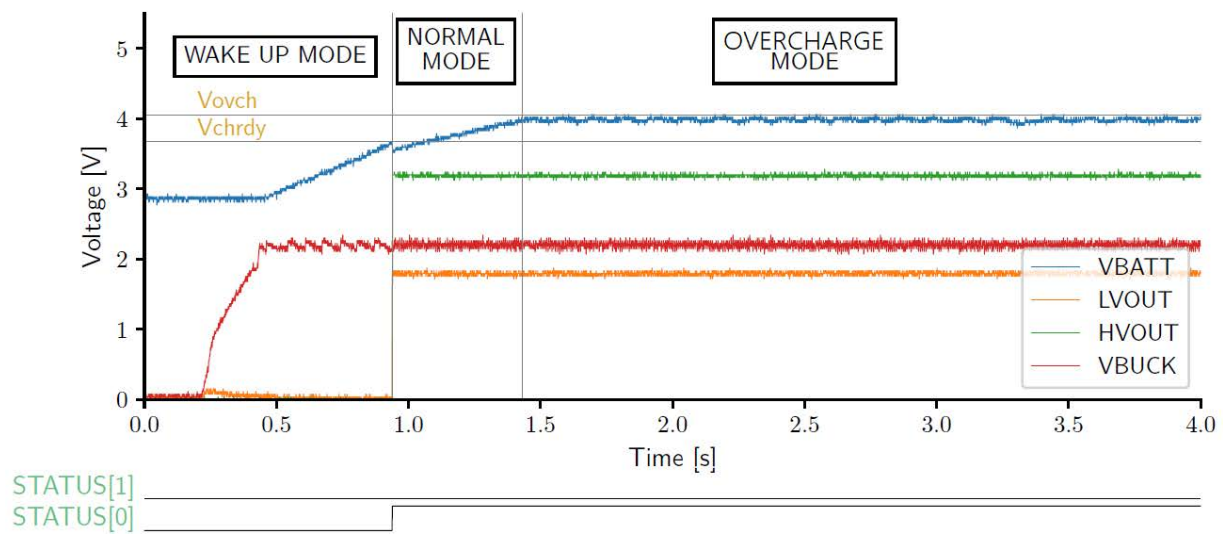


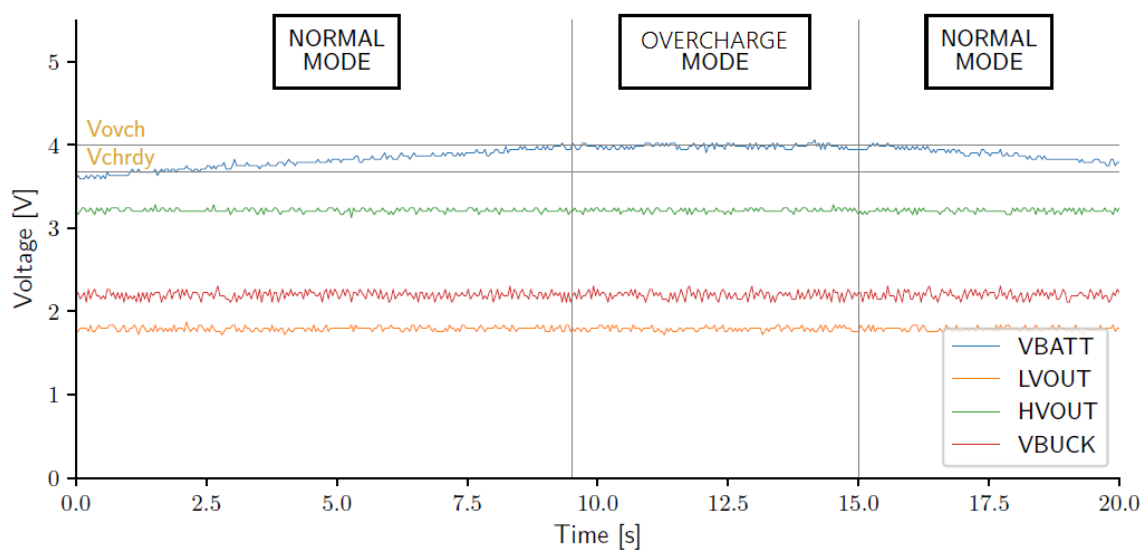
Figure 12: Cold start with a battery connected to BATT



11.2. Overcharge Mode Behavior

The following figure shows the AEM10941 behavior in **OVERCHARGE MODE** with the following settings:

- **CFG[2:0]** = HHH
- **SELMPP[1:0]** = LH (75%)
- **C_{BATT}** = 4.85 mF
- **SRC**: 1 mA current source with 3 V voltage compliance
- **ENHV** = **ENLV** = H
- 22 kΩ resistive load on **LVOUT**
- 2 kΩ resistive load on **HVOUT**



STATUS[1]

STATUS[0]

Figure 13: Overcharge mode

11.3. Shutdown Mode Behavior

11.3.1. Without Primary Battery

The following figure shows the AEM10941 behavior in **SHUTDOWN MODE** with the following settings:

- **CFG[2:0]** = LHL
- **SELMPP[1:0]** = LH (75%)
- **C_{BATT}** = 4.85 mF
- **SRC**: left floating to let the storage element on **BATT** discharge
- **ENHV** = **ENLV** = H
- 22 kΩ resistive load on **LVOUT**
- 22 kΩ resistive load on **HVOUT**
- **PRIM**, **FB_PRIM_U** and **FB_PRIM_D** connected to GND

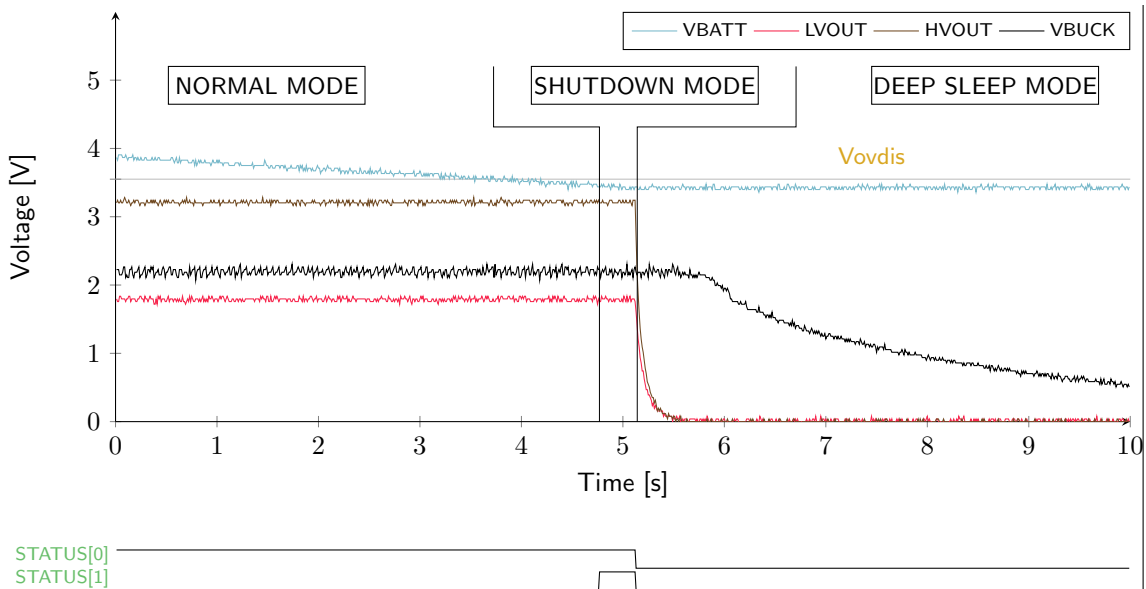


Figure 14: Shutdown mode (without primary battery)

11.3.2. With Primary Battery

The following figure shows the AEM10941 behavior in **SHUTDOWN MODE** with the following settings:

- CFG[2:0] = HHH
- SELMPP[1:0] = LH (75%)
- C_{BATT} = 4.85 mF
- SRC: left floating to let the storage element on BATT discharge
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 22 kΩ resistive load on HVOUT
- PRIM: 3 V voltage source with 1 mA current compliance
- R7 = 68 kΩ
- R8 = 330 kΩ

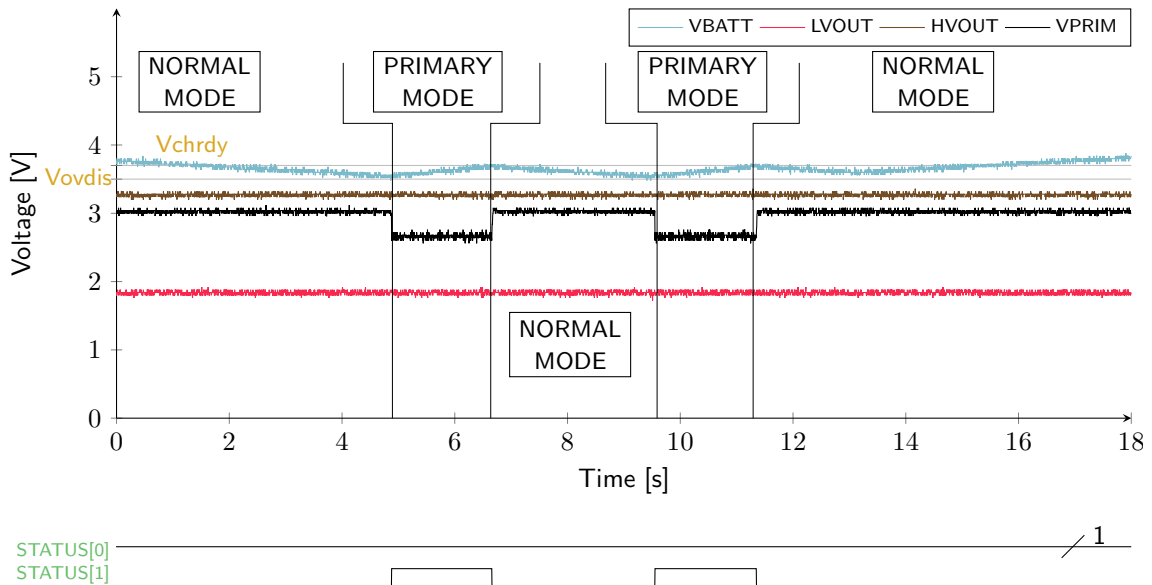


Figure 15: Switching to primary battery when battery is overdischarged

12. Performance Data

12.1. BOOST Conversion Efficiency for LBOOST = 10 μ H

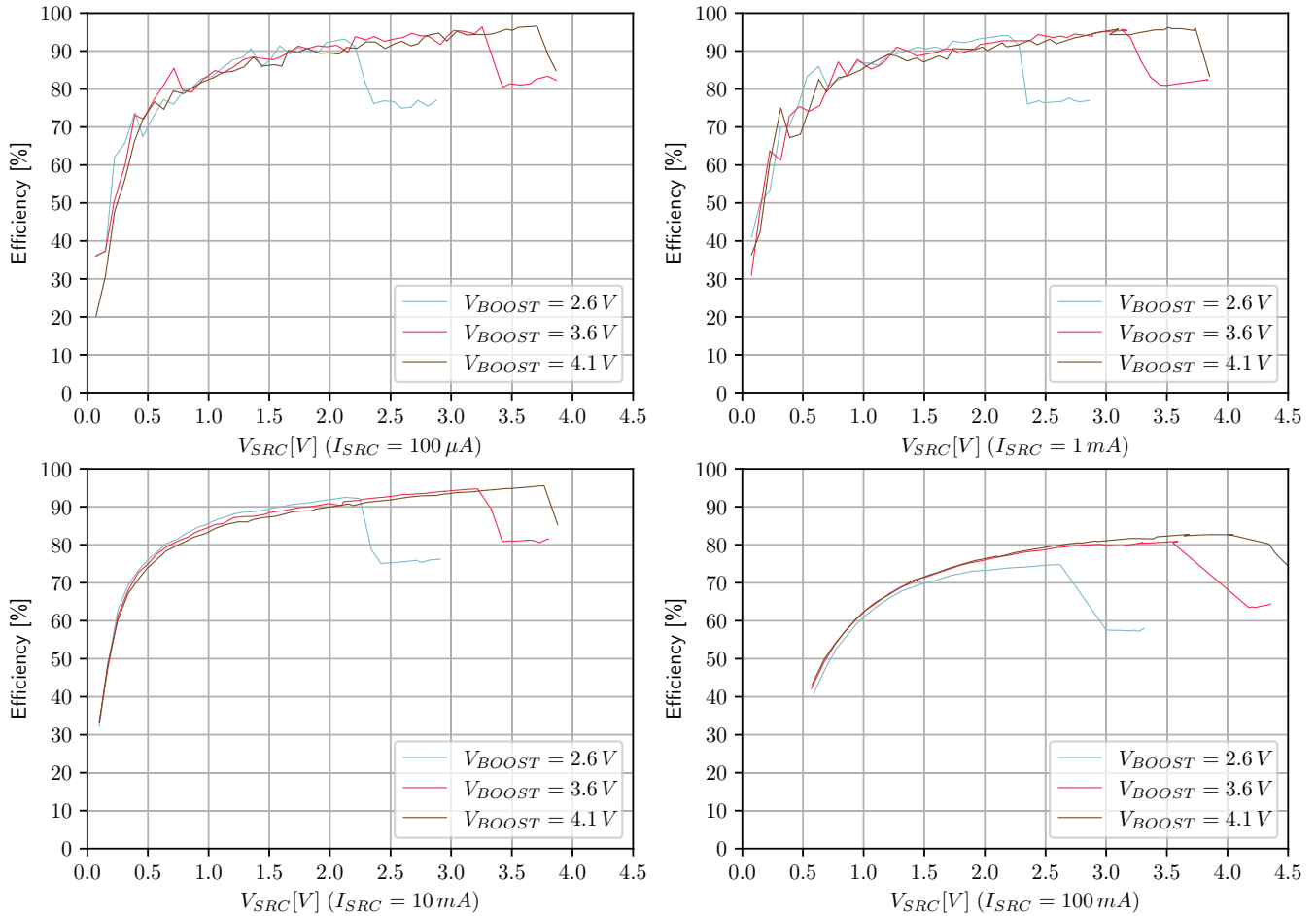


Figure 16: Boost efficiency for I_{SRC} at 100 μA , 1 mA, 10 mA and 100 mA ($L_{BOOST} = 10 \mu H$)

12.2. BOOST Conversion Efficiency for LBOOST = 22 μ H

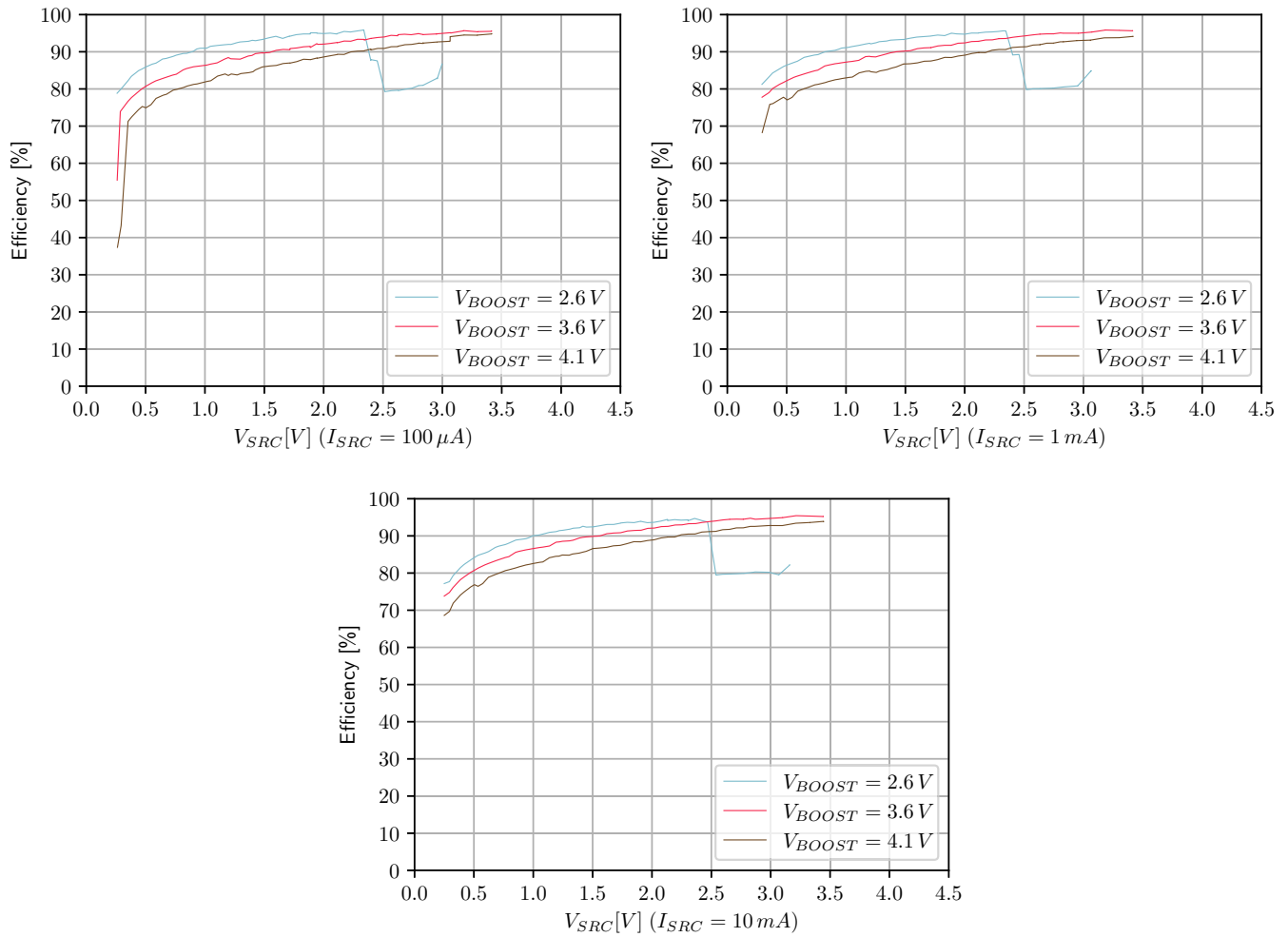


Figure 17: Boost efficiency for I_{src} at 100 μ A, 1mA and 10mA ($L_{BOOST} = 22 \mu\text{H}$)

12.3. BUCK Conversion Efficiency

The following graph shows the buck converter efficiency from **BATT** to **BUCK** with the AEM10941 quiescent current I_Q subtracted.

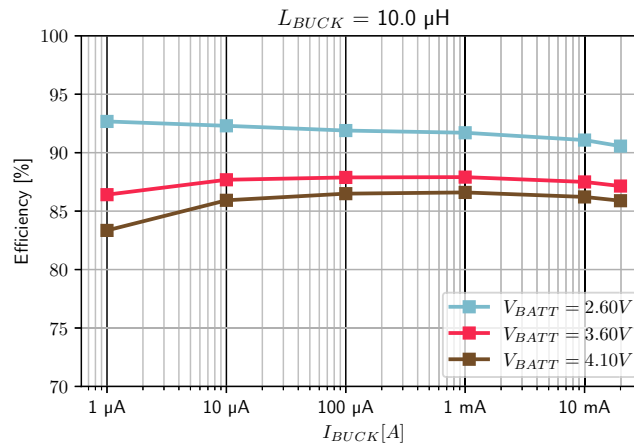


Figure 18: Buck Efficiency ($L_{BUCK} = 10 \mu H$)

12.4. Quiescent Current

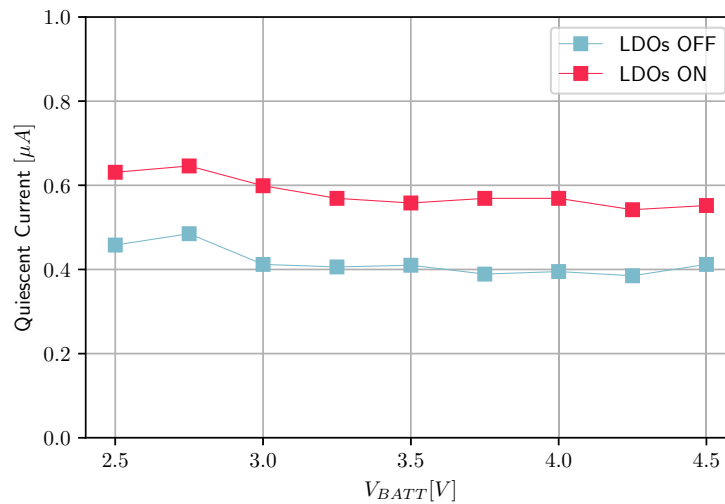


Figure 19: Quiescent current with LDOs on and off



12.5. High-voltage LDO Regulation

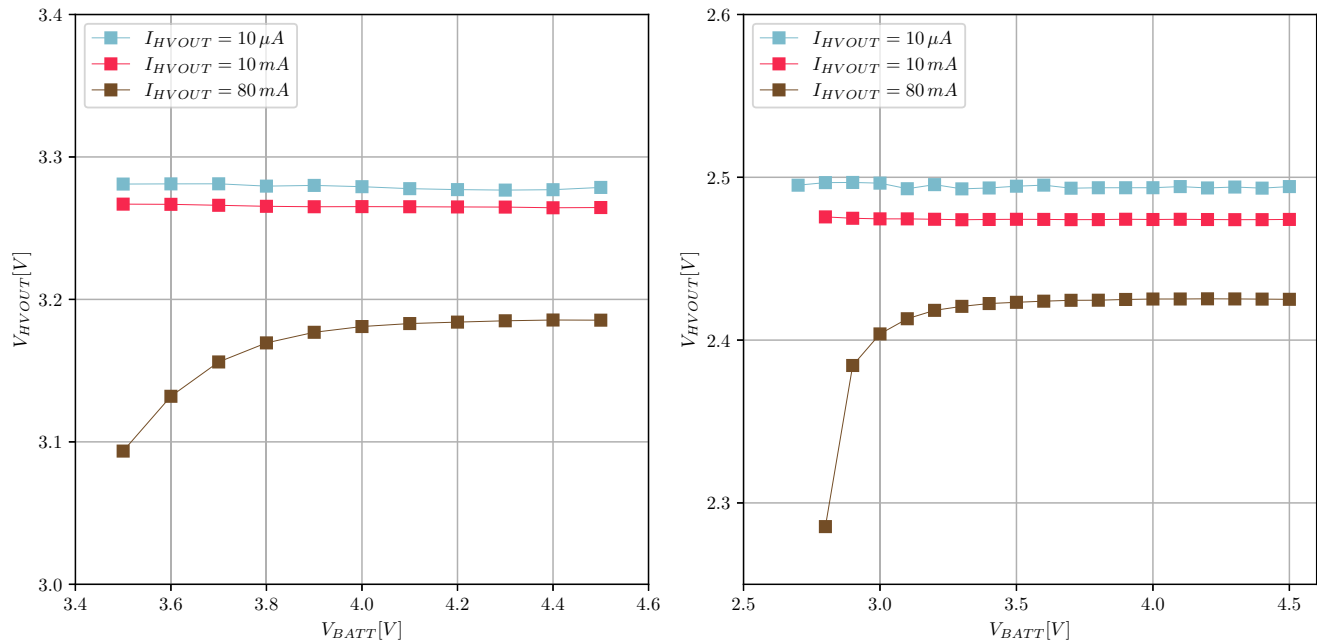


Figure 20: HVOUT at 3.3 V and 2.5 V

12.6. Low-voltage LDO Regulation

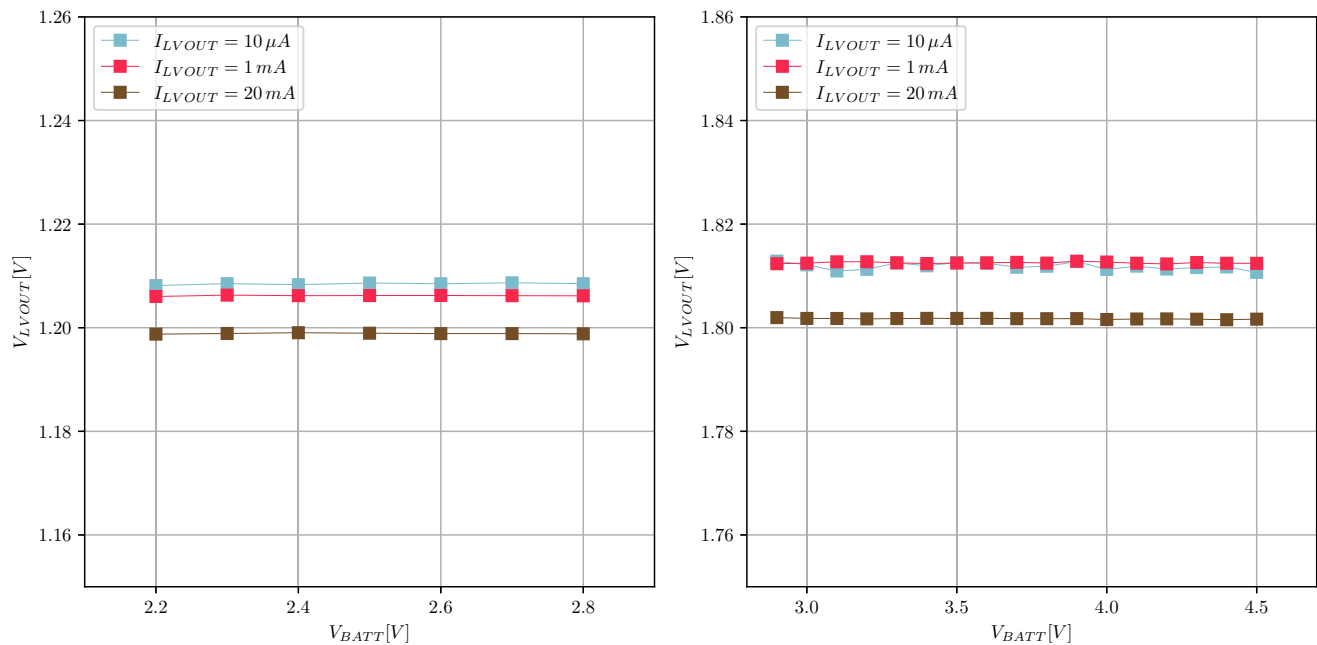


Figure 21: LVOUT at 1.2 V and 1.8 V

12.7. High-voltage LDO Efficiency

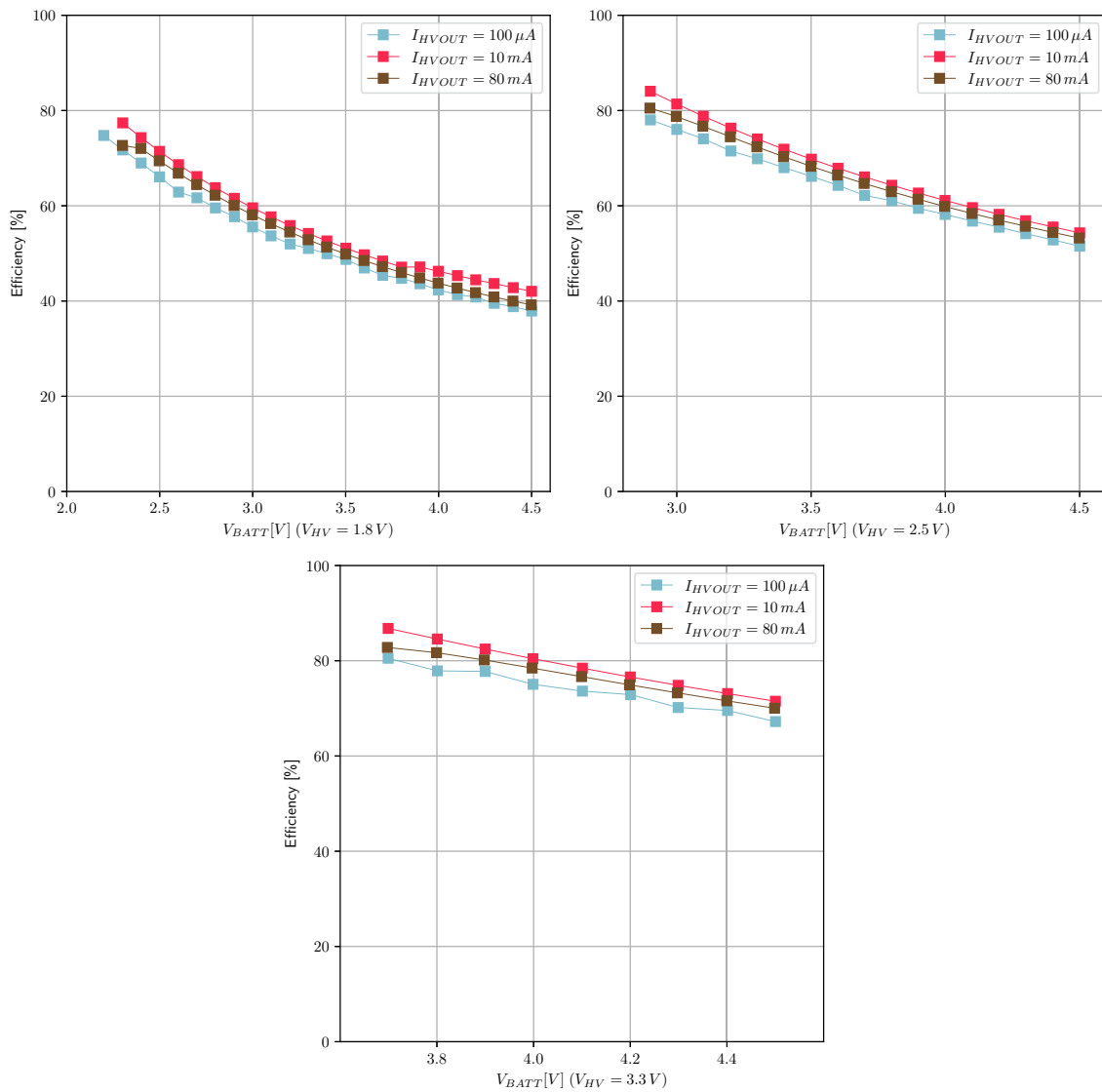


Figure 22: HVOUT efficiency at 1.8V, 2.5V and 3.3 V

The theoretical efficiency of an LDO can be calculated as V_{out} / V_{in} if quiescent current can be neglected with regards to the output current. For the high-voltage LDO, the theoretical efficiency is equal to V_{HV} / V_{BATT} .

12.8. Low-voltage LDO Efficiency

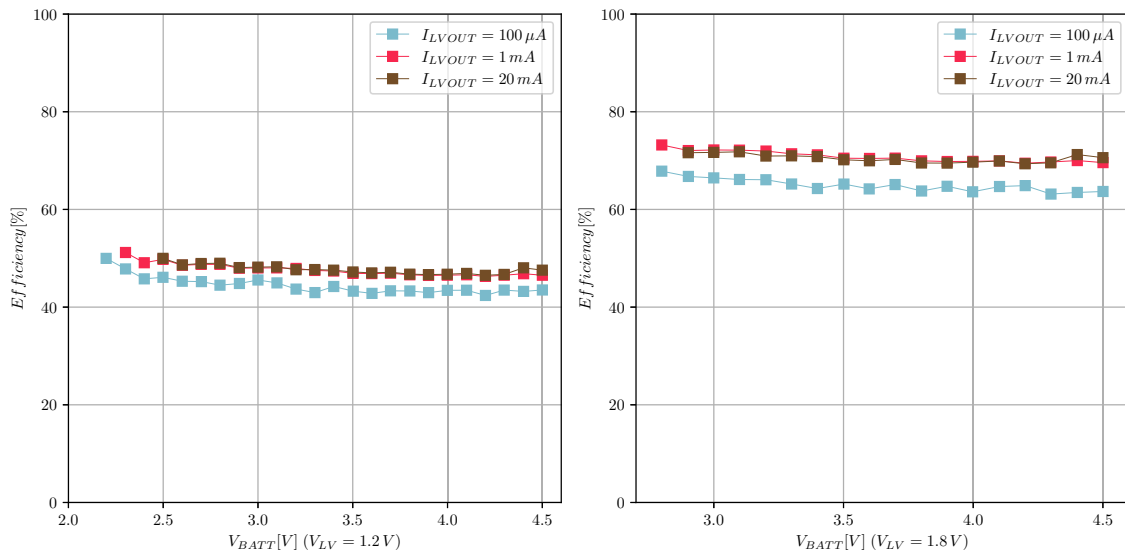


Figure 23: Efficiency of buck cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of an LDO can be calculated as V_{LV} / V_{BUCK} . Starting from the battery, the efficiency of the buck converter (η_{BUCK}) has to be taken into account (see Figure 4).

The efficiency between V_{BATT} and V_{LV} is therefore equal to:

$$\eta_{BUCK} \cdot \frac{V_{LV}}{V_{BUCK}}$$

13. Schematic

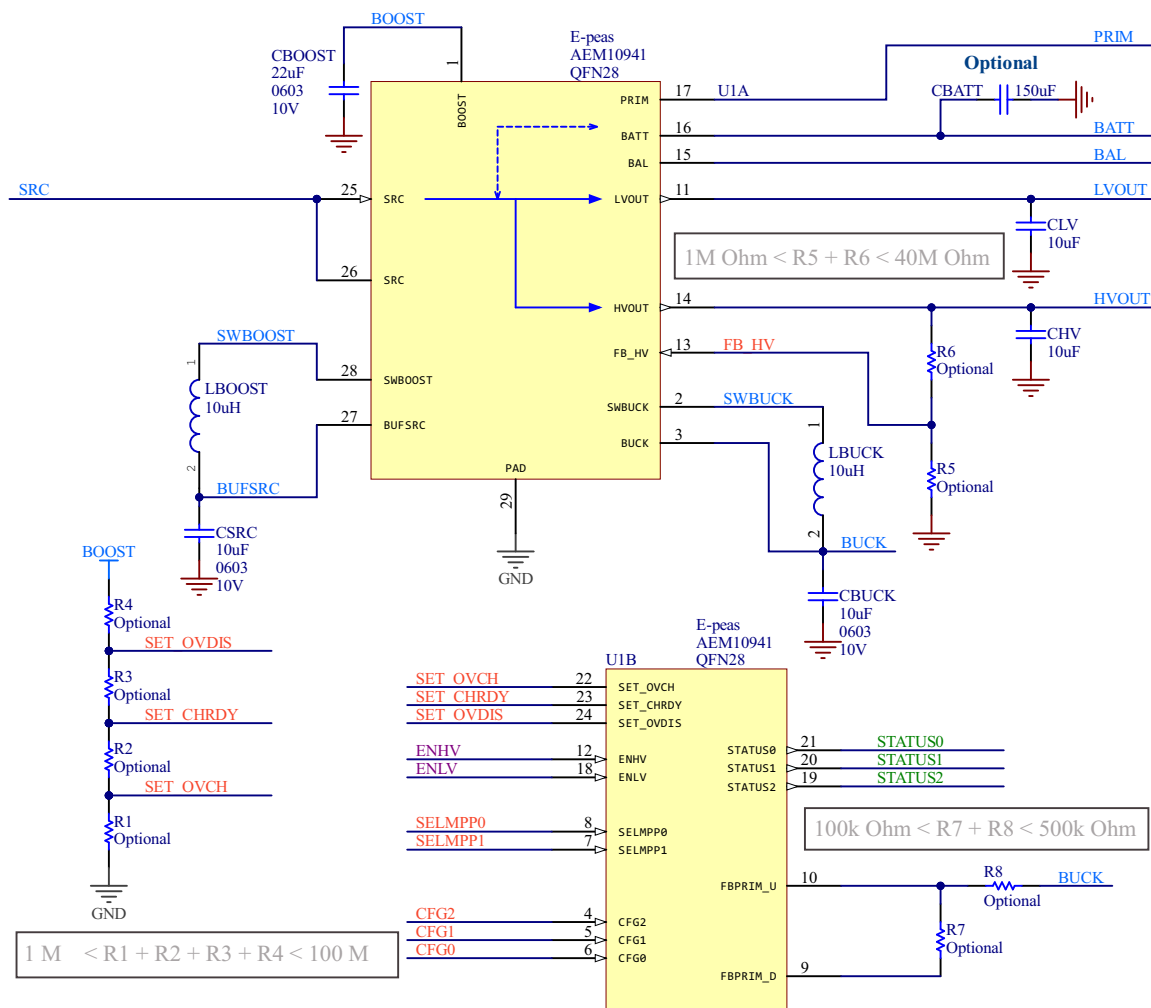


Figure 24: Schematic example

Designator	Description	Quantity	Manufacturer	Part Number
U1	AEM10941	1	e-peas	order at sales@e-peas.com
L _{BOOST}	Power Inductor 10 µH - 0,90 A - LPS4018	1	Coilcraft	LPS4018-103MR
L _{BOOST} (alt.)	Power Inductor 10 µH - 0,84 A - 3015	1	Würth	744 040 321 00
L _{BOOST} (alt.)	Power Inductor 22 µH - 0,65 A - LPS4018	1	Coilcraft	LPS4018-223MR
C _{BOOST}	Ceramic Cap 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
L _{BUCK}	Power Inductor 10 µH - 0,25 A - 0603	1	TDK	MLZ1608M100WT
C _{BUCK}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C _{SRC}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C _{HV}	Ceramic Cap 10 µF, 25 V, 10%, X7S, 0805	1	TDK	C2012X7S1E106K125AE
C _{LV}	Ceramic Cap 10 µF, 10 V, 20%, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C _{BATT}	Ceramic Cap 150 µF, 6.3 V, 20%, X5R, 1206	1	TDK	GRM31CR60J157ME11L

Table 10: BOM example for AEM10941 and its required passive components

14. Layout

14.1. Guidelines

Good layout practices are mandatory in order to obtain good AEM10941 stability, best efficiency and avoid EMI problems.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM10941:

- The switching nodes (**BUFSRC**, **SWBOOST**, **SWBUCK** and **BUCK**) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between these switching nodes and the AEM10941 pins. Minimal capacitance is obtained by maintaining a large distance between the switching nodes and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under **LBOOST** and **LBUCK** footprints, as well as adding distance between **BUFSRC/SWBOOST** and the top ground pour, as shown in Figure 25.
- The decoupling capacitors (**CBOOST** - **CBUCK** - **CSRC** - **CHV** - **CLV** - **CBATT**) must be placed as close as possible to the AEM10941, with direct connection and minimum track resistance for the corresponding power nodes (**BOOST**, **BUCK**, **BUFSRC**, **HVOUT**, **LVOUT** and **BATT**).
- The **GND** return path between the decoupling capacitors and the AEM10941 thermal pad, which is the AEM10941 main **GND** connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance. In Figure 25, this **GND** return path is done on an internal plane.
- The external DC power connections (**SRC**, **HVOUT**, **LVOUT** and **BATT**) must be connected to the AEM10941 with low resistance tracks.
- The **BAL** pin connection track must be able to handle at least 40 mA.
- The custom mode setting pins **SET_OVDIS**, **SET_CHRDY** and **SET_OVCH** are high impedance analog inputs typically connected to a resistive divider with high resistor values, making those three nodes prone to pickup noise. Thus, it is recommended to keep those as short as possible and as far as possible to noise sources such as DCDC switching nodes.
- The configuration pins and the status pins have minimal layout restrictions.

14.2. Layout Example

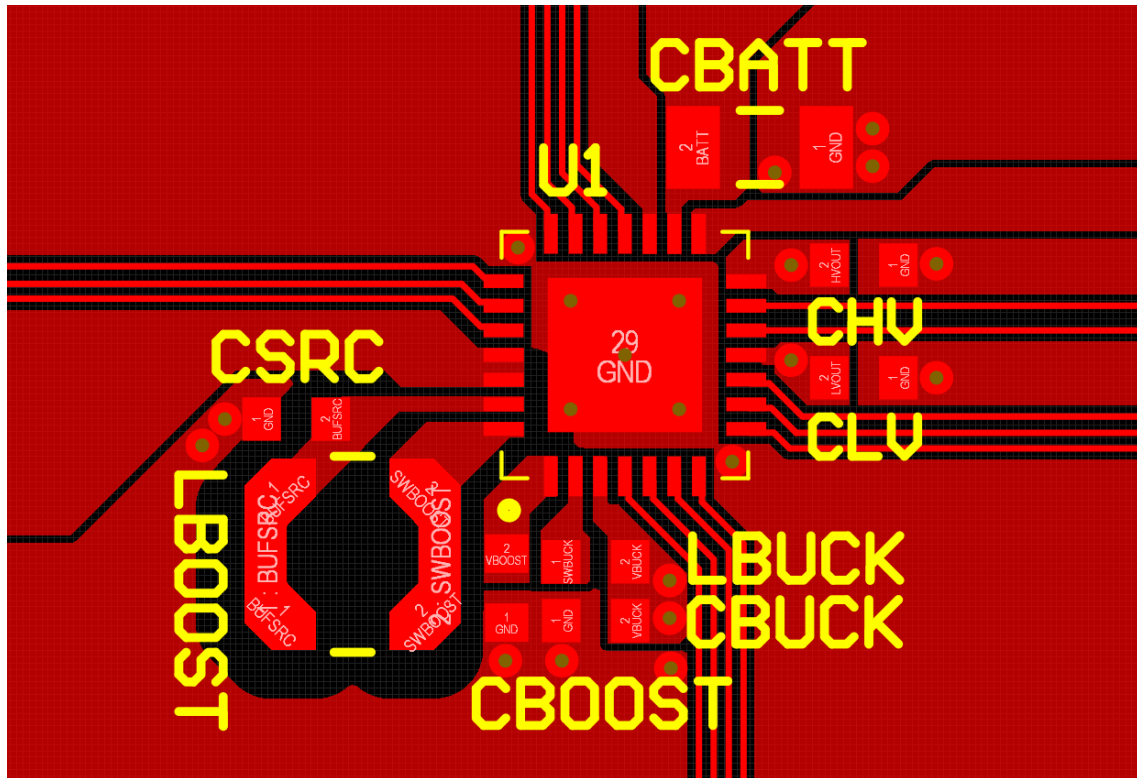


Figure 25: Layout example for the AEM10941 and its passive components

15. Package Information

15.1. Plastic Quad Flatpack No-lead (QFN 28-pin 5x5mm)

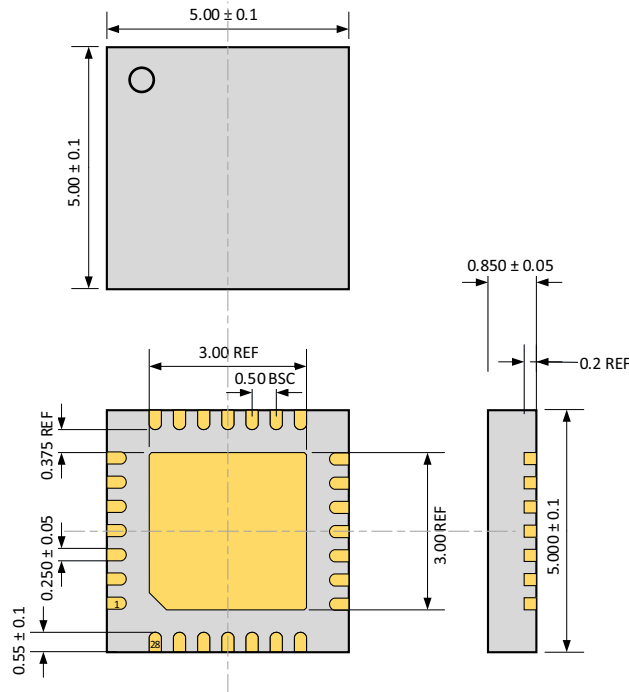


Figure 26: QFN 28-pin 5x5mm drawing (all dimension in mm)

15.2. Board Layout (QFN 28-pin 5x5mm)

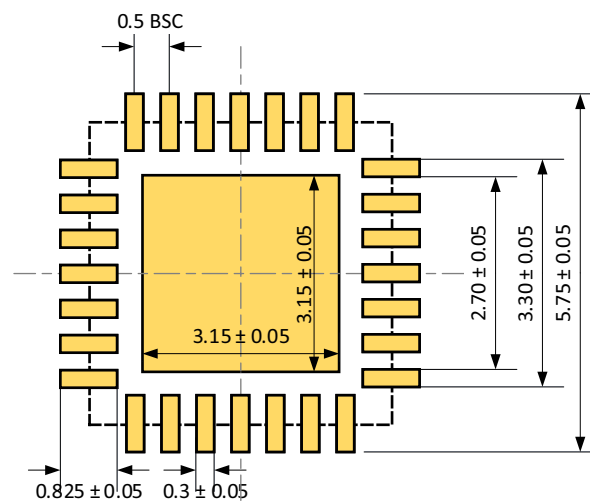


Figure 27: Recommended board layout for QFN 28-pin 5x5mm (all dimension in mm)

16. Glossary

AEM

Ambient Energy Manager.

BOM

Bill Of Materials.

C_{BATT}

Capacitor connected on the **BATT** pin (if no storage element connected).

C_{BOOST}

Output capacitor of the BOOST converter.

C_{BUCK}

Output capacitor of the BUCK converter.

C_{HV}

High-voltage LDO regulator decoupling capacitor.

C_{LV}

Low-voltage LDO regulator decoupling capacitor.

C_{SRC}

BUFSRC pin decoupling capacitor.

GPIO

General Purpose Input / Output.

I_{BUCK}

Total load current supplied by the **BUCK** converter (including the **LVOUT** current I_{LV}).

I_{HV}

Load current supplied by the high-voltage LDO regulator.

I_{LV}

Load current supplied by the low-voltage LDO regulator.

I_{PRIM}

Current from the primary battery.

I_Q

Quiescent current on **BATT** when no energy is available on **SRC**.

I_{SRC}

Harvested current from the energy source.

L_{BOOST}

BOOST converter inductor.

L_{BUCK}

BUCK converter inductor.

LDO

Low Drop-Out.

MPPT

Maximum Power Point Tracking.

PCB

Printed Circuit Board.

P_{SRC_CS}

Minimum power available on **SRC** for the AEM10941 to coldstart.

R_p

Sum of resistors for setting the primary battery minimum voltage. $R_p = R_7 + R_8$.

R_T

Sum of resistors for setting the battery protection threshold voltages in custom mode.
 $R_T = R_1 + R_2 + R_3 + R_4$.

R_V

Sum of resistors for setting the output voltage of the high-voltage LDO in custom mode. $R_V = R_5 + R_6$.

T_{CRIT}

Time before shutdown once **STATUS[1]** has been asserted.

$T_{MPPT,VOC}$

Open-circuit duration for the MPP evaluations.

$T_{MPPT,PERIOD}$

Time between two MPP evaluations.

V_{BATT}

Voltage on the **BATT** pin.

V_{BOOST}

Output voltage of the BOOST converter.

V_{BUCK}

Output voltage of the BUCK converter.

V_{CHRDY}

Charge ready voltage on the **BATT** pin.

$V_{FB_PRIM_U}$

Feedback for the minimal voltage level on the primary battery.

V_{HV}

Output voltage of the high-voltage LDO regulator.

V_{LV}

Output voltage of the low-voltage LDO regulator.



V_{MPP}

Target regulation voltage on **SRC** when extracting power.

V_{OC}

Open-circuit voltage of the harvester connected to the **SRC** pin.

V_{OVCH}

Over-charge voltage on the **BATT** pin.

V_{OVDIS}

Over-discharge voltage on the **BATT** pin.

V_{PRIM}

Voltage on the primary battery.

V_{PRIM,MIN}

Voltage at which the primary battery is considered fully depleted.

V_{SRC}

Voltage on the **SRC** pin.

17. Revision History

Revision	Date	Description
1.0	July, 2018	Creation of the document.
1.3	June, 2019	- LDOs efficiency measurements updated. - ESD specifications added. - HVOUT maximum value modified from 4.2 V to 4.1 V on Figure 1.
1.4	November, 2020	- IPRIM typical value and ISRC maximum value added in Table 5. - SET_OVDIS switched with SET_OVCH on Figure 10. - VchrDY and Vovch positions changed on Figure 12. - BATT pin values changed (from 3.6 V and 4.12 V to 3.5 V and 4.5 V) on Figure 10. - ENHV and ENLV inverted on Figure 10. - STONBATT removed from Table 6. - ESD qualification added. - Changed the spelling from “cold-start” or “coldstart” to “cold start” throughout the document.
1.5	June, 2022	- CBUCK value changed from 10 μF to 22 μF throughout the document.
1.6	May, 2023	- External component names color changed to orange instead of blue. - First page: - Maximum MPPT voltage operation range corrected to 4.5 V. - SET_OVCH and SET_OVDIS swapped on AEM diagram. - Link to e-peas website added for evaluation boards information. - Table of contents, list of Figures and list of Tables widths changed to page width. - Aesthetic changes on Figures 1, 3, 4, 5, 9, 10 and 24 and Table 5. - SET_OVCH, SET_CHRDY and SET_OVDIS pins changed from “left floating” to “connected to BUCK” when not used in Table 1 and in Section 9.1. - “See page ...” column removed from Table 1. - Voltage of BATT and PRIM added in Absolute Maximum Ratings table. - Table 5: - Footnotes added. - VMPP minimum and maximum values added. - ISRC value added for LBOOST value of 22 μH. - SELMPP[1:0] row placed under CFG[2:0] row. - Different minimum values for VBATT depending on used storage element removed. - VHV maximum value changed from “VBATT - 0.3 V” to “VOVDIS - 0.3 V”. - Table 6: - CSRC maximum value changed from 150 μF to 22 μF. - CBOOST and CBUCK maximum values removed. - CBUCK minimum and typical values modified from 15 μF and 22 μF to 8 μF and 10 μF. - ENHV minimum and maximum values removed. - ENLV minimum value replaced by VBUCK. - Condition to go from SHUTDOWN mode to NORMAL mode corrected to “If VBATT > VOVDIS” in Figure 5 and Section 8.2.5. - Maximum Power Point Tracking section rephrased. - Custom mode section reworked. - Second CBATT value added of 22 μF when storage element not connected and LDOs not used (Section 9.6). - Second LBOOST recommended value of 22 μH added in Section 9.7 and Table 10. - SET_OVCH, SET_CHRDY and SET_OVDIS pins connected to VBUCK on Figure 9. - New section created to place the circuit behavior figures. - Changed the way of displaying the settings used for the circuit behavior figures. - Layout example replaced by a more recent version.
2.0	June, 2023	Removed FB_COLD.

Table 11: Revision history (Part 1)

Revision	Date	Description
2.1	December, 2023	- Added "Pin Configuration and Functions" section containing the pinout diagram and description. - Added all the missing pins in the Absolute Maximum Ratings table. - Added IBUCK, IQ, TMPPT.VOC and TMPPT.PERIOD in electrical characteristics table. - Divided electrical characteristics table into 2 parts. - Removed LBOOST maximum value and specified CBATT minimum value if LDOs enabled or disabled in the Recommended Operating Conditions table. - Modified LDOs configuration table design. - Added MPP evaluation behavior figure in the Maximum Power Point Tracking section. - Added how to use BUCK to supply an application, and BUCK converter performances. - Modified VOVDIS, R2, R3 and R4 values in Example Circuit 2. - Replaced LBOOST LPS4012-103MR by LPS4018-103MR in BOM example table. - Updated example figures and layout example figure. - Added layout guidelines section and glossary section. - Replace 0 by L for logic low and 1 by H for logic high in tables and texts.

Table 11: Revision history (Part 2)