AT89RFD-10 / EVLB002
Non-Dimmable Fluorescent Ballast

User Guide

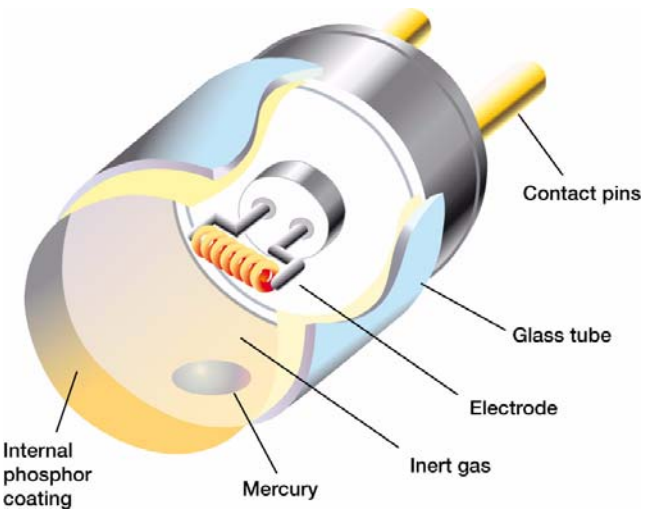
Section 1

Introduction

Efficient fluorescent lamps and magnetic ballasts have been the standard lighting fixture in commercial and industrial lighting for many years. Several lamp types, rapid start, high output, and others are available for cost effective and special applications. This user guide covers operation and development details of the non-dimmable version of our fluorescent ballast for operating a variety of lamps that are available today. This guide also covers power electronic circuits that find wide utilization in other applications beyond lighting alone, which include Power Factor Correction, Half-Bridge Inverter Drives, and Charge Pump Regulators all employing a variety of IXYS / Atmel parts.

Typical rapid start fluorescent lamps have two pins at each end with a filament across the pins. The lamp has argon gas under low pressure and a small amount of mercury in the phosphor coated glass tube. As an AC voltage is applied at each end and the filaments are heated, electrons are driven off the filaments that collide with mercury atoms in the gas mixture. A mercury electron reaches a higher energy level then falls back to a normal state releasing a photon of ultraviolet (UV) wavelength. This photon collides with both argon assisting ionization and the phosphor coated glass tube. High voltage and UV photons ionize the argon, increasing gas conduction and releasing more UV photons. UV photons collide with the phosphor atoms increasing their electron energy state and releasing heat. Phosphor electron state decreases and releases a visible light photon. Different phosphor and gas materials can modify some of the lamp characteristics.

Figure 1-1. Fluorescent Tube Composition



Since the argon conductivity increases and resistance across the lamp ends decreases as the gas becomes excited, an inductance (ballast) must be used to limit and control the gas current. In the past, an inductor could be designed to limit the current for a narrow range of mains voltage and frequency. A better method to control gas current is to vary an inductor's volt-seconds to achieve the desired lamp current and intensity. A variable frequency inverter operating from a DC bus can do this. If the inductor is part of an R-L-C circuit, rapid start ignition and operating currents are easily controlled depending on the driving frequency versus resonant frequency.

Utility is enhanced by designing a power factor correcting boost converter (PFC) to achieve the inverter DC bus over a wide mains voltage range of 90 - 265VAC, 50/60 Hz. Since a PFC circuit keeps the mains current and voltage in phase with very low distortion, mains power integrity is maintained. Additional utility is achieved by designing a microcontroller for the electronic ballast application that can precisely and efficiently control power levels in the fluorescent lamp. An application specific microcontroller offers the designer unlimited opportunity to enhance marketability of lighting products. The final design topology is shown in the block diagram of Figure 1-3.

1.1 General Description

Fluorescent ballast topology usually includes line conditioning for CE compliance, a power factor correction block including a boost converter to 380 V for universal input applications and a half bridge inverter. Varying the frequency of the inverter permits time for filament preheat and ignition for rapid starting, including precise power control. As shown in the block diagram, figure 3, all of these functions can be timed, regulated, and diagnosed with the Atmel AT89EB5114 microcontroller.

1.2 Ballast Demonstrator Features

- Automatic microcontroller non-dimmable ballast
- Universal input _ 90 to 265 VAC 50/60 Hz, 90 to 370 VDC
- Power Factor Corrected (PFC) boost regulator
- Power feedback for stable operation over line voltage range
- Variable frequency half bridge inverter
- 18W, up to 2 type T8 lamps
- Automatic single lamp operation

Figure 1-2. Ballast demonstrator assembled board

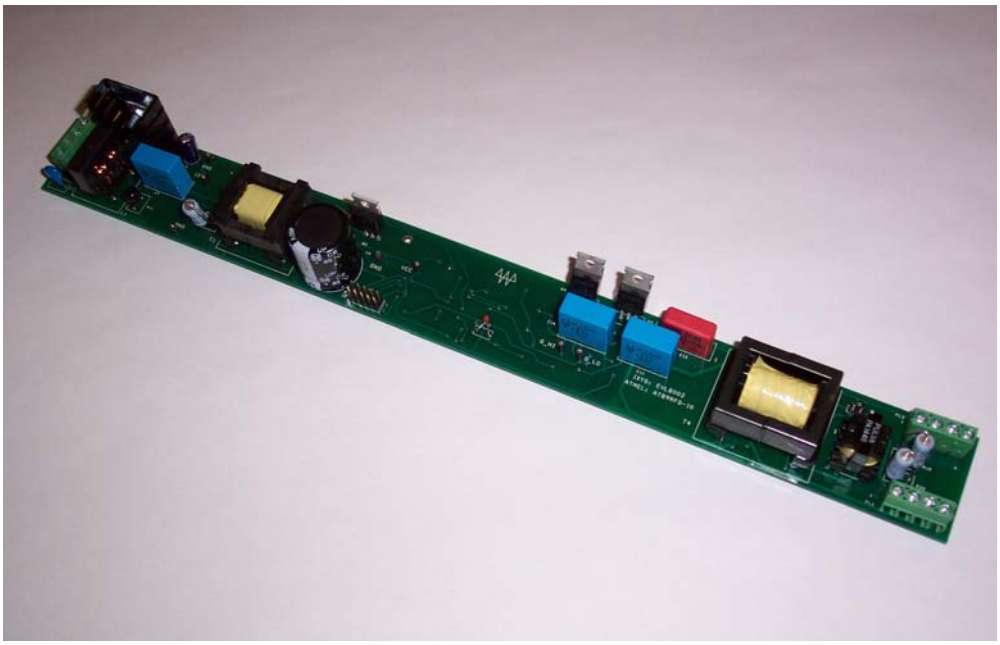
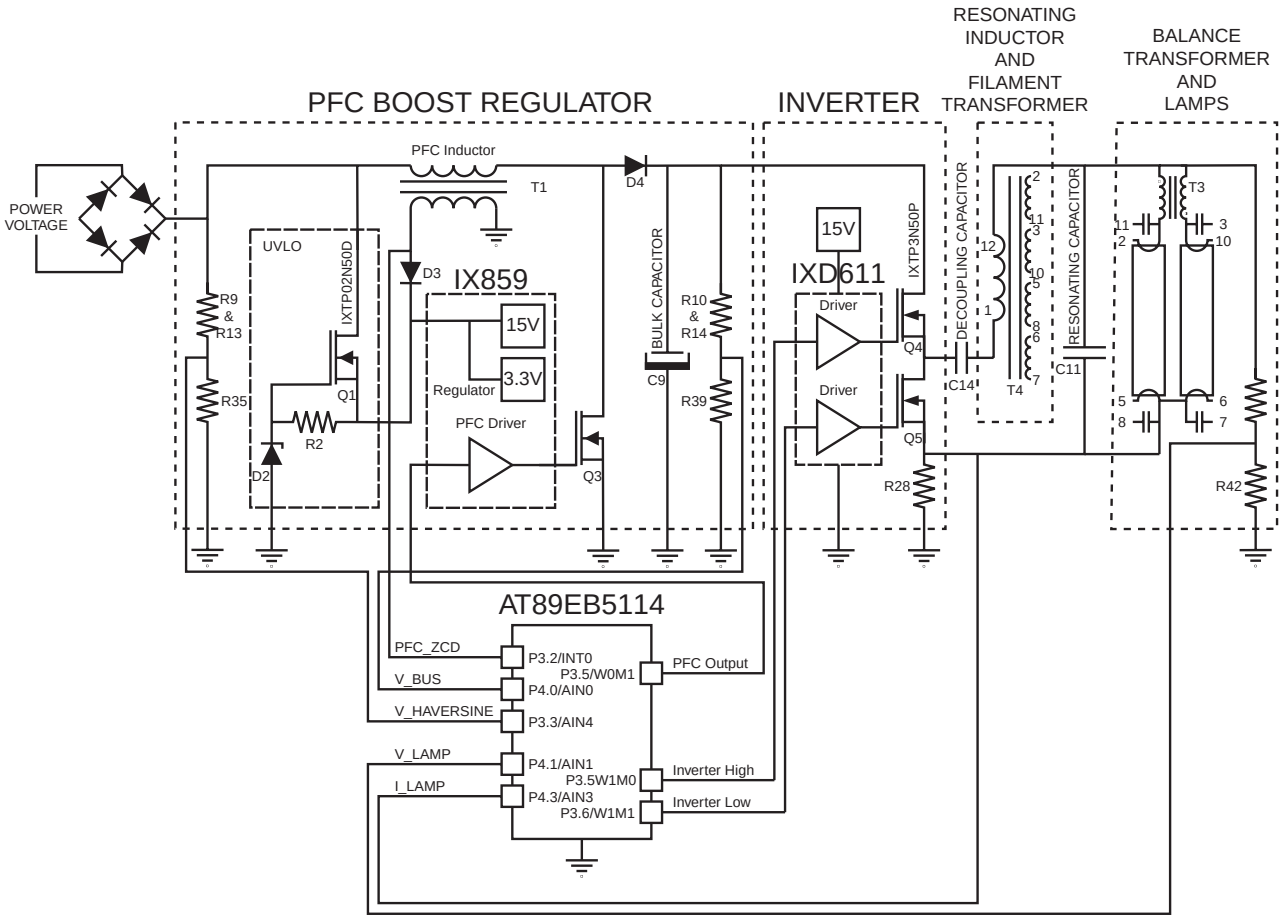


Figure 1-3. Non-Dimmable Ballast block diagram



Section 2

Ballast Demonstrator Device Features

2.1 Atmel Supported Products

AT89EB5114 Microcontroller

- High speed configurable PWM outputs for PFC and ½ bridge inverter
- 6 Analog inputs for A/D conversion, 2.4V internal reference level
- 3 High speed PWM outputs used for the PFC and ½ bridge driver
- A/D with programmable gain used for efficient current sensing
- SOIC 20 pin package

2.2 IXYS Supported Products

IXI859 Charge pump with voltage regulator and MOSFET driver

- 3.3V regulator with undervoltage lockout
- Converts PFC energy to regulated 15VDC
- Low propagation delay driver with 15V out and 3V input for PFC FET gate

IXTP3N50P MOSFET

- 500V, low R_{DS} (ON) power MOSFET, 3 used in design

IXD611S MOSFET driver

- Up to 600mA drive current
- ½ bridge, high and low side driver in a single surface mount IC
- Undervoltage lockout

Section 3

Ballast Description

3.1 Circuit Topology

- Line conditioning with input filter and varistor for noise suppression and protection.
- Low Voltage supply
- PFC / boost regulator
- PFC magnetics
- Lamp drive
- Microprocessor control
- Charge pump regulator
- ½ bridge driver
- ½ bridge power MOSFET stage for up to 2 lamps

3.1.1 Line Conditioning

An input filter section consisting of C1, C3, and common mode choke L1 prevent switching signal frequencies and their harmonics from the PFC boost converter from being conducted to the mains. Varistor RV1 protects the ballast circuit from line voltage transients. Full wave bridge rectifier BR1 converts the line AC to a DC haversine. Diode D2 is used to provide a point ahead of the boost inductor and filter where the haversine signal can be sensed by the microcontroller. This is necessary for the proper timing of the PFC control drive signal which must maintain a constant ON time pulse width over a haversine period.

3.1.2 Low Voltage Supply

3.3V microcontroller power and ~ 15V FET drive power are provided by the low voltage supply consisting of a current source (Q1) and multipurpose IC U1 (IXI589). Internal to U1 are a 3.3V linear regulator, a 15V (nominal) two point regulator, under-voltage lockout comparators and control, charge pump switching circuitry, and a FET driver. (See more detailed description of the IXI859 below) For startup, the current source formed by Q1, and its associated components sources current into C6 until the voltage at U1 pin 1 reaches the under-voltage lockout upper limit of approximately 14.1V. The current source voltage output is limited by zener diode D3 to about 16 V. When the under-voltage lockout limit is reached, the IXI859 begins to supply 3.3V to the microcontroller. The microcontroller then begins to supply drive pulses to the PFC FET Q3 through the IXI859 FET gate driver. The charge pump regulator circuit is then able to supply 15V power by efficiently converting energy from the PFC switching circuit. This feature is not used in the non-dimmable demonstrator design. Rather, a voltage doubler circuit consisting of D4, D20 and C31 connected to the PFC transformer secondary provides 15V power after startup.

3.1.3 PFC Boost Regulator

The PFC (Power Factor Correcting) boost regulator circuit is used to convert the rectified input line voltage to a 380V DC supply while maintaining a sinusoidal average input current in phase with the input voltage. The microcontroller accomplishes this by switching the PFC FET with ON times that are constant over a haversine period and by maintaining nearly critical conduction conditions. Since the current in the PFC inductor is nearly triangular and its peaks are proportional to the input haversine voltage, the average current is proportional to the input waveform. Therefore, the power factor is maintained near unity.

3.1.4 PFC Magnetics

Without going into the derivations of the formulas used, the transformer design is as follows:

L = [(1.4 * 90VAC) * (20 uS)] / 3.6A peak = 700 uH

A 3.6 Apk maximum FET current is 1.8 A approximately divided by the ON/OFF ratio. The ON time has been discussed earlier and the OFF time maximum will occur at high line condition at the peak of the haversine. A 16 mm core was chosen for the recommended power density at 200 mT and 50 KHz.

3.1.5 Lamp Drive

The microcontroller sends rectangular pulses to the half-bridge driver (IXD611). The IXD611 contains high side and low side FET drivers and floating high side supply circuitry to produce high side gate drive. (See more detailed description of the IXD611 to follow) The pulses from the microcontroller are non-overlapping and 180 degrees out of phase. A deadband time between HBRIDGE HI and HBRIDGE LO pulses insures that both drivers are never on at the same time. The lamp drive is constant in duty cycle. The power to the lamps is controlled by varying the frequency of the drive signals. The IXD611 drives two FETs (IXTP3N50P) in a half-bridge configuration.

The output of the half-bridge is AC coupled by C11 to the lamps through a resonating transformer and capacitor (T4 and C12). Additional windings on T4 supply filament current to the lamps. Balance transformer T3 forces the current to be shared equally by the two lamps. The lamp currents are conducted to circuit common through a 1 Ohm resistor which is used to sense the lamp current so that lamp power may be controlled by the microcontroller.

3.1.6 Control

The ballast is controlled by microcontroller U3. U3 is an Atmel AT8xEB5114 with an 80C51 core and specialized circuitry for controlling the ballast. Included are two PWM units that are used for controlling the PFC drive and the half-bridge drive with deadtime. An internal analog to digital converter converts input signals so the processor can monitor and control the ballast.

The AT8xEB5114 pin connections for ballast control and scale factors for analog inputs are as follows:

- P4.0/AIN0 VBus monitor input (VBus = AIN0 x 201)
- P4.1/AIN1 Rectified Lamp Voltage Sense (Vlamp = AIN1 x 294)
- P4.2/AIN2 Lamp AC Voltage (VAC ~= AIN2 x 446)
- P4.3/AIN3 Lamp Current (Amplify by 10) (Ilamp = AIN3/1Ohm)
- P3.3/AIN4 Haversine Voltage input (Vhaversine = AIN4 x 201)
- P3.4/AIN5 Temperature sensor (Vtemp = 1.1V @ 25C || .264V @ 85C)
- P3.6 NC (No Connection)
- P3.5/W1M0 PFC Drive
- P3.2/INT0 Current Zero Crossing Detect (Interrupt)
- P3.1/W0M1 Half Bridge high side drive

- P3.0/W0M0 Half Bridge low side drive

The Temperature monitor is a thermistor with a nominal 10K resistance at 25°C and 1.74K resistance at 80°C. It is mounted on the circuit board and so monitors ambient temperature in the lamp housing.

Additional dedicated pins allow in-circuit programming of the flash memory using header J2. Other pins provide connections for the oscillator and voltage reference components.

3.1.7 IXYS IXI859 Charge Pump Regulator

The IXI859 charge pump regulator integrates three primary functions central to the PFC stage of the ballast demonstrator. First it includes a linear regulated supply voltage output, and in this application the linear regulator provides 3.3V to run the microcontroller. The second function is a gate drive buffer that switches an external power MOSFET used to boost the PFC voltage to 380V. Once the microcontroller is booted up and running, it generates the input signal to drive the PFC MOSFET through the IXI859 gate drive buffer. Finally, the third function provides two point regulated supply voltage for operating external devices. As a safety feature, the IXI859 includes an internal Vcc clamp to prevent damage to itself due to over-voltage conditions.

In general applications at start-up, an R-C combination is employed at the Vcc supply pin that ramps up a trickle voltage to the Vcc pin from a high voltage offline source. The value of R is large to protect the internal zener diode clamp and as a result, can't supply enough current to power the microcontroller on it's own. C provides energy to boot the microcontroller. At a certain voltage level during the ramp up, the Under Voltage Lock Out point is reached and the IXI859 enables itself. The internal voltage regulator that supplies the microcontroller is also activated during this time. However, given the trickle charge nature of the Vcc input voltage, the microcontroller must boot itself up and enable PFC operation to provide charge pump power to itself. This means that the R-C combination must be sized carefully so that the voltage present at the Vcc pin does not collapse too quickly under load and causes the UVLO circuitry to disable device operation before the microcontroller can take over the charge pump operation. There are a couple of problems associated with this method. Namely, under normal operation as previously mentioned, the internal zener diode clamps the input Vcc pin voltage and R must dissipate power as long as the zener diode is clamped. Assuming that a rectified sine wave is supplied at the Vcc means that the internal zener will be clamped and R will be dissipating power as long as the input voltage is greater than the zener voltage. Another problem is that when a universal range is used at the Vcc pin, 90-265V, R must dissipate nine times the power, current squared function for power in R, over a three-fold increase of voltage from 90V at the low end to 265V on the high end.

As an alternative and as used in the ballast demonstrator, the Vcc pin is fed voltage by way of a constant current source. This circuit brings several advantages over the regular R-C usage. First we can reduce power consumed previously by R and replace it with a circuit that can provide power at startup and once the microcontroller is running, shut off current into the Vcc pin. The constant current source also has the ability to provide sufficient power to run the microcontroller unlike the R-C combination. This would be an advantage in the case that a standby mode is desired. Overall power consumption can be reduced by allowing the microcontroller to enter a low power mode and shut down PFC operation without having to reboot the microcontroller. Since the R-C combination cannot provide enough power to sustain microcontroller operation, the microcontroller must stay active running the PFC section to power itself.

3.1.8 IXYS IXTP02N50D Depletion Mode MOSFET used as a current source

The IXYS IXTP02N50D depletion mode MOSFET is used in this circuit to provide power and a start-up voltage to the Vcc pin of the IXI859 charge pump regulator. The IXTP02N50D acts as a current source and self regulates as the source voltage rises above the 15V zener voltage and causes the gate to become more negative than the

source due to the voltage drop across the source resistor. Enough energy is available from the current source circuit during the conduction angles to keep the IXI859 (U1) pin 1 greater than 14VDC as required to enable the Under Voltage Lock Out (UVLO) circuitry in the IXI859.

3.1.9 IXYS IXD611 Half bridge MOSFET driver

The IXD611 half bridge driver includes two independent high speed drivers capable of 600mA drive current at a supply voltage of 15V. The isolated high side driver can withstand up to 650V on its output while maintaining its supply voltage through a bootstrap diode configuration. In this ballast application, the IXD611 is used in a half-bridge inverter circuit driving two IXYS IXTP3N50P power MOSFETs. The inverter load consists of a series resonant inductor and capacitor to power the lamps. Filament power is also provided by the load circuit and is wound on the same core as the resonant inductor. Pulse width modulation (PWM) is not used in this application, instead the power is controlled through frequency variation. It is important to note that pulse overlap, which could lead to the destruction of the two MOSFETs due to current shoot through, is prevented via the input drive signals through the microcontroller. This parameter, also known as dead time, is not available on this particular driver. However, a dead time option is built in on other driver models within the IXYS bridge driver family.

Other features of the IXD611 driver include:

- Wide supply voltage operation 10-35V
- Matched propagation delay for both drivers
- Undervoltage lockout protection
- Latch up protected over entire operating range

- +/- 50V/ns dV/dt immunity

3.1.10 IXYS IXTP3N50P PolarHV N-Channel Power MOSFET

The IXTP3N50P is a 3A 500V general purpose power MOSFET that comes from the family of IXYS PolarHV MOSFETs. When comparing equivalent die sizes, PolarHT results in 50% lower R DS(ON), 40% lower R THJC (thermal resistance, junction to case), and 30% lower Qg (gate charge) enabling a 30% - 40% die shrink, with the same or better performance verses the 1st generation power MOSFETs.

Within the ballast demonstrator itself the IXTP3N50 serves two functions. The first of which is the power switching pair of devices in the half-bridge circuit that drives the lamps. While a third device serves duty in the main PFC circuit as the power switch that drives the PFC inductor.

Section 4

Circuit Operation

General requirements

- One or two lamps, type T8 of any characteristics
  - Ballast to compensate automatically
  - Hardware is capable of up to 40W per lamp
- Line voltage of 90 to 265 VAC, 50 or 60 Hz
  - 380 volt DC bus as provided by a power factor correcting boost regulator (PFC)

4.1 PFC

Upon application of mains power, without the PFC running, the filter cap C9 will charge to the peak line voltage. The current source will supply the low voltages. After the DC bus voltage is 0.9 times the haversine peak and the under voltage lockout (UVLO) requirements are met, a series of fixed width soft-start pulses are sent to the PFC FET of 10 uS at a 20 KHz rate. At very low 380V load current the 380DVC bus should rise to 380V. If the bus rises to 410 VDC, all PFC pulses stop. The zero crossing detector (P3.2/INT0) starts to sense zero crossings from the PFC transformer secondary. A 380V DC bus and a zero crossing event starts the PFC control loop.

Checks are made for the presence of the rectified mains (haversine) and bus voltage throughout normal operation. Mains sense (P3.3/AIN4) < 0.76 V pk (90 VAC) or > 2.24 V pk (265 VAC) faults the PFC to off, turns off the ½ bridge and initiates a restart.

The control consists of measuring the 380V bus error from the 380V setpoint of 1.89 V at P4.0/AIN0 to determine the PFC drive pulse width (PW). The PW is made proportional to the error, and has to be constant during a complete half period, so the update is done each time the haversine is null. A maximum PW limit should be coded to limit the FET current under upset of high error and high haversine (265VAC*1.4). The maximum pulse width allowed is inversely proportional to the peak haversine voltage and varies between 6 uS at high line and 20 uS at low line.

$$\mathbf{PW_{max} = K/V_{haversine}}$$

Current sensing of the PFC FET source is not needed as the peak current allowed can be set by the haversine peak detect.

$$t_{max} = L\ Ipk / V_{haversine}$$

With L at 700 uH and Ipk at 3.2 A, tmax = 6 uS at high line (265 Vrms). This also effectively limits the FET dissipation under upset conditions. Under normal operation, a pulse

width maximum of 20 uS is allowed for maximum 380 VDC error but with the high line limitation. 1% regulation of the 380 VDC bus was achieved with this control scheme.

After the PFC FET ON pulse, the PFC inductor flyback boosts the voltage through D6 to the bulk filter capacitor. The boost current decays as measured by the inductor secondary. After the current goes to zero, the next pulse is started. This ensures operation in near critical conduction boost mode. The current zero crossing detect of P3.2/INT0 sets the PFC off time. This off time is effectively proportional to the haversine amplitude with the lowest PFC frequency occurring at the haversine crest and the highest frequency at the haversine zero. Because of the haversine voltage, and di=v*dt/L the mains current envelope should follow the voltage for near unity power factor. This assumes a nearly constant error (di) of the 380 VDC bus over each haversine period.

The PFC on time is modified proportionally to the error between 380V and the actual value of the 380VDC BUS. In case the Vbus reaches the overshoot value (410V) the pulse is reduce to 0.

4.1.1 PFC Sequence

1. Power on.
2. IXI859 function block supplies 3.3V to microcontroller
3. Microcontroller undervoltage lockout released
4. Disable half-bridge drive output
5. Disable P3.2/INT0 comparator.
6. P3.3/AIN4 must be >0.76 Vmin (90VAC) & <2.24 (265VAC) Vmax (haversine peak) for the PFC to start.
7. Check AC line condition every 200 mS maximum (10 cycles of 50 Hz).
8. If fail check, halt PFC, and Half-Bridge. Do not restart until line within specs to protect PFC.
9. Soft start PFC with 10 uS pulses at 50 uS period for 800 uS.
10. Monitor for a zero crossing of the PFC inductor secondary voltage. This occurs after the 10 uS start pulse burst.
11. If no Zero Crossing & after 800 uS halt PFC Drive, wait 1 second & provide PFC Drive with 10 uS pulses for 800 uS. Try 10 times
12. After Zero Crossing and 380 VDC (1.89 V at P4.0/AIN0) enable PFC control loop
13. If > 410V (2.04 V at P4.0/AIN0) then inhibit PD0 pulse
14. If < 380V (1.89 V at P4.0/AIN0) then use the control loop to establish the pulse width.
15. Limit pulse width to 25 uS or as determined by the haversine peak voltage.
16. After PFC pulse, wait until Zero Crossing detected (PFC off time) then enable PFC pulse with width calculated from bus error and haversine peak.

4.2 Lamp Circuit

4.2.1 General

T4 primary and C12 form a series resonant circuit driven by the output half bridge. Since the output is 380V pulsed DC, DC isolation is provided by C11 to drive the lamp circuit with AC. The lamp is placed across the resonating capacitor C12. The lamp filaments are driven by windings on T4 secondaries to about 3 Vrms so that the resonating inductor current provides the starting lamp filament current.

Sequentially, the lamp is started at a frequency well above resonance at 100 KHz before ramping down to 55 KHz ignition. 80 KHz provides a lagging power factor where most of

the drive voltage appears across the inductor. A smaller voltage appears across the resonating capacitor and the lamps. However with 1 mH gapped inductance, there is sufficient inductor current to power the filaments.

For lamp ignition, the frequency is reduced from 80 KHz to 40 KHz at 30 KHz/sec towards resonance causing the lamp voltage to rise to about 340 Vpeak.

Ignition occurs at about 40 KHz for a 18W T8 lamp. The plasma established in the lamp presents a resistive load across the resonating capacitor thereby reducing the voltage across the capacitor and shifting the reactive power in the bridge circuit to resistive power in the lamp.

A further reduction in frequency to 32 KHz at 30 KHz/sec establishes maximum brightness as the resonant circuit now has a leading (capacitive) power factor causing more voltage and current (approx. 360 Vpeak) across the capacitor and the lamp.

4.2.1.1 Single lamp operation

Single lamp operation can be detected from the 380VDC bus current through the 1 Ohm sense resistor. At preheat the current for one lamp is half that for two lamps. This current is also used to sense open filament condition or lamp removed under power condition. An abrupt change in the bus current is a good indicator of lamp condition that does not require a high frequency response nor a minimal response due to reactive currents.

Once single lamp condition is detected, the minimum run frequency is determined by Ix380V = Single Lamp Power. If the single lamp condition occurs during "run" as noted by a decrease in current of more than 20% from the preset level, increase the frequency until the single lamp power conditions are met. If the current increases by more than 20% , assume the lamp has been replaced. Step Increase the frequency to 80 KHz to restart the ignition process. This is necessary to preheat the new lamp filament to ensure that the hot lamp will not ignite much sooner than the cold lamp exceeding the balance transformer range.

Repeat ignition sequence. With one cold lamp in parallel with one hot lamp, it may be necessary to restart several times to get both lamps to ignite.

The AT8xEB5114 internal amplifier has the gain preset in the program to 10. This scales the lamp current input to a reasonable A/D resolution.

4.2.1.2 Lamp Number Sequence

After Vbus = 380 V start preheat

Start half-bridge drive with 12.5 uS total period (80 KHz)

If I > 20 ma, then 2 lamps. If I < 20 ma assume a single lamp.

I < 10 ma assume an empty fixture = fault & shutdown.

4.2.1.3 Start Ignition Sequence

1. Sweep half-bridge frequency down at 30 KHz/sec
2. Stop sweep at 40 KHz or 25 uS period (12.5 uS pulses for each ½ bridge FET)
3. Check I > 100 ma (2 lamps) or > 30 ma (1 lamp) for proof of ignition
4. Hold ignition frequency for 10 mS
5. Measure the lamp voltage collapse for proof of ignition (P4.1/AIN1 < 200 mV)
6. If the lamp voltage has not collapsed, increase frequency to 77 KHz for preheat for 1 second. Repeat ignition sequence.
7. Proceed to full power setting at 30 KHz/sec rate after ignition is detected.

4.2.1.4 Power Control

Calculate input power for both lamps = I x 380VDC.

Adjust freq. up (lower power) or down (higher power) at 30 KHz/sec rate.

Limit freq. to 32 KHz to 80 KHz range.

If lamp currents exceed power limits by 10% (as determined by lamp type), set half-bridge drive off due to over current. Start re-ignition sequence. Repeat 6 times and if still out of spec, shutdown PFC and half-bridge drive.

PD6 rectified AC drive

Checks are made for the presence of the rectified mains (haversine) and bus voltage throughout normal operation. Mains voltage < 90 VAC or 265 VAC peak faults the PFC to off, turns off the half-bridge and initiates a restart.

Section 5

AT8xEB5114 Non-dimmable Software

This section of the document describes the software architecture utilizing the following source code files and related state machines.

Main_at8xeb5114_fluo_demo.c

– ADC State Machine

Pfc_ctrl.c

– PFC State Machine

Lamp_ctrl.c

– Lamp State Machine

And their associated header files.

- main_at8xeb5114_fluo_demo.h

– Pfc_ctrl.h

– Lamp_ctrl.h

Including the following peripherals:

- TIMER0, ADC, amplifier, PWM0, and PWM1.

In order for the ballast to operate, there are two primary control systems that run simultaneously. The first is for the PFC control and second for the Lamp control.

Furthermore in order to work properly, the state machines require input data. This analog data is provided via an auto running interrupt mode ADC state machine.

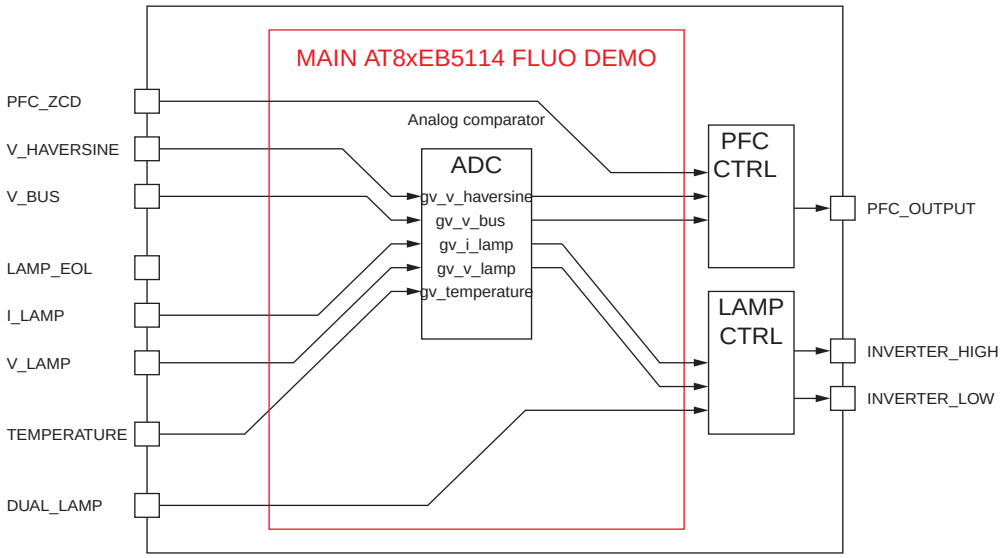
The complete software package for the application is split into the functional blocks in the diagram shown below. While the variables are identified as follows.

- g_ global
- gv_global volatile
- gs_ global static

Voltage and current variables are identified by the following examples

- g_v or g_i global - voltage/current
- gv_v or gv_i global volatile - voltage/current
- gs_v or gs_i global static - voltage/current

Figure 5-1. Main AT8xEB5114 FLUO DEMO



5.1 Main_AT8xEB5114_fluo_demo.c

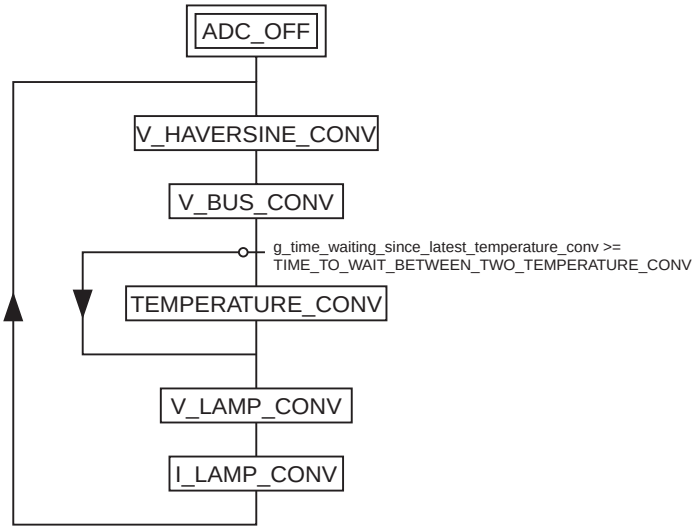
This file executes all the peripherals initializations and then schedules the different control tasks.

The ADC state machine is included in this file. The ADC state machine is controlled via interrupts.

5.1.1 ADC STATE MACHINE

The ADC state machine functional diagram is shown below:

Figure 5-2. ADC state machine diagram



The different states are outlined below:

ADC_OFF

The ADC was previously off, this is the first conversion and is not necessarily valid.

Start the first V_HAVERSINE_CONV conversion.

V_HAVERSINE_CONV

Get back the v_haversine result.

Start the V_BUS_CONV next conversion.

V_BUS_CONV

Get back the v_bus result.

Start the V_HAVERSINE_CONV, the TEMPERATURE_CONV, or the V_LAMP_CONV conversion depending on g_time_waiting_since_latest_temperature_conv.

TEMPERATURE_CONV

Get back the temperature_result.

Start the V_LAMP_CONV conversion.

V_LAMP_CONV

Get back the v_lamp result.

Start the I_LAMP_CONV conversion.

I_LAMP_CONV

Get back the i_lamp result.

Start the next conversion cycle with a V_HAVERSINE_CONV conversion.

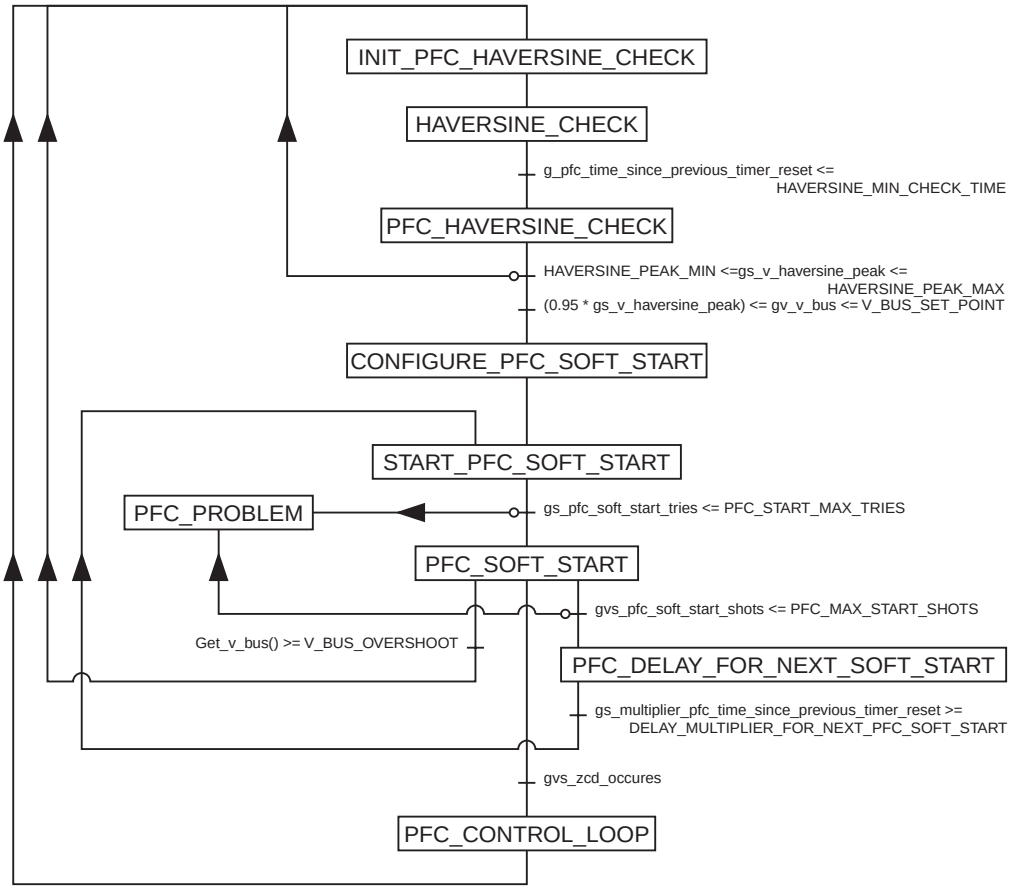
5.2 Pfc_ctrl.c

This file executes the PFC state machine according to the scheduler in the Main_AT8xEB5114_fluo_demo.c file.

5.2.1 PFC STATE MACHINE

The PFC state machine functional diagram is shown below:

Figure 5-3. PFC State Machine Diagram



The different states are outlined below:

INIT_PFC_HAVERSINE_CHECK

Initialize the control values of the PFC. This is the initial state set by the main_AT8xEB5114_fluo_demo.c file.

Then jump to the HAVERSINE_CHECK state.

HAVERSINE_CHECK

Measure the haversine peak voltage during HAVERSINE_MIN_CHECK_TIME.

Then jump to the PFC_HAVERSINE_CHECK state.

PFC_HAVERSINE_CHECK

PFC haversine peak must be included between HAVERSINE_PEAK_MIN and HAVERSINE_PEAK_MAX (90VAC and 265VAC).

If the haversine value is OK, set the maximum pulse width allowed and jump to the CONFIGURE_PFC_SOFT_START state.

Else go back to INIT_PFC_HAVERSINE_CHECK state.

CONFIGURE_PFC_SOFT_START

Configures the peripherals PWM1 and interrupt 0 to soft start the PFC.

Then jump to START_PFC_SOFT_START.

START_PFC_SOFT_START

Check that the soft start has been tried less than PFC_START_MAX_TRIES

If OK then start PWM1 and jump to PFC_SOFT_START state.

Else immediately jump to PFC_PROBLEM state.

PFC_SOFT_START

The PFC soft start consists on PFC_MAX_START_SHOTS pulses configured on PFC_SOFT_START_CONFIGURATION.

If a zero crossing detection appears, jump to the PFC_CONTROL_LOOP state

Else go to INIT_PFC_HAVERSINE_CHECK, PFC_DELAY_FOR_NEXT_PFC_SOFT_START, or PFC_PROBLEM state depending on the different conditions detailed in the PFC diagram.

PFC_DELAY_FOR_NEXT_PFC_SOFT_START

In case the soft start fails, the software has to wait DELAY_FOR_NEXT_PFC_SOFT_START*DELAY_MULTIPLIER_FOR_NEXT_PFC_SOFT_START, before trying a new soft start by going back to the START_PFC_SOFT_START state.

PFC_CONTROL_LOOP

A zero crossing detection occurs so the PFC is now started and the PFC can be configured on autoretrigg mode.

The PFC is now running. This is the normal PFC loop control.

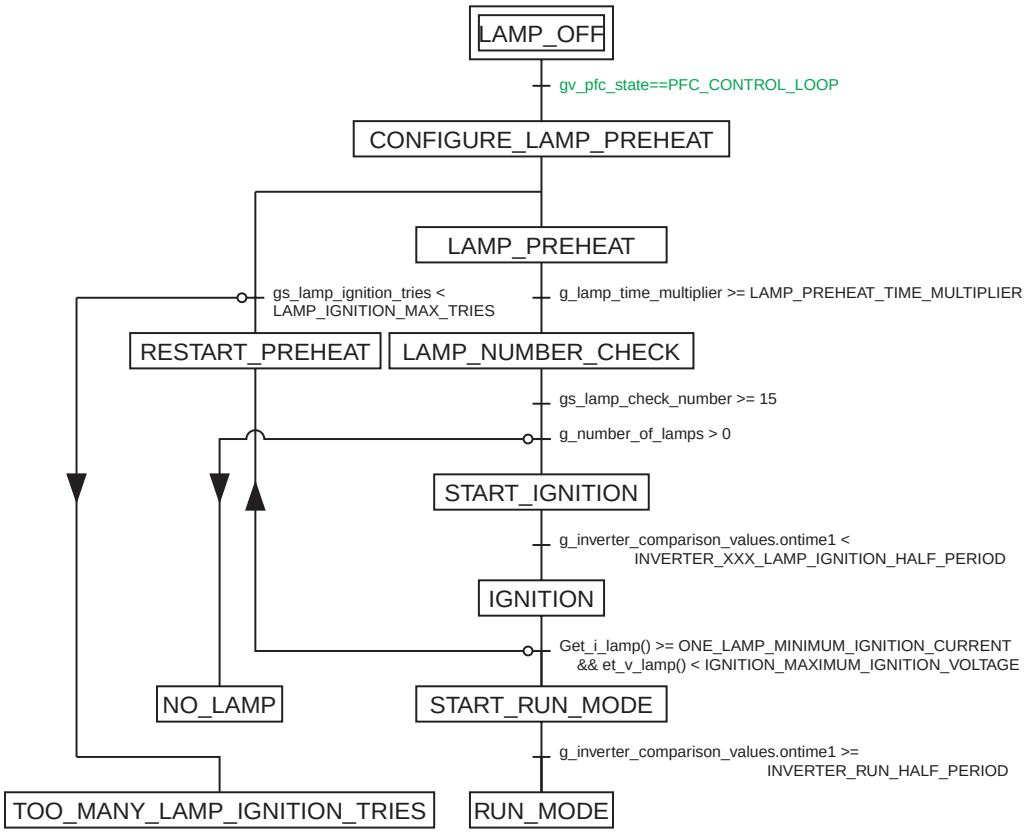
5.3 Lamp_ctrl.c

This file executes Lamp state machine according to the scheduler in the Main_AT8xEB5114_fluo_demo.c file.

5.3.1 Lamp State Machine

The Lamp state machine functional diagram is shown below:

Figure 5-4. LAMP state machine



The different states are outlined below:

LAMP_OFF

Nothing happens, the exiting of this state takes place as soon as the gv_pfc_state is set to PFC_CONTROL_LOOP.

CONFIGURE_LAMP_PREHEAT

This is the first time the lamp has tried to be started since the user has requested the switch on.

Configure the Amplifier0 which is used to measure the current then configure the PSC2 according to the definitions in the config.h file, and initialize all the lamp control variables.

Then jump to the LAMP_PREHEAT state.

LAMP_PREHEAT

Let the preheat sequence for LAMP_PREHEAT_TIME.

Then jump to the LAMP_NUMBER_CHECK state.

LAMP_NUMBER_CHECK

Check the preheat current in order to know whether there is one or two lamps

Then jump to the START_IGNITION state.

In case there is no lamp, jump to the NO_LAMP state.

START_IGNITION

Decrease the frequency from the init frequency down to INVERTER_IGNITION_HALF_PERIOD.

Then jump to IGNITION state.

IGNITION

The ignition sequence consists in maintaining the ignition frequency determined by INVERTER_IGNITION_HALF_PERIOD for 10ms, then checking for ignition by measuring lamp current and voltage.

In case it is... START_RUN_MODE.

In case it isn't... RESTART_PREHEAT.

RESTART_PREHEAT

Reconfigure the Inverter with the Restart parameters, then LAMP_PREHEAT.

If Ignition fails too many times... Go to TOO_MANY_LAMP_IGNITION_TRIES.

START_RUN_MODE

Increase the frequency from the init frequency, INVERTER_IGNITION_HALF_PERIOD.

Then jump to RUN_MODE state.

RUN_MODE

Normal control loop to have the light in accordance with the gv_lamp_preset_current.

TOO_MANY_LAMP_IGNITION_TRIES

If the ignition has failed LAMP_IGNITION_MAX_TRIES, the lamp is switched off.

NO_LAMP

If during the LAMP_NUMBER_CHECK number no lamp is detected, the lamp is switched Off.

Section 6

Conclusion

The ballast demonstrator shows that the Atmel microcontroller and supporting IXYS devices can control and regulate one or more fluorescent lamps with precision and efficiency, therefore providing the lamp controller manufacturer with maximum flexibility with their design. Universal input and power factor control adds to the flexibility of the design with a minimal addition of more expensive active components.

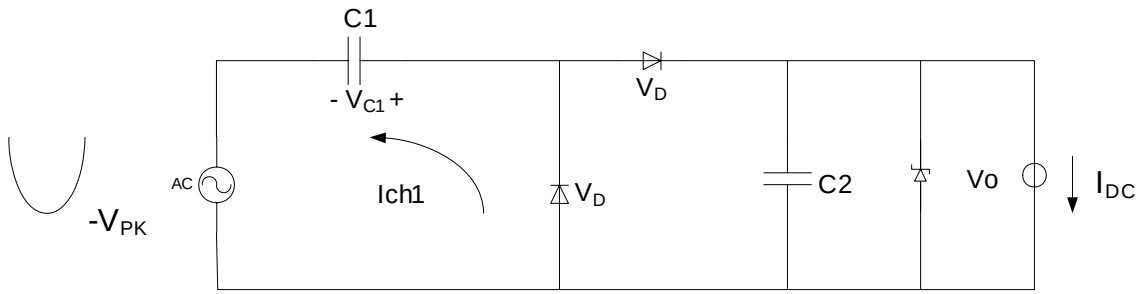
Additionally, the programmability of the microcontroller offers the lamp manufacturer the flexibility to add or modify design features to enhance their market position. The ballast demonstrator, with its many features, does not address all the possibilities available to the lamp controller designer.

6.1 Appendix 1: Capacitor Coupled Low Voltage Supply

Small currents for the low voltage supply can be obtained from the AC line at low loss by means of capacitor coupling as shown in the figures below. To estimate the required size of the coupling capacitor, use the following relationships for current, charge, voltage and capacitance.

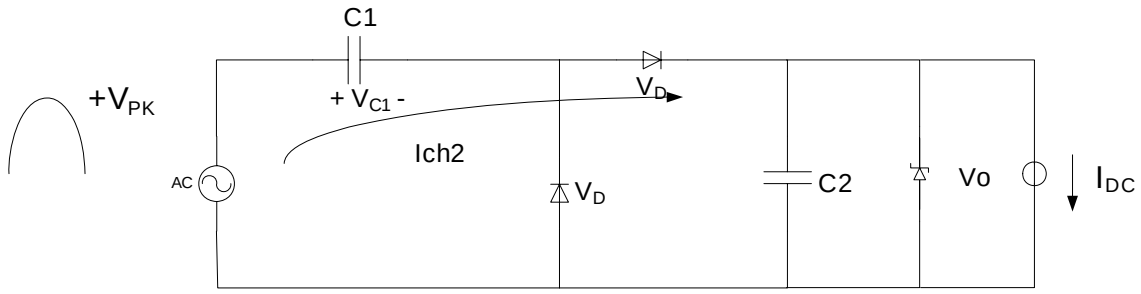
$1.dQ/dt = I_{DC}$

Figure 6-1. Negative Line Half Cycle



"Negative" line half-cycle:
C1 charges to Vpk - V_D with polarity shown.

Figure 6-2. Positive Line Half Cycle



"Positive" line half-cycle:
C1 charges to Vpk - V_D - Vo with polarity shown.

1. $dV = 2Vpk-Vo-2V_D$
2. $dQ = CdV$ or $C = dQ/dV$

For example, to obtain 15 ma at 20 VDC from a 220 Vrms 50 Hz line:

1. dQ/dt = (15 millijoules/sec)/(50 cycles/sec) or 0.3 millijoules / cycle.
2. Over 1 cycle, the coupling capacitor (C1) will charge from –220V x 1.4 to +220V x 1.4 – 20V- V_D. $dV = 2*Vpk-Vo-2V_D$. dV ~= 600V.
3. The required C1 ~ 0.3 millijoules/600V or 0.5 uF

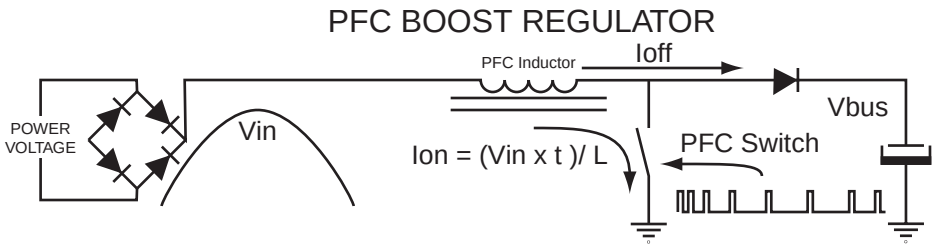
In practice, C1 may have to be larger depending on the amount of ripple allowed by C2 and to account for component tolerances, minimum voltage, and current in the regulator diode. C1 must be a non-polarized type with a voltage rating to withstand the peak line voltage including transients. A high quality film capacitor is recommended.

6.2 Appendix 2: PFC Basics

The function of the PFC boost regulator is to produce a regulated DC supply voltage from a full wave rectified AC line voltage while maintaining a unity power factor load. This means that the current drawn from the line must be sinusoidal and in phase with the line voltage.

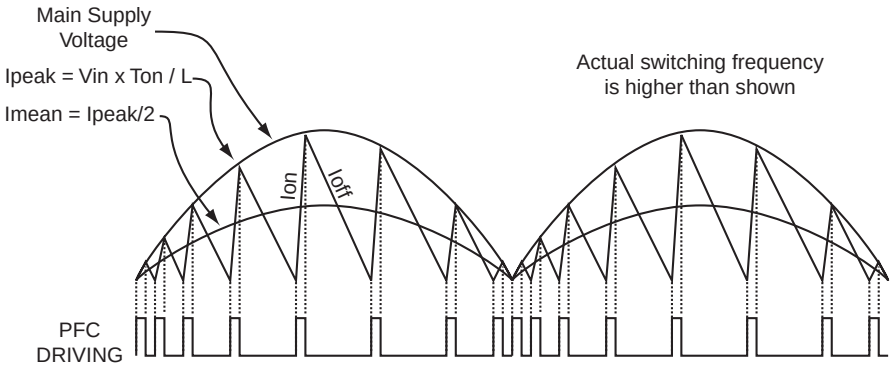
The ballast PFC circuit accomplishes this by means of a boost converter operating (See Figure 6-3) at critical conduction so that the current waveform is triangular (See Figure 6-4).

Figure 6-3. PFC Boost Regulator



The boost switch ON time is maintained constant over each half cycle of the input voltage sinusoid. Therefore the peak current for each switching cycle is proportional to the line voltage which is nearly constant during Ton. (Ipeak = Vin x Ton/L). Since the average value of a triangular waveform is half its peak value, the average current drawn is also proportional to the line voltage.

Figure 6-4. Main voltage supply cutting



6.3 Appendix 3: Bill of Materials

Item Quantity Reference Part Manufactures Part # Distributors Part # Distributor

Table 6-1. Bill of Materials

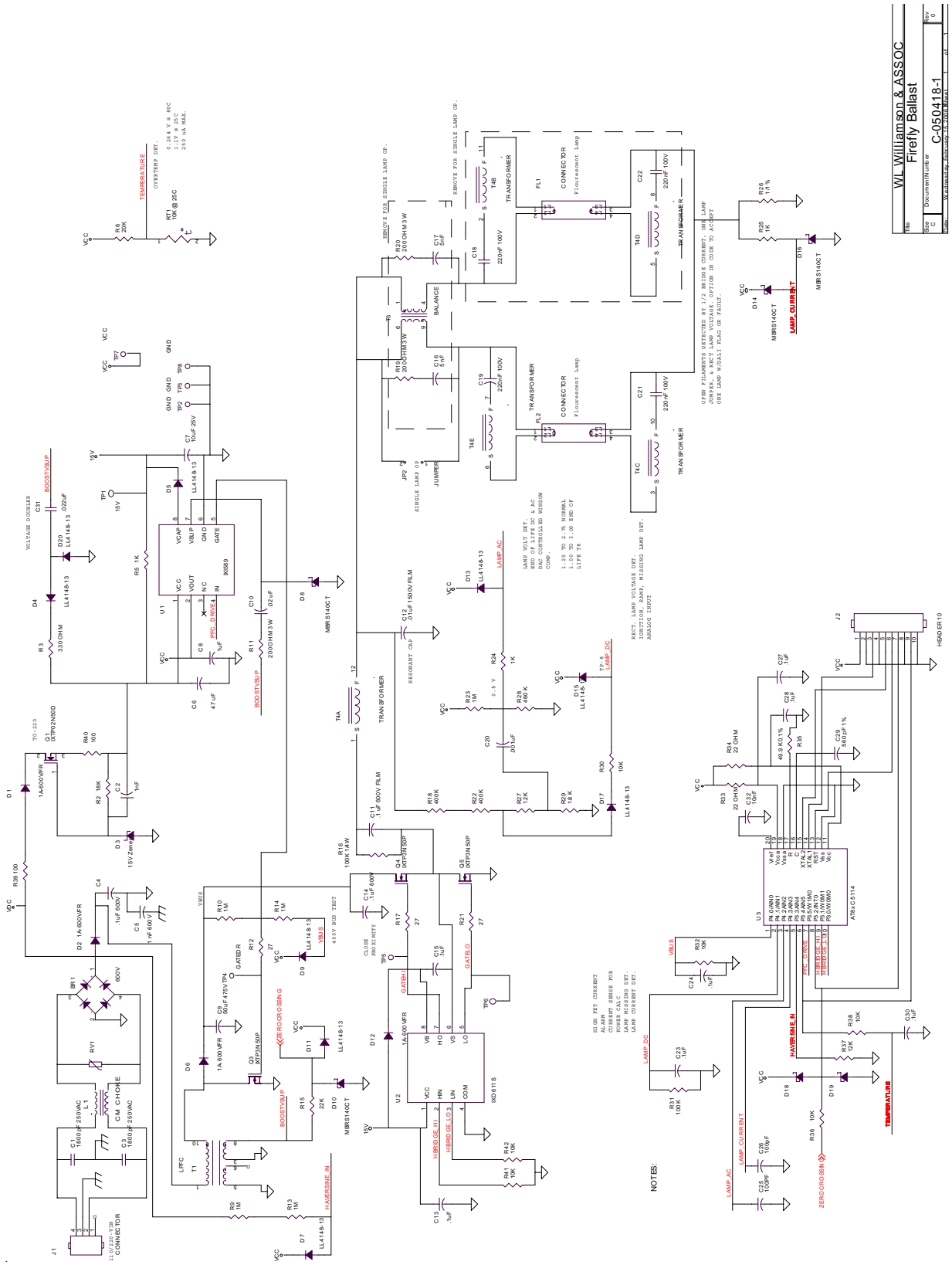
Item	Quantity	Reference	Part	Manufactures Part #
1	1	BR1	600V	DF10S
2	2	C1,C3	1800 pF 250VAC	WYO182MCMBF0K
3	1	C2	1 nF 50V	ECJ-2VB1H102K
4	3	C4,C11,C14	.1 uF 600V	MKP1840410634
5	1	C5	1 nF 250 VAC	ECK-NVS102ME
6	1	C6	47 uF 63V	ECA-1JM470
7	1	C7	10 uF 25V	T491C106K025AS
8	1	C8	1 uF	GRM219F51E105ZA01D
9	1	C9	47 uF 450V	ECO-S2WP470BA
10	2	C10,C31	.022 uF	ECJ-2VF1H223Z
11	1	C12	.01 uF 1500V FILM	MKP100.01/2000/5
12	7	C13,C15,C23,C24,C27,C28,	.1 uF	GRM216F51E104ZA01D
		C30		
13	2	C16,C17	4.7 nF 630V	ECJ-3FB2J472K
14	4	C18,C19,C21,C22	220 nF 100V	ECJ-4YB2A224K
15	1	C20	.001 uF	GRM2165C1H102JA01D
16	2	C25,C26	100 pF	ECJ-2VC1H101J
17	1	C29	560 pF 5%	ECJ-2VC1H561J
18	1	C32	.01 uF	ECJ-2VB1H103K
19	4	D1,D2,D6,D12	1A-600V/FR	MURS160-13
20	1	D3	15V Zener	MMSZ5245B-7-F
21	9	D4,D5,D7,D9,D11,D13,D15,	LL4148-13	LL4148-13
		D17,D20		
22	6	D8,D10,D14,D16,D18,D19	MBRS140CT	MBRS140TR
23	3	J1,FL1,FL2	CONNECTOR	1935187
24	1	JP2	JUMPER	929834-03-36
25	1	J2	HEADER 10	10-88-1101
26	1	L1	CM CHOKE	ELF-15N007A
27	1	Q1	IXTP02N50D	IXTP02N50D
28	3	Q3,Q4,Q5	IXTP3N50P	IXTP3N50P
29	1	RT1	10K @ 25C	01C1002JP
30	1	RV1	VARISTOR265VAC	ERZ-V05D471
31	1	R2	18K 5%	
32	1	R3	1 OHM 5%	
33	3	R5,R24,R25	1K 5%	
34	1	R6	20K 5%	
35	5	R9,R10,R13,R14,R23	1M 5%	
36	2	R19,R20	200 OHM 2W	ERG-3SJ201
37	3	R12,R17,R21	27 OHM 5%	
38	1	R15	22K 5%	
39	1	R16	100K 1/4W 5%	

Table 6-1. Bill of Materials

Item	Quantity	Reference	Part	Manufactures Part #
40	2	R18,R22	402K 5%	
41	1	R26	1 /1%	
42	1	R27	1.2K 5%	
43	1	R28	464K 5%	
44	1	R29	1.8K 5%	
45	4	R30,R32,R41,R42	10K 5%	
46	1	R31	100K 5%	
47	2	R33,R34	22 OHM 5%	
48	1	R35	49.9K 1%	
49	2	R36,R38	4.7K 5%	
50	1	R37	12K 5%	
51	2	R39,R40	100 OHM 5%	
52	1	TP1	15V	5001
53	3	TP2,TP3,TP8	GND	5001
54	1	TP4	GATEDR	5001
55	1	TP5	GATEHI	5001
56	1	TP6	GATELO	5001
57	1	TP7	VCC	5001
58	1	T1	LPFC	PA1438
59	1	T3	BALANCE	PA1440
60	1	T4	LRES	PA1439
61	1	U1	IXI859	IXI859
62	1	U2	IXD611S	IXD611S
63	1	U3	AT8xC5114	AT8xC5114
64	1	Q3	Heat Sink	531002B02500
	1	R11 Leave off		

6.4 Appendix 4: Schematic

Figure 6-5.



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