Data Sheet
HSCDHD005A

☐Electronic Compass function
☐Accelerometer function

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1. OVERVIEW

HSCDHD series is integrated digital output three axis terrestrial magnetism sensor and three axis acceleration sensor in one package.
A high sensitivity magnetic sensor that detects the terrestrial magnetism element and a low-noise linear acceleration sensor that compensates tilt, detects motion input are mounted.
It provides with the drive circuit, the signal processing circuit, and the serial interface.
The electronic compass function and the angular velocity calculate function are achieved by combining with our software.

2. FEATURES

☐Function:

- 3-Axis magnetic sensor has magnetic field full-scale of ±2.4mT, 0.15μT/LSB resolution.
- 3-Axis acceleration sensor has ±2, ±4, ±8, ±12, ±16g ranges and 8, 10 or 14bit resolution.
- Digital Output, X, Y, Z axis magnetic field strength and X, Y, Z axis acceleration.
- I2C Serial interface
  6-axis sensor acts as two slave devices that are a magnetometer and a accelerometer.
  Magnetic sensor has I2C slave interface (SS、FS、FS+、HS) PhilipsI2C revision .2.1 and NXP UM10204 I2C-bus specification and user manual Rev.03-19 June 2007 is supported.
  Acceleration sensor has I2C(SS,FS).

- Magnetic Function
  - Initialization Function (Power on reset)
  - Functional Mode — Stand-by Mode; Active Mode
  - Measurement — Force State; Normal State (Data Rate 0.5,10,20,100Hz Selectable)
  - Temperature Compensation Function
  - Offset Calibration Function
  - Offset Drift Function
  - Self Test Function

- Acceleration Function
  - Tap Detection

☐ Operating temperatures: -40 to +85℃

☐ Operating supply voltage:
- VDD 1.7 to 3.6 V

☐ Package:
- Package type 12 pin, LGA
- Package size 2mm x 2mm x t0.95mm

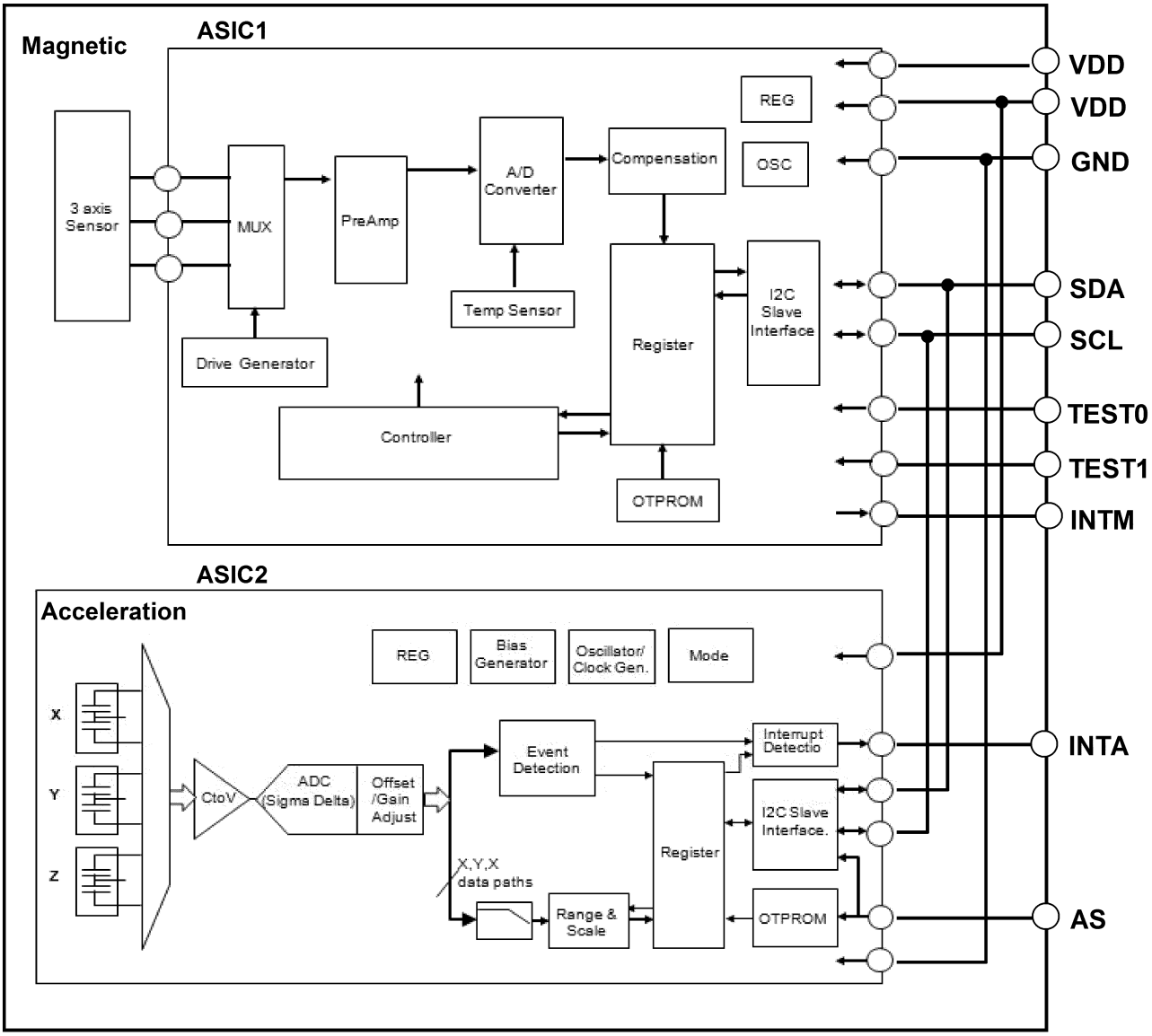
☐ Lead free, RoHS instruction, Halogen free conformed

3. Table of Contents

3. Table of Contents

4. Circuit Configrations

4.1. Block Daigram

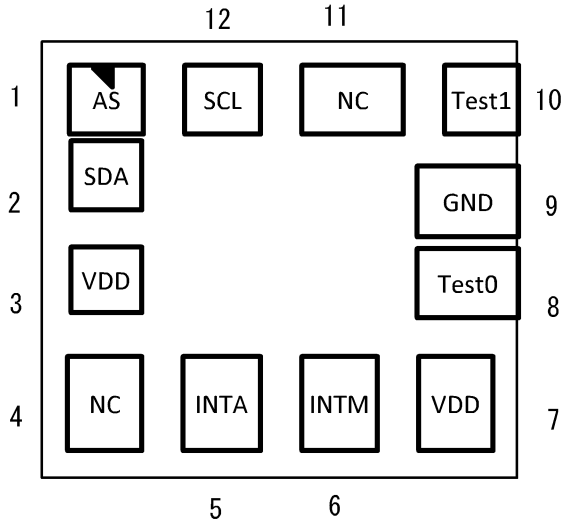


4.2. Pin Assignment

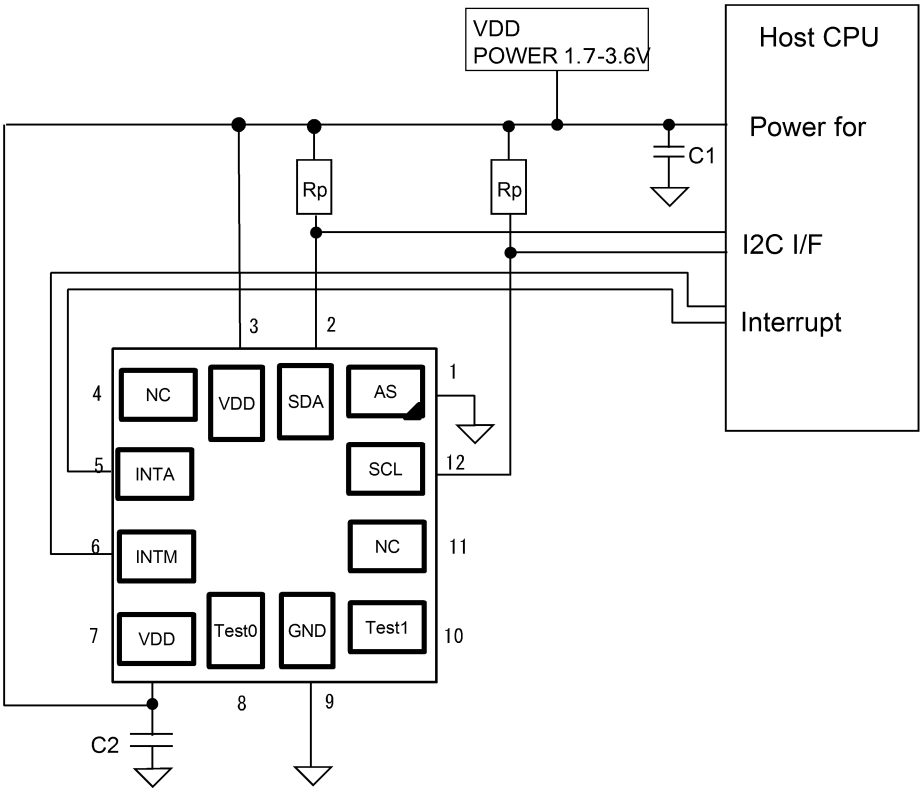
Pin	Symbol	Type	Description	Connect Pin
1	AS	Input, CMOS	Accel I2C Address Select and Factory Program(VPPA)	VDD/GND
2	SDA	Input / Output CMOS / Open drain	Control data input/output pin.[1]	SDA
3	VDD	Power	Power supply pin.	VDD
4	NC	-	Not Internally Connected	NC/VDD/GND
5	INTA	Output, CMOS	Accel Interrupt Active Low and Factory Test [2]	INT/NC
6	INTM	Output, CMOS	Data ready signal for geomagnetic sensor The active is selectable with LOW or HIGH	INT/NC
7	VDD	Power	Power supply pin.	VDD
8	TEST0	Input, CMOS	Magnetometer Factory Test [3]	NC/GND
9	GND	Power	Ground pin.	GND
10	TEST1	Input, CMOS	Magnetometer Factory Program [3]	NC/VDD/GND
11	NC	-	Not Internally Connected	NC/VDD/GND
12	SCL	Input, CMOS CMOS / Open drain	Control data clock[1]	SCL

Notes 1) I2C pin requires a pull-up resistor, typically 4.7kΩ to DVDD.
2) Output mode is programable to open-drain output or push-pull output (MODE: Register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to DVDD.
3) Test pin uses only the Manufacturing test.

Top view



4.3. Typical Application Circuit

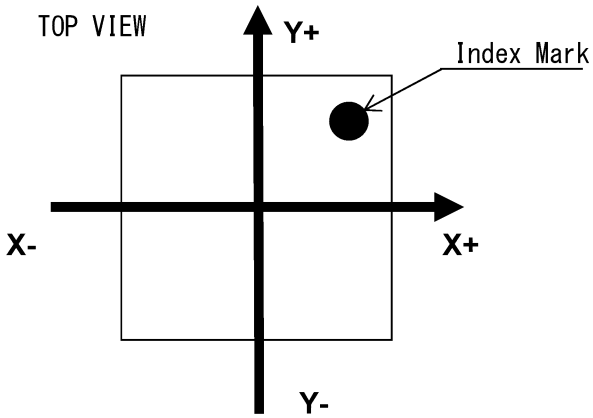


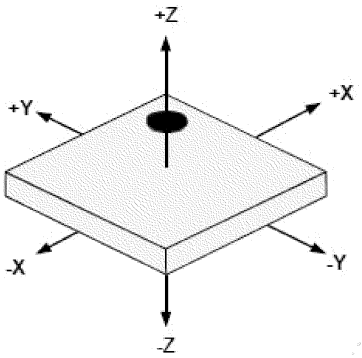
Connection ie at I2C Interface

Notes
- Capaciter recommendation : C1, C2 = 100nF (0.1μ F)
- Resistors recommendation : Rp = 4.7Kohm

4.4. Package Directions

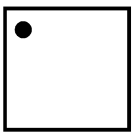
- X, Y, Z presents measurement directions of 3 axis sensor.
- Magnetic sensor output value of each axis is positive when turned toward magnetic north.



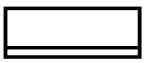


Direction of sensing axes

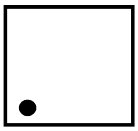
Direction of
Earth gravity
Acceleration
Magnetic field



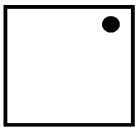
Xout= +1g, +|B|uT
Yout= 0g, 0uT
Zout= 0g, 0uT
TILT= UP



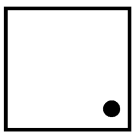
Xout= 0g, 0uT
Yout= 0g, 0uT
Zout= +1g, +|B|uT
TILT= FRONT



Xout= 0g, 0uT
Yout= -1g, -|B|uT
Zout= 0g, 0uT
TILT= LEFT



Xout= 0g, 0uT
Yout= +1g, +|B|uT
Zout= 0g, 0uT
TILT= RIGHT



Xout= -1g, -|B|uT
Yout= 0g, 0uT
Zout= 0g, 0uT
TILT= DOWN

Xout= 0g, 0uT
Yout= 0g, 0uT
Zout= -1g, -|B|uT
TILT= BACK

5. Overall Characteristics

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	-0.3	-	+3.6	V
Input Voltage	VIN	-0.3	-	+3.6	V
Acceleration, any axis, duration 100us	gmax	-	-	10,000	g
Strage Temperature	Tstg	-40	-	+125	℃

5.2. Recommended Operating Conditions

Unless otherwise specified: VDD = 2.8V, Ta = 25℃

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	1.7	2.8	3.6	V
Operating Temperature	Ta	-40	-	+85	℃
External capacitance : VDD-GND	-	-	100	470	nF
Pull-up Resistor for SDA, SCL	-	-	4.7	-	KOhm

Note : Pin 3 and Pin 7 must be supplied same voltage as VDD.

5.3. Electrical Characteristics

5.3.1. Magnetic Sensor Characteristics

Unless otherwise specified: VDD = 2.8V, Ta = 25℃

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Measurement Range (x, y, z) [4]	Brg	-2.4	-	+2.4	mT
Measurement Nonlinearity (±1.2mT)		-2	-	+2	%FS
Measurement Sensitivity		-	0.150	-	μT/LSB
Supply Current Consumption (Total)					
Stand-by Mode	IDD	-	3	10	μA
Active Mode, Average (ODR = 10Hz)	IDD	-	60	85	μA
Active Mode, Maximum	IDD	-	2.5	3	mA
Output Data Rate (Normal State) [4]	ODR	0.5	-	100	Hz
Output Resolution [4]		-	-	15	bit
Measurement Time [4]		-	-	5	msec
Control Timing [4]					
Turn On Time (Off to Stand-by Mode)		-	-	3	msec
Turn On Time (Stand-by to Active Mode)		-	-	5	μsec
Turn Off Time (Active to Stand-by Mode)		-	-	5	μsec

Note 4) Values are based on device characterization, not tested in production.

5.3.2. Acceleration Sensor Characteristics

Unless otherwise specified: VDD = 2.8V, Ta = 25°C

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Measurement Range *Resolution and range set in OUTCFG: Output Configuration Register			±2 ±4 ±8 ±12 ±16		g
Measurement Sensitivity *Depends on settings in OUTCFG: Output		16		4096	LSB/g
Output Data Rate *Depends on settings in SRTFR: Sample Rate and Tap Feature	ODR	0.25	-	256	Hz
Supply Current Consumption (Total) [5] Stand-by Mode Wake Mode (ODR = 128Hz) (highly dependent on sample rate)	 IDD IDD	 - -	 4 85	 - -	 μA μA
Sensitivity Temperature Drift [5] -40≦Ta≦+85°C	TCSg	-	±0.025	-	%/°C
Zero-g Offset [5]	OFF0g	-	±40	-	mg
Zero-g Offset Temperature Drift [5] -40≦Ta≦+85°C	TCOg	-	±1	-	mg/°C
Noise Density [5]	Nrms	-	200	-	μg/√Hz
Nonlinearity [5]		-	±0.5	-	%FS
Cross-axis Sensitivity [5] Between any two axes		-	2	-	%

Note 5) Values are based on device characterization, not tested in production.

5.3.3. I2C Electrical Characteristics

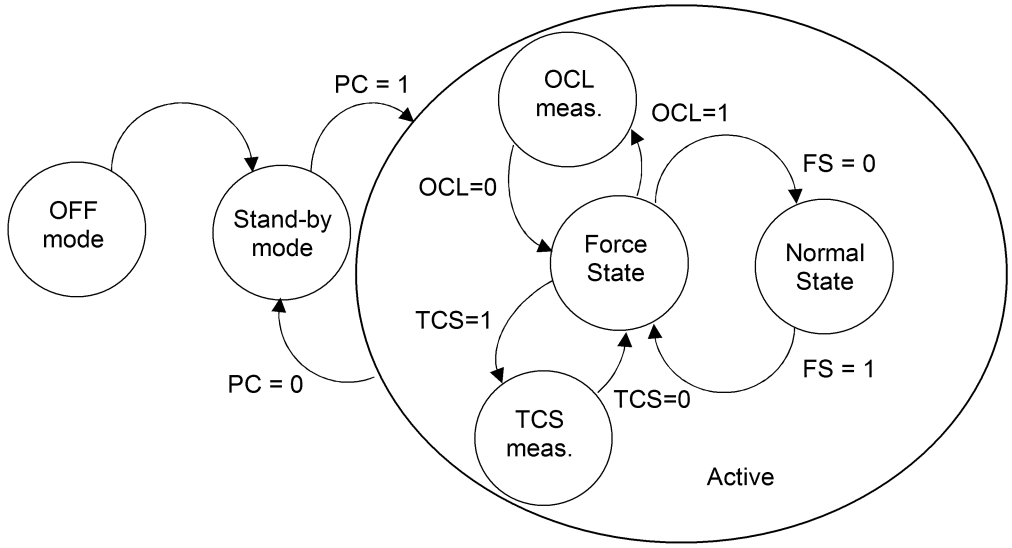
Unless otherwise specified: VDD = 2.8V, Ta = 25°C

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input Voltage High	VIH	0.8 x DVDD	-	DVDD	V
Low	VIL	0	-	0.2 x DVDD	V
Output Voltage High	VOH	0.9 x DVDD	-	DVDD	V
Low Iol ≦1mA	VOL	0	-	0.1 x DVDD	V
Output Voltage pin INT, Iol ≦2mA	VOH	0	-	0.9 x DVDD	V
	VOL	0	-	0.4	V
Capacitance, pin SDA and SCL	Ci	-	-	10	pF

6. Magnetic Sensor Functional Specifications

6.1. Function List

Name	Description
Initialization	Power on reset is performed by turning on the power. All circuits and registers are set to default and mode is set to stand-by mode automatically by POR. Software reset is performed by writing to control register. All register is reloaded form OTP and internal compensation table is reloaded.
Self Test	Self test confirm the operation on sensor by register command
Functional Modes	This sensor has stand-by mode and active mode for power control. There are two states in active mode.
Off mode	The sensor is not active when AVDD and/or DVDD_IO are disable.
Stand-by Mode	Low power waiting state. Stand-by mode can access to register. Reading/Writing register is enable on stand-by mode.
Active Mode	Change from stand-by to active mode by register command to control register.
Force State	Start to measure and output data by register command. Force state is default.
Normal State	Perform to measure and output data by using the internal timer trigger.
Data Ready Function	Informs when new measured results are updated. It is possible that data ready inform the signal to the INTM pin when updated output data.
Offset Calibration Function	Sensor offset can be canceled by using internal ADC circuit and digital compensation function when the register command is set.
Offset Drift Function	When magnetic field strength have offset drift, output data values can be compensated by writing in the offset value registers.
Temperature Measurement Function	Retrieve temperature data from internal temperature sensor. Temperature data is used for internal compensation for output data.
Temperature Compensation Function	Compensate gain in digital circuit by temperature measurement results.



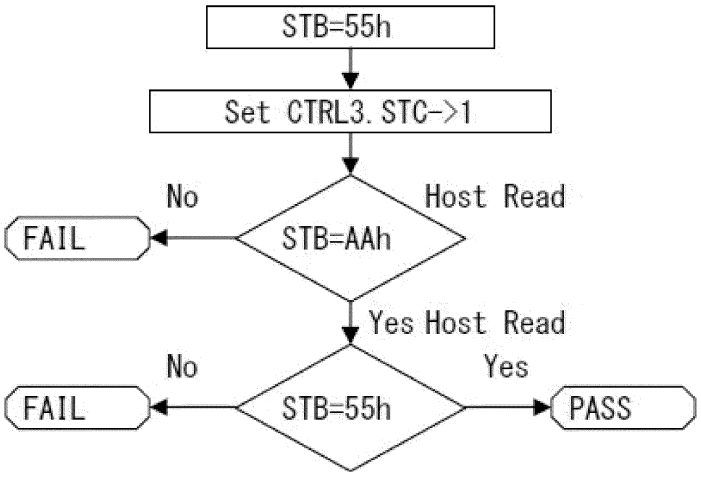
State Machine

6.1.1. Initialization

- All internal circuits and all register values are initialized with POR (Power On Reset) after power-on.
- After initialization, the functional mode move to standby mode automatically.
- The software reset set by the register command SRST=1 makes all register value to defaults and reload the compensation values for internal sensor calculation.

6.1.2. Selftest

-Selftest can be used to confirm with the inner I/F and the digital logic.
-Selftest is performed with reading the STB register and setting the register command CTRL3 STC bit to Hi.
-The following chart show the procedure of selftest .
-The value of response register STB is back to 55h after reading it.



The flow chart of selftest

6.1.3. Functional Modes

OFF mode

-The sensor is not active when VDD are disable.
-The following table show the each status of off mode.

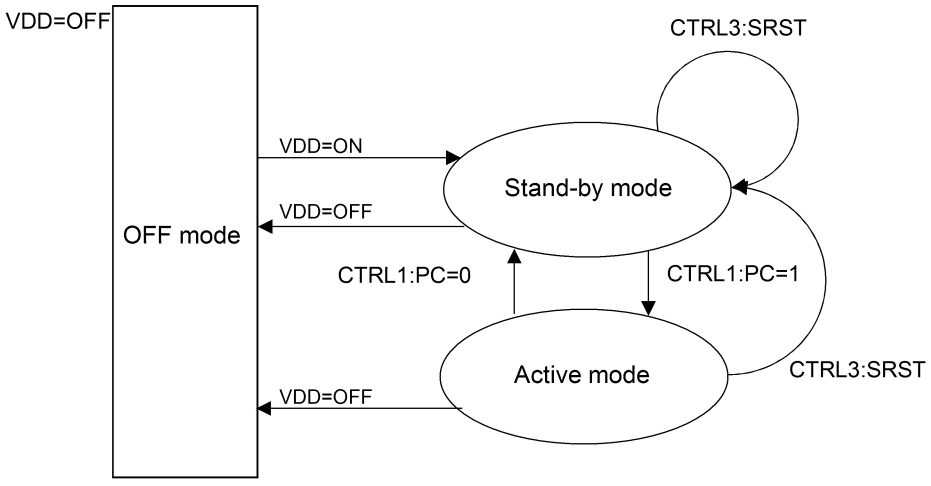
VDD	Operation State
0V	Sensor is not active, There are no inference on the interface bus.
1.7V to 3.6V	Sensor is active, There are inference on the interface bus.

Stand-by mode

-After loading the POR (Power On Reset), internal state is moved to the standby mode automatically.
-Read and Write access function is limitative as follows at the stand-by mode.
-Write: (CTRL3) FORCE, TCS and STC are disable
-Read: All resister can be read.
-Register is cahnged form the Active mode to the Stand-by mode by set PC=0(CNTL1) as follows.

Active mode

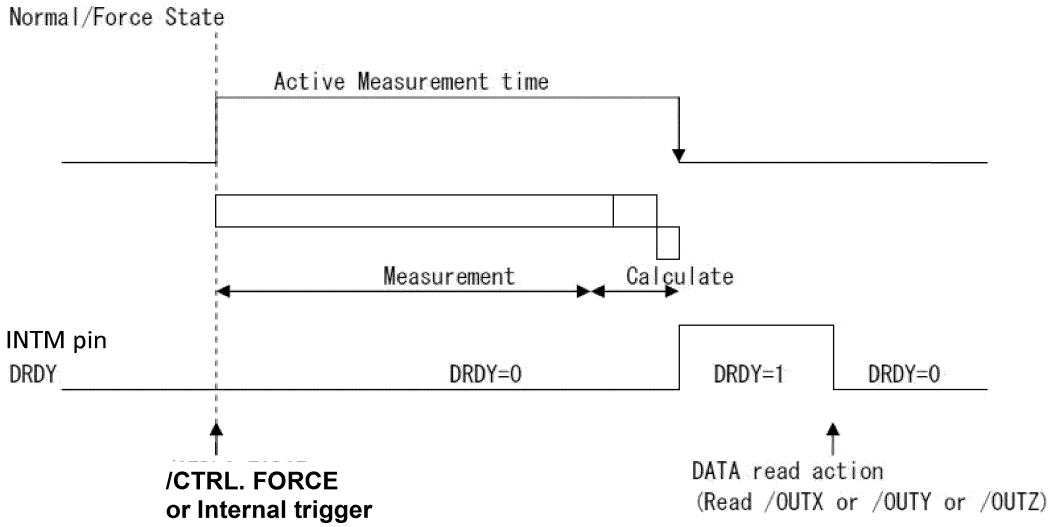
-At active mode, each function can be performed by setting control register 3(CTRL3).
-To transfer to active mode, it sets the PC=1(CTRL1).
-There are two types of measurement state. One is periodical measurement "Normal state " controlled by inner timer. and the other is "Force state" controlled by register command form outside.
-The measurement state is selectable with FS bit on control register 1(CTRL1)
-The default of measurement state is the force state (FS=1) after POR or reset running.



The diagram on mode transfer

6.1.4. Data ready function

-This function is used for notice that output data was updated.
-Data ready output is enable on the outside terminal (INTM pin), when the data was updated.
- Information of data ready can be read with the status register (STAT).
-DRDY is changed to LOW after reading data on the output register.
- Conditions of data ready function can be set on the control register (CTRL2).



Control function for Data Ready terminal with CTRL2 register

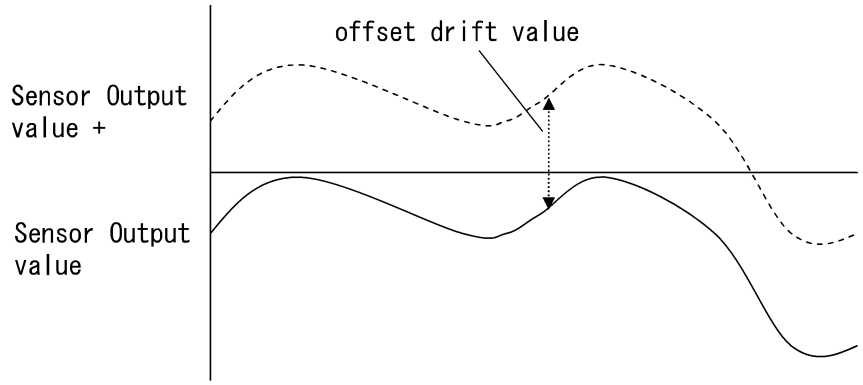
CTRL2 bit	Bit Name	Default	Condition
3	DEN	0	Output control on INTM pin 0 = Disable 1 = Enable
2	DRP	1	The polarity setting on INTM pin 0 = Active Low 1 = Active High

6.1.5 Offset calibration function

-This function is enable when the control register (CNTL3:OCL) was set to Hi during the Force State.
-The offset value for inner ADC output is calculated with the measured sensor offset, and then set compensation values for the amplitude offset and also the digital offset automatically.
-The OCL bit is changed to be low after updating the compensation offset value, and then the status is back to before measurement.

6.1.6. Offset drift function

-This function can make the digital compensation output that is add with values wrote by the host CPU on the offset drift register (OFFX,OFFY,OFFZ).
-Offset drift values can be set with 15bit signed value.

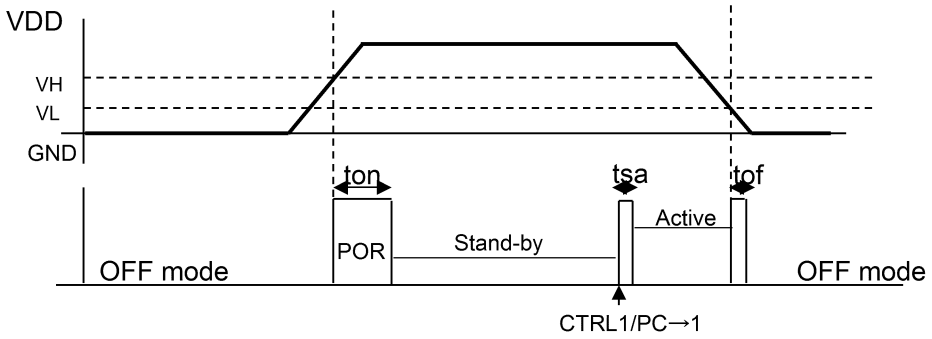


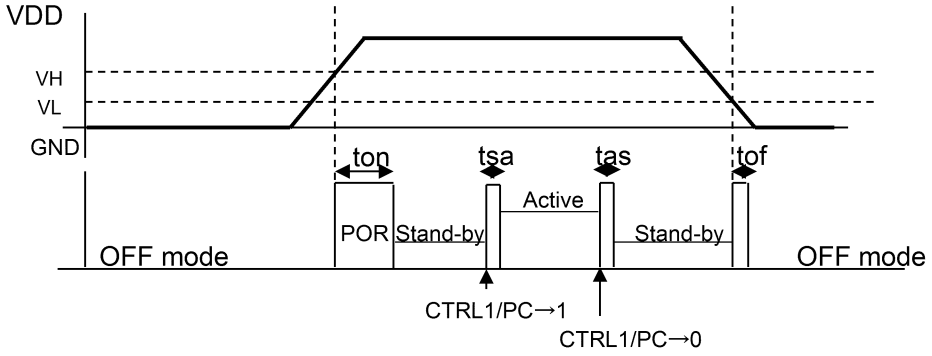
6.1.7. Temperature Measurement and Compensation Function

- The temperature measurement function will be executed when the register command TCS is set "1" during the Force State. After measurement, TCS bit change to "0" and back to before measurement.
-The measurement result is wet on the temperature value register (TEMP).
-Sensor output values are compensated with the temperature value register(TEMP)

6.1.8. Control Timing Specifications

Power Supply Sequence





Parameters on Supply voltage sequence (All Condition)

Transition	Symbol	Typ.	Max.	Unit
OFF→Stand-by	ton	-	3	ms
Stand-by→Active	tsa	-	5	μ s
Active→Stand-by	tas	-	5	μ s
Active or Stand-by→OFF	tof	-	10	ms

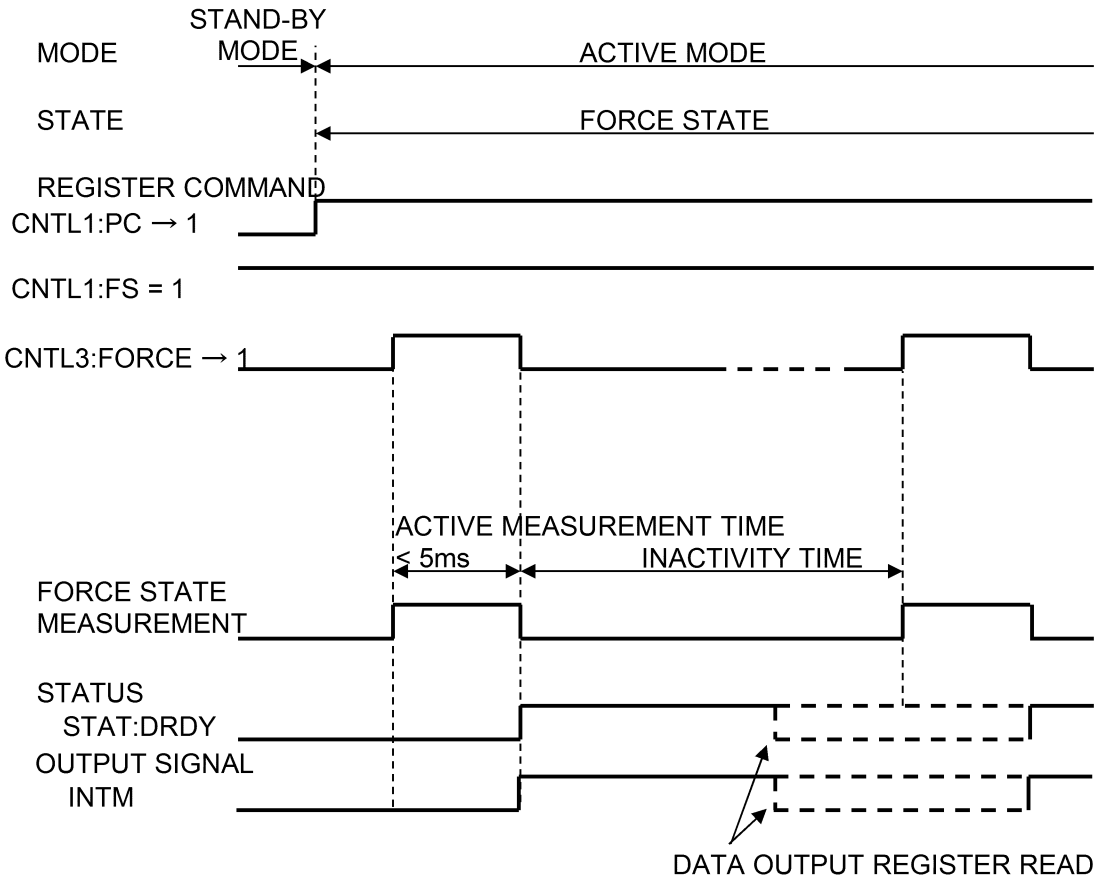
Parameters on Supply voltage sequence (All Condition)

Characteristics	Symbol	Min.	Max.	Unit
VDD ON	VH	1.53	-	V
VDD OFF	VL	-	0.17	V

6.1.8. Control Timing Specifications

Force state

- Force state is used for synchronous measurement (selected from register CTRL3, bit FRC), and measurement starts after forced register command to register via bus.
- Functional mode changes from Stand-by mode to Active mode by setting register (Control1: bit PC) to "1".
- Force state is set by control register (CNTL1: bit FS) "1".
- Acquired data stored to output register (OUTX, OUTY, OUTZ), and status register (STAT: bit DRDY) is set to "1" and output signal (INTM pin) are set to active.
- Output on external INTM pin is set by control register (CNTL2)
- During reading data, out put register is not updating. After reading is complete, reading data is updated.
- Change of state from Normal to Force is valid after measurement if control register is set during the Active measuring in Normal state.

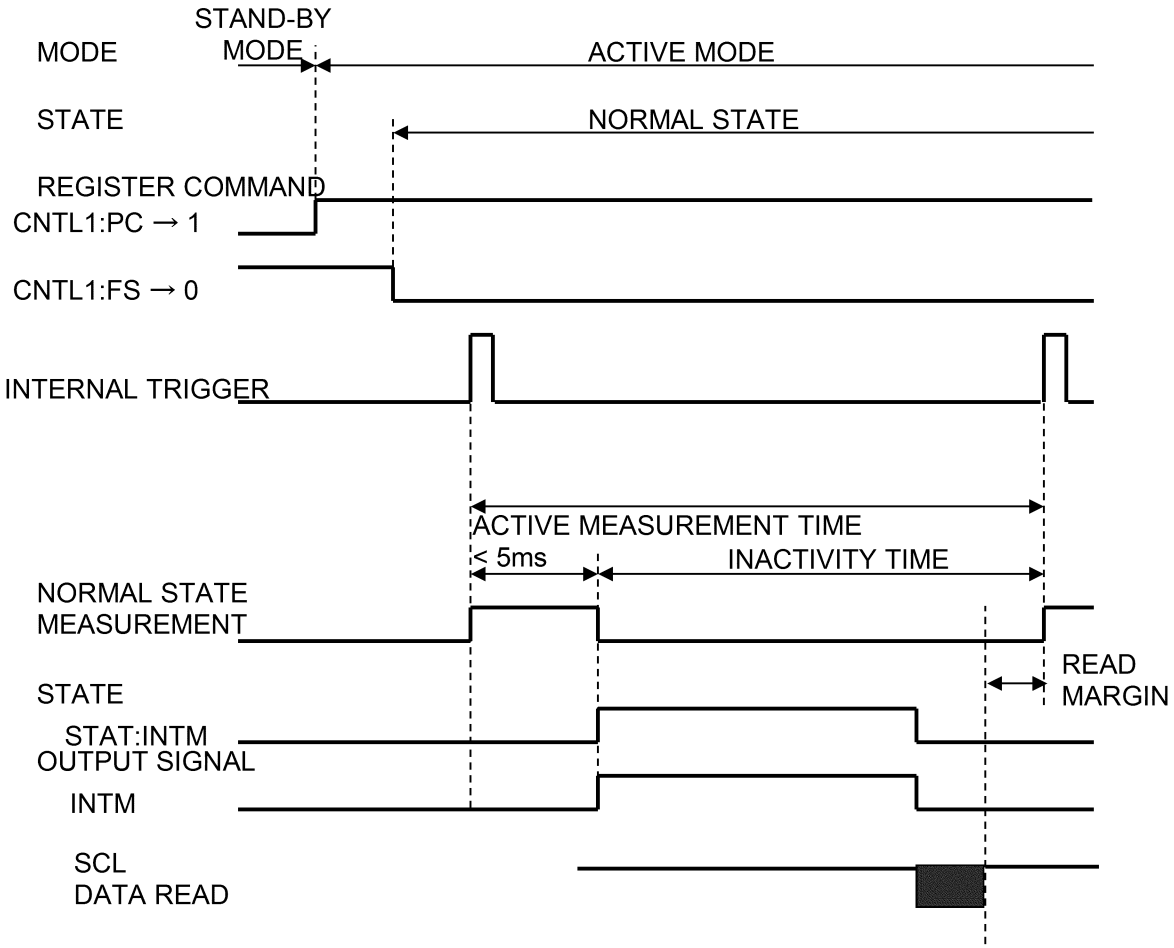


Measurement control timing (Force state)

6.1.8. Control Timing Specifications

Normal state

- Normal state is continuous measurement state, and when Normal state is set by setting “0” to control register (CNTL1: bit FS), channels measurement is started.
- Measurement time and interval are managed with internal clock.
- Functional mode changes from Stand-by mode to Active mode by setting register (CNTL1: bit PC) to "1".
- Output data rate (ODR) is selectable with 0.5Hz or 100Hz by register (CNTL1: bit ODR).
- Acquired data are stored to register (OUTX, OUTY, OUTZ), status register (STAT: bit DRDY) is set to "1" and output PIN signal are control with (CNTL2:bit DEN).



Note: READ MARGIN is need more than "0msec" in normal state.

. DATA READ Time should be set less than 1msec including clock starch.
Minimum case is happen in ODR=11(100Hz) on measurement function.

Measurement control timing (Normal state)

7. Acceleration Sensor Functional Specifications

7.1. Function List

Name		Description
Initialization		Power on reset is performed by turning on the power. All circuits and registers are set to default and mode is set to stand-by mode automatically by POR. Software reset is performed by writing to control register. All register is reloaded form OTP and internal compensation table is reloaded.
Functional Modes		This sensor has stand-by mode and wake mode for power control.
	Stand-by Mode	Low power waiting state. Stand-by mode is the default state after power-up. Reading/Writing register and is enable, but interrupts cannot be serviced. Internal clocking is disabled.
	Wake Mode	Change from stand-by to active mode by register command to control register. Continuous sampling and reading data of sensor. Only writing register is enable to the MODE: Register. Full read access is enable in all states.
Sensor Sampling Function		The internal sampling rate range can be selected between 0.25 Hz and 256 Hz. The sensor readings data appear as selected resolution upto 14-bit.
Offset and Gain Calibration Function		Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of assembly influences and stresses which may cause the sensor readings to be offset from their factory values.
Tap Detection Functon		The tap detection allows the device to detect user events such as pressing button on-screen.
Interrupts Function		The sensor device utilizes output pin INTA to signal to an external microprocessor that an event has been sensed. The event detections are TAP event and sensor update.

7.1.1. Functional Modes

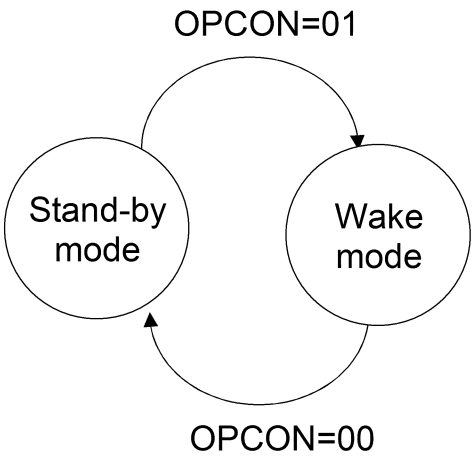
-The device has two states of operation: STANDBY (the default state after power-up), and WAKE.
-The STANDBY state offers the lowest power consumption.
The I2C interface allows write access to all registers only in the STANDBY state.
-In WAKE state, the only I2C register write access permitted is to the MODE: Mode Control Register.
Full read access is allowed in all states.

state	I2C Bus	Description
STANDBY	Device responds to I2C bus (R/W)	・Device is powered; Registers can be accessed via I2C. Lowest power state. No interrupt generation, internal clocking disabled. Default power-on state.
WAKE	Device responds to I2C bus (Read)	・Continuous sampling and reading of sense data. All registers except the MODE: Register are read-only.

Accelerometer Operational State Flow

-The operational state may be forced to a specific state by writing into the OPCON bits, as shown below.
-The operational state will stay in the mode specified until changed.

state	Set	Description
Force Wake mode	OPCON[1:0] = 01	・Switch to Wake mode and stay there ・Continuous sampling data
Force stand-by mode	OPCON[1:0] = 00	・Switch to Stand-by mode and stay there ・Disable sensor and event sampling



State Machine

7.1.2. Sensor Sampling

-The sampling rate can be selected between 0.25 Hz and 256 Hz.
-This register can be used to set the range and resolution of the accelerometer measurements.
-Measurement data is stored in the “extended” registers XOUT_EX, YOUT_EX, and ZOUT_EX.
-The byte with the lower address of the byte pair is the least significant byte
while the byte with the next higher address is the most significant byte.
-The measurement data is represented as 2’s complement format.
For example, 10-bit samples occupy bits [9:0], with bits [15:9] occupied by the sign bit.
14-bit samples occupy bits [13:0], with bits [15:13] occupied by the sign bit.
-The desired resolution and full scale acceleration range of ±2g, ±4g, ±8g, ±12g, ±16g are set in OUTCFG: Output Configuration Register.
-The device sample rate is set in SRTFR(SAMPLE RATE AND TAP REGISTER).

7.1.3. OFFSET AND GAIN CALIBRATION

-Digital offset and gain calibration can be performed on the sensor.
If necessary, in order to reduce the effects of post-assembly influences and
stresses which may cause the sensor readings to be offset from their factory values.

7.1.4. TAP DETECTION

-The device supports directional tap detection in ±X, ±Y or ±Z.
-Each axis is independent, although only one direction per axis is supported simultaneously.
-The threshold, duration, and dead-time of tap detection can be set for each axis,
and six flag/status bits are maintained in a status register.
-The tap uses a second order high-pass filter to detect fast impulse/transition acceleration events.
-The external interrupt pin can be used to indicate that a tap event has been detected.

7.1.5. INTERRUPTS

-The INTA pin is used in order to tell to an external microprocessor that the event occurred.
- If interrupts are used, the microprocessor must set up the registers due to detect a event.
- If polling is used, no need to setup the interrupt registers.

Accelerometer Enabling and Clearing Interrupts

-The SR (Status Register) contains the flag bits for the sample acquisition interrupt ACQ_INT.
-The INTEN (Interrupt Enable Register) determines which events generate interrupts.
When an event is detected, it is masked with an interrupt enable bit in this register and the corresponding status bit is set in the SR (Status Register).
-The INTA pin is cleared during the next I2C bus cycle.
-When an interrupt is triggered, the first I2C read access to the device clears INTA pin.
The condition which generated the interrupt will remain held in the SR until it is read.
-The polarity and the mode of INTA pin may be chosen by setting IPP and IAH bits in the MODE Register.

Accelerometer ACQ_INT Interrupt

-The ACQ_INT flag bit in the SR (Status Register) is always active. This bit is cleared when it is read.
Tthe frequency of this ACQ_INT bit being set active is always the same as the sample rate.

Accelerometer Continuous Sampling

-The device has the ability to read in a continuous sampling mode.
The device always updates the XOUT, YOUT, and ZOUT registers at the chosen ODR.
An optional interrupt can be generated each time the sample registers have been updated (ACQ_INT interrupt bit in the INTEN).

8. I2C Interface

8.1. I2C Slave Interface

- Conformable to Philips I2C-Bus Specification Version 2.1 and NXP UM10204 I2C-bus specification and user manual Rev.03-19 June 2007
- Slave address of magnetic sensor is fixed '0001100'. (7bit device address 0x0C)
- Slave address of acceleration sensor are selectable with '1001100' and '1101100' (0x4C and 0x6C)
- The acceleration sensor I2C device address depends upon the state of the pin AS during power-up as shown in the table below.

7-bit Device ID	8-bit Address – Write	8-bit Address – Read	Pin AS level power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

8.2. I2C Timing Characteristics

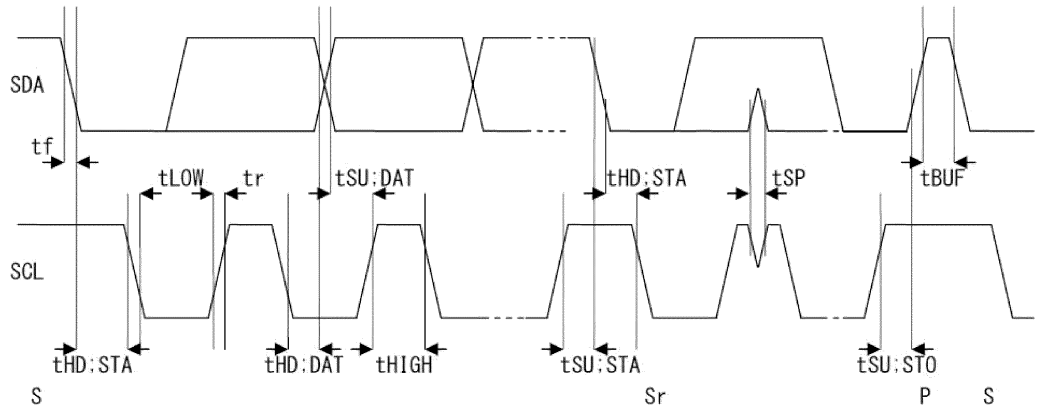
- Acceleration sensor supports Standard mode and Fast mode.
- Magnetic sensor supports Standard mode, Fast mode , Fast mode Plus and Hi speed mode.
- It is seemless change from Fast mode to Hi speed mode to use the master code (00001XXX)
- Support Multiple Read and Write mode.
- Clock stretch function is not available.

I2C bus interface timing diagram 1

Parameters	Symbol	Standard Mode		Fast mode		Fast mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold time (re)start condition	$t_{HD:STA}$	4.0	–	0.6	–	0.26	–	us
Low period of the SCL clock	t_{LOW}	4.7	–	1.3	–	0.5	–	us
High period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	0.26	–	us
Set-up time for (re)start condition	$t_{SU:STA}$	4.7	–	0.6	–	0.26	–	us
Data hold time	$t_{HD:DAT}$	0	–	0	–	0	–	us
Data set-up time	$t_{SU:DAT}$	250	–	100	–	50	–	ns
Rise time of SDA and SCL	t_r	–	1000	–	300	–	120	ns
Fall time of SDA and SCL	t_f	–	300	–	300	–	120	ns
Set-up time for stop condition	$t_{SU:STO}$	4.0	–	0.6	–	0.26	–	us
Bus free time between a stop and start condition	t_{BUF}	4.7	–	1.3	–	0.5	–	us
Capcacitive load for SDA/SCL	C_b	–	400	–	400	–	300	pF
Data valid time	$t_{VD:DAT}$	–	3.45	–	0.9	–	0.45	us
Data valid acknowledge time	$t_{VD:ACK}$	–	3.45	–	0.9	–	0.45	us
Noise margin at the low level	VnL	0.1* DVDD	–	0.1* DVDD	–	0.1* DVDD	–	V
Noise margin at the high level	VnH	0.2* DVDD	–	0.2* DVDD	–	0.2* DVDD	–	V

8.2. I2C Timing Characteristics

I2C bus interface timing diagram 2



Parameters	Symbol	Hs-mode C_b=100pF (max)		Hs-mode C_b=400pF		Unit
		Min.	Max.	Min.	Max.	
SCLH clock frequency	f_{SCLH}	0	3.4	0	1.7	MHz
Hold time (re)start condition	$t_{HD:STA}$	160	–	160	–	ns
Low period of the SCLHclock	t_{LOW}	160	–	320	–	ns
High period of the SCLH clock	t_{HIGH}	60	–	120	–	ns
Set-up time for (re)start condition	$t_{SU:STA}$	160	–	160	–	ns
Data hold time	$t_{HD:DAT}$	0	70	0	150	ns
Data set-up time	$t_{SU:DAT}$	10	–	10	–	ns
Rise time of SCLH	t_{rCL}	10	40	20	80	ns
Fall time of SCLH	t_{fCL}	10	40	20	80	ns
Rise time of SDAH	t_{rDA}	10	80	20	160	ns
Fall time of SDAH	t_{fDA}	10	80	20	160	ns
Set-up time for stop condition	$t_{SU:STO}$	160	–	160	–	ns
Capcacitive load for SDA/SCL	C_b	–	100	–	400	pF
Noise margin at the low level	V_{nL}	0.1* DVDD	–	0.1* DVDD	–	V
Noise margin at the high level	V_{nH}	0.2* DVDD	–	0.2* DVDD	–	V

8.3. I2C Protocol Format

- Data transfers follow the combined format with 7-bit addressing of I2C interface.
- Data is transferred with the most significant bit (MSB) first and little endian.
- Auto-increment of previous accessed register address is available when the internal register address is written during the first data byte. Data then can be transferred continuously.

Bus protocol definitions

S: Start condition
SAD+W: Slave Address + write bit
SAD+R: Slave Address + read bit
SAD+R/W: Slave Address + read or write bit
SAK: Slave Acknoledge
REG: Register Address(2nd byte)
Sr: Repeat Start condition
A: (Master) Acknowledge
/A: (Master) Non-Acknowledge
DATA: Data(load)
P: Stop condition
M-code: Master code (00001XXX)

Read Formats

One byte read flow

master	S	SAD+W		REG		SR	SAD+R			/A	P
slave			SAK		SAK			SAK	DATA		

Multiple byte reads flow

master	S	SAD+W		REG		SR	SAD+R			A		/A	P
slave			SAK		SAK			SAK	DATA		DATA		

Write Format

One byte wirte flow

master	S	SAD+W		REG		DATA		P
slave			SAK		SAK		SAK	

Multiple byte writes flow

master	S	SAD+W		REG		DATA		DATA		P
slave			SAK		SAK		SAK		SAK	

HS mode data trasfer

HS mode is enable after writeing Mcode.

speed	F/S-mode			Hs-mode						FS-
master	S	Mcode	/A	SR	SAD +R/W		DATA	/A	P	
slave						A	DATA	A		
									Hs- continue	
master									SR	SAD +R/W

9. Magnetic Sensor Register Interface

9.1. Register MAP

- Register addresses and definitions are as follows.
- Sensor output values are signed integer (2's compliment) presentation and little Endian order.

Address	Name	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	Default hex
0C	Self-Test response	STB[7:0]								55
0D	"More Info version"	0	0	0	1	0	0	0	1	11
0E	"More Info ALPS"	0	0	0	1	0	1	0	1	15
0F	"Who I Am"	0	1	0	0	1	0	0	1	49
10	Output x LSB	OUTX[7:0]								00
11	Output x MSB	OUTX[15:8]								00
12	Output y LSB	OUTY[7:0]								00
13	Output y MSB	OUTY[15:8]								00
14	Output z LSB	OUTZ[7:0]								00
15	Output z MSB	OUTZ[15:8]								00
18	Status	-	DRDY	DOR	-	-	FFU	TRDY	ORDY	00
1A	-	-								00
1B	Control1	PC	-	-	ODR[1:0]		-	FS	-	0A
1C	Control2	-	-	-	-	DEN	DRP	DTS	DOS	04
1D	Control3	SRST	FORCE	-	STC	-	-	TCS	OCL	00
1E	Control4	MMD[1:0]		-	RS	AS	-	-		80
1F	-	-	-	-	-	-	-	-	-	00
20	Offset x LSB	OFFX[7:0]								00
21	Offset x MSB	-	OFFX[14:8]							00
22	Offset y LSB	OFFY[7:0]								00
23	Offset y MSB	-	OFFY[14:8]							00
24	Offset z LSB	OFFZ[7:0]								00
25	Offset z MSB	-	OFFZ[14:8]							00
30	-	-								00
31	Temperature value	TEMP[7:0]								19

9.2. Self Test Response Register (STB)

Address : 0Ch, Self Test Response (Read Only)

Bit	Name	Description
7:0	STB 7:0	Self test starts by STC bit (CNTL3 register). AAh is stored when CNTL3: bit STC sets to 1. 55h is stored after STB register is read.

9.3. Information Registers

Address : 0Dh, "More Info version" (Read Only)

Bit	Name	Description
7:0	INFO1 7:0	Information Value1 (11h)

Address : 0Eh, "More Info ALPS" (Read Only)

Bit	Name	Description
7:0	INFO2 7:0	Information Value2 (15h)

Address : 0Fh, "Who Am I" Value (Read Only)

Bit	Name	Description
7:0	WIA 7:0	Identify byte (49h)

9.4. Output Data Register (OUTX, OUTY, OUTZ)

- 15bit integer and 1FFFh (16383d) ～ E000h (-16834d)

Address : 10h, X-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTX 7:0	X-axis Output Data, Signed Integer.

Address : 11h, X-axis Output Data MSB (Read Only)

Bit	Name	Description
7	X	Not Used
6:0	OUTX 14:8	X-axis Output Data, Signed Integer.

Address : 12h, Y-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTY 7:0	Y-axis Output Data, Signed Integer.

Address : 13h, Y-axis Output Data MSB (Read Only)

Bit	Name	Description
7	X	Not Used
6:0	OUTY 14:8	Y-axis Output Data, Signed Integer.

Address : 14h, Z-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTZ 7:0	Z-axis Output Data, Signed Integer.

Address : 15h, Z-axis Output Data MSB (Read Only)

Bit	Name	Description
7	X	Not Used
6:0	OUTZ 14:8	Z-axis Output Data, Signed Integer.

9.5. Status Register (STAT)

Address : 18h, Status (Read Only)

Bit	Name	Description
7	X	Not Used
6	DRDY	Data Ready Detection 0 = Not Detected, 1 = Detected
5	DOR	Data Overrun Detection 0 = Not Detected, 1 = Detected Note: if Read Output Data Register.
4:3	X	Not Used
2	FFU	Must be use Default setting. 0 = (Default) ※
1	TRDY	Must be use Default setting. 0 = (Default) ※
0	ORDY	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

9.6. Control 1 Register (CTRL1)

Address : 1Bh, Control 1 (Write/Read)

Bit	Name	Description
7	PC	Power Mode Control 0 = Stand-by Mode (Default), 1 = Active Mode
6:5	X	Not Used (Read Only)
4:3	ODR 1:0	Output Data Rate Control in Normal State 00 = 0.5 Hz 01 = 10Hz (Default) 10 = 20Hz 11 = 100Hz
2	X	Not Used (Read Only)
1	FS	State Control in Active Mode 0 = Normal State 1 = Force State (Default)
0	X	Not Used (Read Only)

9.7. Control 2 Register (CTRL2)

- When a CTRL2 register value was changed during the measurement, The contents of the change are reflected after measurement.

Address : 1Ch, Control 2 (Write/Read)

Bit	Name	Description
7	−	Must be use Default setting. 0 = (Default) ※
6	−	Must be use Default setting. 0 = (Default) ※
5	−	Must be use Default setting. 0 = (Default) ※
4	−	Must be use Default setting. 0 = (Default) ※
3	DEN	Data Ready Function Control Enable 0 = Disabled (Default), 1 = Enabled
2	DRP	DRDY signal active level control 0 = ACTIVE LOW, 1 = ACTIVE HIGH (Default)
1	DTS	Must be use Default setting. 0 = (Default) ※
0	DOS	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

9.8. Control 3 Register (CTRL3)

- Bit control at the same time is prohibited.
- Priority of this register is MSB.

Address : 1Dh, Control 3 (Write/Read)

Bit	Name	Description
7	SRST	Soft Reset Control Enable 0 = No Action (Default), 1 = Soft Reset Note: return to zero after soft reset.
6	FRC	Start to Measure in Force State 0 = No Action (Default), 1 = Measurement Start Note: return to zero after measurement.
5	X	Not Used (Read Only)
4	STC	Self Test Control Enable 0 = No Action (Default) 1 = Set parameters to Self Test Response (STB) register. Note: return to zero immediately.
3:2	X	Not Used (Read Only)
1	TCS	Start to Measure Temperature in Active Mode 0 = No Action (Default), 1 = Measurement Start
0	OCL	Start to Calibrate Offset in Active Mode 0 = No Action (Default), 1 = Action

9.9. Control 4 Register (CTRL4)

- When a CTRL4 register value was changed during the measurement,
  The contents of the change are reflected after measurement.

Address : 1Eh, Control 4 (Write/Read)

Bit	Name	Description
7:6	MMD	Must be use Default setting. 10 = (Default) ※
5	X	Not Used (Read Only)
4	RS	Set Dynamic range of output data. 0 = 14 bit signed value (-8192 to +8191) (Default) 1 = 15 bit signed value (-16384 to +16383)
3	AS	Must be use Default setting. 0 = (Default) ※
2:0	X	Not Used (Read Only)

※. The change of this bit is prohibited.

9.10. Offset Drift Value Register (OFFX, OFFY, OFFZ)

- Data is 14bit integer and 1FFFh (8191d) ～ E000h (-8192d)

Address : 20h, 14 bits X-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFX 7:0	X-axis Offset Drift Value, Signed Integer.

Address : 21h, 14 bits X-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFX 14:8	X-axis Offset Drift Value, Signed Integer.

Address : 22h, 14 bits Y-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFY 7:0	Y-axis Offset Drift Value, Signed Integer.

Address : 23h, 14 bits Y-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFX 14:8	Y-axis Offset Drift Value, Signed Integer.

Address : 24h, 14 bits Z-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFZ 7:0	Z-axis Offset Drift Value, Signed Integer.

Address : 25h, 14 bits Z-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFX 14:8	Z-axis Offset Drift Value, Signed Integer.

9.11. Temperature Data Register (TEMP)

- Temperature measurement is performed by setting register command (CNTL3 : bit TCS) when in the active mode
- Result is stored to temperature register (TEMP）
-Sensor output value are compensated with the temperature value stored TEMP register.

Address : 31h, Temperature Data (Read Only)

Bit	Name	Description
7:0	TEMP7:0	Temperature Data, Signed Integer. LSB = 1℃ 1000 0000 = -128℃ 0000 0000 = 0℃ 0111 1111 = 127℃

10. Acceleration Sensor Register Interface

10.1. Register MAP

- Register addresses and definitions are as follows.
- Sensor output values are signed integer (2's compliment) presentation and little Endian order.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W [6]
0x00-0x02		RESERVED [7]										
0x03	SR	Status Register	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R
0x04	OPSTAT	Operational Device Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R
0x05		RESERVED [7]										
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0 [8]	OPCON [1]	OPCON [0]	0x00	W
0x08	SRTFR	Sample Rate and Tap Feature Register	TAP_LATCH	FLIP_TAZ	FLIP_TAY	FLIP_TAX	RATE[3]	RATE[2]	RATE[2]	RATE[0]	0x00	W
0x09	TAPEN	Tap Control Register	TAP_EN	THRDUR	TAPZNEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W
0x0A	TTTRX	X Tap Duration and Threshold Register	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	0x00	W
0x0B	TTTRY	Y Tap Duration and Threshold Register	TTTRY[7]	TTTRY[6]	TTTRY[5]	TTTRY[4]	TTTRY[3]	TTTRY[2]	TTTRY[1]	TTTRY[0]	0x00	W
0x0C	TTTRZ	Z Tap Duration and Threshold Register	TTTRZ[7]	TTTRZ[6]	TTTRZ[5]	TTTRZ[4]	TTTRZ[3]	TTTRZ[2]	TTTRZ[1]	TTTRZ[0]	0x00	W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R
0x13-0x1F		RESERVED [7]										
0x20	OUTCFG	Output Configuration Register	0 [8]	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W

Note

[6] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.

[7] Registers designated as 'RESERVED' should not be accessed by sof

[8] Software must always write a zero '0' to this bit.

10. Acceleration Sensor Register Interface (Continued)

10.1. Register MAP

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W [6]
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x28	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A-0x3F		RESERVED										

Register Summary [9]

[9] No registers are updated with new event status or samples while a I2C cycle is in process.

10.2. Status Register (SR)

- This register contains the flag/event bits for tap detection and sample acquisition.
- The TAP bits will only transition if the enable bit has been set in register 0x09, the TAP control register.
- Each read to this register will clear the latched event(s) and re-arm the flag for the next event.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x03	TAPR	Tap Status Register	ACQ_INT	Resv	TAP_ZN	TAP_ZP	TAP_YN	TAP_YP	TAP_XN	TAP_XP	0x00	R

SR Status Register

TAP_XP	Positive X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_XN	Negative X-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YP	Positive Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_YN	Negative Y-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZP	Positive Z-axis TAP detected, flag is set in polling mode or interrupt mode.
TAP_ZN	Negative Z-axis TAP detected, flag is set in polling mode or interrupt mode.
ACQ_INT	Sample has been acquired, flag bit is set in polling mode or interrupt mode. This bit cannot be disabled and is always set be hardware when a sample is ready. The host must poll at the sample rate or faster to see this bit transition.

10.3. Device Status Register (OPSTAT)

- The Operational State status register reports which operational state the device is in, either WAKE or STANDBY as shown in Table of Operational State Status Register

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x04	OPSTAT	Operational Device Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x00	R

Operational State Status Register

OPSTAT[1:0]	Sampling State Register Status, Wait State Register Status 00: Device is in STANDBY state, no sampling 01: Device is in WAKE state, sampling at set sample rate 10: Reserved 11: Reserved
I2C_WDT	I2C watchdog timeout 0: No watchdog event detected 1: Watchdog event has been detected by hardware, I2C slave state machine reset to idle. This flag is cleared by reading this register.
OTPA	One-time Programming (OTP) activity status 0: Internal memory is idle and the device is ready for use 1: Internal memory is active and the device is not yet ready for use

10.4. Interrupt Enable Register (INTEN)

- The interrupt enable register allows the flag bits for specific TAP and sample events.
- This is the only effect these bits have as the flag bits will be cleared by accessing register 0x03.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	TIZNEN	TIZPEN	TIYNEN	TIYPEN	TIXNEN	TIXPEN	0x00	W

Interrupt Enable Register Settings

TIXPEN	Positive X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIXNEN	Negative X-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIYPEN	Positive Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIYNEN	Negative Y-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIZPEN	Positive Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
TIZNEN	Negative Z-axis TAP interrupt enable 0: Disabled (default) 1: Enabled. The corresponding TAP enable bit in register 0x09 must be enabled. The INTA pad will transition.
ACQ_INT_EN	Generate Interrupt 0: Disable automatic interrupt on INTA pad after each sample (default). 1: Enable automatic interrupt on INTA pad after each sample.

10.5. MODE Register (MODE)

- The MODE register controls the active operating state of the device.
- This register can be written from either operational state (STANDBY or WAKE).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0 *	OPCON [1]	OPCON [0]	0x00	W

Note * Software must always write a zero '0' to Bit 2.

MODE Register Functionality

OPCON [1:0]	00: STANDBY state (default) 01: WAKE state 10: Reserved 11: Reserved	Set Device Operational State. WAKE or STANDBY
I2C_WDT_NEG	0: I2C watchdog timer for negative SCL stalls disabled (default) 1: I2C watchdog timer for negative SCL stalls enabled	WDT for negative SCL stalls
I2C_WDT_POS	0: I2C watchdog timer for positive SCL stalls disabled (default) 1: I2C watchdog timer for positive SCL stalls enabled	WDT for positive SCL stalls
IPP	0: Interrupt pin INTA is open drain (default) and requires an external pull-up to VDD. 1: Interrupt pin INTA is push-pull. No external pull-up resistor should be installed.	Interrupt Push Pull
IAH	0: Interrupt pin INTA is active low (default) 1: Interrupt pin INTA is active high	Interrupt Active High

10.6. Sample Rate and Tap Feature Register (SRTFR)

- This register sets the sampling output data rate (ODR) for sensor.
- The upper 4 bit control functions related to tap hardware.
- The lower 4 bits control the rate, as shown in the table below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x08	SRTFR	Sample Rate and Tap Feature	TAP_LATCH	FLIP_TAPZ	FLIP_TAPY	FLIP_TAPX	RATE[3]	RATE[2]	RATE[1]	RATE[0]	0x00	W

SRTFR Register Functionality

RATE[3:0]	0000: 32 Hz (default) 0001: 16 Hz 0010: 8 Hz 0011: 4 Hz 0100: 2 Hz 0101: 1 Hz 0110: 0.5 Hz 0111: 0.25 Hz 1000: 64 Hz 1001: 128 Hz 1010: 256 Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
FLIP_TAPX	0: X positive and X negative tap are not switched (default) 1: X positive and X negative tap are switched
FLIP_TAPY	0: Y positive and Y negative tap are not switched (default) 1: Y positive and Y negative tap are switched
FLIP_TAPZ	0: Z positive and Z negative tap are not switched (default) 1: Z positive and Z negative tap are switched
TAP_LATCH	0: Multiple TAPs (of those which are enabled) are detected and latched (default) 1: First TAP detected (e.g. of those enabled) is latched, all others ignored until serviced by reading register 0x03.

10.7. Tap Control Register (TAPEN)

- This register allows the enabling and disabling of tap detection for axes and direction.
- Bit 7 disables tap detection completely.
- Bit 6, switches the feature controlled by registers 0xA, 0xB, and 0xC.
- When bit 6 is '0', the tap duration and quiet parameters are accessed in 0xA to 0xC, and when '1' the tap detection threshold is accessed.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x09	TAPEN	Tap Control Register	TAP_EN	THRDUR	TAPZNEN	TAPZPEN	TAPYNEN	TAPYPEN	TAPXNEN	TAPXPEN	0x00	W

TAPEN Register Settings

TAPXPEN	0: Disable positive tap detection on X-axis (default) 1: Enable positive tap detection on X-axis
TAPXNEN	0: Disable negative tap detection on X-axis (default) 1: Enable negative tap detection on X-axis
TAPYPEN	0: Disable positive tap detection on Y-axis (default) 1: Enable positive tap detection on Y-axis
TAPYNEN	0: Disable negative tap detection on Y-axis (default) 1: Enable negative tap detection on Y-axis
TAPZPEN	0: Disable positive tap detection on Z-axis (default) 1: Enable positive tap detection on Z-axis
TAPZNEN	0: Disable negative tap detection on Z-axis (default) 1: Enable negative tap detection on Z-axis
THRDUR	0: Registers 0xA, 0xB, 0xC point to tap duration and quiet period (default) 1: Registers 0xA, 0xB, 0xC point to tap threshold settings. See description of TTTRX, TTTRY and TTTRZ.
TAP_EN	0: All tap detection is disabled, regardless of bits [5:0] (default) 1: Tap detection is enabled, individual enables control detection (bits 5-1)

10.8. X, Y and Z Tap Duration and Threshold Registers (TTTRX,TTTRY, TTTRZ)

- These 3 registers allow control of both the tap duration settings and tap threshold settings, depending upon the setting of the THRDUR bit (bit 6) in the TAPEN register (0x09).

When THRDUR=0, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Quiet-	TAP X Duration Register	TAP_X_QUIET[3]	TAP_X_QUIET[2]	TAP_X_QUIET[1]	TAP_X_QUIET[0]	TAP_X_DUR[3]	TAP_X_DUR[2]	TAP_X_DUR[1]	TAP_X_DUR[0]	0x00	W
0x0B	Tap Y Quiet-	TAP Y Duration Register	TAP_Y_QUIET[3]	TAP_Y_QUIET[2]	TAP_Y_QUIET[1]	TAP_Y_QUIET[0]	TAP_Y_DUR[3]	TAP_Y_DUR[2]	TAP_Y_DUR[1]	TAP_Y_DUR[0]	0x00	W
0x0C	Tap Z Quiet-	TAP Z Duration Register	TAP_Z_QUIET[3]	TAP_Z_QUIET[2]	TAP_Z_QUIET[1]	TAP_Z_QUIET[0]	TAP_Z_DUR[3]	TAP_Z_DUR[2]	TAP_Z_DUR[1]	TAP_Z_DUR[0]	0x00	W

When THRDUR=1, the register meaning is as follows:

Addr	Name	Description	TTTRX[7]	TTTRX[6]	TTTRX[5]	TTTRX[4]	TTTRX[3]	TTTRX[2]	TTTRX[1]	TTTRX[0]	POR Value	R/W
0x0A	Tap X Thresh	TAP X Threshold Register	TAP_X_TH[7]	TAP_X_TH[6]	TAP_X_TH[5]	TAP_X_TH[4]	TAP_X_TH[3]	TAP_X_TH[2]	TAP_X_TH[1]	TAP_X_TH[0]	0x00	W
0x0B	Tap Y Thresh	TAP Y Threshold Register	TAP_Y_TH[7]	TAP_Y_TH[6]	TAP_Y_TH[5]	TAP_Y_TH[4]	TAP_Y_TH[3]	TAP_Y_TH[2]	TAP_Y_TH[1]	TAP_Y_TH[0]	0x00	W
0x0C	Tap Z Thresh	TAP Z Threshold Register	TAP_Z_TH[7]	TAP_Z_TH[6]	TAP_Z_TH[5]	TAP_Z_TH[4]	TAP_Z_TH[3]	TAP_Z_TH[2]	TAP_Z_TH[1]	TAP_Z_TH[0]	0x00	W

TTTRX, TTTRY and TTTRZ Register Settings

TAP_X_DUR[3:0] TAP_Y_DUR[3:0] TAP_Z_DUR[3:0]	This 4-bit value (0 to 15) sets the maximum number of samples an event must qualify as a tap before it is rejected. For example, if the value is 4, a fast acceleration event which exceeded the threshold for more than 4 consecutive samples would not trigger a tap event.
TAP_X_QUIET[3:0] TAP_Y_QUIET[3:0] TAP_Z_QUIET[3:0]	This 4-bit value (0 to 15) sets the number of samples to be ignored after successful tap detection. Detection is rearmed after the specific number of samples has passed.
TAP_X_TH[7:0] TAP_Y_TH[7:0] TAP_Z_TH[7:0]	This 8-bit unsigned value sets the minimum magnitude a snap event must reach before a tap is considered detected. Setting this parameter to a higher value will effectively reject all but the largest acceleration events as tap. Some experimentation in the final form-factor may be needed to find an appropriate setting for a particular product.

10.9. X, Y, Z-Axis Acceleration Registers(XOUT_EX, YOUT_EX & ZOUT_EX)

- The measurements from sensors for the 3-axes are available in these 3 registers.
  The most-significant bit of the value is the sign bit, and is sign extended to the higher bits.
  14-bit samples occupy bits [13:0], with bits [15:13] occupied by the sign bit.
  10-bit samples occupy bits [9:0], with bits [15:9] occupied by the sign bit.

Extended Accelerometer Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R

10.10. Output Configuration Register (OUTCFG)

- This register can be used to set the range and resolution of the accelerometer measurements.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	OUT CFG	Output Configuration Register	0*	RANGE[2]	RANGE[1]	RANGE[0]	Resv	RES[2]	RES[1]	RES[0]	0x00	W

OUTCFG Resolution and Range Select Register Settings

RES[2:0]	Accelerometer g Resolution 000: Select 6-bits for accelerometer measurements (Default) 001: Select 7-bit for accelerometer measurements 010: Select 8-bit for accelerometer measurements 011: Select 10-bit for accelerometer measurements 100: Select 12-bit for accelerometer measurements 101: Select 14-bit for accelerometer measurements 110: Reserved 111: Reserved
RANGE[2:0]	Accelerometer g Range 000: Select +/- 2g range (Default) 001: Select +/- 4g range 010: Select +/- 8g range 011: Select +/- 16g range 100: Select +/- 12g range 101: Reserved 111: Reserved

10.11. X-Axis Offset Registers (XOFFL, XOFFH)

- The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.
- When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

X-Axis Offset Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W

10.12. Y-Axis Offset Registers (YOFFL, YOFFH)

Y-Axis Offset Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W

10.13. Z-Axis Offset Registers (ZOFFL, ZOFFH)

Z-Axis Offset Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W

10.14. X-Axis Gain Registers (XGAIN)

- The gain value is an unsigned 9-bit number.
- When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

X-Axis Gain Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB Register	**XGAIN[8]**	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register MSB Register	**XGAIN[7]**	**XGAIN[6]**	**XGAIN[5]**	**XGAIN[4]**	**XGAIN[3]**	**XGAIN[2]**	**XGAIN[1]**	**XGAIN[0]**	Per chip	W

10.15. Y-Axis Gain Registers (YGAIN)

Y-Axis Gain Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB Register	**YGAIN[8]**	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x28	YGAIN	Y Gain Register MSB Register	**YGAIN[7]**	**YGAIN[6]**	**YGAIN[5]**	**YGAIN[4]**	**YGAIN[3]**	**YGAIN[2]**	**YGAIN[1]**	**YGAIN[0]**	Per chip	W

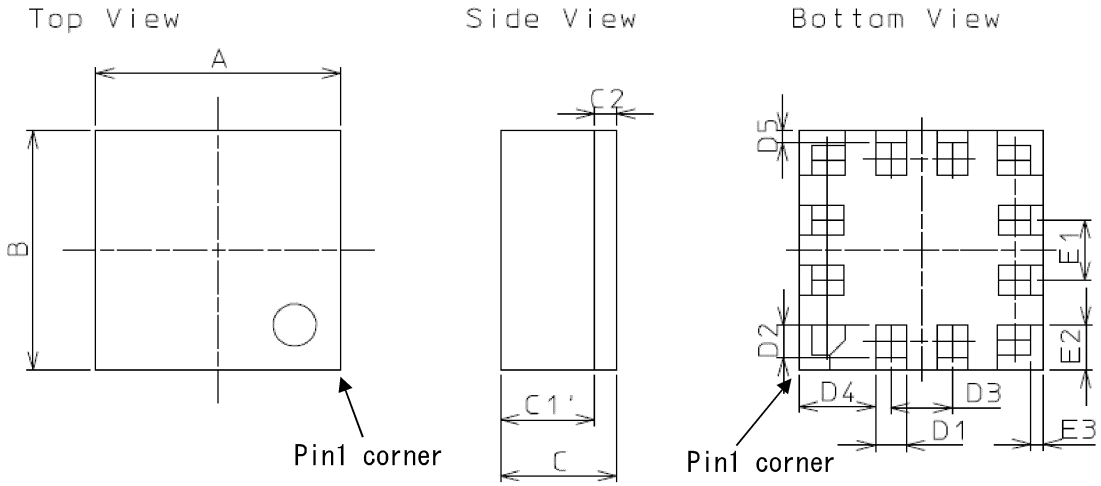
10.16. Z-Axis Gain Registers (ZGAIN)

Z-Axis Gain Registers

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB Register	**ZGAIN[8]**	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x29	ZGAIN	Z Gain Register MSB Register	**ZGAIN[7]**	**ZGAIN[6]**	**ZGAIN[5]**	**ZGAIN[4]**	**ZGAIN[3]**	**ZGAIN[2]**	**ZGAIN[1]**	**ZGAIN[0]**	Per chip	W

11. Package Dimensions

Dimension in millimeters				Dimension in millimeters			
Ref	Min.	Nom.	Max.	Ref	Min.	Nom.	Max.
A	1.90	2.00	2.10	E1	0.47	0.50	0.53
B	1.90	2.00	2.10	E2	---	0.375	---
C	0.90	0.95	1.00	E3	---	0.1	---
C1	---	0.80	---				
C2	0.12	0.15	0.18				
D1	0.22	0.25	0.28				
D2	0.24	0.27	0.30				
D3	0.47	0.50	0.53				
D4	---	0.625	---				
D5	---	0.1	---				



12. Asking that exports this product

1. For the export of products which are controlled items subject to foreign and domestic export laws and regulations, you must obtain approval and/or follow the formalities of such laws and regulations.

2. Products must not be used for military and/or antisocial purposes such as terrorism, and shall not be supplied to any party intending to use the products for such

3. application to equipment and devices which are sold to end-users in the market, such as AV (audio visual) equipment, home electric equipment, office and commercial electronic equipment, information and communication equipment or amusement equipment. The products are not intended for use in, and must not be used for, any application of nuclear equipment, driving control equipment for aerospace or any other unauthorized use.
   With the exception of the above mentioned banned applications, for applications involving high levels of safety and liability such as medical equipment, burglar alarm equipment, disaster prevention equipment and undersea equipment, please contact an Alps sales representative and/or evaluate the total system on the applicability. Also, implement a fail-safe design, protection circuit, redundant circuit, malfunction protection and/or fire protection into the complete system for safety and reliability of the total system.

4. Before using products which were not specifically designed for use in automotive applications, please contact an Alps sales representative.

13. History of revision

Revision	Date	Page	Note
1.0	29.Sep. 2014		First edition
1.1	04.Nov. 2014	10	Revised measurement range, Zero-g offset and added note of Measurement Sensitivity
1.2	05.Dec. 2014	12	Added Output Data Rate for Acceleration Sensor
1.3	20.Feb. 2015		Change the "Confidential" Mark
1.4	06.May. 2016	7, 9	Pullup Register 3.3 -> 4.7 [kohm] , bug fixed
		18	Add Read Margin in normal mode of mag sensor
		41	Fixed typo RES[2:0]
1.5	13.Sep. 2016	20	Fixed OPCON[1:0] value of stand-by mode