Hardware User Guide

Zipcores FMC-SDI Mezzanine Card

ZIP-FMC-SDI Rev. B
September 2024

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Overview

Introduction

The Zipcores FMC-SDI Mezzanine card is a dual-channel SDI video-signal transceiver. The two SDI inputs are fully independent and are capable of de-serializing all standard SMPTE serial video formats up to 2.97 Gbps. Likewise, the two SDI outputs are also fully independent and support all the standard SMPTE formats up to 2.97 Gbps.

Example standards include: 3G-SDI (SMPTE 424M), HD-SDI (SMPTE 292M), ED-SDI (SMPTE 344M), SD-SDI (SMPTE 259M) and also DVB-ASI stream. The card conforms to the ANSI/VITA 57.1 FMC™ mezzanine specification, allowing connection to a wide range of base-boards and FMC-compliant systems. Examples include development boards from AMD/Xilinx®, Intel/Altera®, Avnet®, Digilent® and Microchip®. For evaluation boards with two or more FMC connectors then the FMC-SDI card may easily be scaled-up to provide 4 or more SDI video input and output channels.

One key advantage of the FMC-SDI card is the fact that it uses a simple LVDS interface with the base board or host system. This means that the card is suitable for a wide range of FPGA and SoC devices that don't feature high-speed serial transceivers. Examples include the lower-cost Zynq-7000 SoCs and Spartan-7 FPGAs from AMD/Xilinx® and the low-cost, low-power Cyclone 10 series from Intel/Altera®. In addition, the card features adaptive cable-equalization to allow long cable lengths of over 30 meters at 3G-SDI speeds. Finally, the card also performs full recovery of the video pixel clock. This makes the card ideal for video processing, switching and pass-through applications without the need for a video frame buffer or external clock synchronization circuitry. Figures (1) and (2) show the general board layout and the distribution of main board components.

Board layout

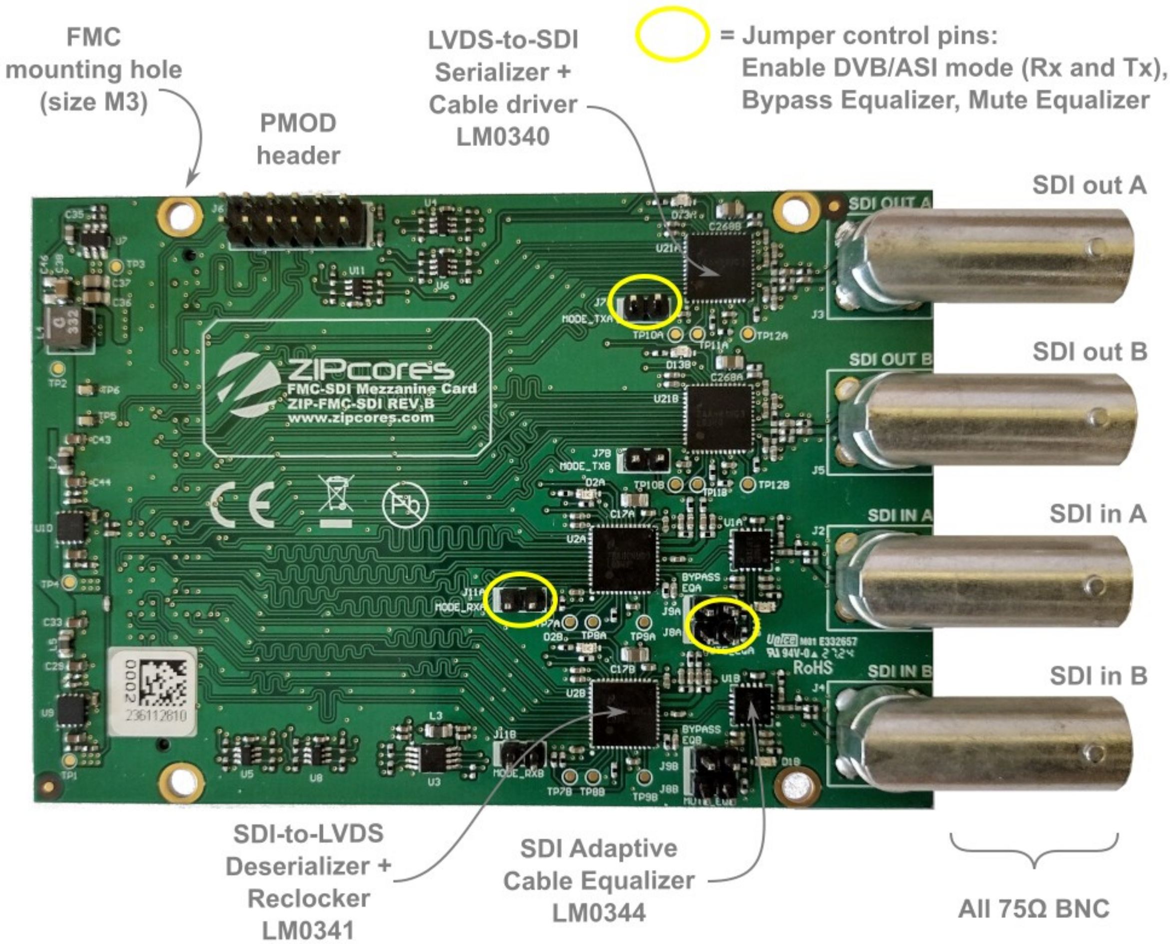

Figure 1: ZIP-FMC-SDI Rev.B board (top view)

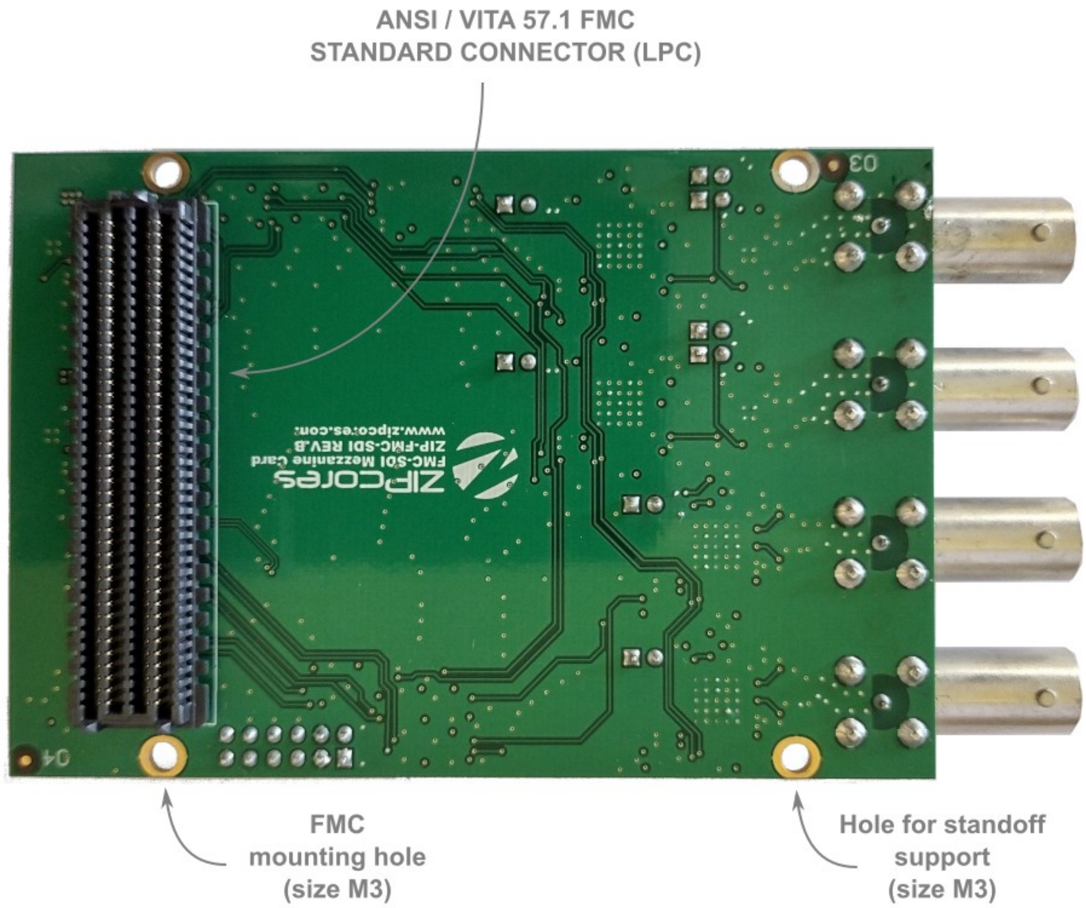

Figure 2: ZIP-FMC-SDI Rev.B board (bottom view)

Key features

- 2 x SDI video inputs (75Ω nominal)
- 2 x SDI video outputs (75Ω nominal)
- Standard BNC (right angle) female connectors x 4
- Standard ANSI/VITA 57.1 FMC™ LPC connector
- Also compatible with FMC-HPC and FMC+
- Support for 3G-SDI, HD-SDI, ED-SDI, SD-SDI and DVB-ASI
- SMPTE 344M, SMPTE 259M, SMPTE 292M, SMPTE 424M
- Support for 30m coaxial cable lengths @ 3G-SDI rates
- 2 x Adaptive cable equalizers TI® (LMH0344)
- 2 x SDI-to-LVDS de-serializer / re-clockers TI® (LMH0341)
- 2 x LVDS-to-SDI serializer / drivers TI® (LMH0340)
- SDI input and output channels fully independent
- Full pixel clock recovery on both SDI input channels
- Carrier detect and video clock locked indicator LEDs
- Manual jumper settings for bypass, mute and DVB/ASI mode
- 5 x pairs of LVDS data and 1 x LVDS clock (each channel)
- Programmable H/W resets (each channel)
- Independent SDI video lock inputs
- Main power drawn from the 12V pin on the FMC connector
- Compatible with all FMC VADJ settings up to 2.5V (max)
- 2 x general-purpose PMOD™ headers for debug and GPIO
- 2 x M3 mounting holes for securing the FMC connector
- 2 x M3 mounting holes for supporting standoff 'legs'
- Compatible with a wide range of FMC base-boards

Block diagram

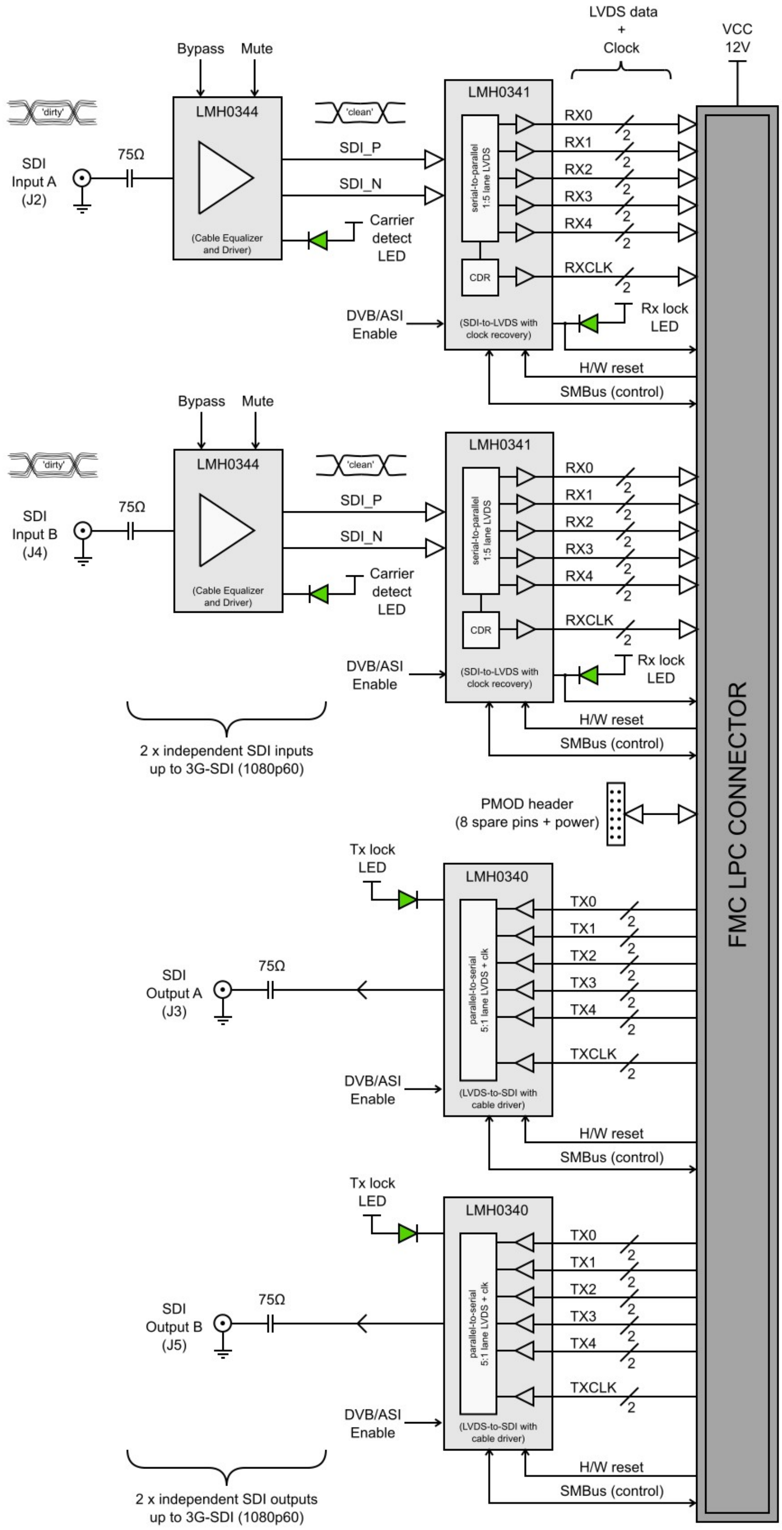

Figure 3: Block diagram of the main functions showing connectivity with the FMC (LPC) connector

Detailed description

SDI Adaptive cable equalizers

The SDI inputs to the mezzanine card are standard SMPTE signals with a maximum data rate of 2.97 Gbps and a minimum rate of 125 Mbps. The input connectors are 75Ω female BNC. On entering the card, the input signals feed into a pair of adaptive cable equalizer ICs, part number LMH0344 from Texas Instruments. The equalizer ICs perform a number of operations including: filtering, DC level correction and amplification. The end result is a clean differential output signal with improved SNR that is then passed to the SDI de-serialization stages. The equalizer ICs also feature a carrier detect signal that is connected to a green LED indicator. The LED will light when a valid SMPTE signal is detected at the SDI inputs.

The FMC-SDI card also features a pair of jumpers on the board which operate the mute and bypass functions of the equalizers. When mute is asserted then the SDI outputs are disabled. When bypass is asserted then the equalizer function is bypassed and the SDI signals pass straight through. If a particular input is not used then it is recommended that the input be held in the mute state in order to save power.

SDI De-serializers with LVDS interface

After signal clean-up and DC restoration the differential SDI signals pass into a pair of de-serializer ICs, part number LMH0341 from Texas Instruments. Both channels A and B are completely independent and are served by a separate de-serializer component. As such, it is possible to receive a different format SMTPE stream on either input if necessary. For instance, one channel running HD-SDI and the other 3G-SDI.

The interface with the FMC connector is a standard LVDS interface with 5 data lanes for the 10-bit SMPTE data and 1 clock lane for the recovered pixel clock. The 100Ω LVDS termination must be implemented in the receiving device. For example, this is easily achieved in AMD/Xilinx FPGAs with the I/O property 'DIFF_TERM' set to TRUE in the design constraints file.

Note that by default, the recovered LVDS clock (RXCLK) runs at 2 x the pixel clock rate. So for instance, if the video mode is HD1080p60 (SMPTE 424M), then the RXCLK will be running at 297 MHz. This is double the pixel clock frequency of 148.5 MHz for this mode of operation.

Figure (4) on the following page shows an (annotated) excerpt from the LMH0341 datasheet that gives more detailed timing information.

SDI Serializers with LVDS interface

The SDI serializer ICs perform the reciprocal operation to the de-serializers. The LVDS interfaces and clocking are identical save for the signal direction. As with the de-serializers, both channels A and B are completely independent and are served by a separate component, part number LMH0340 from Texas Instruments. The SDI outputs feed into 75Ω female BNC connectors.

Note that the LVDS timing waveforms are exactly the same as for the de-serializer components described in Figure 4. The LVDS outputs and LVDS clock are supplied via the FMC connector on the host board. For a simple pass-through of the SDI input to the SDI output then the LVDS data and clock of the de-serializer may be connected directly to the LVDS data and clock of the serializer.

Note on H/W reset signals

It is recommended that the SDI components be held in the reset state while the host board is powering up. The resets are all active low. Once the system is stable then the H/W reset into the ICs may be asserted high to begin normal operation.

Furthermore, in applications where one or more of the SDI inputs or outputs are not used, then the user may choose to maintain the corresponding IC in the reset state in order to save power.

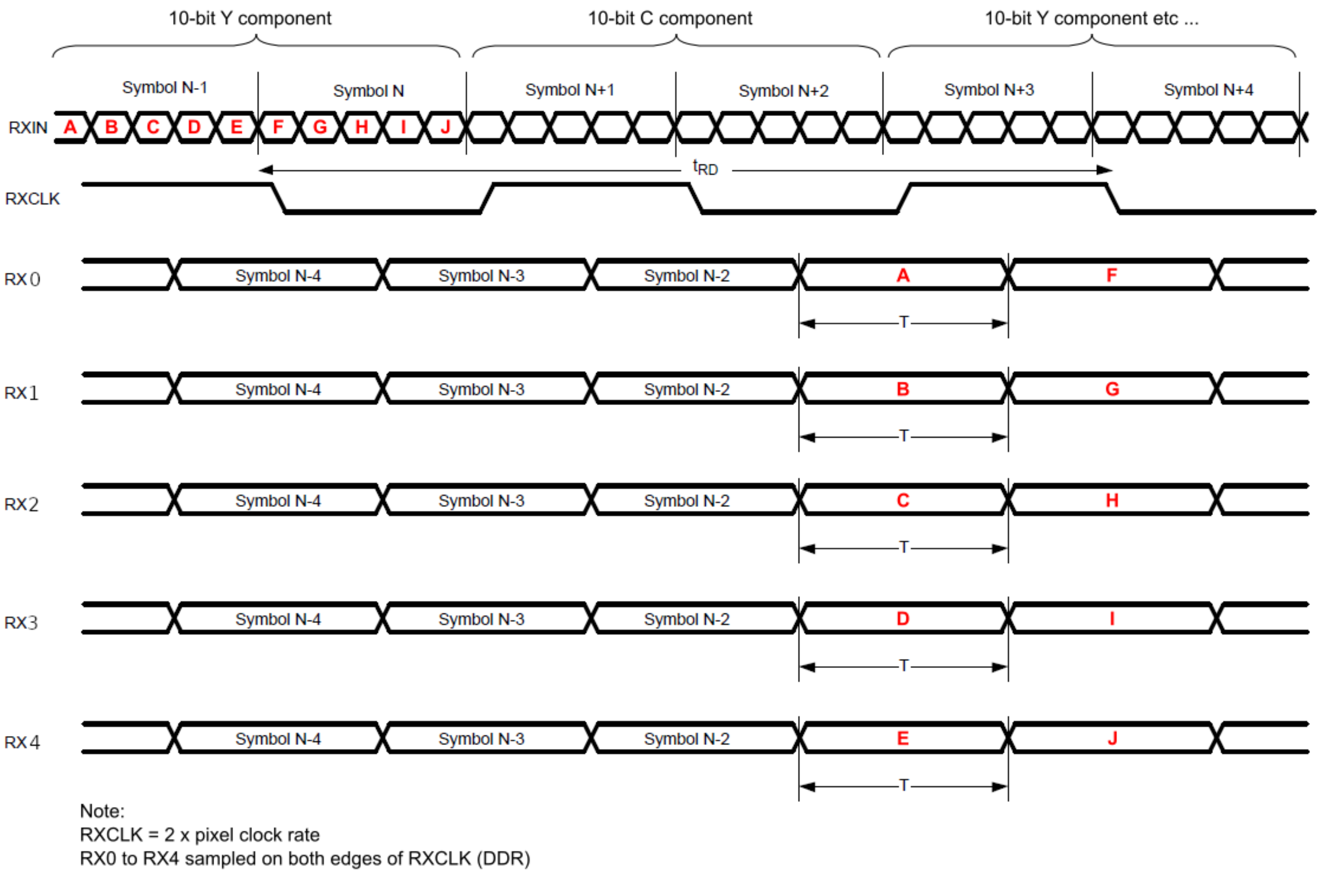

Figure 4: LVDS interface timing diagram showing relationship between the bit sampling, clock and data lanes

DVB-ASI mode

DVB-ASI mode is enabled with a jumper setting on the FMC card. There is one jumper for each SDI component. When enabled, the SDI ICs are configured to process a standard DVB-ASI stream.

When the DVB-ASI mode is enabled, the 8b10b decoder/encoder are arranged such that the data appearing on LVDS lanes 0 to 3 are treated as a nibble of 8b10b data. The data bit on lane 4 is used to control the idle character which is normally the K28.5 symbol by default.

For more detailed information regarding the DVB-ASI mode of operation then please refer to the LMH0341 and LMH0340 datasheets.

Note on data sampling and the SMPTE video codec

Normally the LVDS input data will be captured in the host system using the input DDR registers or ISERDES components that are available in the FPGA or SoC on the base board. In addition, there are PLL or clock management resources on the FPGA that may be used to generate the pixel clock from the RXCLK. Data sampling must be done in accordance with the timing described in Figure (4) above.

The end result after data capture is a parallel 20-bit stream that contains the raw SMPTE video data in YCbCr 4:2:2 format. This 20-bit stream then requires descrambling, framing and decoding inside the FPGA logic in order to recover the original standard SMPTE video signal. This will normally be in a format such as SMPTE 296M (HD720p) or SMPTE 274M (HD1080p) depending the SDI standard used.

Similarly, for the generation of the LVDS output data, most FPGAs provide output DDR registers or OSERDES components which may be used to convert the 20-bit SMPTE stream to LVDS output signals.

To help with project development, Zipcores provides a complete set of demo source files that perform the LVDS data capture, decoding and encoding functions in order to process a standard SMPTE video stream. These demo files are provided for the AMD/Xilinx 7-series devices. In addition, other devices may be supported on request. Texas Instruments also have free evaluation IP Cores for the video decoding and encoding functions. For more information, please refer to Appendices D and E that describe the application demo in more detail.

General purpose PMOD™ header

The board features a 12-pin male header (J6) that conforms to the PMOD standard for a general purpose bi-directional GPIO interface. The PMOD pins are connected to some of the spare pins on the FMC connector and are useful for general debug and additional board connectivity.

Note that the VCC pin is connected to the VADJ voltage on the FMC connector which is a slight deviation from the normal PMOD specification (normally 3.3V fixed). The VADJ voltage is adjustable according to the setting on the base-board. When using the PMOD connector, please ensure that the voltage does not exceed VADJ (maximum). If it does then there is a risk of damage to the host system. Figure (5) below describes the pinout of the PMOD header.

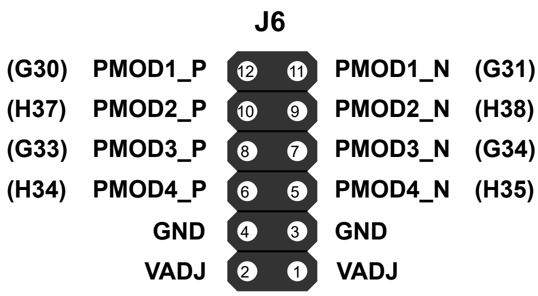

Figure 5: General purpose PMOD header
(Pins in brackets are the FMC connector pin numbers)

ANSI/VITA 57.1 FMC™ connector

The mezzanine card uses a standard ANSI/VITA 57.1 FMC connector. The pinouts of the connector are configured with the Low-Pin-Count (LPC) option occupying sub-sets of rows D/C and G/H. Although the pinouts are designed for the LPC connector, the mezzanine card is also compatible with the High-Pin-Count connector (HPC) and the latest generation FMC+ connectors featured on some of the higher-end evaluation boards. A detailed specification of the FMC connector may be found on the Samtec® website here:

https://www.samtec.com/standards/vita/fmc

The FMC standard connector is used in a wide selection of FPGA development boards from vendors such as AMD/Xilinx®, Intel/Altera®, Avnet® and Digilent®. AMD in particular have adopted the FMC standard in all their FPGA and SoC development boards. Appendix A gives some examples of FMC compatible base-boards. More information can be found on the AMD website just here:

https://www.xilinx.com/products/boards-and-kits/fmc-cards.html

A full description of the FMC connector pinout with the mezzanine card is given in Appendix B.

Board power supplies

The main power on the board is derived from the fixed 12V supply on the FMC connector corresponding to pins C35 and C37. A series of linear regulators are used to generate the 3.3V and 2.5V supplies used by the board components.

The adjustable voltage setting (VADJ) is used for the FMC differential LVDS pins and other control pins on the card. The VADJ supply corresponds to pins G29 and H40 on the FMC connector. Most base-boards have a jumper setting that permits the VADJ voltage to be set to 1.8V or 2.5V. Setting VADJ to 2.5V is recommended to achieve the best possible noise immunity and performance of the LVDS I/O. However, a 1.8V setting will also work correctly and has been tested on AMD/Xilinx devboards with 7-series FPGAs and Zynq SoCs.

During normal un-muted operation with both the SDI input and output channels being driven the *maximum* power dissipation of the mezzanine card is ~3W with a peak current draw of 250 mA.

Appendices

Appendix A: Examples of supported FMC base-boards

ZYNQ-BASED SYSTEMS

Base-board name	***No. of FMCs***	***VADJ options***
Zynq-7000 SoC ZC702 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc702-g.html	2 x LPC	2.5V fixed
Zynq-7000 SoC ZC706 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html	1 x LPC + 1 x HPC	2.5V fixed
Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html	2 x HPC	1.2V, 1.5V, 1.8V
Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit www.xilinx.com/products/boards-and-kits/zcu104.html	1 x LPC	1.2V, 1.5V, 1.8V
Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit www.xilinx.com/products/boards-and-kits/zcu106.html	2 x HPC	1.2V, 1.5V, 1.8V

GENERAL FPGA-BASED SYSTEMS

Base-board name	***No. of FMCs***	***VADJ options***
Spartan-7 FPGA SP701 Evaluation Kit www.xilinx.com/products/boards-and-kits/sp701.html	1 x LPC	2.5V fixed
Artix-7 FPGA AC701 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html	1 x HPC	1.8V, 2.5V, 3.3V
Kintex-7 FPGA KC705 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-k7-kc705-g.html	1 x LPC + 1 x HPC	1.8V, 2.5V, 3.3V
Virtex-7 FPGA VC707 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html	2 x HPC	1.2V, 1.5V, 1.8V
Virtex-7 FPGA VC709 Connectivity Kit www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html	1 x HPC	1.8V fixed

ULTRASCALE-BASED SYSTEMS

Base-board name	***No. of FMCs***	***VADJ options***
Kintex UltraScale FPGA KCU105 Evaluation Kit www.xilinx.com/products/boards-and-kits/kcu105.html	1 x LPC + 1 x HPC	1.2V, 1.5V, 1.8V
Kintex UltraScale+ FPGA KCU116 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html	1 x HPC	1.8V fixed
Virtex UltraScale FPGA VCU108 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html	2 x HPC	1.2V, 1.5V, 1.8V
Virtex UltraScale+ FPGA VCU118 Evaluation Kit www.xilinx.com/products/boards-and-kits/vcu118.html	1 x HPC	1.2V, 1.5V, 1.8V

VERSAL-BASED SYSTEMS

Base-board name	***No. of FMCs***	***VADJ options***
Versal Prime Series VMK180 Evaluation Kit www.xilinx.com/products/boards-and-kits/vmk180.html	2 x FMC+	1.0V, 1.2V, 1.5V
Versal Premium Series VPK180 Evaluation Kit www.xilinx.com/products/boards-and-kits/vpk180.html	1 x FMC+	1.0V, 1.2V, 1.5V
Versal AI Core Series VCK190 Evaluation Kit www.xilinx.com/products/boards-and-kits/vck190.html	2 x FMC+	1.0V, 1.2V, 1.5V

[Note: This is not an exclusive list and only lists AMD products. Almost every evaluation board that features an FMC connector is compatible with the Zipcores FMC-SDI card. If in doubt, please contact Zipcores customer support for more information].

Appendix B: FMC connector pinout (rows H/G)

FMC pin	***VITA net name***	***FMC-SDI net name***	***FMC pin***	***VITA net name***	***FMC-SDI net name***
H1	VREF_A_M2C	N/C	G1	GND	GND
H2	PRSNT_M2C_L	N/C	G2	CLK1_M2C_P	RXC_CHA_P
H3	GND	GND	G3	CLK1_M2C_N	RXC_CHA_N
H4	CLK0_M2C_P	RXC_CHB_P	G4	GND	GND
H5	CLK0_M2C_N	RXC_CHB_N	G5	GND	GND
H6	GND	GND	G6	LA00_P_CC	FMC_SMB_SDA
H7	LA02_P	FMC_SMB_CS_RXB	G7	LA00_N_CC	FMC_SMB_SCK
H8	LA02_N	FMC_SMB_CS_RXA	G8	GND	GND
H9	GND	GND	G9	LA03_P	FMC_RSTN_RXA
H10	LA04_P	RX1_CHB_P	G10	LA03_N	FMC_RSTN_RXB
H11	LA04_N	RX1_CHB_N	G11	GND	GND
H12	GND	GND	G12	LA08_P	RX4_CHA_P
H13	LA07_P	RX0_CHB_P	G13	LA08_N	RX4_CHA_N
H14	LA07_N	RX0_CHB_N	G14	GND	GND
H15	GND	GND	G15	LA12_P	RX2_CHA_P
H16	LA11_P	RX0_CHA_P	G16	LA12_N	RX2_CHA_N
H17	LA11_N	RX0_CHA_N	G17	GND	GND
H18	GND	GND	G18	LA16_P	TX4_CHB_P
H19	LA15_P	TX2_CHB_P	G19	LA16_N	TX4_CHB_N
H20	LA15_N	TX2_CHB_N	G20	GND	GND
H21	GND	GND	G21	LA20_P	TX0_CHB_P
H22	LA19_P	TXC_CHB_P	G22	LA20_N	TX0_CHB_N
H23	LA19_N	TXC_CHB_N	G23	GND	GND
H24	GND	GND	G24	LA22_P	TX4_CHA_P
H25	LA21_P	TX3_CHA_P	G25	LA22_N	TX4_CHA_N
H26	LA21_N	TX3_CHA_N	G26	GND	GND
H27	GND	GND	G27	LA25_P	TX1_CHA_P
H28	LA24_P	FMC_SMB_CS_TXB	G28	LA25_N	TX1_CHA_N
H29	LA24_N	FMC_SMB_CS_TXA	G29	GND	GND
H30	GND	GND	G30	LA29_P	FMC_PMOD1_P
H31	LA28_P	FMC_RSTN_TXB	G31	LA29_N	FMC_PMOD1_N
H32	LA28_N	FMC_RSTN_TXA	G32	GND	GND
H33	GND	GND	G33	LA31_P	FMC_PMOD3_P
H34	LA30_P	FMC_PMOD4_P	G34	LA31_N	FMC_PMOD3_N
H35	LA30_N	FMC_PMOD4_N	G35	GND	GND
H36	GND	GND	G36	LA33_P	FMC_LOCK_RXA
H37	LA32_P	FMC_PMOD2_P	G37	LA33_N	FMC_LOCK_RXB
H38	LA32_N	FMC_PMOD2_N	G38	GND	GND
H39	GND	GND	G39	VADJ	VADJ
H40	VADJ	VADJ	G40	GND	GND

Appendix C: FMC connector pinout (rows D/C)

FMC pin	***VITA net name***	***FMC-SDI net name***	***FMC pin***	***VITA net name***	***FMC-SDI net name***
D1	PG_C2M	N/C	C1	GND	GND
D2	GND	GND	C2	DP0_C2M_P	N/C
D3	GND	GND	C3	DP0_C2M_N	N/C
D4	GBTCLK0_M2C_P	N/C	C4	GND	GND
D5	GBTCLK0_M2C_N	N/C	C5	GND	GND
D6	GND	GND	C6	DP0_M2C_P	N/C
D7	GND	GND	C7	DP0_M2C_N	N/C
D8	LA01_P_CC	RX4_CHB_P	C8	GND	GND
D9	LA01_N_CC	RX4_CHB_N	C9	GND	GND
D10	GND	GND	C10	LA06_P	RX3_CHB_P
D11	LA05_P	RX2_CHB_P	C11	LA06_N	RX3_CHB_N
D12	LA05_N	RX2_CHB_N	C12	GND	GND
D13	GND	GND	C13	GND	GND
D14	LA09_P	RX3_CHA_P	C14	LA10_P	RX1_CHA_P
D15	LA09_N	RX3_CHA_N	C15	LA10_N	RX1_CHA_N
D16	GND	GND	C16	GND	GND
D17	LA13_P	TX3_CHB_P	C17	GND	GND
D18	LA13_N	TX3_CHB_N	C18	LA14_P	TX1_CHB_P
D19	GND	GND	C19	LA14_N	TX1_CHB_N
D20	LA17_P_CC	N/C	C20	GND	GND
D21	LA17_N_CC	N/C	C21	GND	GND
D22	GND	GND	C22	LA18_P_CC	N/C
D23	LA23_P	TX2_CHA_P	C23	LA18_N_CC	N/C
D24	LA23_N	TX2_CHA_N	C24	GND	GND
D25	GND	GND	C25	GND	GND
D26	LA26_P	TX0_CHA_P	C26	LA27_P	TXC_CHA_P
D27	LA26_N	TX0_CHA_N	C27	LA27_N	TXC_CHA_N
D28	GND	GND	C28	GND	GND
D29	TCK	N/C	C29	GND	GND
D30	TDI	N/C	C30	SCL	N/C
D31	TDO	N/C	C31	SDA	N/C
D32	3P3VAUX	N/C	C32	GND	GND
D33	TMS	N/C	C33	GND	GND
D34	TRST_L	N/C	C34	GA0	N/C
D35	GA1	N/C	C35	12P0V	12V
D36	3P3V	N/C	C36	GND	GND
D37	GND	GND	C37	12P0V	12V
D38	3P3V	N/C	C38	GND	GND
D39	GND	GND	C39	3P3V	N/C
D40	3P3V	N/C	C40	GND	GND

Appendix D: List of supporting design files

The FMC-SDI card has a number of supporting design files and documents that may be downloaded from the Zipcores website at: www.zipcores.com/downloads.html. Most of the design files are source-code files that are required for building and running the example demo as described in Appendix E. A list of these files and a brief description is given below:

Folders and important files	***Description***
docs/	Folder containing various design documents.
zip_fmc_sdi_user_guide.pdf zip_fmc_sdi_schematic.pdf zip_fmc_sdi_safety_info.pdf zip_fmc_sdi_gerber.pdf zip_fmc_sdi_bom.pdf zip_fmc_sdi_assembly.pdf	FMC-SDI hardware user guide (this document). FMC-SDI design schematics. FMC-SDI regulatory compliance and safety information. FMC-SDI gerber (summary). FMC-SDI bill of materials. FMC-SDI assembly drawings.
const/	Folder containing the physical constraints for the Vivado project.
fmc_sdi_top.xdc	Example master 'XDC' file that defines all the top-level pinouts and design constrains for the FMC-SDI card when connected to the SP701 base-board. This file may be adapted for use with all AMD/Xilinx FPGAs.
vivado/	This folder contains the Vivado project environment for the demo.
fmc_sdi_top.xpr	Vivado project setup file (double click to invoke project).
vhdl/	This folder contains the top-level VHDL source-code files for the example demo. The main top-level files are:
fmc_sdi_top.vhd fmc_sdi_top_bench.vhd	The top-level component. The top-level testbench for the VHDL simulation.
modelsim/	This folder contains the Modelsim® simulation environment in order to run a VHDL hardware simulation of the demo. You will need to obtain a copy of Mentor Graphics Modelsim in order to use these files.
fmc_sdi_top.mpf	Modelsim project setup file (double click to invoke project).
misc/	This folder contains various datasheets, schematics and design notes for the components on the FMC-SDI card.

Zipcores offers a wide range of IP Cores and custom solutions for the FMC-SDI mezzanine card. As well as AMD/Xilinx devices, we can provide IP for other FPGAs or SoCs on request. If you have a specific requirement or simply want to discuss a potential solution then please get in touch. Further details may be found by visiting our website or contacting us at: www.zipcores.com/help.php.

Appendix E: Running the example demo

An example demo is provided to get started with the FMC-SDI card. The demo demonstrates the reception, decoding, encoding and re-transmission of 2 x SDI signals (channels A and B) operating at 1080p. The demo will work with either 60 or 30 Hz refresh rates corresponding to either 1080p60 or 1080p30 video modes (3G-SDI or HD-SDI). The basic video pipeline for both video input and output channels is as follows:

SDI in → LVDS Rx I/O → Descrambler/Framer → SMPTE decode → FIFO → SMPTE encode → Framer/Scrambler → LVDS Tx I/O → SDI out

In addition, the demo provides a series of sync/debug flags on the PMOD header of the FMC card. These are useful in order to verify that the video mode and refresh rate have been detected correctly. In order to run the demo, the following basic lab setup is recommended:

- SDI video signal generator capable of generating an HD-SDI or 3G-SDI signal (e.g. Questtel 1B-SDI-PTG). Example video formats could be 1080p60 or 1080p30.
- SDI monitor capable of receiving an HD-SDI or 3G-SDI signal. Alternatively use of an HDMI monitor in combination with an SDI-to-HDMI converter box (e.g. MicroConverter SDI to HDMI 3G from Blackmagic Design).
- Oscilloscope for monitoring the sync/debug flags on the PMOD headers for each channel (e.g. Tektronix MDO3014).
- Scope probes for connecting to the PMOD header.
- 2 x coaxial cables (75Ω) with BNC connectors and/or adapters.
- AMD/Xilinx (Spartan 7) SP701 evaluation board (http://zedboard.org/product/zedboard). This will be used as the base board on which the FMC-SDI Mezzanine card will be mounted. (Note: other base boards may be supported on request. Please contact us for more details).
- Spacers and screws (size M2.5) in order to secure the FMC-SDI card to the base-board and provide structural support for the card on the bench.
- AMD/Xilinx Vivado Software (rev. 2019.1 or later) together with the SP701 board definition files.
- USB cable for programming the SP701.

Connect the SDI video source to SDI input A and the SDI video sink to SDI output A. Alternatively, Connect the SDI video source to SDI input B and the SDI video sink to SDI output B. (If you have dual sources and sinks then both inputs and outputs may be connected at the same time).

Once the equipment is set up then the user should invoke the Vivado software and load the project environment 'fmc_sdi_top.xpr' which is in the 'vivado' folder as described in Appendix D above. The same directory structure should be maintained so that the links and dependencies are correctly resolved. If the project loads correctly, the initial project layout should look something like Figure 6 on the following page:

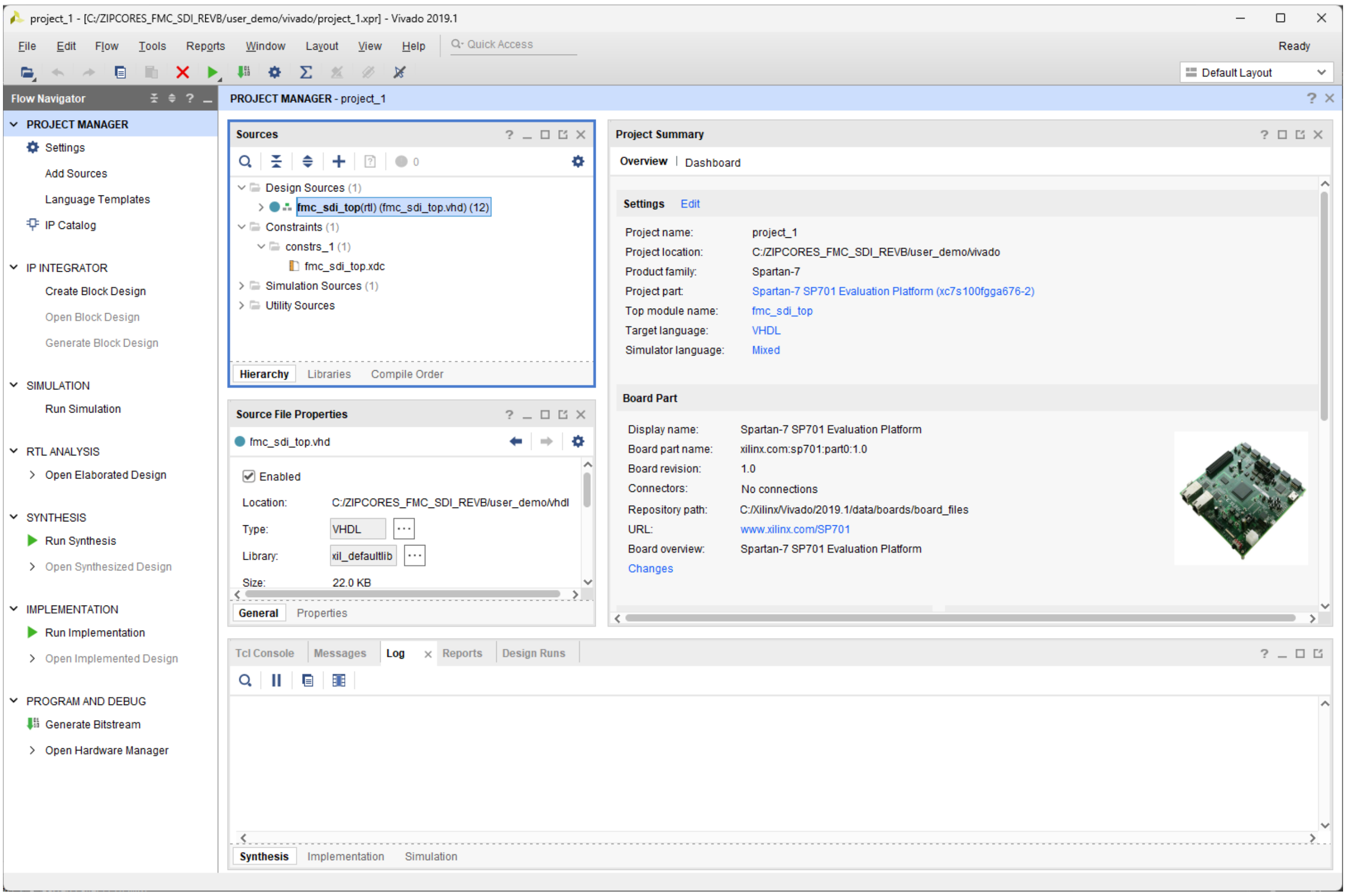

Figure 6: Initial Vivado project startup for demo

Once the project is loaded then the next step is to build the bitstream for programming the FPGA. Click on 'Generate Bitstream' in the project manager window and wait for the compile process to complete. After the bitstream is generated then open the hardware manager and program the SP701. Figure (7) below shows an example bench setup with the FMC-SDI card connected to the SDI signal generator on input A and the SDI output A connected to a monitor via an SDI-to-HDMI converter box.

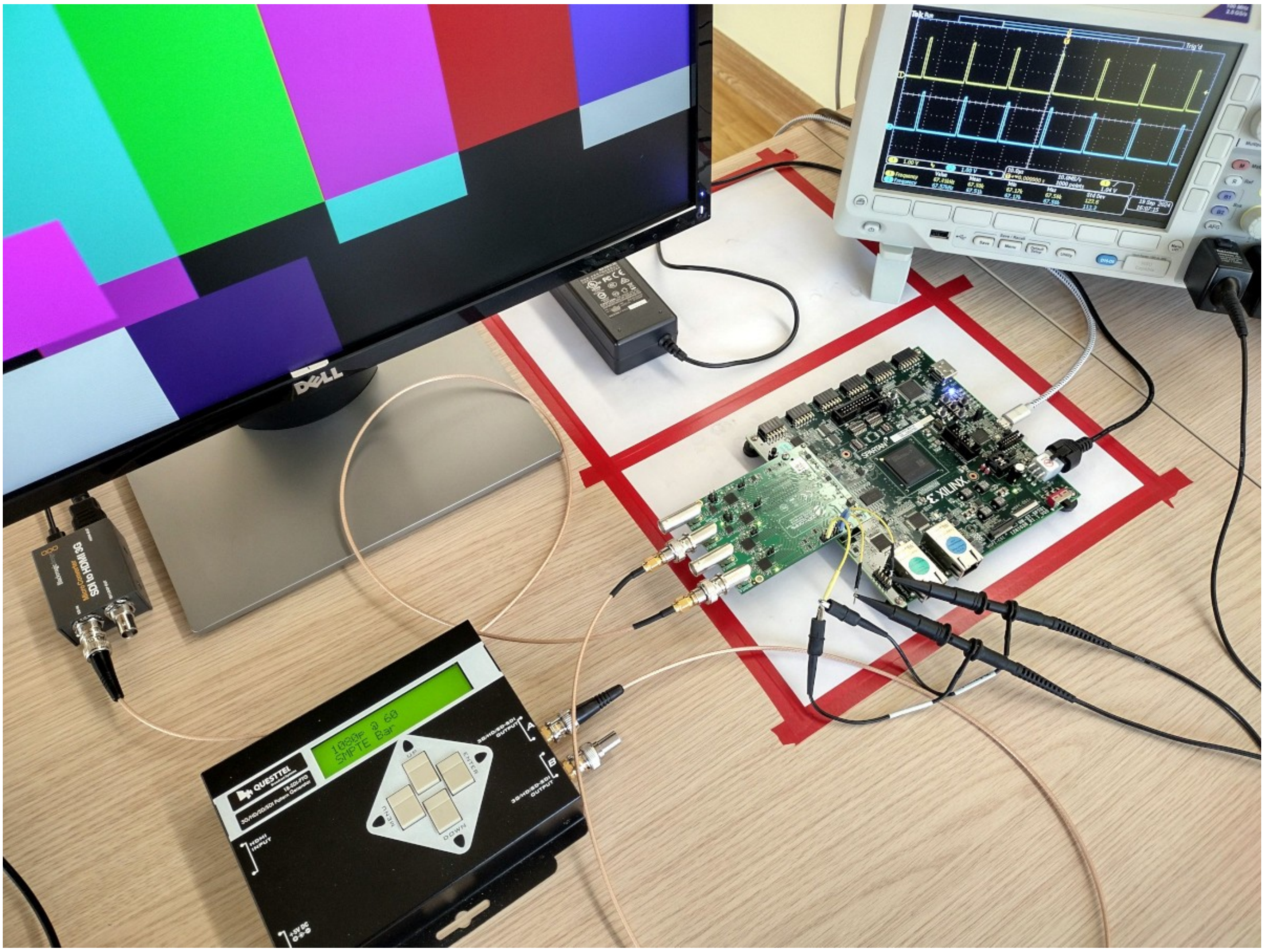

Figure 7: Bench setup showing FMC-SDI card connected to the AMD SP701 evaluation board and the scope connected to the PMOD header for debug

Note that ''CPU_RESET' push button on the SP701 board serves as the main H/W reset. If there are any issues with the SDI signal failing to lock then the H/W reset may me pressed to reset the H/W to initial conditions.

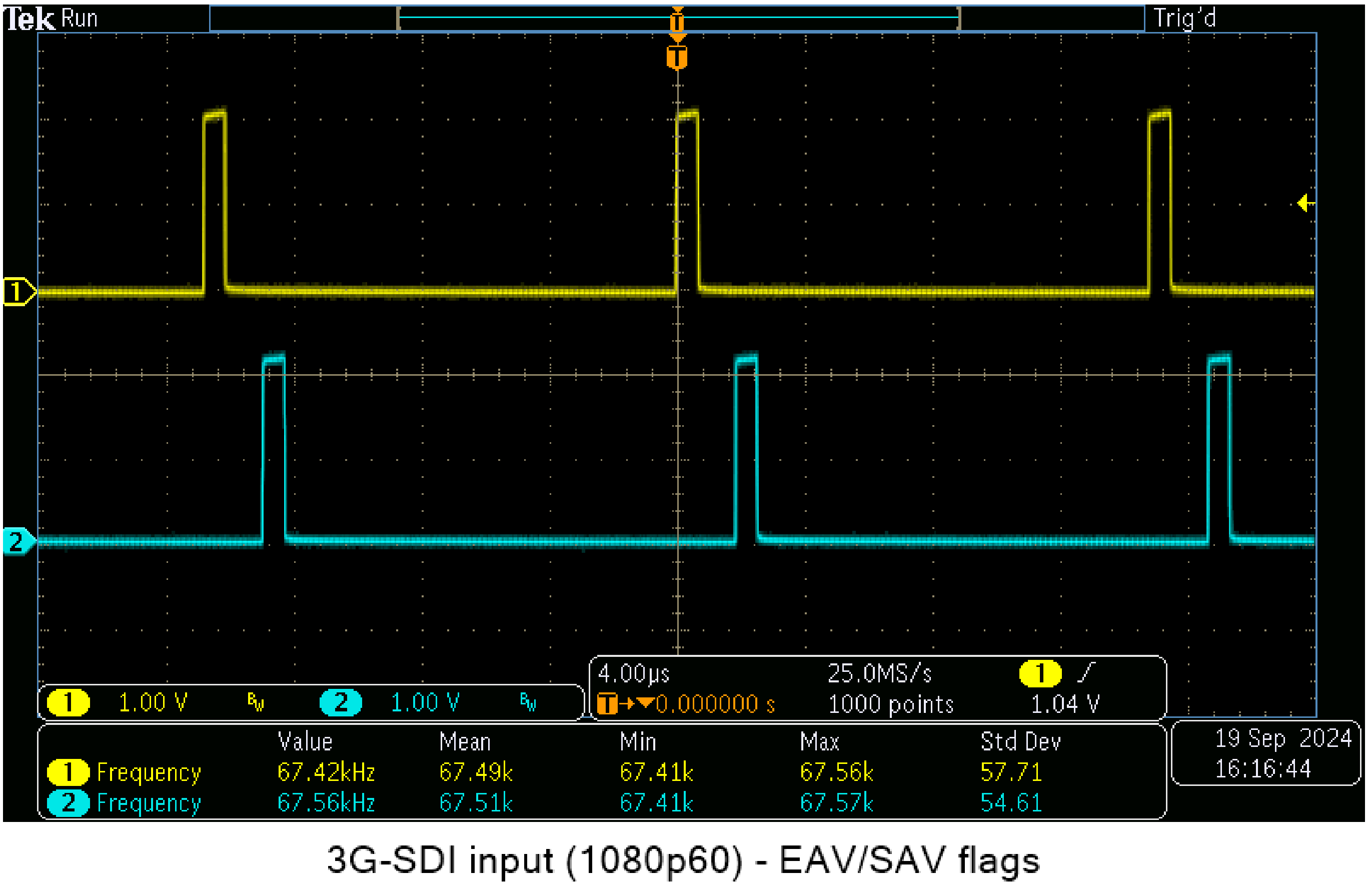

Figure 8: Scope traces on the PMOD connector showing debug flags for a 3G-SDI (HD1080p60) locked input signal

For the demo, the PMOD connector (J6) is wired as follows:

FMC_PMOD1_P - EAV flag input A
FMC_PMOD1_N - SAV flag input A
FMC_PMOD2_P - HD-SDI mode detected input A (active high)
FMC_PMOD2_N - 3G-SDI mode detected input A (active high)

FMC_PMOD3_P - EAV flag input B
FMC_PMOD3_N - SAV flag input B
FMC_PMOD4_P - HD-SDI mode detected input B (active high)
FMC_PMOD4_N - 3G-SDI mode detected input B (active high)