swissbit®

Product Data Sheet

Industrial microSD Memory Card

S-60ou Series

UHS-I Interface, SLC

Standard and Extended Temperature Grade

Date: September 18, 2024
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Made in Germany

Contents

S-600u Series – Industrial microSD Memory Card, SLC 512 MBytes up to 2 GBytes

1. Product Summary

- **Capacities:** 512 MBytes, 1 GBytes, 2 GBytes
- **Form Factor:** Standard microSD Memory Card form factor – 15.0 x 11.0 x 0.7mm (1.0mm)
- **Compliance[1]:** Fully compliant with SD Memory Card specification 3.0
    - Speed class 10 and U1 according SD3.0 specification
    - Fully compatible with UHS-I/SDR104 hosts
    - SD2.0 SDHC backward compliant, default speed and high speed mode
    - FAT16
- **Environmental:** RoHS / REACH Compliant
- **Compatibility:** Support SD SPI mode
- **Performance (max. capacity):**
    - SD Default speed
    - SD High speed
    - SD UHS-I
    - Read performance: sequential read up to 35 MBytes/s
    - Write performance: sequential write up to 21 MBytes/s
- **Operating Temperature Range:**
    - Extended: -25 °C to 85 °C
    - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 100 °C
- **Operating Voltage:** 2.7 ... 3.6V (Low-power CMOS technology)
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Reliability:**
    - Mean Time Between Failure (MTBF): > 3,000,000 hours
    - Number of insertions: up to 20,000
- **Shock/Vibration:** 1,500 *g* /50 *g*
- **Electromagnetic Compatibility Test:** Radiated Emission; Radiated Immunity; Electrostatic Discharge

[1] The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.

2. Product Features

- Optimized FW algorithms especially for read/write access, highest random write performance and best endurance with long data retention
    - Designed for usage in applications with highest requirements regarding reliability like data logging, POS/POI, Medical and other demanding use-cases
    - Especially suitable for intensive read/write operations
    - Advanced power-off reliability technology
    - Wear Leveling technology
      Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed
    - The S-600u series is optimized for high read/write traffic for demanding industrial applications
    - Read Disturb Management
      The read commands are monitored and the content is refreshed when critical levels have occurred
    - Data Care Management
      The interruptible background process maintain the user data for Read Disturb effects or Retention degradation due to high temperature effects
    - Near miss ECC technology
      Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes the ECC margin level and refresh data if necessary
    - Diagnostic features with Life Time Monitoring tool support
- High reliability
    - SLC Flash
    - The product is optimized for long life cycle that requires good data retention because of high temperature mission profile.
    - Number of card insertions/removals 20,000
    - Industrial Temperature range -40° up to 85°C inclusive full cross temperature support[2]
    - SIP (System In Package) process for extreme dust, water and ESD proof
- Controlled "Locked" BOM & PCN process
- Manufactured in a TS 16949 certified factory
- Customized options like CID registers, CPRM keys, firmware incl. settings and marking on request
- In-field firmware update[3]
- Swissbit Device Manager (SBDM) Tool and SDK for SBDM (on request)

[2] Cross temp. stability of 125 Kelvin: Feasible temperature difference between write/read of same data, e.g. write @-40°C, read @85°C.
[3] The support of In-Field FW update capabilities on host systems is recommended.

3. Ordering Information

Table 1: Standard Product List

Capacity	Extended Temperature	Industrial Temperature
	Part Number	Part Number
512 MBytes	SFSD0512NgAS1T0-E-xx-2y1-STD	SFSD0512NgAS1T0-I-xx-2y1-STD
1 GBytes	SFSD1024NgAS1T0-E-xx-2y1-STD	SFSD1024NgAS1T0-I-xx-2y1-STD
2 GBytes	SFSD2048NgAS1T0-E-xx-2y1-STD	SFSD2048NgAS1T0-I-xx-2y1-STD

g = product generation; xx = flash configuration; y = firmware revision

Table 2: Available Part Numbers

Firmware 2		
Capacity	Extended Temperature	Industrial Temperature
	Part Number	Part Number
512 MBytes	SFSD0512N1AS1T0-E-ME-221-STD	SFSD0512N1AS1T0-I-ME-221-STD
1 GBytes	SFSD1024N1AS1T0-E-DF-221-STD	SFSD1024N1AS1T0-I-DF-221-STD
2 GBytes	SFSD2048N1AS1T0-E-QG-221-STD	SFSD2048N1AS1T0-I-QG-221-STD

Firmware 3		
Capacity	Extended Temperature	Industrial Temperature
	Part Number	Part Number
512 MBytes	SFSD0512N1AS1T0-E-ME-231-STD	SFSD0512N1AS1T0-I-ME-231-STD
1 GBytes	SFSD1024N1AS1T0-E-DF-231-STD	SFSD1024N1AS1T0-I-DF-231-STD
2 GBytes	SFSD2048N1AS1T0-E-QG-231-STD	SFSD2048N1AS1T0-I-QG-231-STD

4. Product Description

The microSD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- SD and UHS-I card modes
- SPI mode

The microSD Memory Card also supports SD Default and High Speed mode with up to 50MHz clock frequency as well as UHS-I modes.
The cards are compliant with

- SD Memory card Specification Part 1, Physical layer Specification V3.01
- SD Memory card Specification Part 2, File System Specification V3.00
- SD Memory card Specification Part 3, Security Specification V3.00
- MICRO SD Memory Card Addendum V4.20

Simplified specifications are available at https://www.sdcard.org/

The Card has an internal intelligent controller which manages interface protocols, data storage and retrieval as well as hardware BCH Error Correction Code (ECC), defect handling, diagnostics and clock control.
The advanced wear leveling mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to detect and correct up to 24 defect bits per 1kByte.
The controller performs control read operations and checks the consistence of the data. If an error of some bits is detected, the card refreshes all data in the flash cells to prevent data retention problems.

The card has a power-loss management feature to prevent data corruption after power-down.
The cards are RoHS compliant and lead-free.

4.1 Performance Specifications

Table 3: Read/Write Performance

System Performance	typ[4]			Unit
	512MB	1GB	2GB	
Sequential Read	33	35	35	MB/s
Sequential Write	16	20	21	
Random Read 4k	850	850	850	IOPS
Random Write 4k	1000	1100	1200	
Speed class	10 / U3			-

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

The recommended operating conditions for the S-600u microSD Memory Card are provided in Table 4 below.

Table 4: SD Memory Card recommended operation conditions

Parameter	Value[5]
Extended Operating Temperature	-25 °C to 85 °C
Industrial Operating Temperature	-40 °C to 85 °C

[4] Sustained Speed measured with USB3.0-SD Memory Card reader in UHS mode. It depends on burst speed, flash number, and file size.
[5] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected.

4.2.2 Recommended Storage Conditions

The recommended storage conditions are listed below in Table 5.

Table 5: SD Memory Card recommended Storage Conditions

Parameter	Value[6]
Extended Storage Temperature	-25 °C to 100 °C
Industrial Storage Temperature	-40 °C to 100 °C

4.2.3 Humidity & EMC

The humidity and EMC conditions are listed below in Table 6.

Table 6: Humidity & EMC

Parameter	Value
Humidity (Non-Condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

4.2.4 Environmental Conditions

Table 7: Environmental Conditions

Parameter	Value
UV light exposure	UV: 254nm, 15Ws/cm2 according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140KeV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each non-operating, JESD22B110/B104 Condition B
Vibration	50G, p-p, 20..2000Hz, sweep xyz-axis, 4 pulses each, non-operating, MIL-STD-883 M2007.3 Condition B

[6] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected.

4.3 Regulatory Compliance

The S-600u devices comply with the regulations / standards listed in Table 8.

Table 8: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE – 2014/30/EU FCC – 47 CFR Part 15 UKCA – S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

4.4 Physical Dimensions

The physical dimensions of the S-600u devices are listed in the following table.

Table 9: Measured Physical Dimensions

Physical Dimensions		Unit
Length	15.0±0.1	mm
Width	11.0±0.1	
Thickness (Max)	0.7 (1.0)±0.1	
Weight (Typ)	0.4	g

4.5 Reliability

Table 10: Reliability

Parameter	Value[7]
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (100k PE cycles) @ 40°C	1 year

[7] After every 50 power on cycles the card reads the whole flash and performs a data refresh if necessary. So, the data retention can be much longer in most use cases.

4.6 Endurance

Endurance represented as TeraBytes Written (TBW) is provided in the following Table 11:

Table 11: Endurance[8, 9]

Drive Capacity	TeraBytes Written (TBW) @ Seq. Write 1MB Operation	TeraBytes Written (TBW) @ Random Write 128kB Operation	TeraBytes Written (TBW) @ Random Write 4kB Operation
512 MBytes	53	21	4,3
1 GByte	106	31	7,1
2 GBytes	212	62	13,9

5. User density specification

The S-600u drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown below in Table 12.

Table 12: SD Memory Card capacity specification

Raw Capacity	Total LBA	User Addressable Bytes
512 MBytes	967,680	495,452,160
1 GBytes	1,953,792	1,000,341,504
2 GBytes	3,938,304	2,016,411,648

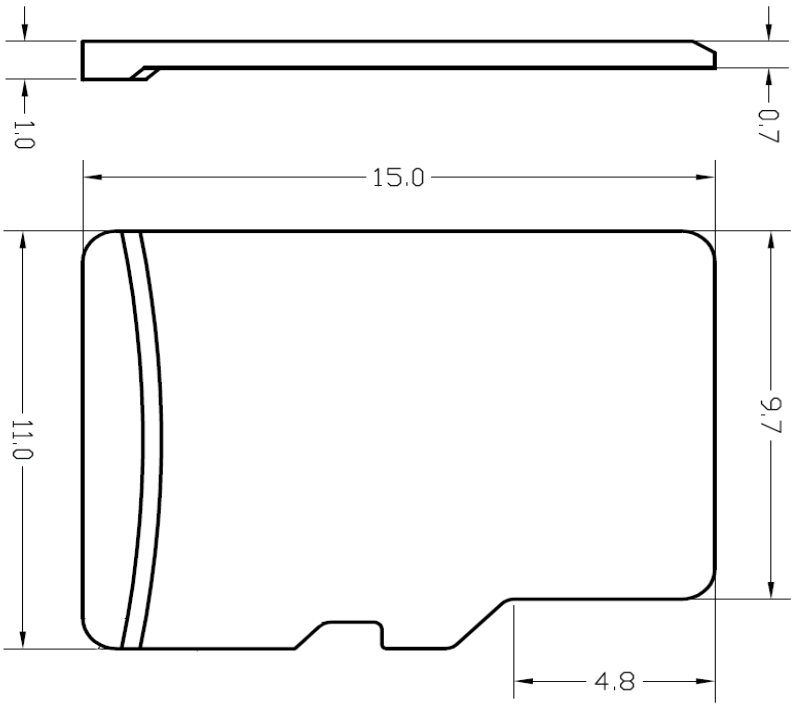
[8] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

[9] Sequential write 1MB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

6. Card physical

The microSD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1: Simplified mechanical dimensions microSD Memory Card



The dimensions and tolerances are according to the SD specification.

7. Electrical interface

7.1 Electrical description

Figure 2: microSD Memory Card shape and interface (Bottom view)

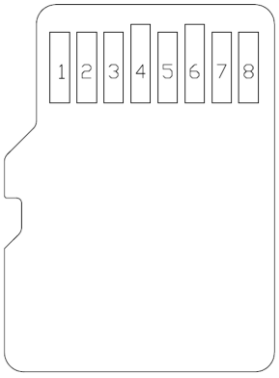


Table 13: Pad Assignment – SD Mode

Pin	SD Mode		
	Name	Type[10]	Description
1	DAT2[11]	I/O/PP	Data Line [Bit 2]
2	CD/DAT3[12]	I/O/PP[13]	Card Detect/ Data Line [Bit 3]
3	CMD	PP	Command/Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1[14]	I/O/PP	Data Line [Bit 1]

Table 14: Pad Assignment – SPI Mode

Pin	SPI Mode		
	Name	Type[10]	Description
1	RSV		
2	CS	I[13]	Chip Select (neg true)
3	DI	I	Data In
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		

[10] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

[11] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

[12] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.

[13] At power up this line has a 50kOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

[14] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

7.2 Power up / Power down behavior and reset

7.2.1 Power up

The host can start with communication 1ms after 2.7V is reached according the SDA specification. That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 3.00.

7.2.2 Power down

When the power falls below 2.6V the controller stops the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

After next initialization the controller checks the last written data for consistency and refreshes the data. Either the new or the old data (if the write operation could not be finished) are available.

7.2.3 Power drop

If the voltage drops below 2.6V and rises again, the card performs a reset. The card must be initialized like after a power on.

7.2.4 Operation below minimum voltage

512MB-2GB

If the card is initialized from the host (ACMD41) below 2.7V the card may not be recognized.

7.3 DC characteristics

Measurements are at recommended Operating Conditions unless otherwise specified.

Table 15: DC Characteristics[15]

Symbol	Parameter	Density	Min	Typ	Max	Unit	Notes
I_{DD}	Operating Current Read (SDR50/DDR50)	512MB		75	80	mA	@ 25°C
I_{DD}		1GB-2GB		80	85	mA	@ 25°C
I_{DD}	Operating Current Write (SDR50/DDR50)	512MB		75	80	mA	@ 25°C
I_{DD}		1GB-2GB		95	100	mA	@ 25°C
I_{DD}	Background read and refresh[16]	512MB-2GB		80	100	mA	@ 25°C
I_{DD}	Pre-initialization Standby Current			5	15	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[17]			10	12	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[17]			10	12	mA	@ 85°C
I_{LI}	Input Leakage Current		-2		2	µA	without pull up R
I_{LO}	Output Leakage Current		-2		2	µA	without pull up R

Table 16: SD Memory Card Recommended Operating Conditions

Symbol	Parameter		min	typ	max	unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

7.4 Signal Loading

According to SD specification

[15] Target values

[16] The card can perform auto data read of the whole card to check for ECC errors and performs data refresh

[17] Before auto read the idle current is larger than the typical idle current after auto read

7.5 AC characteristics

7.5.1 Default Speed mode (0–25MHz)

According to SD specification

7.5.2 High Speed mode (0–50MHz)

According to SD specification

7.5.3 UHS modes

UHS modes were driven with a signal level of 1.8V.
The cards support following UHS-I modes:

Table 17: Supported UHS-I modes

Host request	Card Modes (to select by host)	Max. Burst MB/s	Max. Clock frequency MHz
SDR12	SDR12	up to 12.5	up to 25
SDR25	SDR12, SDR25	up to 25	up to 50
SDR50	SDR12, SDR25, SDR50	up to 50	up to 100
DDR50	SDR12, SDR25, SDR50, DDR50	up to 50	50 (rising and falling edge)
SDR104	SDR12, SDR25, SDR50, DDR50	up to 50	up to 100

According to SD specification

8. Host access specification

The following chapters summarize how the host accesses the card:

- Chapter 8.1 summarizes the SD and SPI buses.
- Chapter 8.2 summarizes the registers.

8.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

8.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

8.1.2 SPI Bus Mode Protocol

The Serial Peripheral Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and dataOut signals.

Table 18: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

8.1.3 Mode Selection

The microSD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should re-start the card as Multimedia Card using CMD0 and CMD1.

8.2 Card registers

The microSD Memory Card has the following registers.

Table 19: SD Memory Card registers

Register name	Bit width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA[18]	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific lifetime information

Table 20: CID registers

Register name	Bit width	Description	Function
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	SB PNM Naming
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

[18] RCA register is not available in SPI mode

Table 21: OCR register

OCR bit position	VDD voltage windows	Typ. value	OCR bit position	VDD voltage window	Typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	1
13	2.5-2.6	0	25-29	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*[19]
			31	0=busy; 1=ready	*[20]

[19] This bit is valid only when the card power up status bit is set

[20] This bit is set to LOW if the card has not finished the power up routine

Table 22: CSD register

Register name	Bits	Bit width	Description	Typ. value (max. 2GB)
CSD_STRUCTURE	127:126	2	CSD structure	00
–	125:120	6	Reserved	00000
TAAC	119:112	8	Data read access time 1	00101111
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010 Default speed 00001011 SDR50 or other values
CCC	95:84	12	Card command classes	010111110101
READ_BL_LEN	83:80	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	1
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75:74	2	Reserved	00
C_SIZE	73:62	12	Device size	xxx[21]
VDD_R_CURR_MIN	61:59	3	VDD min read current	111
VDD_R_CURR_MAX	58:56	3	VDD max read current	111
VDD_W_CURR_MIN	55:53	3	VDD min write current	111
VDD_W_CURR_MAX	52:50	3	VDD max write current	111
C_SIZE_MULT	49:47	3	Device size multiplier	111[21]
–	75:70	6	Reserved	-
C_SIZE	69:48	22	Device size	-
–	47	1	Reserved	-
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	1
–	30:29	2	Reserved	00
R2W_FACTOR	28:26	3	Write speed factor	010
WRITE_BL_LEN	25:22	4	Write data block length	1001[21]
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20:16	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)
–	9:8	2	Reserved	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

≤2GB
memory capacity = BLOCKNR * BLOCK_LEN
Where
BLOCKNR = (C_SIZE+1) * MULT
MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
BLOCK_LEN = $2^{READ\_BL\_LEN}$, (READ_BL_LEN < 12)

[21] Drive size and block sizes vary with card capacity

Table 23: SCR register

Field	Bits	Bit width	Typ. value	Remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.01...2.00
SD_SPEC	59:56	4	0010	SD 2.0 or 3.0
DATA_STAT_AFTER_ERASE	55	1	1	data are 0xFF after erase
SD_SECURITY	54:52	3	010	1.01 (SDSC)
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes→ SD3.0
EX_SECURITY	46:43	4	0000	no extended security
Reserved	42:34	9	0	0
CMD_SUPPORT	33:32	2	00	CMD23 / CMD20 not supported
Reserved	31:0	32	0	0

Table 24: RCA register

Field	Bits	Bit width
RCA	16	0x0000[22]

[22] After initialization the card can change the RCA register

Table 25: SSR register

Field	Bits	Bit width	Typ. value	Remark
Data bus width	511:510	2	0x2[23]	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	0x02800000	40MB
Speed class	447:440	8	0x04	Class 10
Move performance	439:432	8	0x05	5 MB/s sequential write
Allocation unit size	431:428	4	0x7	1 MiB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	0x0001	1 AU
Erase unit timeout	407:402	6	0x01	1 second
Erase unit offset	401:400	2	0x1	1 seconds
UHS mode Speed Grade	399:396	4	0x1	10MB/s
Allocation unit size in UHS mode	395:392	4	0x7	1 MiB
Reserved	391:312	80		
Data structure version identifier, currently 1	311:304	8	0x01	version 1
Number of manufacturer marked defect blocks	303:288	16	0x0008	8 initial BB
Number of initial spare blocks (worst chip)	287:272	16	0x00bf	191 spare blocks
Number of initial spare blocks (sum over all chips)	271:256	16	0x017e	382 spare blocks
Percentage of remaining spare blocks (worst chip)	255:248	8	0x64[23]	100%
Percentage of remaining spare blocks (all chips)	247:240	8	0x64[23]	100%
Number of uncorrectable ECC errors (not including ECC errors during startup)	239:224	16	0x0000[23]	0 uncorrectable errors
Number of correctable ECC errors (not including ECC errors during startup)	223:192	32	0x0045074b[23]	4523851 correctable ECC errors
Lowest wear level class	191:176	16	0x0000[23]	0
Highest wear level class	175:160	16	0x0000[23]	0
Wear level threshold	159:144	16	0x01ff	512 block erases per WL class
Total number of block erases	143:96	48	0x00...1ff0[23]	8176 block erase commands
Number of flash blocks, in units of 256 blocks	95:80	16	0x0020	8192 flash blocks
Maximum flash block erase count target, in wear level class units	79:64	16	0x0075	Flash endurance 117 WL classes (59904 erases)
Power on count	63:32	32	0x00000003[23]	3x power on
Firmware version	31:0	32	0xYYMMDDXX	Firmware version

Bit 311:0 are vendor specific, example values in the table

[23] Value change in operation

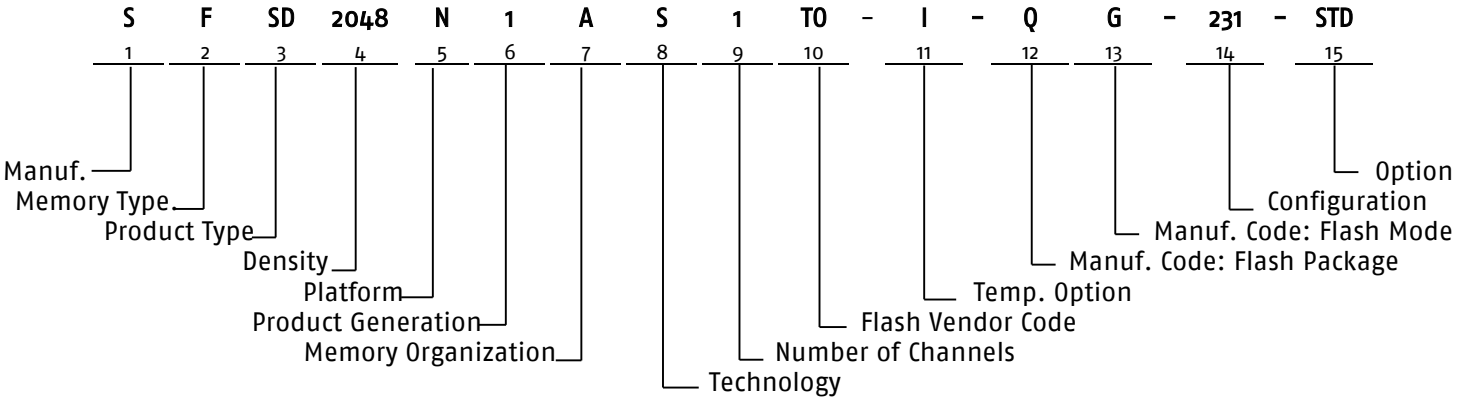
9. Life Time Monitoring

The products support life time monitoring with a vendor specific SD command CMD56 with argument 0x53420001 (read transfer). CMD56 follows the SD protocol specification and returns 512 bytes of data. All multi-byte values are in big endian order (most significant byte first).

Field	Bytes	Byte width	Remark
Unique ID	0:15	16	53 77 69 73 73 62 69 74 «Swissbit» in ASCII
SD CID Register	16:31	16	See chapter 8.2
Firmware Revision	32:42	11	ASCII Null-Terminated
Reserved	43:47	5	All 0x00
User Area Rated Cycles	48:51	4	
User Area Max. Cycle Count	52:55	4	
User Area Total Cycle Count	56:59	4	
User Area Average Cycle Count	60:63	4	
Reserved	64:79	16	All 0x00
Remaining Card Lifetime Percent (user area)	80:80	1	
Reserved	81:85	5	All 0x00
Current SD Card Speed Mode	86:86	1	0x00: Default Speed 0x01: High Speed 0x10: SDR12 0x11: SDR25 0x12: SDR50 0x14: DDR50 0x18: SDR104
Current SD Card Bus Width	87:87	1	0x00: 1 bit width 0x10: 4 bit width
Initial Spare Blocks User Area	88:91	4	
Reserved	92:95	4	All 0x00
Runtime Bad Blocks User Area	96:99	4	
Reserved	100:103	4	All 0x00
Refresh Count User Area	104:107	4	
Reserved	108:111	4	All 0x00
Host Interface CRC count	112:115	4	
Power Cycle Counter	116:119	4	
Read Count Threshold User Area	120:123	4	
Reserved	124:127	4	
Near Miss Count in User Area Blocks	128:131	4	
Reserved	132:143	12	All 0x00
Number of Firmware Refreshes	144:147	4	
Reserved	148:150	3	All 0x00
Auto Refresh	151:151	1	0x00: disabled 0x01: enabled
Total number of blocks scanned during Auto Refresh	152:155	4	
Total number of blocks refreshed by Auto Refresh	156:159	4	

Reserved	160:511	352	All 0x00

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

SD Memory Card	SD

10.4 Density

512 MByte	0512
1 GByte	1024
2 GByte	2048

10.5 Platform

microSD Memory Card	N

10.6 Product Generation

10.7 Memory Organization

x8	A

10.8 Technology

SD Memory Card controller S-6xx platform	S

10.9 Channels

1 Flash channel	1

10.10 Flash Code

Toshiba / Kioxia	T0

10.11 Temperature Option

Extended Temperature Range: -25 °C to 85 °C	E
Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q

10.13 Pin Mode

Single nCE and Single R/nB	E
Dual nCE and Dual R/nB	F
Quad nCE and Quad R/nB	G

10.14 Configuration XYZ

X = Configuration

Configuration	**X**
UHS-I	2

Y = Firmware Revision

FW Revision	**Y**
Firmware 2	2
Firmware 3	3

Z = Optional

Optional	**Z**
Optional	1

10.15 Option

Swissbit/Standard	STD

11. Marking Specification

11.1 Front side

11.2 Back side marking

Part number

Manufacturing date
Lot code

12. Revision History

Table 26: Document Revision History

Date	Revision	Description	Revision Details
13-April-2022	1.00	Initial release	Doc. req. no. 5366
22-April-2022	1.01	adjusted Performance values of 512MB-2GB	Doc. req. no. 5380
15-August-2022	1.02	Updated to firmware "2"	Doc. req. no. 5678
13-June-2024	1.03	Updated to firmware "3"	Doc. req. no. 6951
18-September-2024	1.04	Firmware 3 Products have been added (512MB and 1GB) Corrected values for "System Area Cycle Count" on table 28 (new values =0)	