

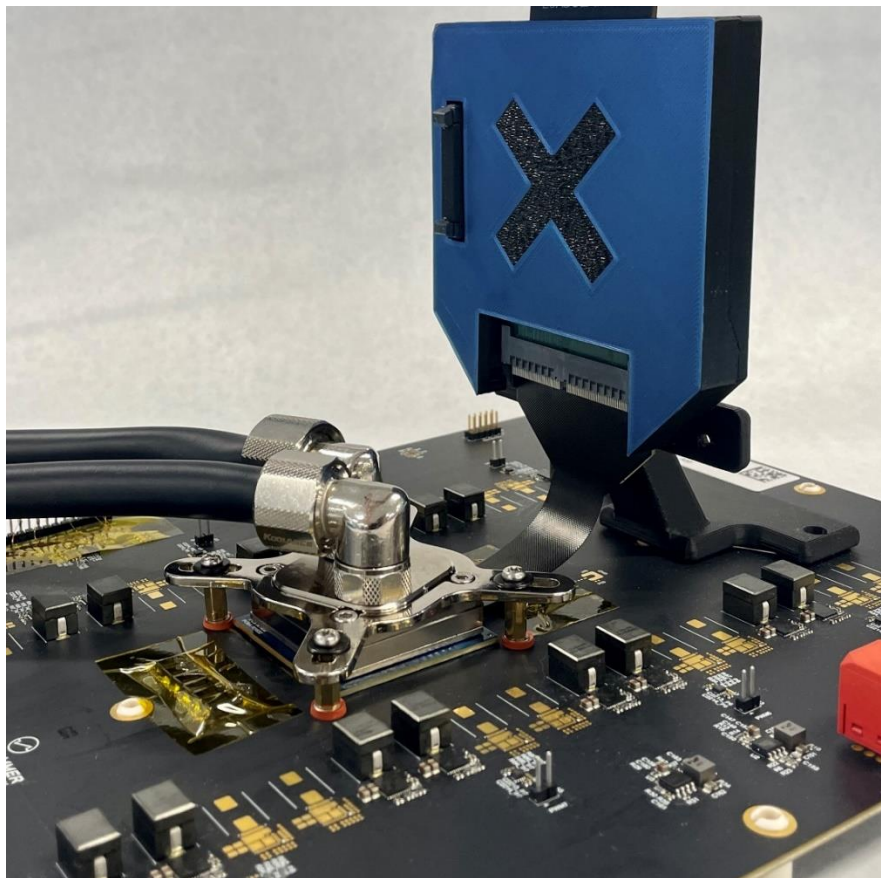
FFED-VC1902-VSVA2197



AMD Xilinx Power Test Adaptor for Versal VC1902-VSVA2197 series FPGAs

ProGrAnalog Corp.
Preliminary V0.3
08/15/2023

**Form Factor Equivalent Device (FFED) for testing
AMD Xilinx Versal ACAP VC1902-VSVA2197 FPGA's**



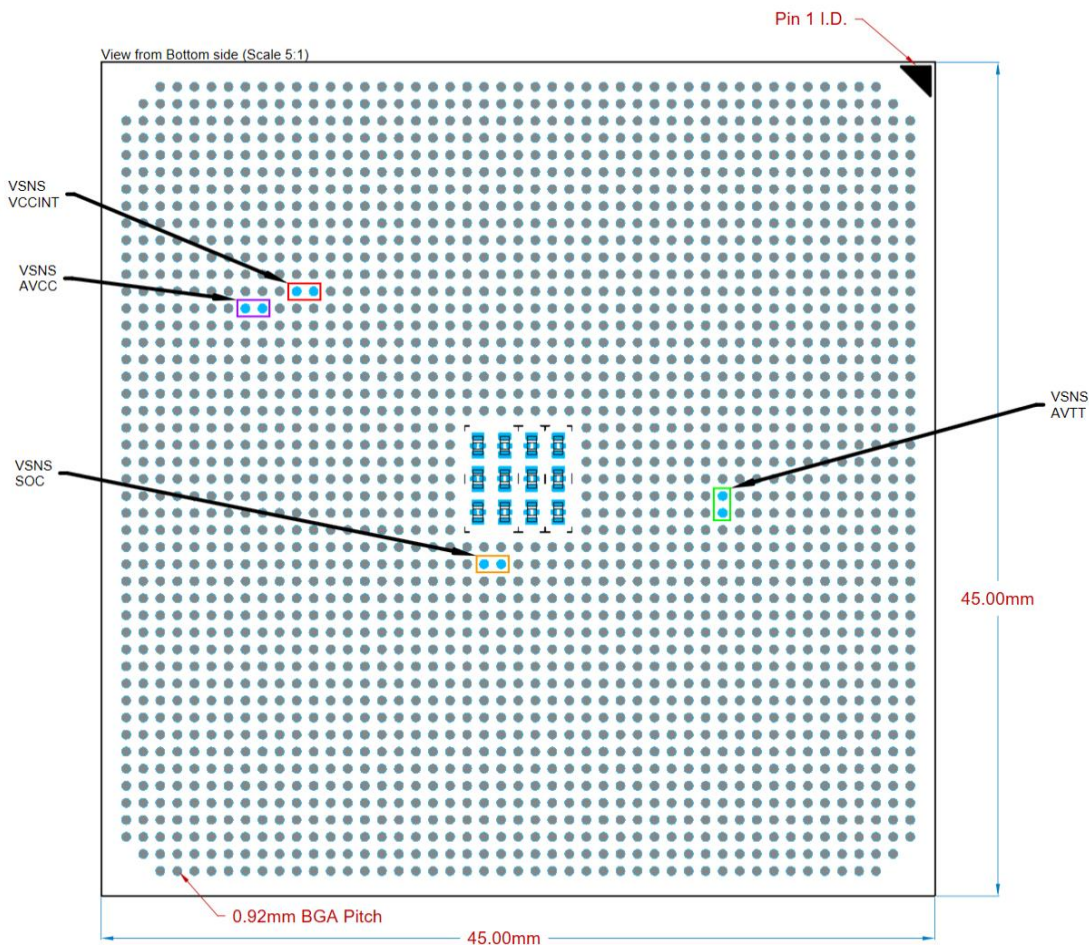
FFED-VC1902-VSVA2197 Features

- Static and high di/ dt transient testing
- 7 Load Cells
- Automatic Report Generation
- Automatic Test Vector Generation
- Allows for fast PDN Optimization and Verification
- As used by AMD Xilinx for internal development purposes
- API support with Command Line Interface (CLI)

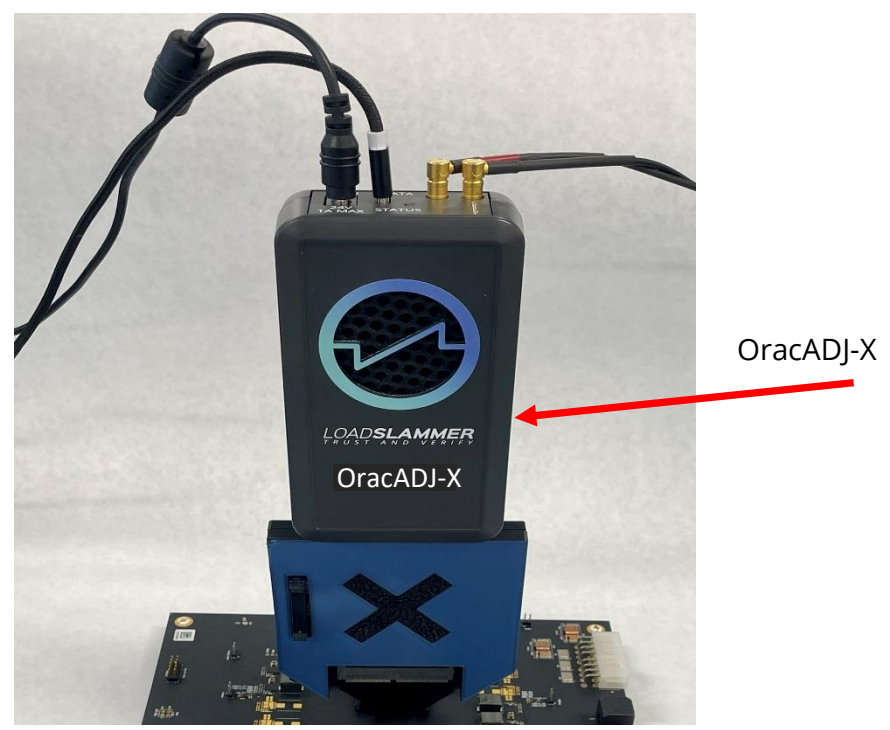
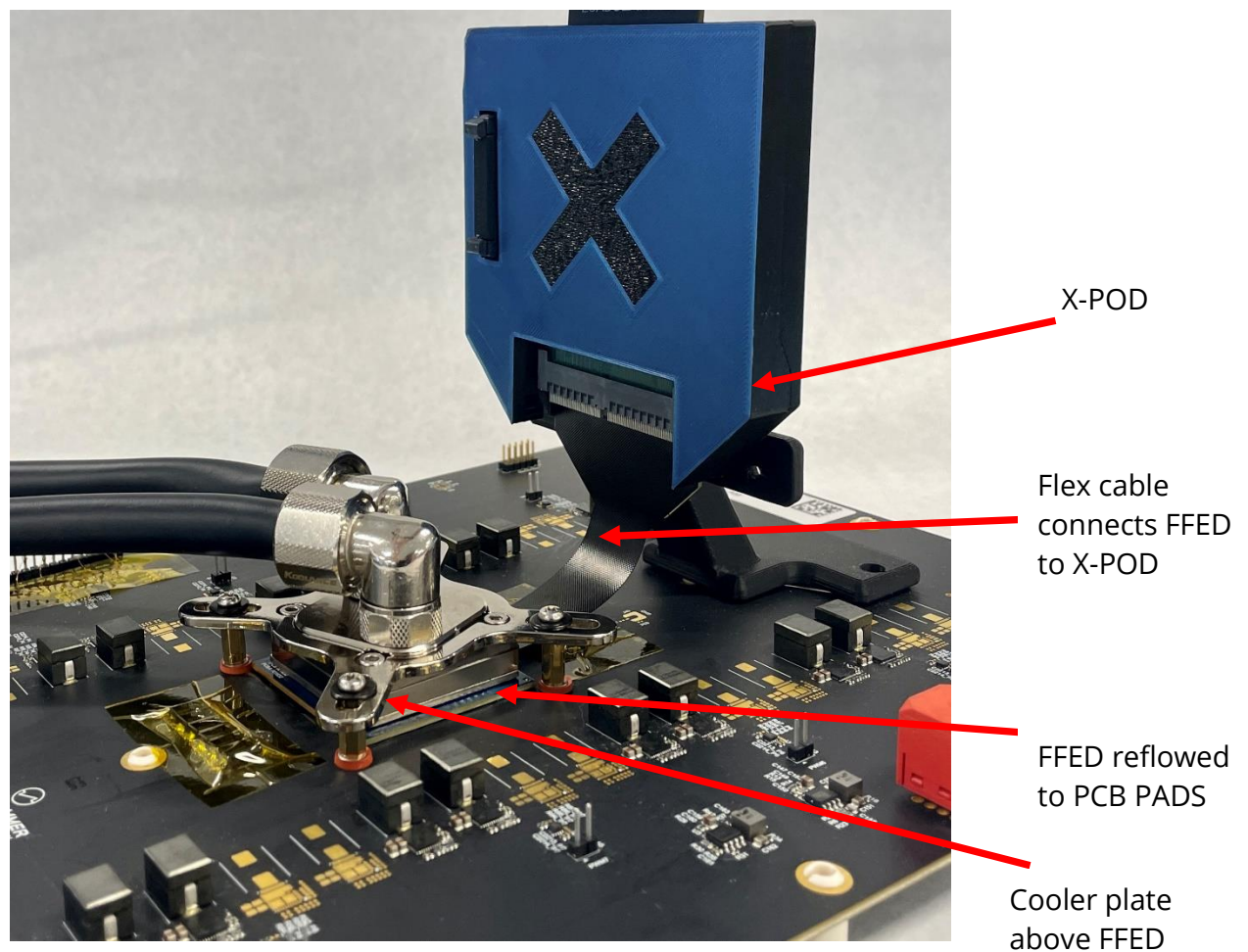
Electrical Specifications

		Estimated Current Specs from AMD Xilinx PDM							
		VCCINT		VCC_SOC		VGYT_AVTT		VGYT_AVCC	
ACAP	Size (mm)	Quiescent (A)	Static/ Dynamic (A)	Quiescent (A)	Static/ Dynamic (A)	Quiescent (A)	Static/ Dynamic (A)	Quiescent (A)	Static/ Dynamic (A)
VC1902 - VSVA2197	45 x 45	20	190	18	18	10	10	6	6

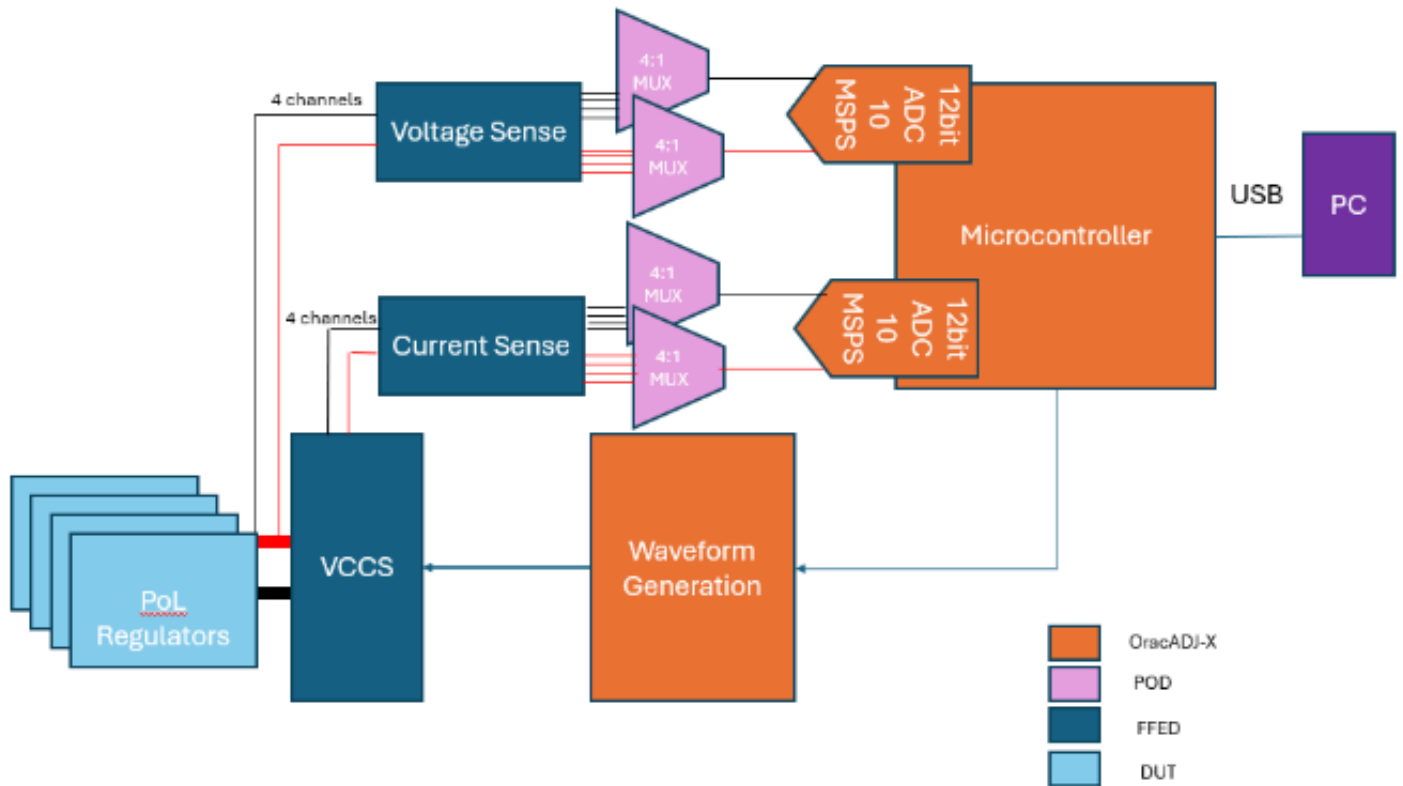
FFED Dimensions & Voltage Sense Points



FFED-VC1902-VSVA2197 Typical Setup

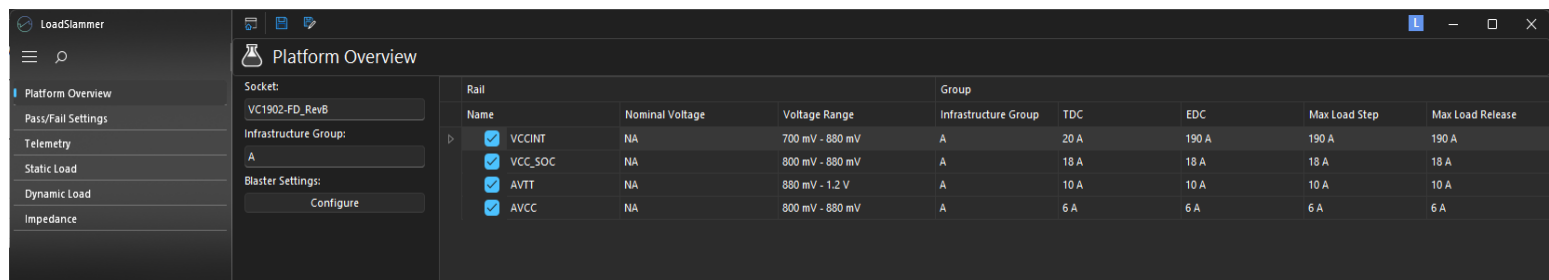


Top Level System Overview



LoadSlammer GUI Setup for FFED-VC1902-VSVA2197

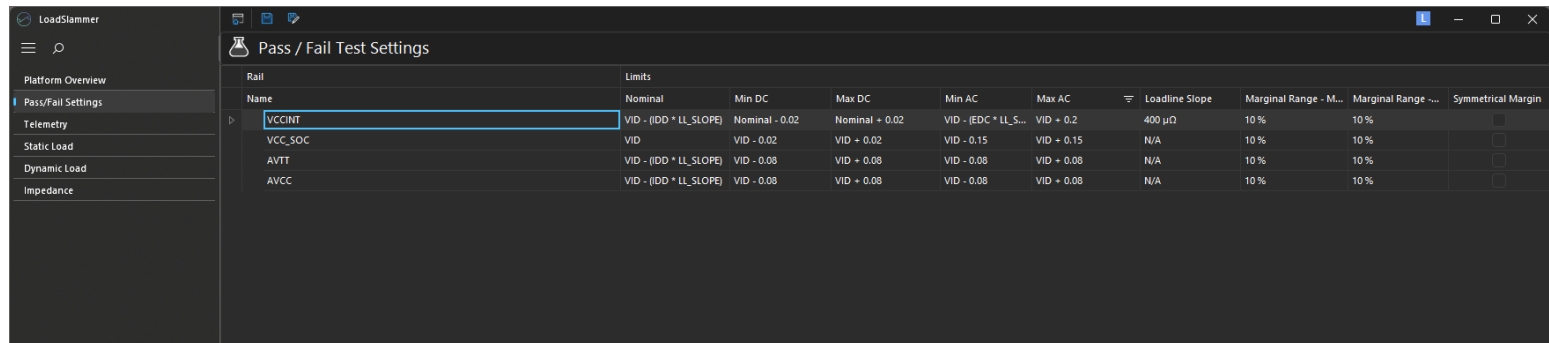
Use Power Design Manager (PDM) settings as inputs to GUI for selecting voltage range and max current.



The screenshot shows the **Platform Overview** tab in the LoadSlammer GUI. The **Socket** is set to **VC1902-FD_RevB**. The **Infrastructure Group** is set to **A**. The **Blaster Settings** are configured. The **Rail** table lists the following rails:

Name	Nominal Voltage	Voltage Range	Group	Infrastructure Group	TDC	EDC	Max Load Step	Max Load Release
☒ VCCINT	NA	700 mV - 880 mV	A	A	20 A	190 A	190 A	190 A
☒ VCC_SOC	NA	800 mV - 880 mV	A	A	18 A	18 A	18 A	18 A
☒ AVTT	NA	880 mV - 1.2 V	A	A	10 A	10 A	10 A	10 A
☒ AVCC	NA	800 mV - 880 mV	A	A	6 A	6 A	6 A	6 A

Setting Pass/Fail and Margins

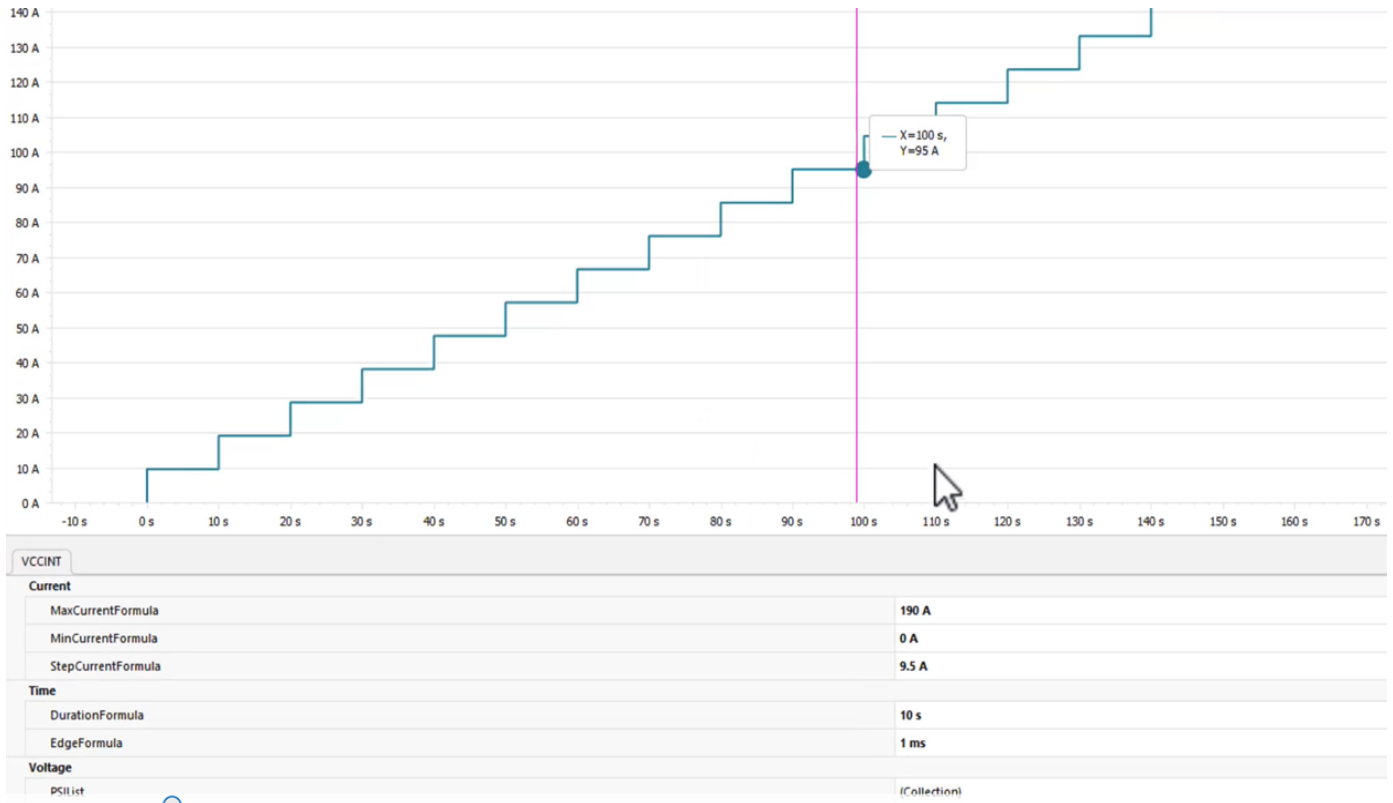


The screenshot shows the **Pass / Fail Test Settings** tab in the LoadSlammer GUI. The **Rail** table lists the following rails with their respective limits and margins:

Name	Limits	Min DC	Max DC	Min AC	Max AC	Loadline Slope	Marginal Range - M...	Marginal Range ...	Symmetrical Margin
☒ VCCINT	VID - (IDD * LL_SLOPE)	Nominal - 0.02	Nominal + 0.02	VID - (EDC * LL_S...	VID + 0.2	400 μ D	10%	10%	☐
☒ VCC_SOC	VID	VID - 0.02	VID + 0.02	VID - 0.15	VID + 0.15	N/A	10%	10%	☐
☒ AVTT	VID - (IDD * LL_SLOPE)	VID - 0.08	VID + 0.08	VID - 0.08	VID + 0.08	N/A	10%	10%	☐
☒ AVCC	VID - (IDD * LL_SLOPE)	VID - 0.08	VID + 0.08	VID - 0.08	VID + 0.08	N/A	10%	10%	☐

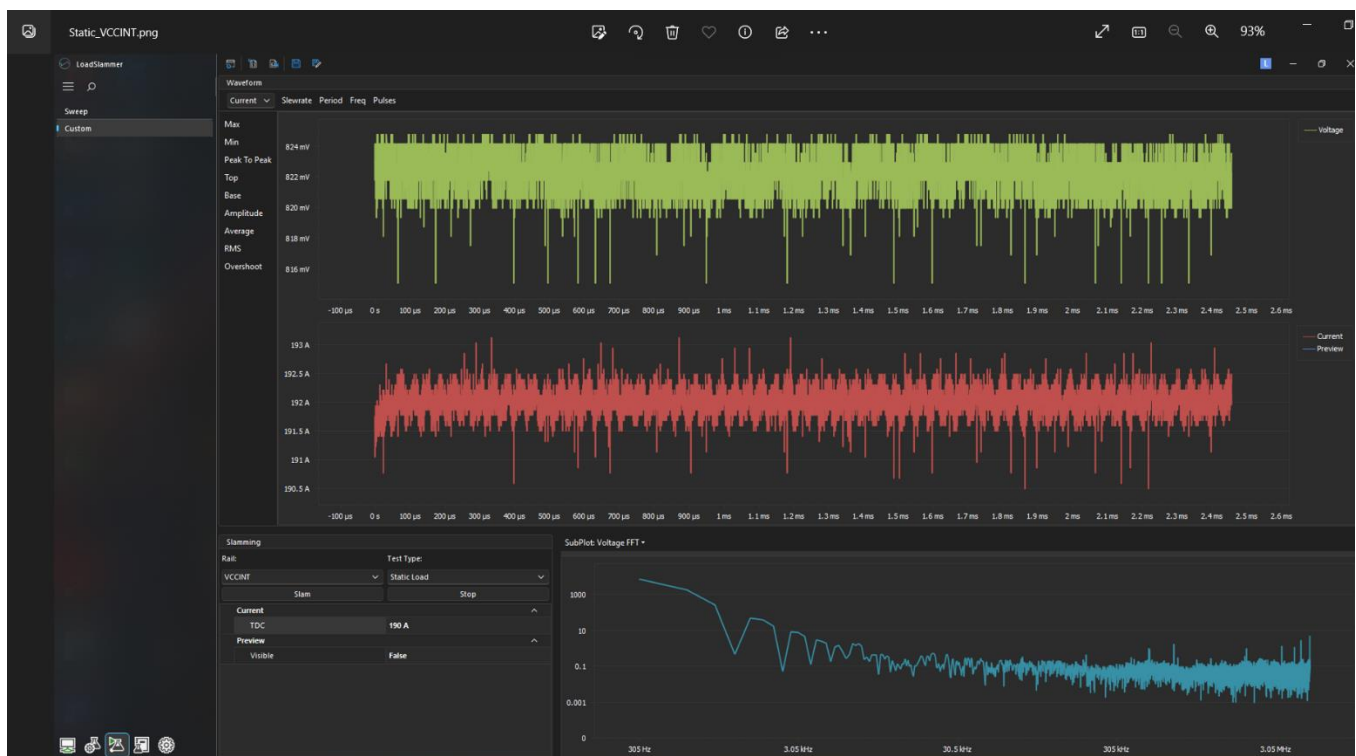
Static Testing

example of static test settings on VCCINT



Transient - Static Testing

Example VCCINT rail



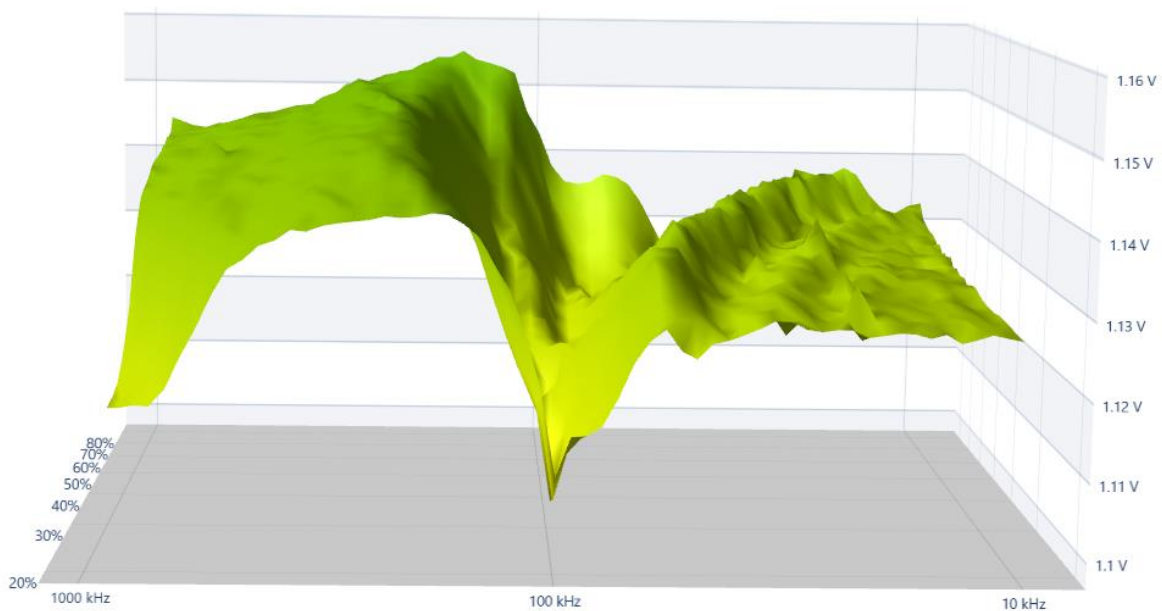
Transient – PWM and Frequency Sweep

Example VCCINT rail



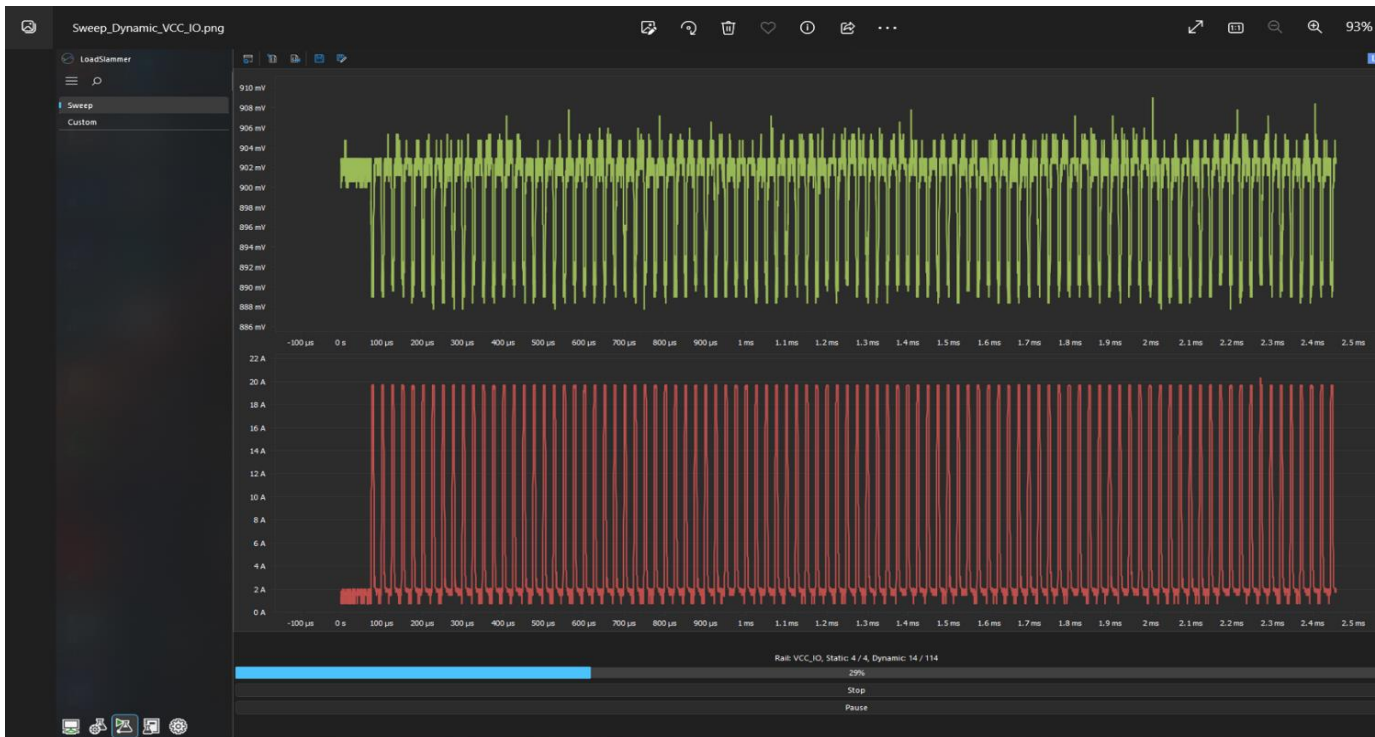
3D Sweep Results

Example VCCINT at 1.12V



Automation – Static & Dynamic Sweep Testing

example shows 4 static, 114 dynamic tests on VCCINT rail



Automated – Report Generation



Summary Report: VC1902-FD - Group A

Report Created By: Roger
Created On: 1/20/2023 4:58:12 PM
Board Serial Number: 0F4043H

Bench: 01

GUI Version: 1.0.0.0

Windows Version: Microsoft Windows NT 10.0.22000.0

Controller: LSP_AD SN: LSP_AD-C56ACEED
HW Revision Number: 0

Software Revision: 8/17/2022 8:40:44 PM

Adapter: 0
Revision: 4

Summary

	Pass	Borderline	Fail	Total
VCCINT	118	0	0	118
VCC_IO	118	0	0	118
VCC_SOC	118	0	0	118
VGTY_AVTT	118	0	0	118
Summary Total	100%	0%	0%	472

Test Settings

VCCINT

Tolerance Settings:

Nominal	DC Range	Min AC	Max AC
VID - (IDD * LL_SLOPE)	Nominal ± 0.02	VID - (EDC * LL_SLOPE) - 0.11	VID +

Marginal Range for Max: 10 %

Marginal Range for Min: 10 %

Load Line Slope: 400 µΩ

Dynamic Load Settings:

EDC:	190 A	Min Current:	0 A
Max Load Step:	190 A	Max Current:	190 A
Max Load Release:	190 A	Step Current:	47.5 A
Duration:	100 ms	Duration:	5 s

Static Load Settings:

Dynamic Analysis:

Rail Name: VCCINT VID: 0 V Nominal Voltage: 0.90 V

Max AC: 1.10 V Min AC: 0.70 V Load Line Slope: 400 µΩ

Frequency	RMS	Min	Max
1 kHz	841.3 mV	773.5 mV	959.1 mV
2 kHz	841.8 mV	774.1 mV	959.7 mV
3 kHz	844.2 mV	773.5 mV	960.3 mV
4 kHz	843.6 mV	773.5 mV	960.9 mV
5 kHz	844.5 mV	772.3 mV	959.7 mV
6 kHz	844.4 mV	771.1 mV	960.9 mV
7 kHz	844.1 mV	770.5 mV	960.9 mV
8 kHz	844.8 mV	770.5 mV	960.9 mV
9 kHz	844.5 mV	770.5 mV	959.7 mV
10 kHz	844.7 mV	770.5 mV	959.7 mV
20 kHz	845.5 mV	775.3 mV	961.5 mV
30 kHz	846.4 mV	775.9 mV	969.7 mV
40 kHz	847.2 mV	775.3 mV	957.3 mV
50 kHz	846.4 mV	775.9 mV	955.4 mV
60 kHz	847.4 mV	775.3 mV	951.8 mV
70 kHz	847.8 mV	775.3 mV	951.8 mV

Dynamic Analysis:

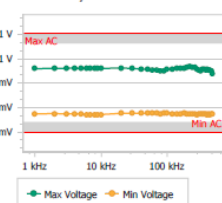
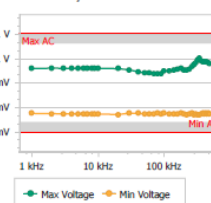
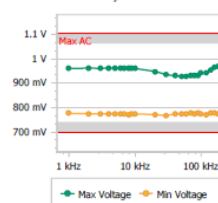
Rail Name: VCCINT VID: 0 V Nominal Voltage: 0.90 V

Max AC: 1.10 V Min AC: 0.70 V Load Line Slope: 400 µΩ

Duty = 25%

Duty = 50%

Duty = 75%



API Support – CLI for configuring and running tests.

```

dynamicTestSettings.json  newTestResults.json
C: > Projects > ProGrAnalog > {} newTestResults.json > ...
1  {}
2      "CompleteTimestamp": "2023-03-07T13:30:10.1363182-08:00",
3      "RailResults": [
4          {
5              "Name": "VDDCR_SOC",
6              "DynamicLoadResults": [
7                  {
8                      "DataType": "ScopeData",
9                      "Tag": "",
10                     "Timestamp": "3/7/2023 1:30:10 PM",
11                     "Duration": "2.5 ms",
12                     "DutyCycle": "50 %",
13                     "EDC": "660 A",
14                     "Offset": "30 A",
15                     "Frequency": "100,000 Hz",
16                     "PSI": "255",
17                     "Edge": "1 μs",

```

Availability

AMD Xilinx part number	ProGrAnalog part number
XCVC1902-XXXX-VSVA2197	FFED-VC1902-VSVA2197

ECN: 3B993

HTS Code: 8471.80.1000

Visit us at:

<https://loadslammer.com>

Questions:

support@progranalog.com

