nPM2100 Hardware Design Guidelines

White Paper

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NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
March 2025	First release

1 Introduction

This document provides guidelines for the hardware design and integration of nPM2100. It is intended for system integrators and hardware engineers.

nPM2100 is an integrated *Power Management Integrated Circuit (PMIC)* designed to provide highly efficient power regulation for any primary-cell application. It has software support for the nRF52 Series, nRF53 Series, and nRF54 Series of wireless multiprotocol *System on Chip (SoC)*s in the nRF Connect SDK from Nordic Semiconductor. nPM2100 is also suitable for use with non-Nordic host devices. It includes a boost regulator and a load switch/*Low-Dropout Regulator (LDO)*.

nPM2100 is targeted at applications where a primary battery is used and provides power supplies not only for the SoC but also for system features such as sensors. It contains an advanced battery management system that helps to accurately monitor the state of the battery and maximizes battery life by utilizing the full battery capacity.

nPM2100 comes in a compact 1.9x1.9 mm *Wafer Level Chip Scale Package (WLCSP)* package or a 4x4 mm *Quad Flat No-lead Package (QFN)* package.

2 Block diagram

The block diagram shows an overview of nPM2100.

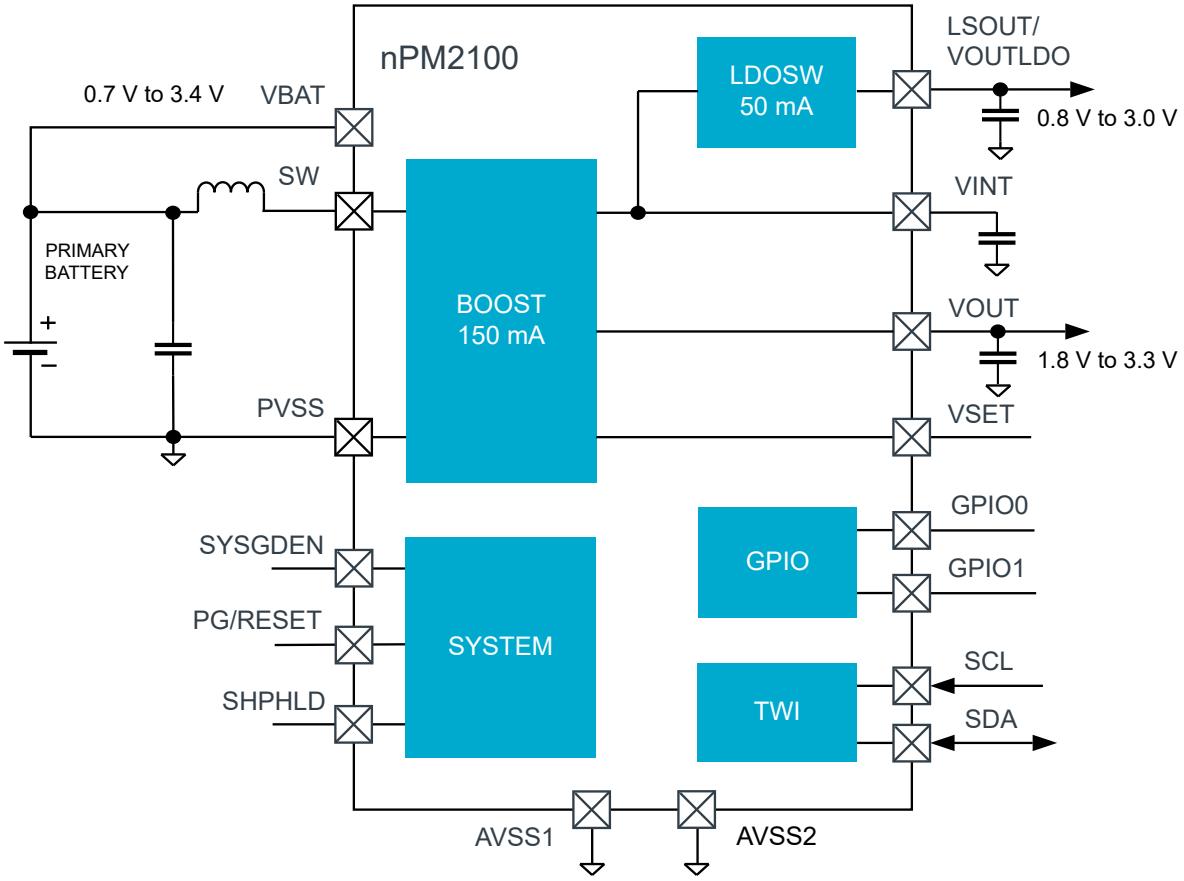

Figure 1: nPM2100 block diagram

3 Hardware integration

This section provides hardware design instructions and tips for successful nPM2100 integration that are related to especially boost component selection to achieve good performance.

For pinout, reference schematic, and layout, see nPM2100 Datasheet and nPM2100 PMIC reference design.

3.1 Selecting inductors for the boost regulator

The nPM2100 boost regulator is designed to operate with a 2.2 µH nominal inductance inductor, which allows up to ± 20% tolerance. To ensure loop stability, do not use inductors with other nominal inductances.

The choice of inductor has a significant effect on the performance of the boost regulator and especially the efficiency of the boost regulator. The choice is typically a compromise between size, performance, and cost.

The saturation current of the inductor should be greater than 550 mA. There are differences in the saturation behavior of soft and hard saturation inductors and how manufacturers specify the saturation current.

When using soft saturation inductors, there is more leeway on the actual saturation current limit for use cases with a light load. Even if the input current to the boost regulator under typical load conditions is much lower than the inductor's saturation current, the saturation current remains an important parameter.

During boost switch pulses, the inductor peak current is higher than the average current at the input. This is especially true in hysteretic Ultra-Low Power (ULP) and Low Power (LP) modes. Typically, the inductor peak current in hysteretic mode is 150 mA. During startup, if the output capacitor is discharged, the inductor current increases temporarily when the capacitor is charged. It is also important to consider other transient events when calculating the inductor's current capability.

Direct Current Resistance (DCR) given by the manufacturer is a key indicator of the performance. However, DCR is not a definitive performance metric as the losses in the inductor also include various frequency-dependent effects like magnetic hysteresis losses, eddy currents, and skin effect.

The following tables show examples of inductor models selected for area, performance, and cost optimized applications. Efficiency numbers were measured with the nPM2100 *Evaluation Kit (EK)*.

Manufacturer	Part number	Size (metric)	Max height (mm)	DCR (mΩ)	Comment
TDK	PLEA85DCA2R2M-1P	1008	0.55	500	Very small, not for high current application
Taiyo Yuden	LSCNB1608HKT2R2MD	1608	0.8	237	Small, good performance
Murata	DFE201210U-2R2M=P2	2012	1	228	Good performance
TDK	MLP2016H2R2MT0S1	2016	1	110	Good performance
Samsung	CIGT201610EH2R2MNE	2016	1	87	Good performance

Table 1: nPM2100 inductor examples

Manufacturer	Part number	Size		Efficiency at 100 µA (%)	Efficiency at 70 mA (%)	ESR (mΩ)	Isat typ (mA)
		(metric)	(inch)				
TDK	PLEA85DCA2R2M-1P	1008	0403	84.4	89.0	500	500
Taiyo Yuden	LSCNB1608HKT2R2MD	1608	0603	86.0	90.7	237	1800
Taiyo Yuden	LSBHB1608KKT2R2M			85.1	89.7	300	580
Taiyo Yuden	MDKK1616T2R2MM	1616	0606	87.2	90.8	215	1800
Murata	DFE201210U-2R2M=P2	2012	0805	87.6	91.0	228	2000
Wurth Electronics	74479275222			87.0	91.0	180	1750
TDK	MLP2016H2R2MT0S1	2016	0806	87.4	91.3	110	550
Samsung	CIGT201610EH2R2MNE			86.4	91.5	73	2900
TDK	VLS201610HBX-2R2M-1			86.3	91.1	142	1900
TDK	TFM201610ALMA2R2MTAA			86.0	88.0	130	2200
Samsung	CIGT252008LM2R2MNE	2520	1008	85.8	90.5	83	2100
Wurth Electronics	74438334022	3030	1212	87.0	91.5	110	6100

Table 2: Boost efficiency comparison with VIN = 1.5 V and VOUT = 1.8 V in ULP and High Power (HP) mode

Manufacturer	Part number	Size		Efficiency at 100 µA (%)	Efficiency at 70 mA (%)	ESR (mΩ)	Isat typ (mA)
		(metric)	(inch)				
TDK	PLEA85DCA2R2M-1P	1008	0403	82.4	87.1	500	500
Taiyo Yuden	LSCNB1608HKT2R2MD	1608	0603	84.0	89.7	237	1800
Taiyo Yuden	LSBHB1608KKT2R2M			81.5	86.7	300	580
Taiyo Yuden	MDKK1616T2R2MM	1616	0606	86.4	90.0	215	1800
Murata	DFE201210U-2R2M=P2	2012	0805	87.2	90.6	228	2000
Wurth Electronics	74479275222			85.8	90.2	180	1750
TDK	MLP2016H2R2MT0S1	2016	0806	86.2	90.3	110	550
TDK	TFM201610ALMA2R2MTAA			84.8	90.5	130	2200
TDK	VLS201610HBX-2R2M-1			84.4	90.3	142	1900
Samsung	CIGT201610EH2R2MNE			84.2	90.9	73	2900
Samsung	CIGT252008LM2R2MNE	2520	1008	85.2	89.4	83	2100
Wurth Electronics	74438334022	3030	1212	85.4	91.1	110	6100

Table 3: Boost efficiency comparison with VIN = 1.5 V and VOUT = 3.0 V in ULP and HP mode

Manufacturer	Part number	Size		Efficiency at 100 µA (%)	Efficiency at 120 mA (%)	ESR (mΩ)	Isat typ (mA)
		(metric)	(inch)				
TDK	PLEA85DCA2R2M-1P	1008	0403	89.8	91.1	500	500
Taiyo Yuden	LSBHB1608KKT2R2M	1608	0603	91.0	92.3	300	580
Taiyo Yuden	LSCNB1608HKT2R2MD			91.0	92.8	237	1800
Taiyo Yuden	MDKK1616T2R2MM	1616	0606	92.2	93.0	215	1800
Murata	DFE201210U-2R2M=P2	2012	0805	92.3	93.1	228	2000
Wurth Electronics	74479275222			92.1	93.2	180	1750
TDK	MLP2016H2R2MT0S1	2016	0806	92.3	93.4	110	550
TDK	TFM201610ALMA2R2MTAA			91.6	93.5	130	2200
Samsung	CIGT201610EH2R2MNE			91.4	93.8	73	2900
TDK	VLS201610HBX-2R2M-1			91.3	93.3	142	1900
Samsung	CIGT252008LM2R2MNE	2520	1008	91.8	92.6	83	2100
Wurth Electronics	74438334022	3030	1212	91.7	93.8	110	6100

Table 4: Boost efficiency comparison with VIN = 2.9 V and VOUT = 3.0 V in ULP and HP mode

Manufacturer	Part number	Size		Efficiency at 100 µA (%)	Efficiency at 120 mA (%)	ESR (mΩ)	Isat typ (mA)
		(metric)	(inch)				
TDK	PLEA85DCA2R2M-1P	1008	0403	89.2	93.1	500	500
Taiyo Yuden	LSCNB1608HKT2R2MD	1608	0603	90.2	94.5	237	1800
Taiyo Yuden	LSBHB1608KKT2R2M			89.9	93.6	300	580
Taiyo Yuden	MDKK1616T2R2MM	1616	0606	91.6	94.6	215	1800
Murata	DFE201210U-2R2M=P2	2012	0805	91.9	94.7	228	2000
Wurth Electronics	74479275222			91.3	94.7	180	1750
TDK	MLP2016H2R2MT0S1	2016	0806	91.5	95.0	110	550
TDK	TFM201610ALMA2R2MTAA			90.8	94.8	130	2200
Samsung	CIGT201610EH2R2MNE			90.6	95.1	73	2900
TDK	VLS201610HBX-2R2M-1			90.5	94.9	142	1900
Samsung	CIGT252008LM2R2MNE	2520	1008	90.8	94.3	83	2100
Wurth Electronics	74438334022	3030	1212	91.0	95.1	110	6100

Table 5: Boost efficiency comparison with VIN = 2.9 V and VOUT = 3.3 V in ULP and HP mode

The following figure shows typical boost regulator efficiencies for an example inductor.

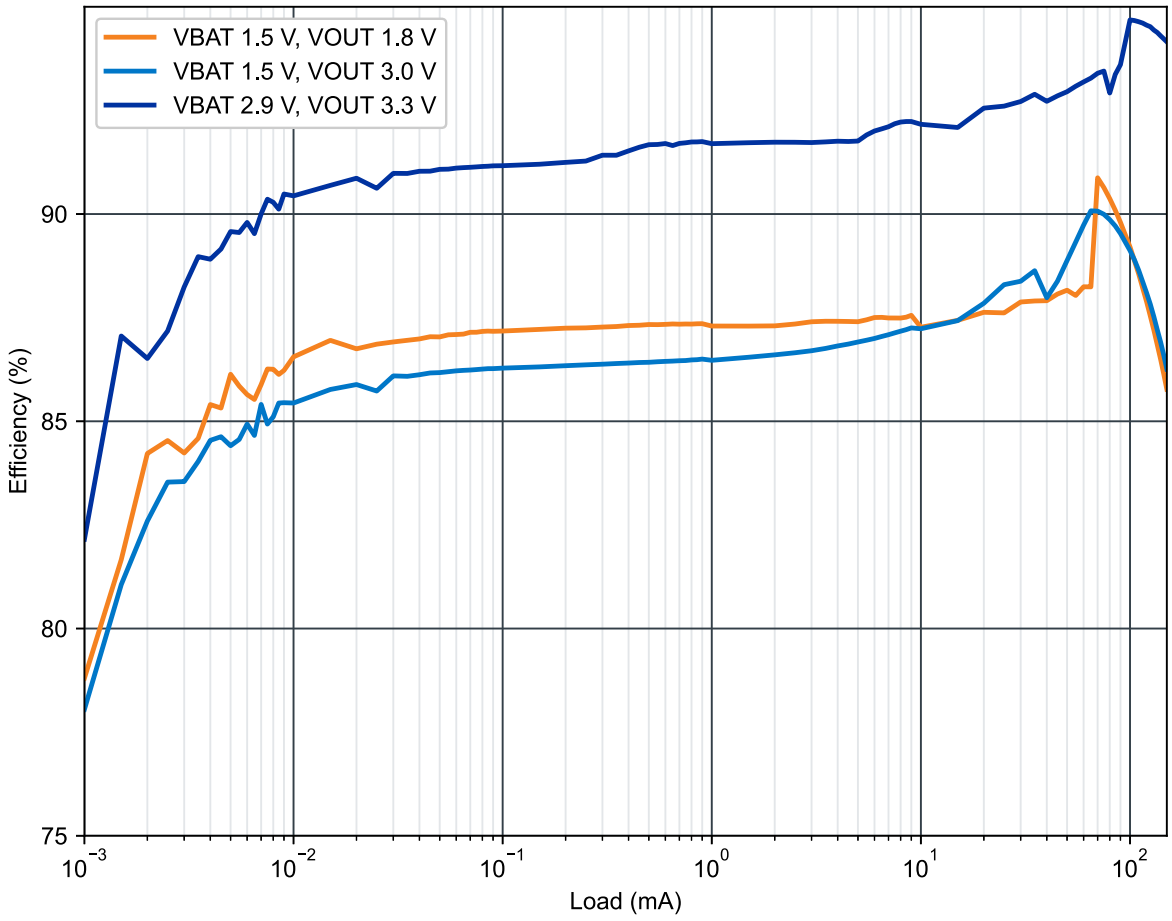

Figure 2: Typical efficiencies for boost regulator using inductor LSCNB1608HKT2R2MD, Auto mode

3.2 Selecting output capacitors for the boost regulator

A boost output capacitor (CVINT) on the **VINT** pin is essential for stability and operation. A capacitor with an effective capacitance of at least 3.5 µF is required.

When selecting a capacitor, consider the effects of DC bias voltage, tolerance, and temperature behavior. The voltage rating should be higher than the maximum output voltage of the boost regulator with at least 6.3 V recommended. For RF sensitive applications, place an additional 1 nF to 100 nF decoupling capacitor parallel to CVINT.

For the **VOUT** pin, a 2.2 µF output capacitor (COUT) is recommended with a minimum requirement of 0.7 µF effective capacitance.

Additional capacitance can be added to the **VINT** pin depending on factors like the use case, battery, and load. Increasing CVINT capacitance can improve load transient response and efficiency in hysteretic Ultra-Low Power (ULP) or Low Power (LP) mode and reduce the ripple in High Power (HP) mode.

If additional bulk capacitance is needed on the output, it is better to place it on the **VINT** pin rather than **VOUT**. This placement avoids the need to charge or discharge high capacitance on **VOUT** during different operation modes, such as Hibernate mode, where **VINT** remains regulated while **VOUT** is switched on only during the active state.

The following tables show examples of capacitor models for CVINT and CVOUT.

Manufacturer	Part number	Size		Capacitance (µF)	Voltage rating (V)	Type
		(metric)	(inch)			
Murata	GRM158R60J226ME01D	0402	1005	22	6.3	X5R
Samsung	CL05A106MQ5NUW	0402	1005	10	6.3	X5R
Murata	GRM155R60J106ME05	0402	1005	10	6.3	X5R
Murata	GRM155R60J106ME15	0402	1005	10	6.3	X5R

Table 6: Example capacitors for CVINT

Manufacturer	Part number	Size		Capacitance (µF)	Voltage rating (V)	Type
		(metric)	(inch)			
Taiyo Yuden	MSASE105CC6225KFNA01	0402	1005	2.2	16	X6S
Murata	GRM155C81C225KE11	0402	1005	2.2	16	X5R
Samsung	CL05X225KP5QUW	0402	1005	2.2	16	X6S
Murata	GRM155R60J225ME01D	0402	1005	2.2	6.3	X5R
Murata	GRM033R60J225ME01	0201	0603	2.2	6.3	X5R

Table 7: Example capacitors for CVOUT

3.3 Selecting input capacitor for VBAT

An input capacitor with an effective capacitance of at least 3.5 µF is required on the **VBAT** pin.

The voltage rating of the input capacitor should in all cases be higher than the maximum input voltage, with an added margin. A minimum voltage rating of 6.3 V is recommended. For RF sensitive applications, place an additional 1 nF to 100 nF decoupling capacitor on **VBAT**.

The following table shows examples of capacitor models for **VBAT**.

Manufacturer	Part number	Size		Capacitance (µF)	Voltage rating (V)	Type
		(metric)	(inch)			
Murata	GRM158R60J226ME01D	0402	1005	22	6.3	X5R
Samsung	CL05A106MQ5NUW	0402	1005	10	6.3	X5R
Murata	GRM155R60J106ME05	0402	1005	10	6.3	X5R
Murata	GRM155R60J106ME15	0402	1005	10	6.3	X5R

*Table 8: Example capacitors for **VBAT***

3.4 Selecting output capacitor for LDOSW

If LDOSW is used as an *LDO*, a 2.2 µF capacitor is needed at the **LSOUT/VOUTLDO** pin for stability. The effective capacitance should be at least 0.7 µF considering the DC bias and temperature effect as well as tolerance. In Load Switch mode there is no need for additional capacitance at the output.

The following table shows examples of capacitor models for LDOSW.

Manufacturer	Part number	Size		Capacitance (µF)	Voltage rating (V)	Type
		(metric)	(inch)			
Taiyo Yuden	MSASE105CC6225KFNA01	0402	1005	2.2	16	X6S
Murata	GRM155C81C225KE11	0402	1005	2.2	16	X5R
Samsung	CL05X225KP5QUW	0402	1005	2.2	16	X6S
Murata	GRM155R60J225ME01D	0402	1005	2.2	6.3	X5R
Murata	GRM033R60J225ME01	0201	0603	2.2	6.3	X5R

Table 9: Example capacitors for LDOSW

3.5 Comparing boost regulator performance using different input and output capacitors

In applications where the load is in short load pulses, such as *Bluetooth*® LE *SoC*, and the battery has a high internal resistance, like a coin cell, the selection of capacitance on the boost regulator input and output affects the overall battery life.

Typically, increasing the output capacitance on a DC/DC regulator improves load transient performance and in a hysteretic operating mode it improves efficiency as well. This is because fewer refresh cycles are needed to maintain output voltage regulation. However, for batteries with high internal resistance, adding capacitance on the input side of the regulator can be more beneficial. The capacitance that is parallel to the battery helps reduce the peak current drawn from the battery and maintains a more stable battery voltage.

The battery's equivalent series resistance (ESR) losses, represented by the formula $P=I^2 \times R$, decrease significantly if the peak current is reduced as the loss is proportional to the square of the current. Increasing output capacitance improves load transient performance but also increases the maximum current peaks from the battery. This increase leads to higher ESR losses, which reduces the benefits of the added capacitance. With a weak battery, these high current pulses can cause the battery voltage to collapse during a boost refresh.

In actual applications, it is essential to consider cost and solution size. Optimizing the placement of capacitors can significantly impact overall performance and battery life.

To demonstrate the boost regulator's performance with different input and output capacitors, a test was set up using the nPM2100 *EK* with a CR2032 battery and nRF52840 with a +8 dBm load profile simulating one Bluetooth LE advertising (RX/TX) event. The target output voltage (VOUT) was programmed to 3.3 V, and the boost regulator was blocked from entering High Power mode (NOHP). The default capacitor configuration for the nPM2100 EK included the following:

- Input capacitor (CVBAT): 10 µF + 1 nF
- Output capacitor (COUT) and boost output capacitor (CVINT): 10 µF + 2.2 µF + 1 nF

The following cases were compared:

1. Baseline battery discharge test conducted without additional capacitors
2. A 100 µF capacitor added to the boost regulator output (**VINT**)
3. A 100 µF capacitor added to the input (**VBAT**)
4. A 100 µF added to both input (**VBAT**) and output (**VINT**)

The tests show that adding capacitance to the output of the boost regulator improves the load transient response and efficiency but causes a higher drop in input voltage and increases peak current, which leads to higher ESR losses. Adding capacitance at the input reduces the ESR losses and keeps the battery voltage more stable. The best setup for extending battery life and improving load transient performance was achieved by adding 100 µF capacitance to both the input and output.

The following table shows the battery life metrics which are calculated as how many Bluetooth LE events can be drawn from the battery.

Configuration	Battery life difference
Default capacitors	Baseline
+100 µF at **VINT**	+2.7%
+100 µF at **VBAT**	+11.6%
+100 µF at **VINT** and **VBAT**	+17.9%

Table 10: Impact of additional capacitance on battery life

The following figures show the response to a Bluetooth LE event for the different test cases.

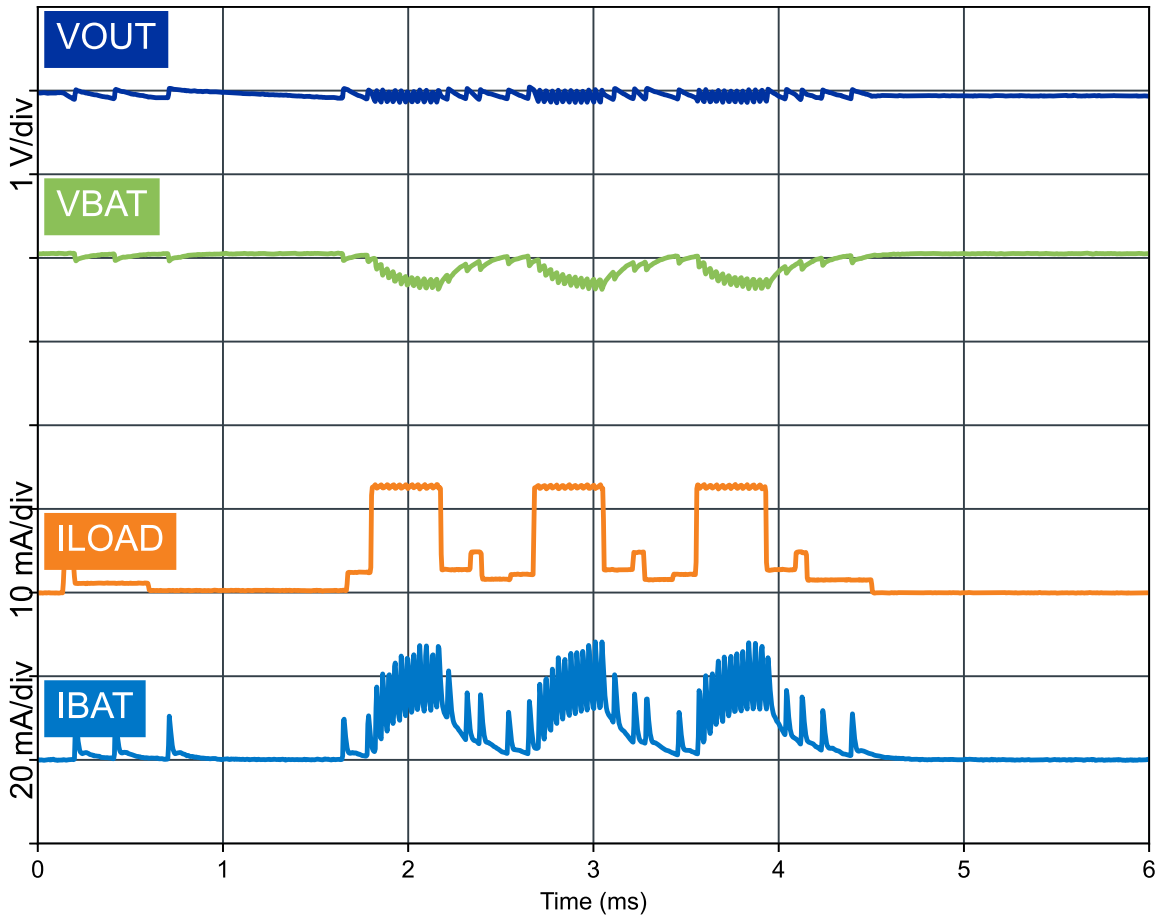

Figure 3: Response to Bluetooth LE event, default capacitors

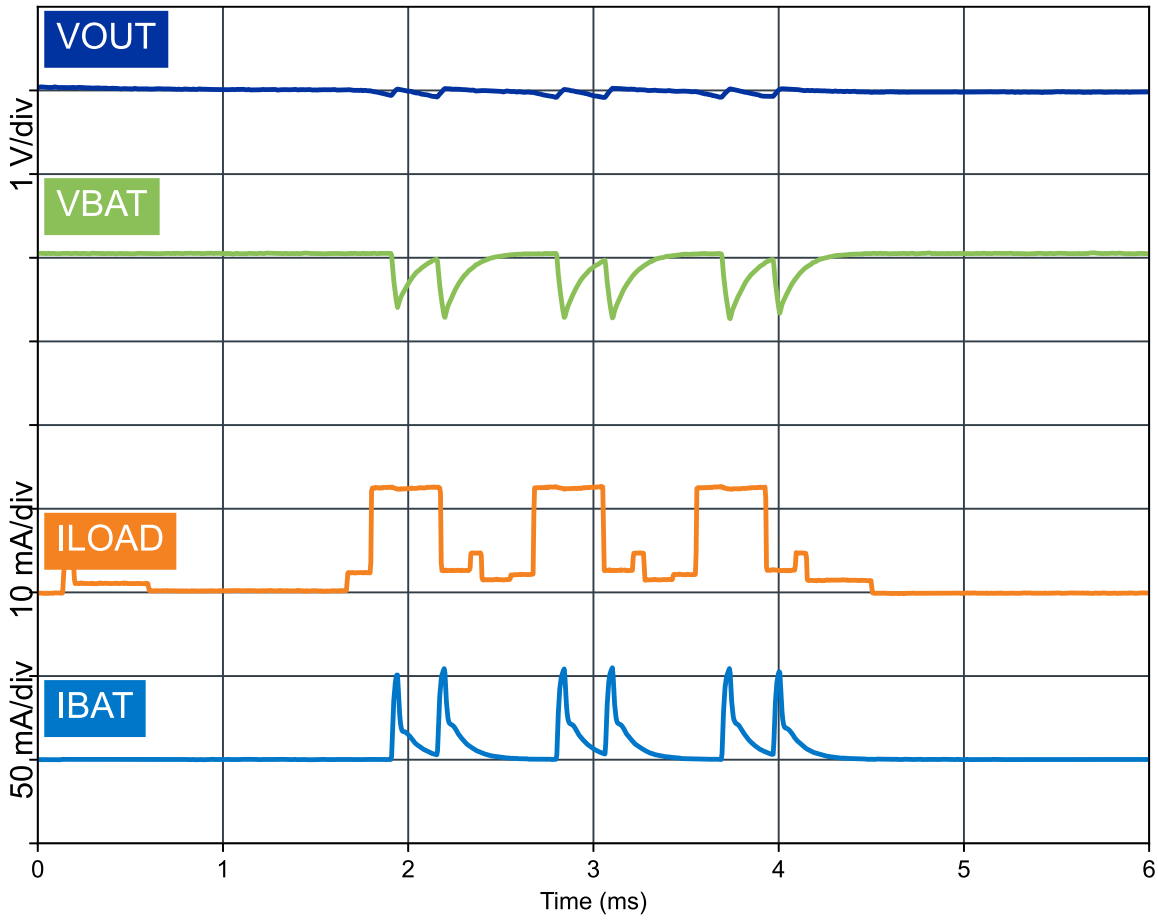

Figure 4: Response to Bluetooth LE event, 100 µF added to the boost regulator output

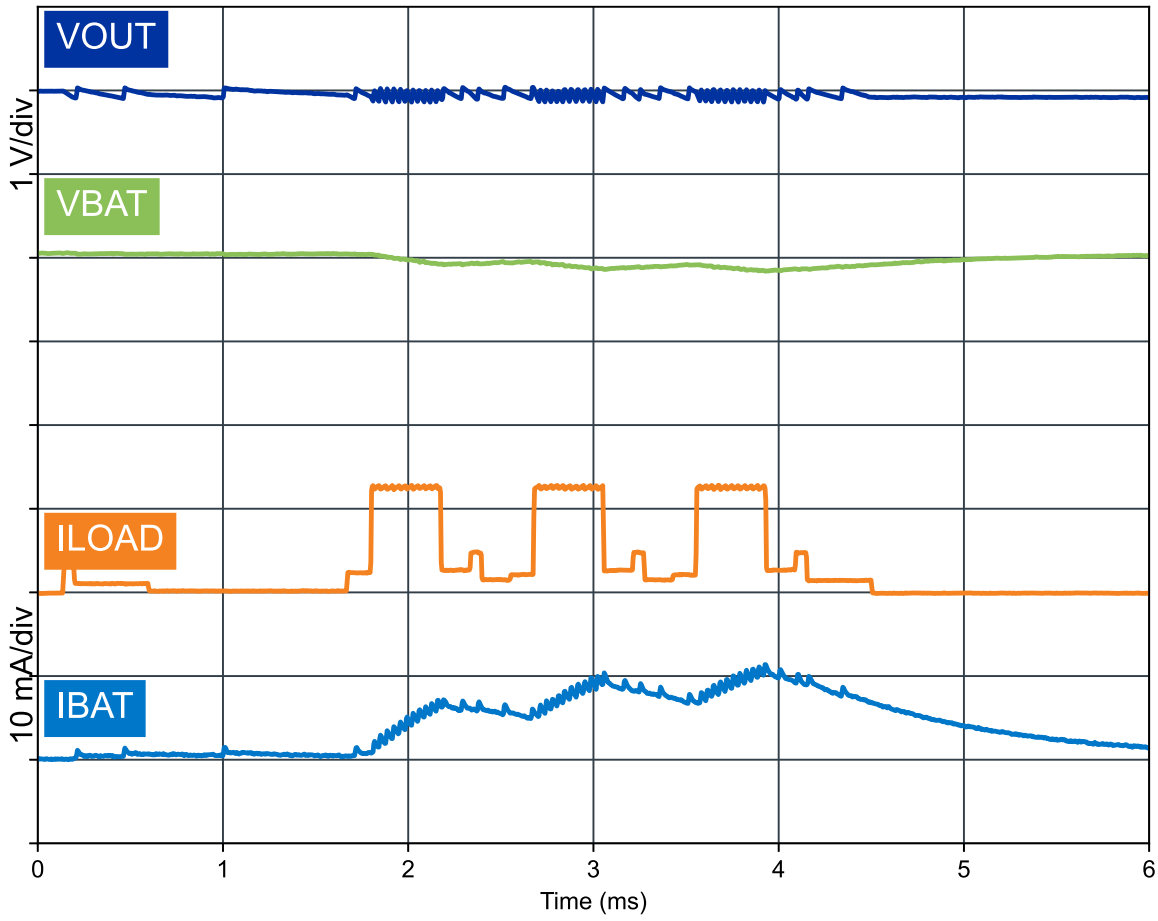

Figure 5: Response to Bluetooth LE event, 100 µF added to the boost regulator input

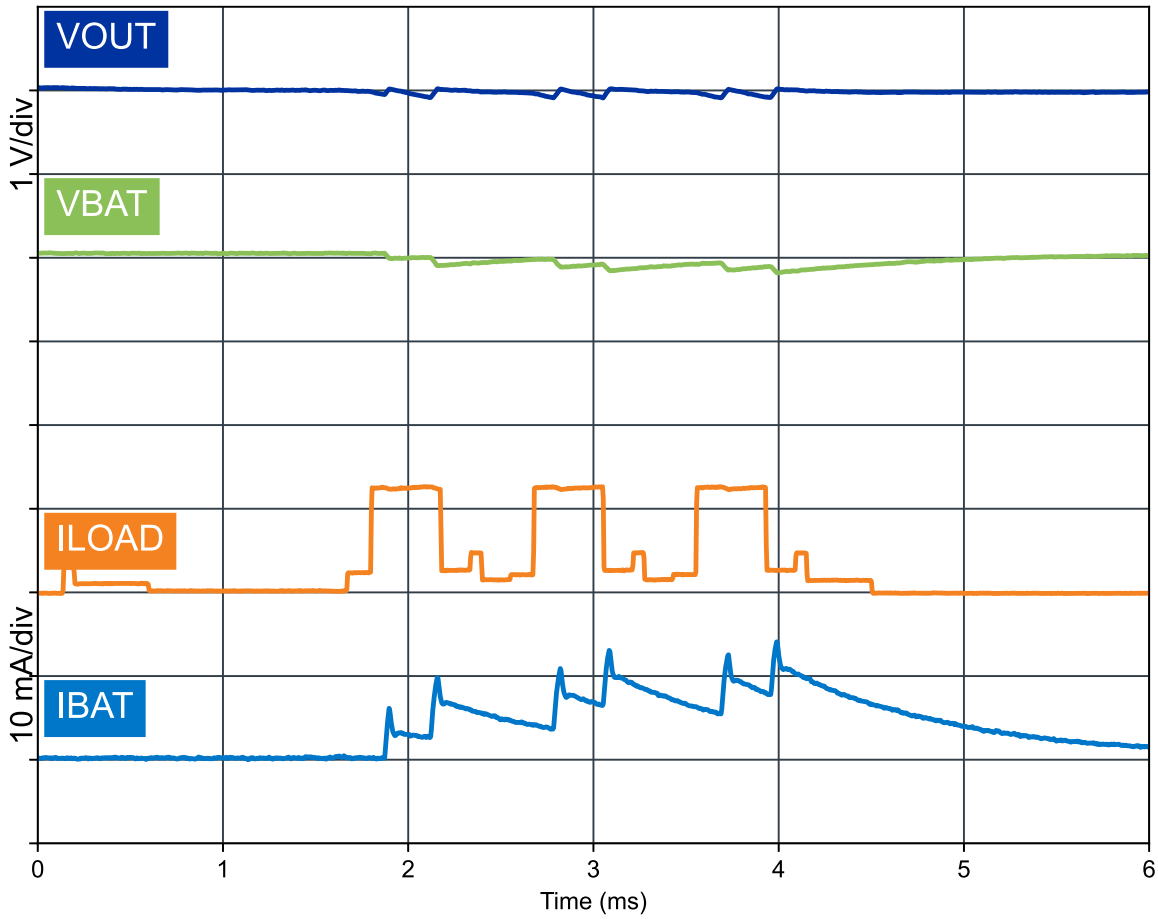

Figure 6: Response to Bluetooth LE event, 100 µF added to the boost regulator input and output

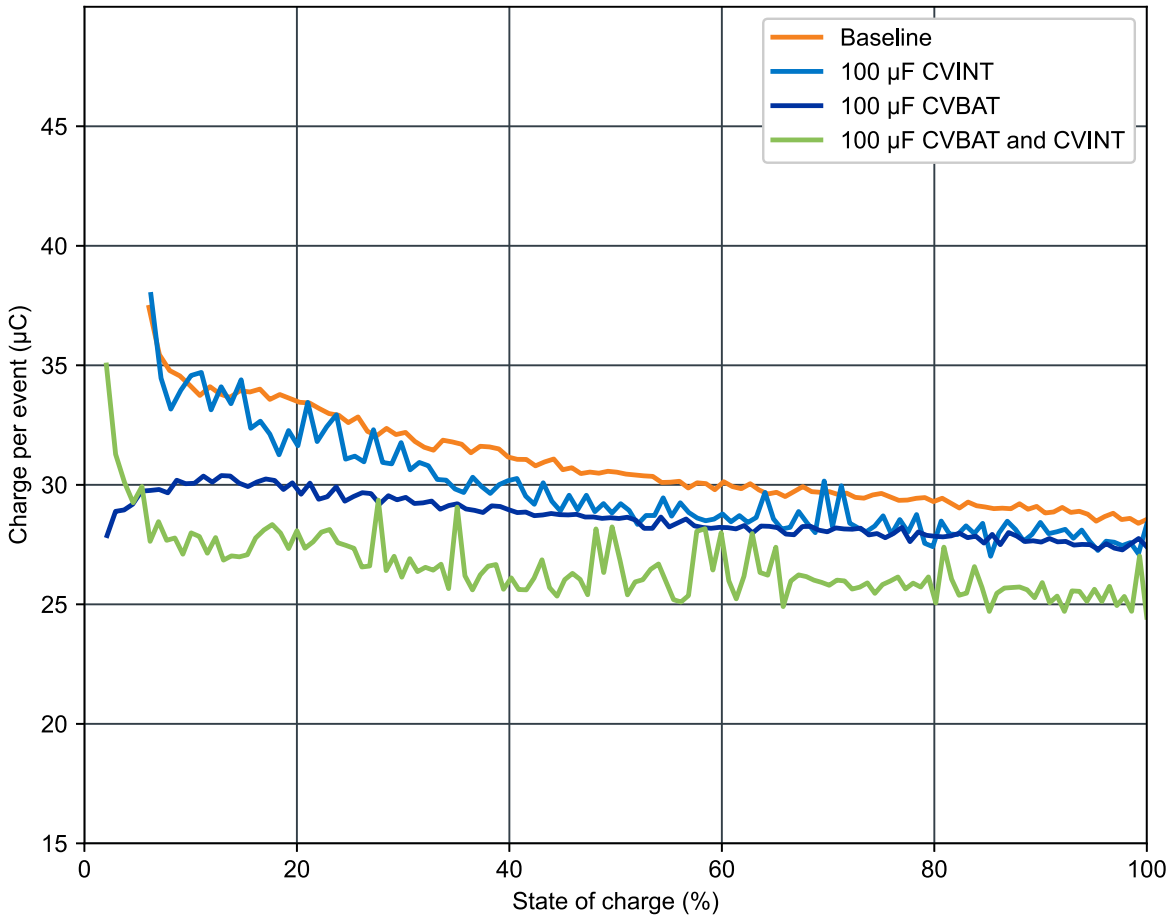

Figure 7: Charge per Bluetooth LE event in discharge test

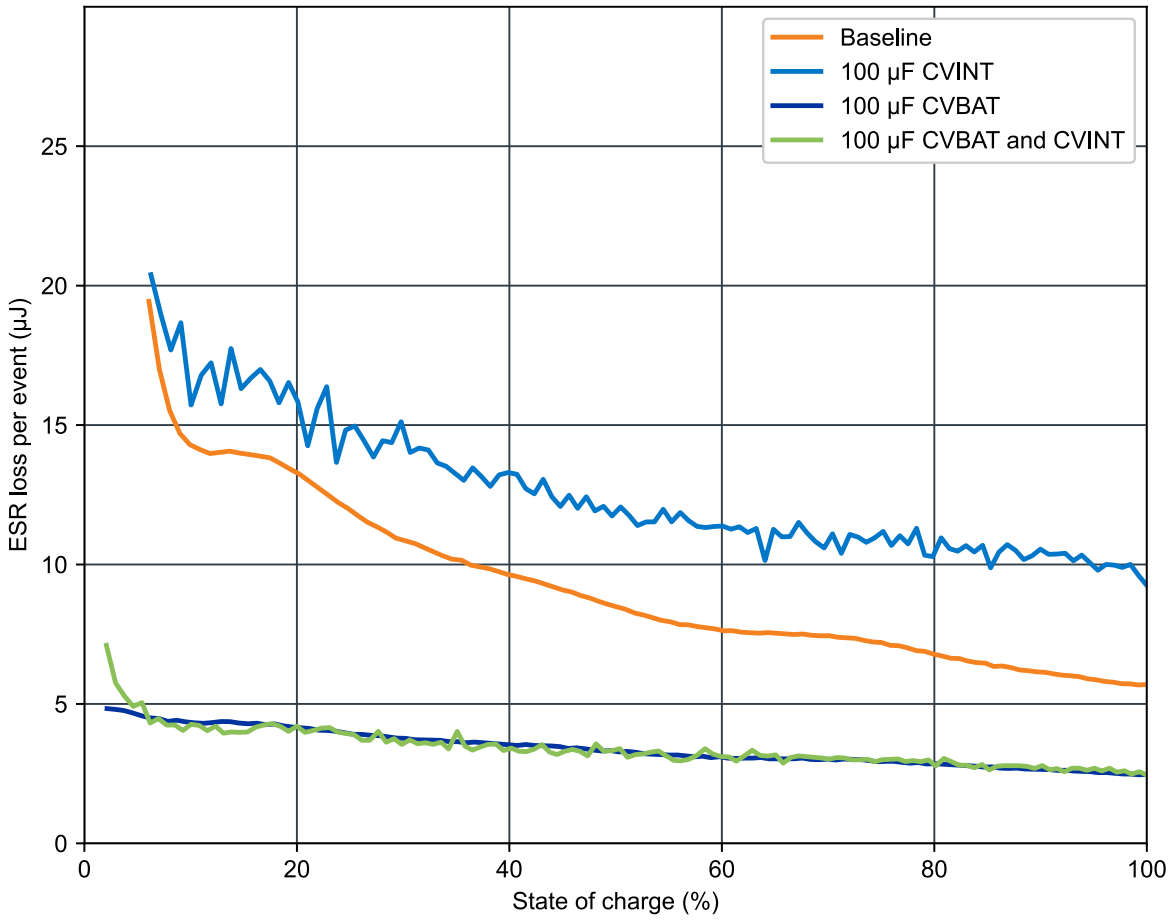

Figure 8: ESR losses per Bluetooth LE event in discharge test

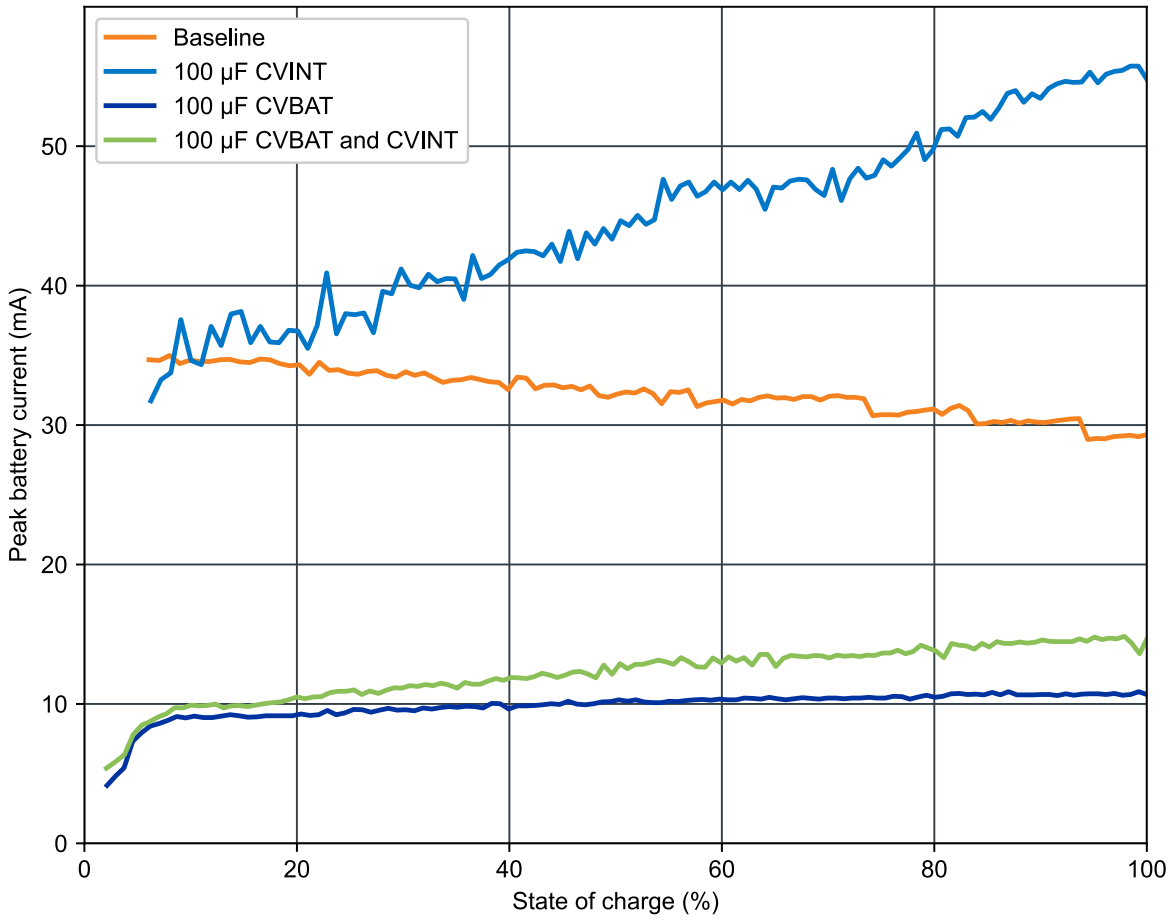

Figure 9: Peak battery current during Bluetooth LE event in discharge test

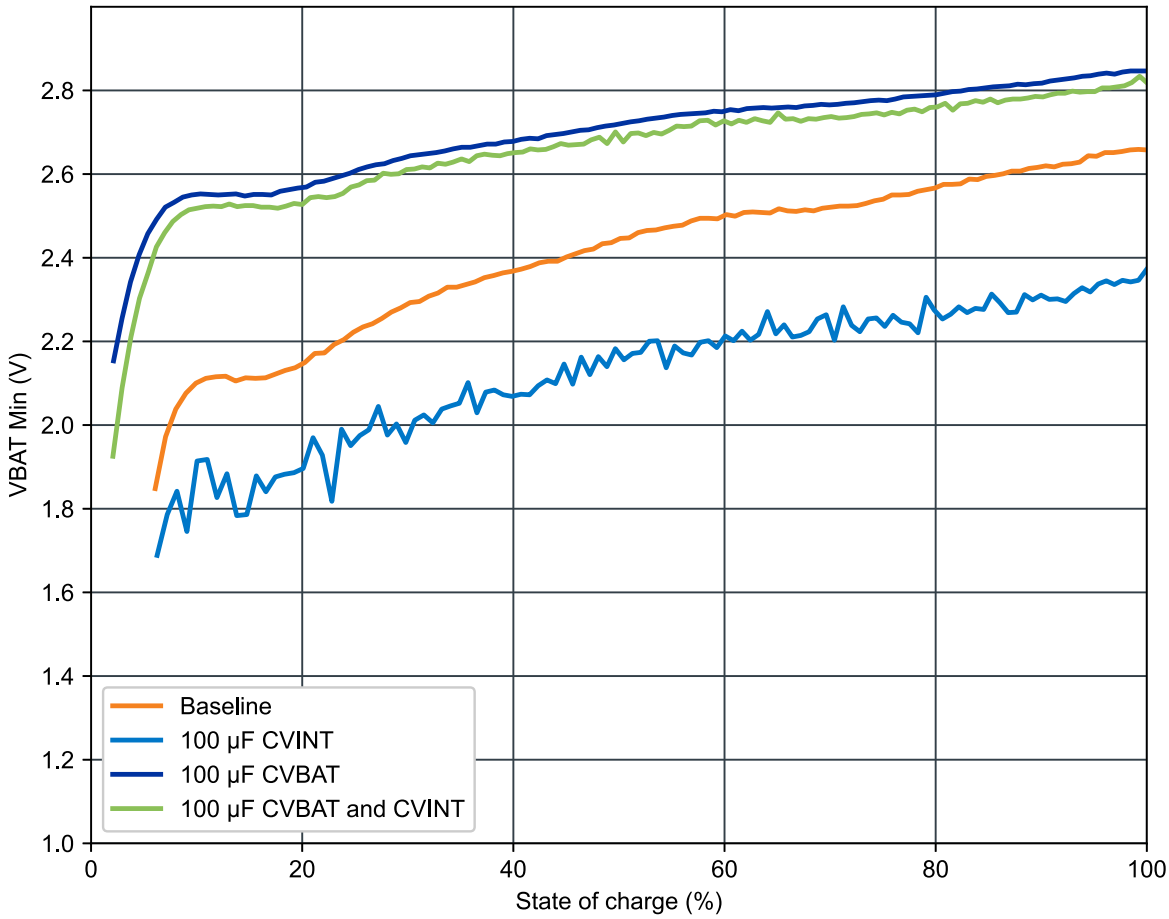

Figure 10: Minimum battery voltage during Bluetooth LE event in discharge test

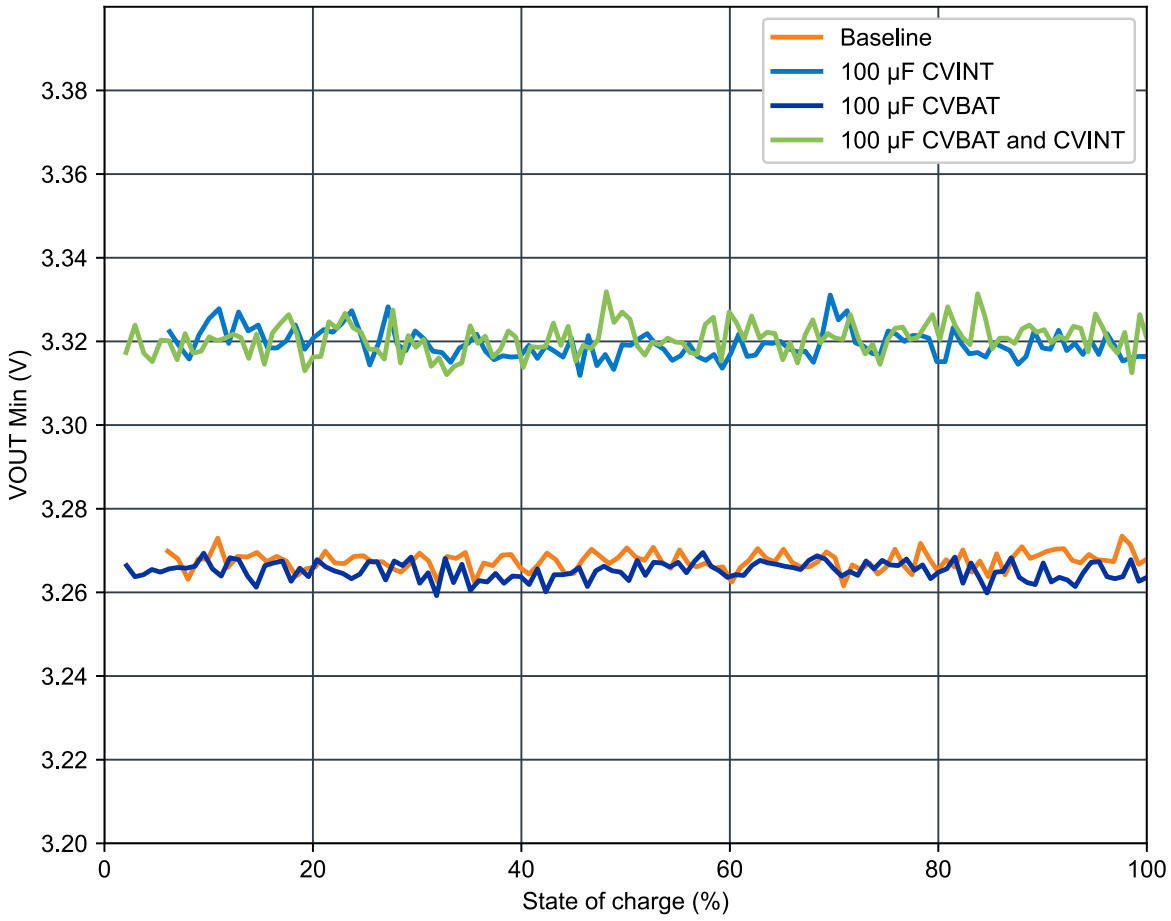

Figure 11: Minimum output voltage during Bluetooth LE event in discharge test

4 End product hardware design

Selecting external components for nPM2100 and having a well-designed PCB layout are crucial for optimal performance.

The design of a product often aims to achieve a small form factor and an attractive appearance. However, to achieve a product with solid performance, other design factors must also be considered. Some of those design factors conflict with the small form-factor target. Typically, this means a compromise in the design that can affect the performance or appearance of the product.

4.1 PCB stack-up

The nPM2100 PMIC reference design layouts use four-layer PCBs. The use of at least four layers is recommended.

The key benefit of using a PCB design with four or more layers is the proper incorporation of ground planes very close to the power and signal routings. Ground planes improve power and signal integrity for the circuit by improving return current paths, reducing crosstalk between signals, and reducing unwanted *Electromagnetic Interference (EMI)*.

It is beneficial to have a large ground plane without discontinuities, since return currents spread across the plane. For higher harmonic return currents, for instance in switching regulators, a ground plane ensures the lowest impedance for the current.

Other benefits of ground planes are controlled impedance in transmission lines, such as RF signals, and heat sinking for self-heating components, which improves the overall longevity of components.

The nPM2100 *QFN* and *WLCSP* can be routed on a two-layer board, but in that case, a solid ground plane must be ensured under high current paths, such as boost input, output, and switch nets. For a WLCSP on a two-layer board or a multilayer board without microvias, the **GPIO0** and **SYSGDEN** pins cannot be routed. This limitation should be considered from the perspective of the use case when designing the end product.

Other components on the board might have requirements for the stack-up, like 50 Ω impedance on RF lines and USB routing differential impedance.

Using microvias and a four-layer PCB might also set restrictions on the stack-up, as an aspect ratio of 1:1 is common for laser cut vias. If nPM2100 WLCSP is used on a board with via in small pads, it is recommended to use via capping to ensure good solderability.

4.2 PCB layout guidelines

A well-designed PCB is necessary to achieve good performance. A suboptimal layout can lead to loss in performance or functionality.

To ensure functionality, it is essential to follow the schematics and layout references closely. This is important especially for the nPM2100 boost regulator.

PCB parasitic extraction tools can be used to analyze and iterate the layout to achieve a good design but following established PCB layout guidelines usually provides satisfactory results.

4.2.1 Routing and component placement

The following guidelines can help you design your PCB layout.

Boost regulator design

For the boost regulator, place the output capacitors (CVINT) as close as possible to the **VINT** pin and power ground (**PVSS**) of nPM2100.

Use wide traces to reduce voltage drop due to parasitic resistance and inductance.

If a high-frequency bypass capacitor is used in parallel with a bulk capacitor, place the small high-frequency capacitor closest to nPM2100.

In boost regulators, the output has the highest rate of current change (di/dt) compared with the input. Therefore, output routing loop area and impedance are critical. See figures Figure 12: Boost regulator switching cycles on page 23 and Figure 13: Boost regulator switch cycles and principle for component placement on page 23.

Keep the trace between the boost regulator output capacitor (CVINT) and the **VINT**/**PVSS** pins as short as possible.

The input capacitor provides a low-impedance voltage source for the boost regulator. Keep the traces short and reduce the parasitic inductance on these traces as much as possible.

Ground layer design

The parasitic inductance can be decreased by using a ground plane as close as possible to the top layer by using a thin dielectric layer between the top layer and the ground plane (layer two).

Avoid high switch currents flowing in the ground plane on the point where a sensitive analog supply decoupling capacitor is connected to the ground plane.

Avoid routing on layers underneath the device that could cut the main ground plane and cause long ground loops.

Splitting ground to power, analog, and digital grounds (star grounding) is generally not recommended.

Place the components so that the digital, analog, and switch powers do not interfere with each other and let the lowest impedance return path form naturally in the ground plane without splitting it.

General design

Avoid routing long high-current or noisy signals on the top or bottom layer. It is recommended to bury them in the mid-layers with solid ground fills on both sides to contain the possible noise.

The **VBAT** pin provides supply voltage to the internal circuitry. It is not part of the boost switch loop or a high current pin.

4.2.2 Improving current loop design

When designing a PCB, follow the guidelines for an improved current loop design.

To reduce the loop antenna area that emits *EMI*, minimize the boost regulator's current loop area. Place components as close as possible to the **PVSS**, **VINT**, and **SW** pins.

Visualize both switching cycles and how the current flows in both cycles on the PCB, including the ground plane. The current should ideally rotate in the same direction in both switching cycles as shown in Figure 12: Boost regulator switching cycles on page 23. This minimizes the change in magnetic field and therefore EMI.

Some inductors have a dot showing the direction of rotation around the core. If possible, place the inductor so that the direction of current follows the rotation of the main current loop.

To minimize current loops, grounds should be close to each other and, if possible, on the same copper area on the top layer and strongly connected to the ground plane.

The following figures show the switching cycles and current paths.

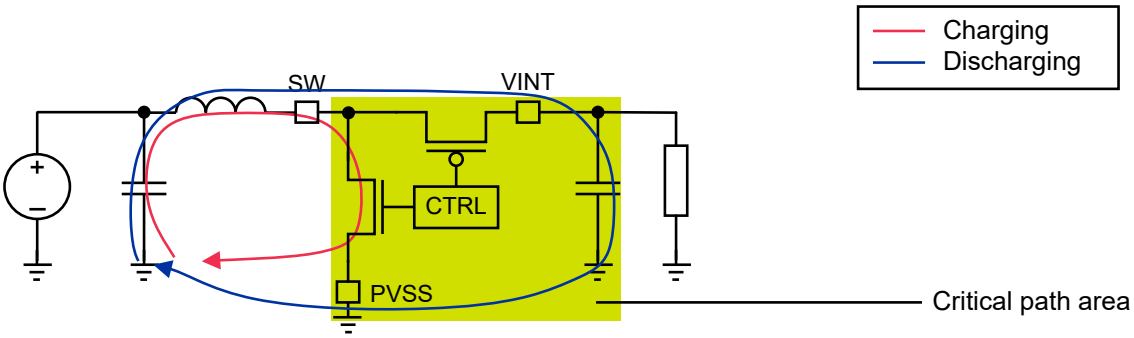

Figure 12: Boost regulator switching cycles

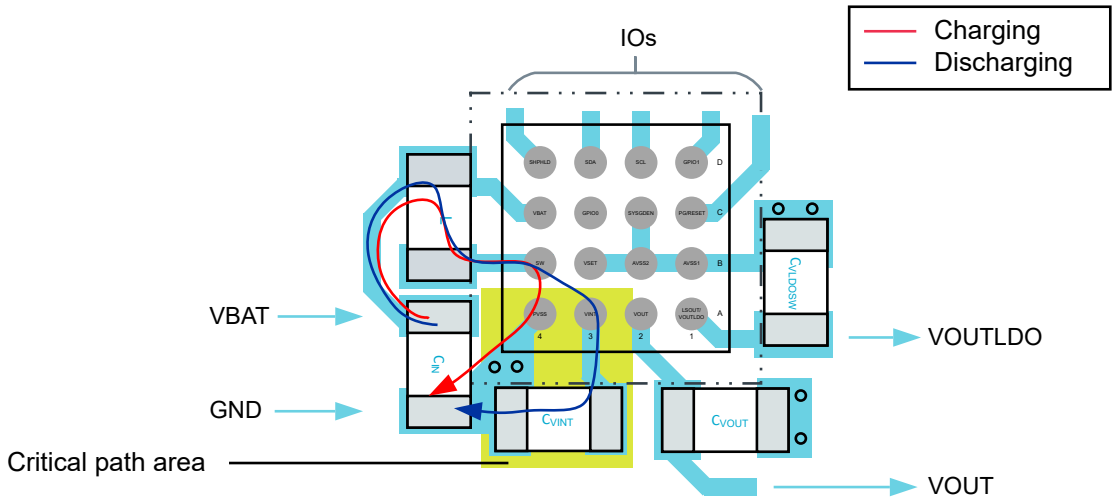

Figure 13: Boost regulator switch cycles and principle for component placement

At low frequencies, the current flows in the path of least resistance, which is typically the shortest path, but at high frequencies the current follows the path of least inductance. This means that at high frequency the return current in the ground plane goes through the path that creates the smallest loop area. In the ground plane this path is right under the positive current on the top layer. Keep the ground plane intact in this area. The following figure shows the current path at low and high frequencies and the area which is marked in grey color where the ground layer should be kept intact.

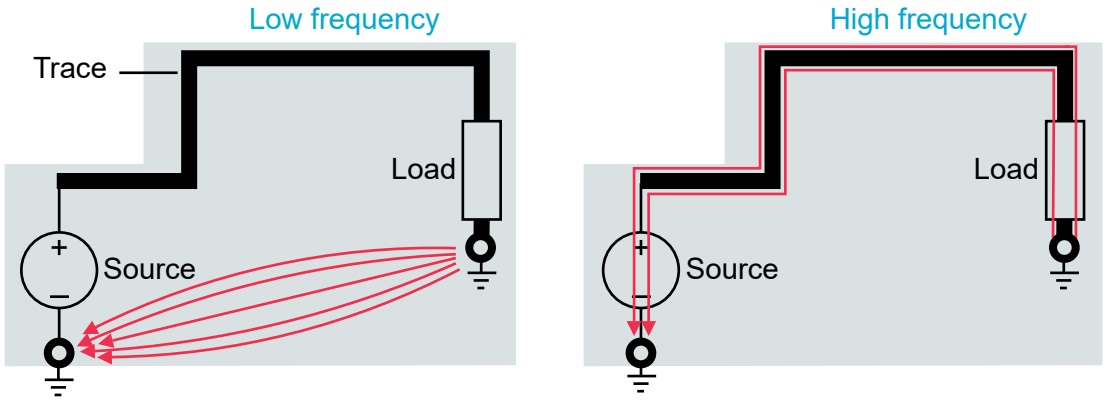

Figure 14: Current paths at low and high frequencies

Consider the following guidelines for the ground layer:

- Keep the ground plane intact.

- A solid ground plane as the second layer is critical. Any traces or routes here are likely to increase the high current loop area and cause issues with EMI, EMC, or radio sensitivity.
- If routing on the ground plane is unavoidable, limit routing directly under nPM2100 to short escape routing and change layer as soon as possible. Do not route under the high current paths on top.
- Distance to the ground plane affects the current loop area. Therefore, it is recommended to use the second layer for ground. Also, using thinner prepreg reduces the loop area.
- Use via stitching to couple the ground plane and ground pours strongly together.

4.2.3 Trace width and via current capability

Follow the design recommendations for trace width and vias.

For high current paths, trace widths must be considered based on the maximum load condition to minimize the voltage drop and inductance.

Via current capabilities must be considered and calculated. The use of more and bigger vias is always better for voltage drop and reduced inductance.

Place ground vias close to the signal via for signal integrity and reduced return path impedance.

Glossary

DC

Direct Current

Electromagnetic Interference (EMI)

Electromagnetic noise or energy that causes disturbance and unwanted effects that interfere with the operation of an electrical circuit.

Evaluation Kit (EK)

A platform used to evaluate different development platforms.

Low-Dropout Regulator (LDO)

A linear voltage regulator that can operate even when the supply voltage is very close to the desired output voltage.

Power Management Integrated Circuit (PMIC)

A chip used for various functions related to power management.

Printed Circuit Board (PCB)

A board that connects electronic components.

Quad Flat No-lead Package (QFN)

A near chip scale package with pads on four sides encapsulated in plastic.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Two-wire Interface (TWI)

An I^2C compatible serial communication protocol that enables devices to exchange data by using a two-wire bus system, allowing multiple devices to be connected and controlled by a master device.

Universal Serial Bus (USB)

An industry standard that establishes specifications for cables and connectors and protocols for connection, communication, and power supply between computers, peripheral devices, and other computers.

Wafer Level Chip Scale Package (WLCSP)

Die size package with an array pattern of solder balls at a pitch that is compatible with circuit board assembly process.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nPM2100 Datasheet
- nPM2100 EK product page
- nPM2100 EK Hardware
- nPM2100 PMIC reference design

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