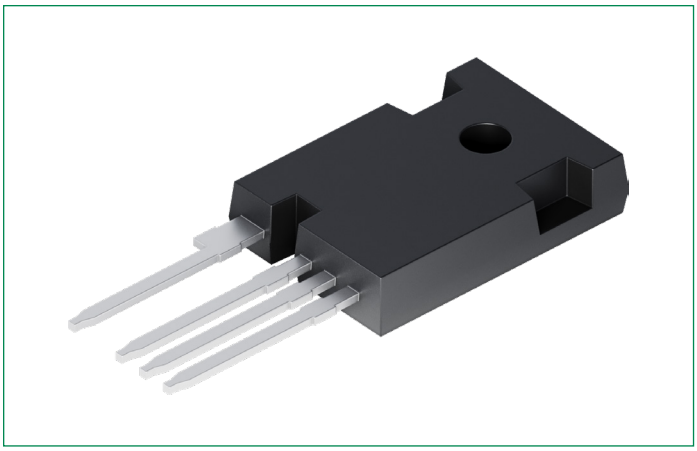
IXSH65N120L2KHV

1200 V, 40 mΩ, 65 A SiC MOSFET

RoHS HF



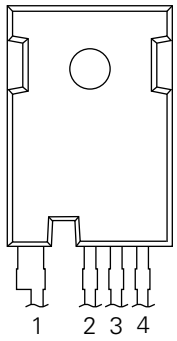
Features

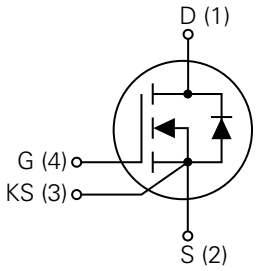
- SiC MOSFET Technology with –3/+15. . .18 V gate drive
- High blocking voltage with low on-state resistance
- High-speed switching with low capacitance
- Maximum virtual junction temperature of T_{vj} = 175 °C
- Ultra-fast intrinsic body diode
- Kelvin source contact
- MSL1 rated

Applications

- Switch mode power supplies
- UPS
- EV charging infrastructure
- Energy storage system

Pinout Diagram (TO-247-4L)





D: Drain; **G:** Gate; **KS:** Kelvin Source; **S:** Power Source

Product Summary

Characteristic	Value	Unit
V_{DSS}	1200	V
$R_{DS(on)}$	40	mΩ
I_D @ 25 °C	65	A

Revised: XZ 01/22/2025 (0.2)

Maximum Ratings (T_c = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value	Unit
V_{DSS}	Drain-source voltage	V_{GS} = 0 V, I_D = 100 µA	1200	V
V_{GSM}	Maximum gate-source voltage	–	–5 to +20	V
	Transient gate-source voltage	$t_{transient}$ = 200 ns, D < 1%	–10 to +23	
I_D	Drain current (continuous) Fig.23	V_{GS} = 18 V, T_c = 25 °C	65	A
		V_{GS} = 18 V, T_c = 100 °C	48	A
I_{DM}	Peak drain current Fig. 25, 26	Pulse width limited by SOA and dynamic $R_{th(j-c)}$	162	A
I_{SM}	Diode pulsed forward current Fig. 25, 26	Pulse width limited by SOA and dynamic $R_{th(j-c)}$	162	A
P_{tot}	Total power dissipation Fig. 24	T_c = 25 °C	375	W
T_{vj}	Virtual junction temperature range	–	–55 to +175	°C
T_{stg}	Storage temperature range	–	–55 to +175	°C
T_{sold}	Soldering temperature	Wave soldering only allowed at leads, 1.6 mm from case for 10 s	260	°C

Recommended Values

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
V_{GSon}	Recommended turn-on voltage	15	–	18	V
V_{GSoff}	Recommended turn-off voltage	–5	–3.5	–2	

Thermal Characteristics

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance from junction to case Fig. 25	–	0.4	–	K/W

Electrical Characteristics – Static (T_c = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DSS}	Drain-source leakage current	V_{DS} = 1200 V, V_{GS} = 0 V	–	5	100	µA
I_{GSS}	Gate leakage current	V_{DS} = 0 V, V_{GS} = –5 ~ 20 V	–	–	±100	nA
$V_{GS(th)}$	Gate threshold voltage Fig. 8, 9	V_{GS} = V_{DS}, I_D = 9 mA	1.8	2.8	4.5	V
		V_{GS} = V_{DS}, I_D = 9 mA, T_{vj} = 175 °C	–	2.1	–	
$R_{DS(on)}$	Drain-source on-state resistance Fig. 4, 5, 6, 7	V_{GS} = 18 V, I_D = 20 A @ T_{vj} = 25 °C	–	40	52	mΩ
		V_{GS} = 18 V, I_D = 20 A @ T_{vj} = 175 °C	–	75	–	
		V_{GS} = 15 V, I_D = 20 A @ T_{vj} = 25 °C	–	50	65	
		V_{GS} = 15 V, I_D = 20 A @ T_{vj} = 175 °C	–	80	–	

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Electrical Characteristics – Dynamic (T_{vj} = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
C_{iss}	Input capacitance Fig. 16	V_{DS} = 800 V, V_{GS} = 0 V, f = 1 MHz, V_{AC} = 25 mV		–	2160	–	pF
C_{oss}	Output capacitance Fig. 16			–	100	–	
C_{rss}	Reverse transfer capacitance Fig. 16			–	5.8	–	
E_{oss}	C_{oss} stored energy Fig. 17			–	40	–	µJ
Q_G	Total gate charge Fig. 18	V_{DS} = 800 V, I_D = 30 A, V_{GS} = –3 to +18 V		–	110	–	nC
Q_{GS}	Gate-source charge Fig. 18			–	25	–	
Q_{GD}	Gate-drain charge Fig. 18			–	59	–	
$R_{g(int)}$	Gate input resistance	f = 1 MHz		–	2.1	–	Ω
E_{on}	Turn-on switching energy Fig. 19, 20	V_{DS} = 800 V, I_D = 30 A, V_{GS} = –3.5 to +18 V, $R_{G(ext)}$ = 3.3 Ω, L = 200 µH	T_{vj} = 25 °C	–	446.3	–	µJ
			T_{vj} = 175 °C	–	644.4	–	
E_{off}	Turn-off switching energy Fig. 19, 20		T_{vj} = 25 °C	–	70	–	
			T_{vj} = 175 °C	–	73.8	–	
$t_{d(on)}$	Turn-on delay time Fig. 19, 20		T_{vj} = 25 °C	–	9.6	–	ns
t_r	Rise time Fig. 19, 20		T_{vj} = 25 °C	–	22.1	–	
$t_{d(off)}$	Turn-off delay time Fig. 19, 20		T_{vj} = 25 °C	–	19.3	–	
t_f	Fall time Fig. 19, 20		T_{vj} = 25 °C	–	10.5	–	

Reverse Diode Characteristics (T_{vj} = 25 °C unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{SD}	Diode forward voltage Fig. 10, 11, 12	I_{SD} = 20 A, V_{GS} = 0 V	–	4.2	–	V
		I_{SD} = 20 A, V_{GS} = 0 V, T_{vj} = 175 °C	–	4	–	V
I_s	Diode forward current (continuous)	V_{GS} = –2 V, T_c = 25 °C	–	–	63	A
		V_{GS} = –2 V, T_c = 100 °C	–	–	36	
t_{rr}	Reverse recovery time	V_{GS} = –3.5 V/+18 V, I_{SD} = 30 A, V_R = 800 V, $R_{G(ext)}$ = 10 Ω, L = 200 µH, di/dt = 3000 A/µs	–	42	–	ns
Q_{rr}	Reverse recovery charge		–	198.1	–	nC
I_{rrm}	Peak reverse recovery current		–	17.4	–	A

Revised: XZ 01/22/2025 (0.2)

Characteristic Curves

Fig. 1. Typical Output Characteristics @ T_{vj} = –55 °C

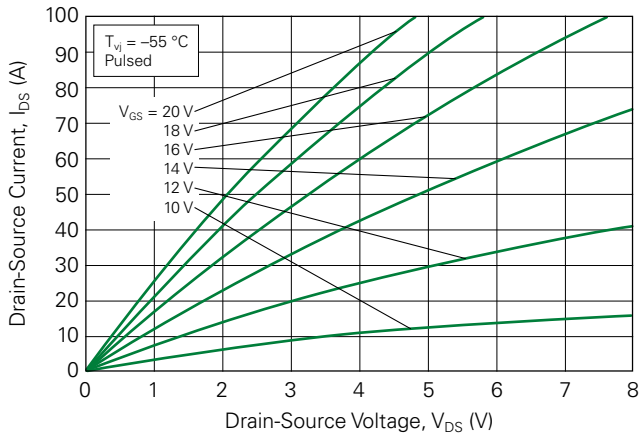


Fig. 2. Typical Output Characteristics @ T_{vj} = 25 °C

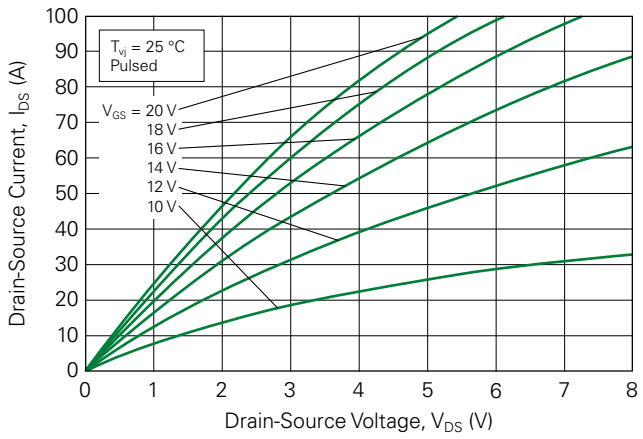


Fig. 3. Typical Output Characteristics @ T_{vj} = 175 °C

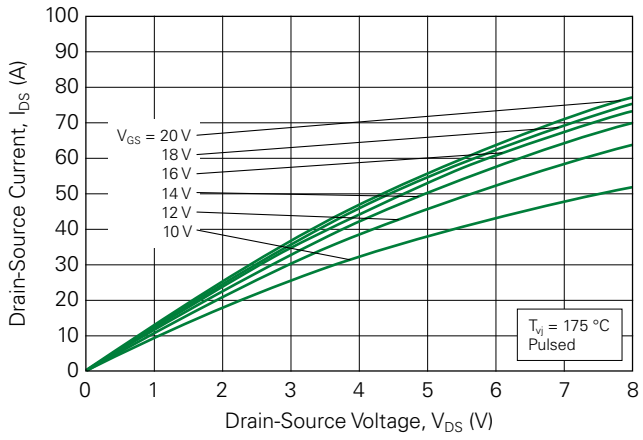


Fig. 4. Typical Drain-source On-state Resistance vs. Junction Temperature

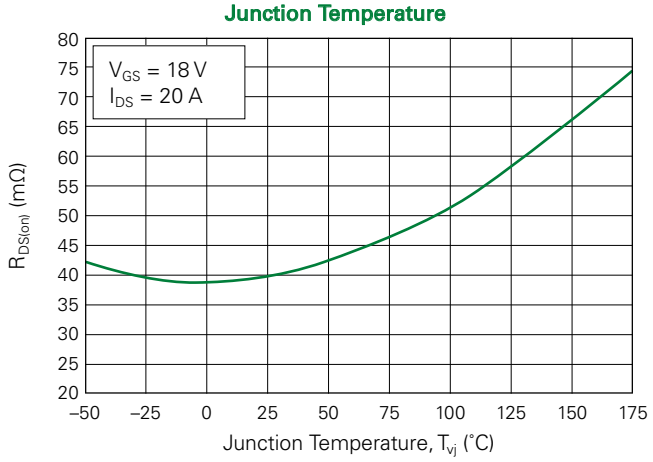


Fig. 5. Typical Drain-source On-State Resistance (Normalized) vs. Junction Temperature

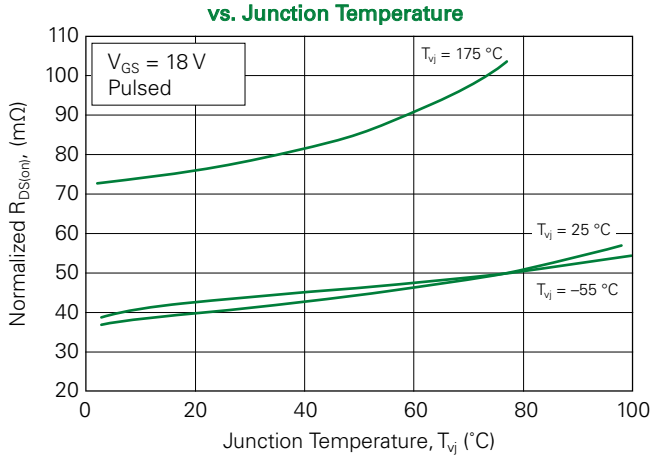


Fig. 6. Typical Drain-source On-state Resistance vs. Drain Current

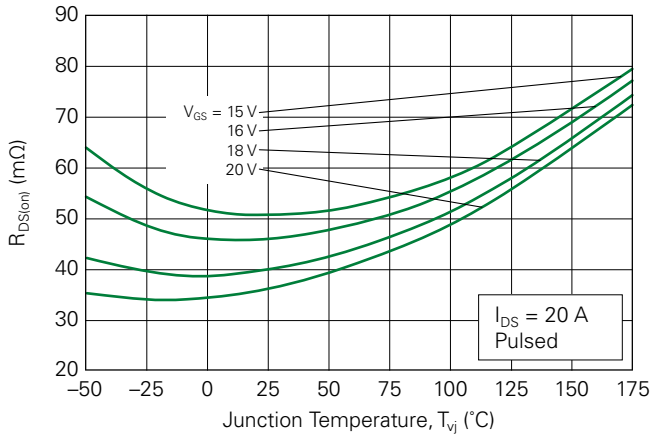


Fig. 7. $R_{DS(on)}$ vs. Temperature

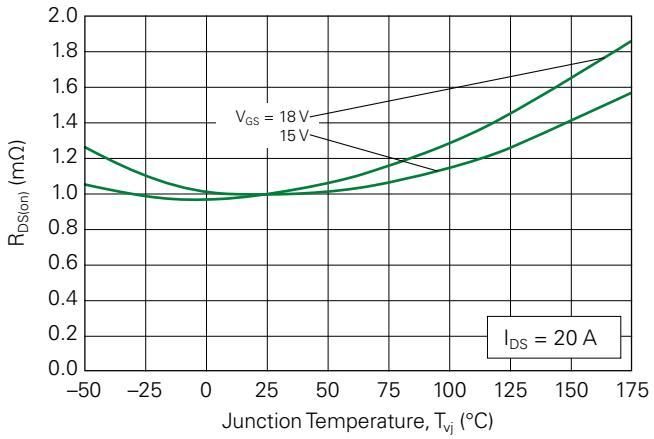


Fig. 8. Transfer Curves

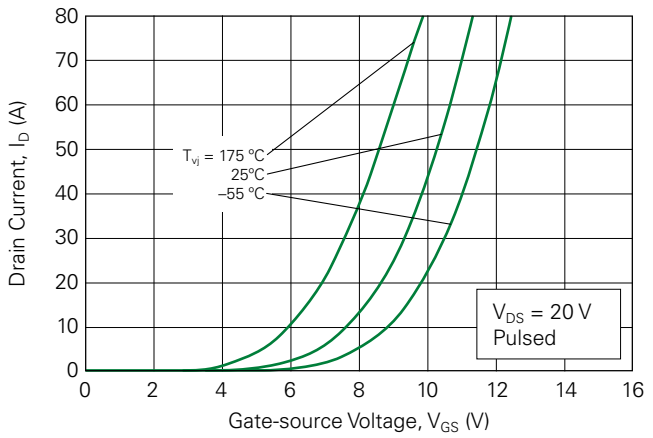


Fig. 9. Threshold Voltage vs. Temperature

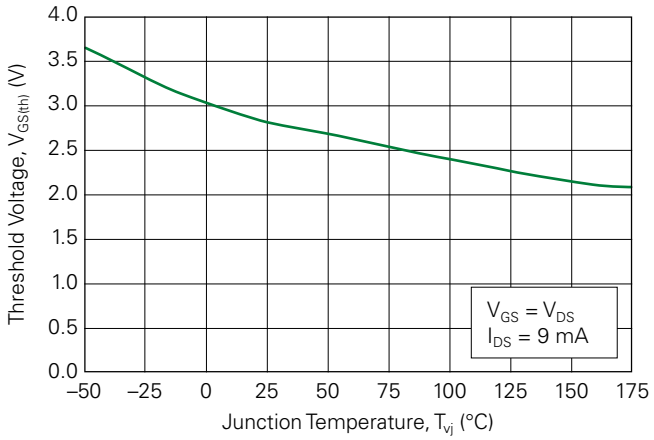


Fig. 10. Body Diode Curves @ T_{vj} = –55 °C

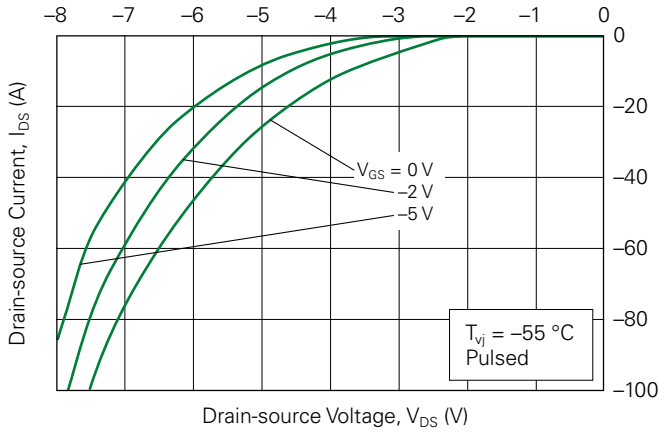


Fig. 11. Body Diode Curves @ T_{vj} = 25 °C

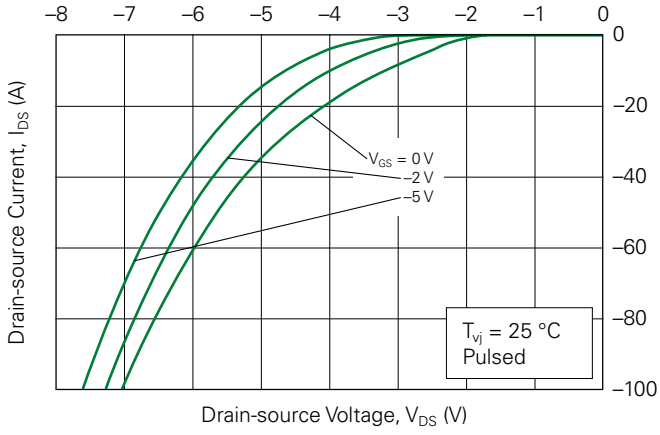


Fig. 12. Body Diode Curves @ T_{vj} = 175 °C

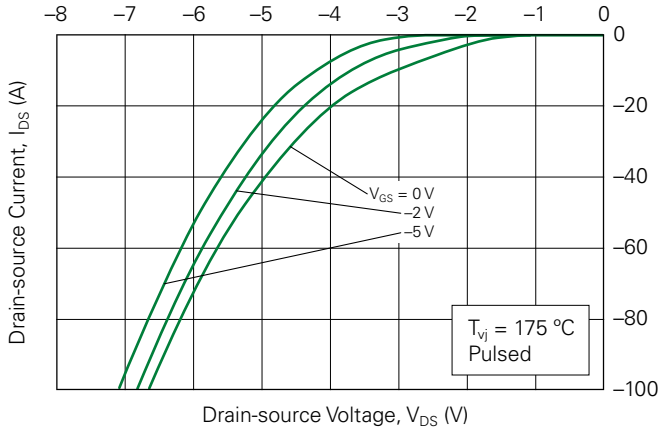


Fig. 13. 3rd Quadrant Curves @ T_{vj} = –55 °C

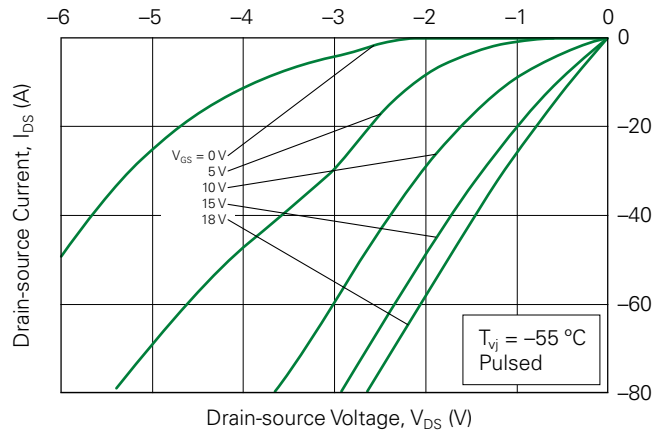


Fig. 14. 3rd Quadrant Curves @ T_{vj} = 25 °C

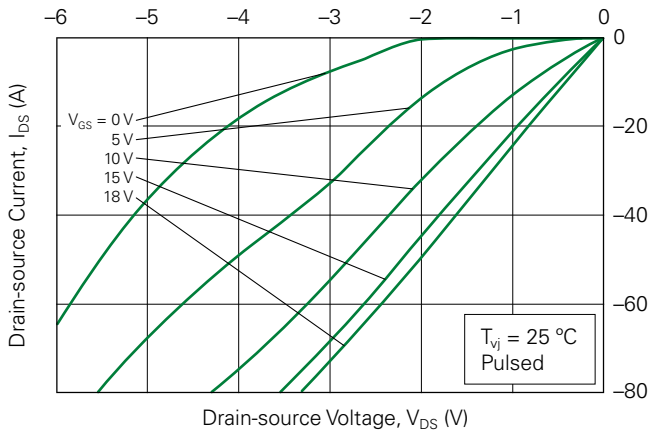


Fig. 15. 3rd Quadrant Curves @ T_{vj} = 175 °C

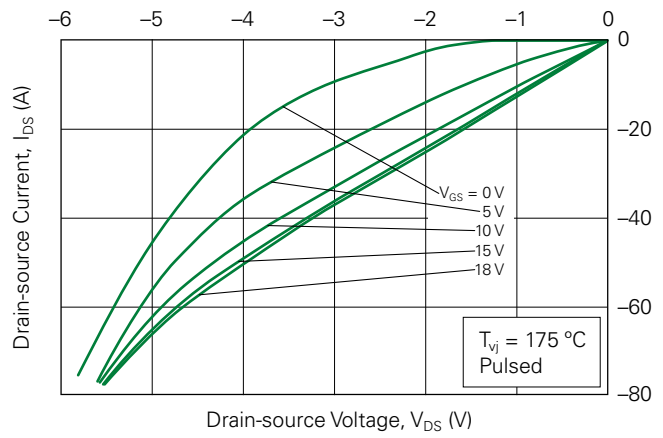


Fig. 16. Capacitance vs. V_{DS}

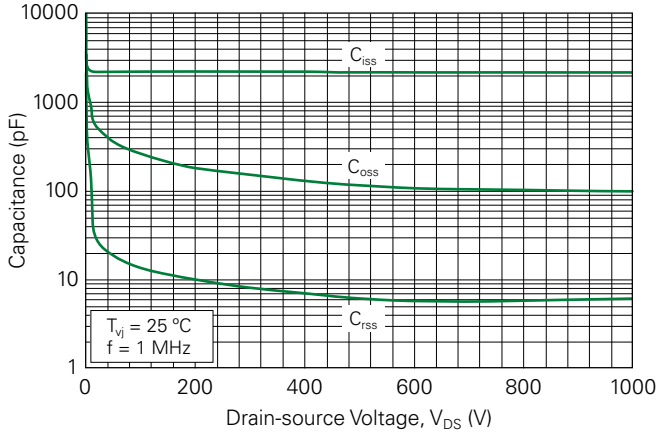


Fig. 17. Output Capacitor Stored Energy

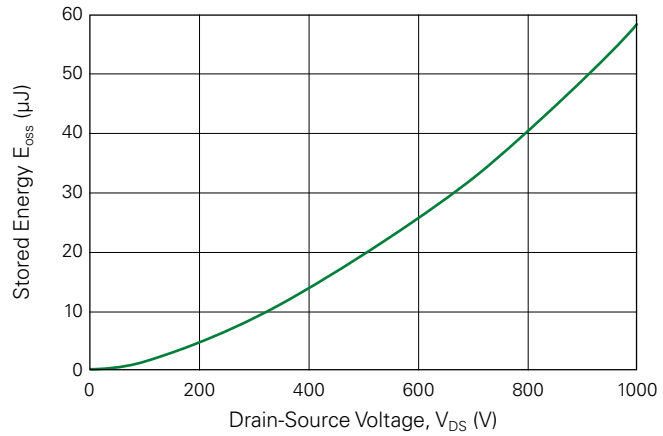


Fig. 18. Gate Charge Characteristics

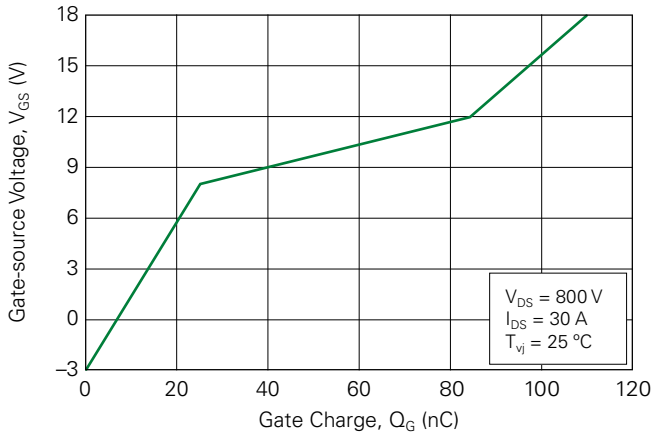


Fig. 19. Switching Energy vs. $R_{G(ext)}$

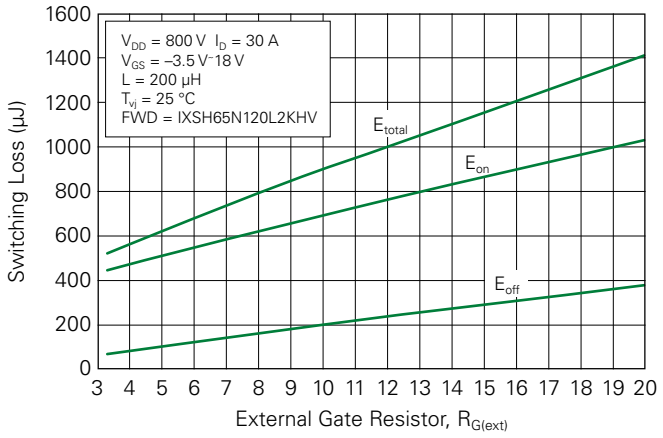


Fig. 20. Switching Times vs. $R_{G(ext)}$

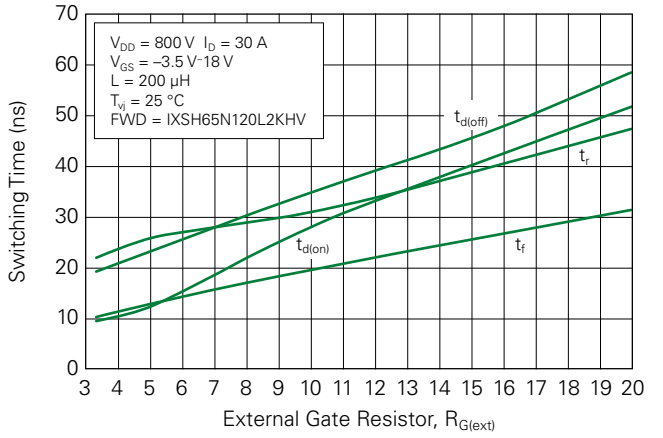


Fig. 21. Switching Energy vs. I_{DS}

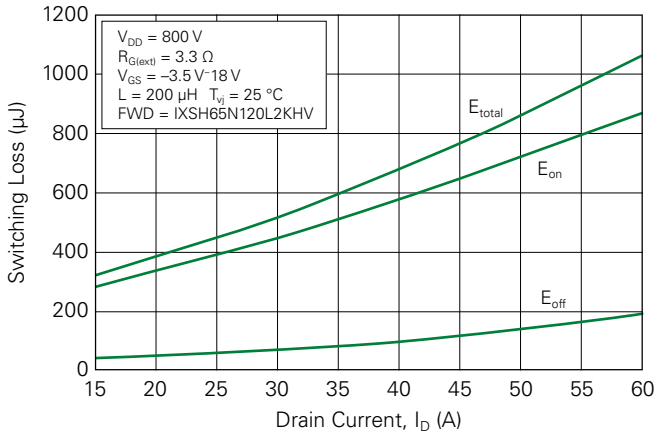


Fig. 22. Switching Energy vs. Temperature

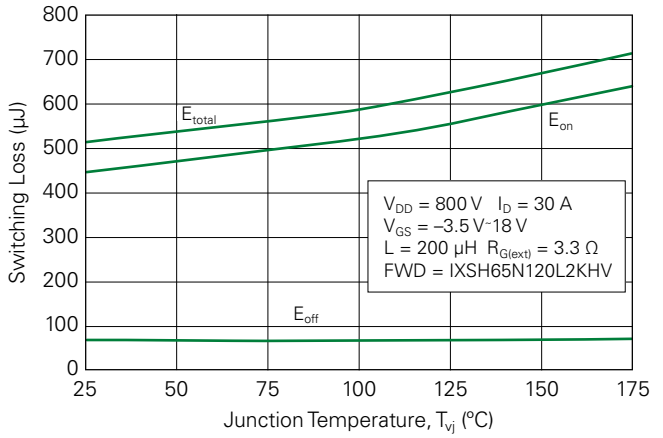


Fig. 23. Continuous Drain Current vs. Case Temperature

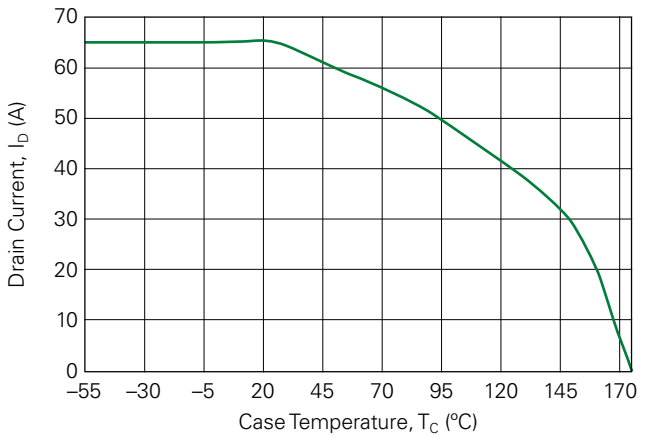


Fig. 24. Max. Power Dissipation Derating vs. Case Temperature

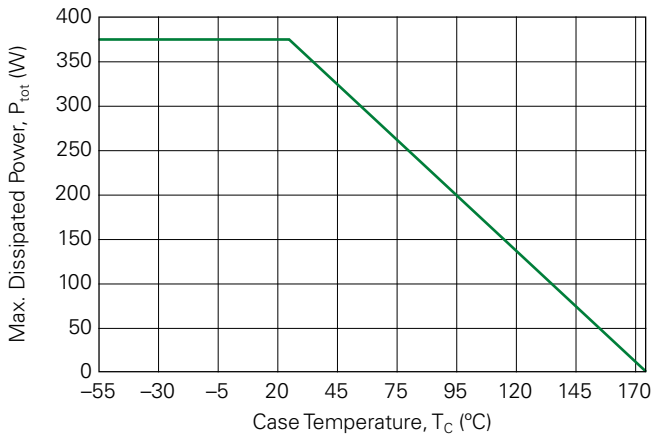


Fig. 25. Thermal Impedance

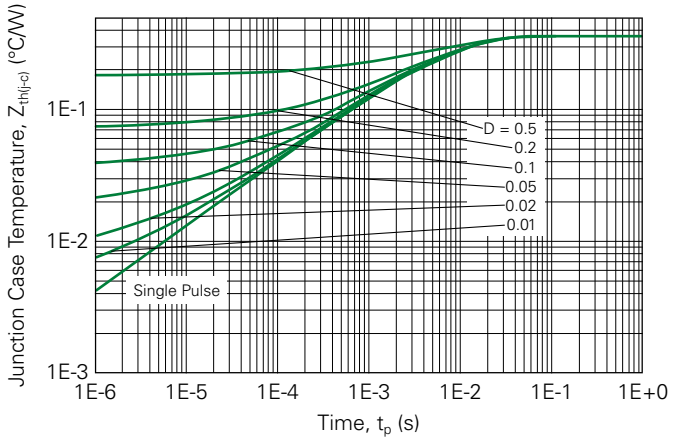
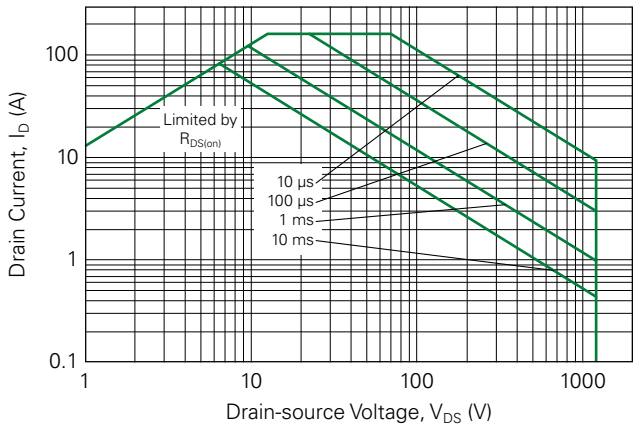
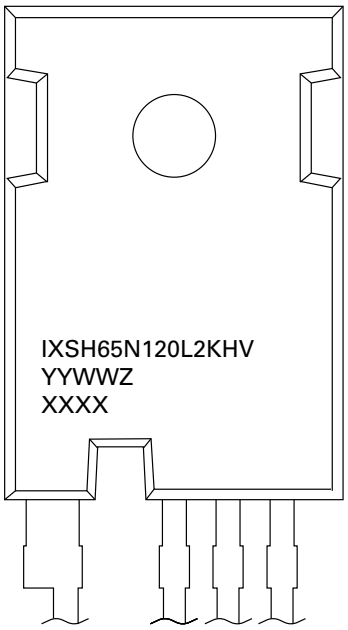


Fig. 26. Safe Operating Area

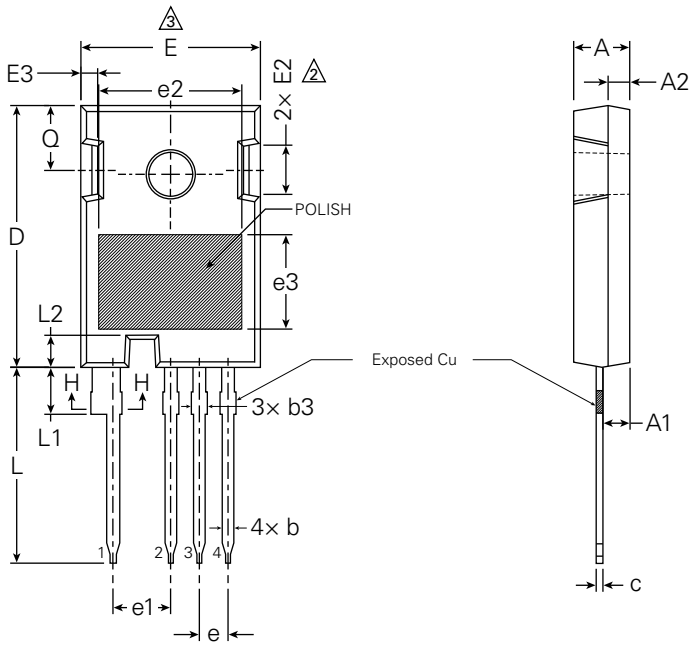


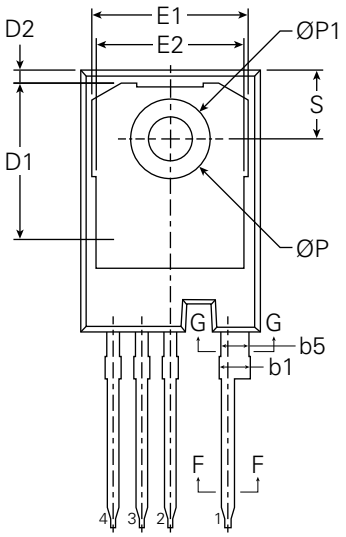
Part Number and Marking

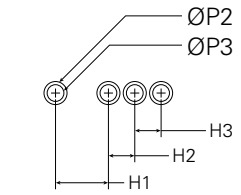


IXSH65N120L2KHV = Specific Device Code
YY = Year
WW = Work Week
Z = Assembly Location
XXXX = Lot Traceability

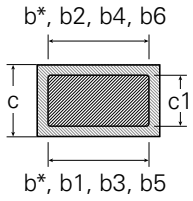
Part Outline Drawing (TO-247-4L)







Recommended Solder Pad Layout



Section F–F, G–G, H–H

Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.190	–	0.205	4.83	–	5.21
A1	0.090	–	0.100	2.29	–	2.54
A2	0.075	–	0.085	1.91	–	2.16
b	0.042	–	0.052	1.07	–	1.33
b*	0.042	–	0.050	1.07	–	1.28
b1	0.094	–	0.116	2.39	–	2.94
b2	0.094	–	0.112	2.39	–	2.84
b3	0.042	–	0.063	1.07	–	1.60
b4	0.042	–	0.059	1.07	–	1.50
b5	0.094	–	0.106	2.39	–	2.69
b6	0.094	–	0.104	2.39	–	2.64
c	0.022	–	0.027	0.55	–	0.68
c1	0.022	–	0.026	0.55	–	0.65
D	0.917	–	0.929	23.30	–	23.60
D1	0.640	–	0.695	16.25	–	17.65
D2	0.037	–	0.049	0.95	–	1.25
E	0.620	–	0.635	15.75	–	16.13
E1	0.516	–	0.557	13.10	–	14.15
E2	0.145	–	0.201	3.68	–	5.10
E3	0.039	–	0.075	1.00	–	1.90
E4	0.487	–	0.529	12.38	–	13.43
e	0.100 BSC			2.54 BSC		
e1	0.200 BSC			5.08 BSC		
e2	–	0.500	–	–	12.70	–
e3	–	0.330	–	–	8.38	–
H1	–	0.200	–	–	5.08	–
H2	–	0.100	–	–	2.54	–
H3	–	0.100	–	–	2.54	–
L	0.681	–	0.702	17.31	–	17.82
L1	0.156	–	0.172	3.97	–	4.37
L2	0.093	–	0.104	2.35	–	2.65
ØP	0.138	–	0.144	3.51	–	3.65
ØP1	0.283 REF.			7.18 REF.		
ØP2	–	0.088	–	–	2.24	–
ØP3	–	0.067	–	–	1.70	–
Q	0.216	–	0.236	5.49	–	6.00
S	0.238	–	0.248	6.04	–	6.30

Note:

1. Package reference: JEDEC TO247, Variation AD
2. Slot required, notch may be rounded
3. Dimension D&E do not include mold flash
4. Subject to change without notice