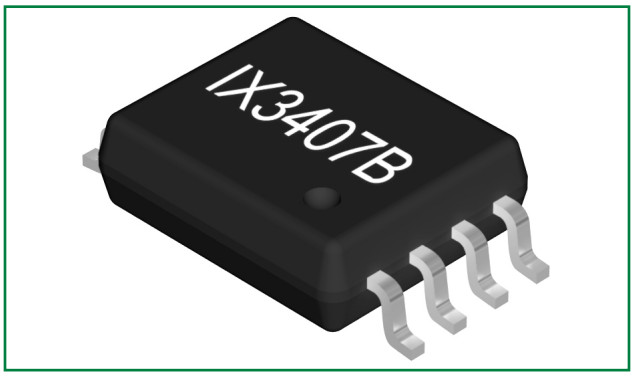
IX3407B

Single-Channel, Isolated IGBT Gate Driver with Separate Outputs



Features

- Drives IGBTs, MOSFETs and SiC MOSFETs
- Separate Source and Sink Outputs
- Source and Sink typical 7A peak Current
- 3.1V to 17V Input Side Operating Voltage Range
- 13V to 35V Output Side Operating Voltage Range
- Under Voltage Lockout (UVLO)
- 2500V_{RMS} Input to Output Isolation

Applications

- AC and Brushless DC Motor Drives
- High Voltage DC/DC Converters and DC/AC Inverters
- Induction Heating Resonant Applications
- UPS Systems
- Welders
- Solar Inverters

Description

The IX3407B is a galvanically isolated, single-channel gate driver that provides a typical 7A peak source and sink output current on separate output pins. Galvanic input to output isolation is provided by isolation technique where low voltage transmitter die and high voltage receiver die are isolated by integrated high voltage capacitors.

Logic inputs tolerant to input voltages up to V_{CC} employ TTL voltage thresholds to support a wide range of control logic devices powered by as low as 3.3V.

Protection is provided for both the input and output sides by Under Voltage Lockout (UVLO) circuitry. Additionally, an active shutdown feature protects the power transistor by pulling OUT– low in the event of an output side voltage supply loss.

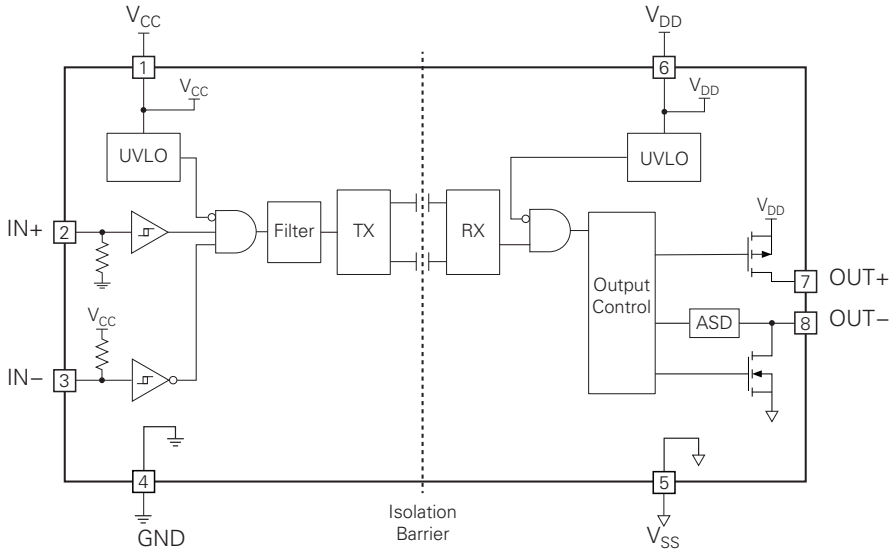
Approvals

- UL 1577 Recognized Component: File E546287

Ordering Information

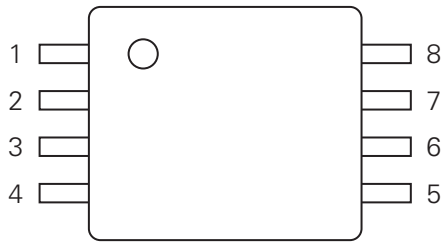
Part Number	Description
IX3407BTR	SOIC-8 Tape and Reel (1000/Reel)

IX3407B Functional Block Diagram



1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin	Name	Pin Type	Description
1	V_{CC}	Power	Input side positive supply voltage
2	IN+	Input	Non-inverting input
3	IN–	Input	Inverting input
4	GND	Power	Input side ground
5	V_{SS}	Power	Output side (Driver) supply return
6	V_{DD}	Power	Output side (Driver) positive supply voltage
7	OUT+	Output	Driver current source output
8	OUT–	Output	Driver current sink output

1.3 Absolute Maximum Ratings

Unless otherwise specified, input side voltages are with respect to GND, output side voltages are with respect to V_{SS}, and electrical ratings are over the operational ambient temperature range.

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Output side supply voltage	V_{DD}	–0.3	+40	V
Driver output voltages (OUT+, OUT–)	V_{OUT}	–0.3	V_{DD} + 0.3	
Input side supply voltage	V_{CC}	–0.3	+18	
Logic input voltages (IN+, IN–)	V_{IN}	V_{GND} – 0.3	V_{CC} + 0.3	
Junction temperature	T_J	–50	150	°C
Storage temperature	T_{STG}	–50	150	
Power Dissipation [1] (T_A = 25 °C)				
Package total	P_{tot}	—	1250	mW
ESD rating (Human Body Model) [2]	V_{ESD}	—	±2	kV

[1] *Dependant on PCB layout and heat dissipation design. Reference the thermal impedance evaluation PCB layout shown in "Figure 2 Thermal Characterization PCB Layout" on page 6.*
[2] *Reference JEDEC JS-001-2017.*

Absolute Maximum Ratings are stress ratings. Stresses in excess of these limits or operation at these limits for extended periods of time can cause permanent damage to the device.

1.4 Recommended Operating Conditions

Input side voltages are referenced to GND and output side voltages are referenced to V_{SS}.

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Output side (Driver) supply voltage	V_{DD}	13	35	V
Input side supply voltage	V_{CC}	3.1	17	
Logic input voltages IN+, IN–	V_{IN}	0	V_{CC}	
Logic input minimum pulse width	t_{IN_min}	130	—	ns
Switching frequency	f_{SW}	—	1	MHz
Ambient temperature	T_A	–40	125	°C
Common Mode Transient Immunity (at 700V) *	CMTI	—	150	kV/µs

** Parameter is not subject to production test - verified by design/characterization.*

1.5 Electrical Characteristics

Unless otherwise noted, performance characteristics are specified at: V_{CC} = 5V, V_{DD} = 15V, $V_{IN–}$ = GND, and –40 °C ≤ T_A ≤ +125 °C. Input side parameters and conditions are referenced to GND with the output side parameters being referenced to V_{SS}. Output "OUT" is OUT+ connected to OUT–.

Typical values are characteristic of the device at T_A = 25 °C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

1.5.1 Input Side Supply Voltage: V_{CC}

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Quiescent supply current						
OUT = High	$V_{IN+} = V_{CC}$	I_{CCQH}	—	11.6	18.7	mA
OUT = Low	V_{IN+} = GND or Open	I_{CCQL}	—	5.35	7.4	
UVLO rising threshold	V_{CC} rising	V_{CCUV_th+}	2.65	2.825	3.0	V
UVLO falling threshold	V_{CC} falling	$V_{CCUV\_th–}$	2.58	2.73	—	
UVLO hysteresis	—	V_{CCUV_hys}	—	95	—	mV

1.5.2 Output Side Supply Voltage: V_{DD}

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Quiescent supply current						
OUT = High	$V_{IN+} = V_{CC}$	I_{DDQH}	—	2.5	4	mA
OUT = Low	V_{IN+} = GND or Open	I_{DDQL}	—	2.35	3.8	
UVLO rising threshold	V_{DD} rising	V_{DDUV_th+}	11.7	12.3	13	V
UVLO falling threshold	V_{DD} falling	$V_{DDUV\_th–}$	10.5	11.4	—	
UVLO hysteresis	—	V_{DDUV_hys}	—	900	—	mV

1.5.3 Logic Inputs (IN+ and IN–)

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Input voltage level						
Logic high	—	V_{IH+}, $V_{IH–}$	2	—	—	V
Logic low		V_{IL+}, $V_{IL–}$	—	—	0.8	
Hysteresis		V_{IN+_hys}, $V_{IN–\_hys}$	0.2	0.3	—	
Input current						
IN+ High	$V_{IN+} = V_{CC}$	I_{IH+}	—	160	260	µA
IN– Low	$V_{IN–}$ = GND	$I_{IL–}$	—	250	360	

1.5.4 Gate Driver Outputs

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Peak output current *						
High level (OUT = High)	$V_{IN+} = V_{CC}$, 1 µF load capacitor	I_{OH}	—	–7	–4	A_P
Low level (OUT = Low)	V_{IN+} = GND	I_{OL}	4	7	—	
Output voltage						
High level	$V_{IN+} = V_{CC}$, $I_{OUT+} = -100$ mA	V_{OH}	V_{DD} – 0.14	—	—	V
Low level	V_{IN+} = GND, I_{OUT-} = 100 mA	V_{OL}	—	—	0.13	
On-resistance						
OUT+	$V_{IN+} = V_{CC}$, $I_{OUT+} = -100$ mA	R_{OH}	—	0.75	1.4	Ω
OUT–	V_{IN+} = GND, I_{OUT-} = 100 mA	R_{OL}	—	0.63	1.3	

** Parameter is not subject to production test - verified by design/characterization.*

1.5.5 OUT+ Short Circuit Clamping

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Clamping voltage ($V_{OUT+} - V_{DD}$) *	$V_{IN+} = V_{CC}$, (OUT+ = High) I_{OUT+} = 500 mA, t ≤ 10 µs	V_{OUT+_CLP}	—	0.5	1	V

** Parameter is not subject to production test - verified by design/characterization.*

1.5.6 Gate Driver Active Shut Down

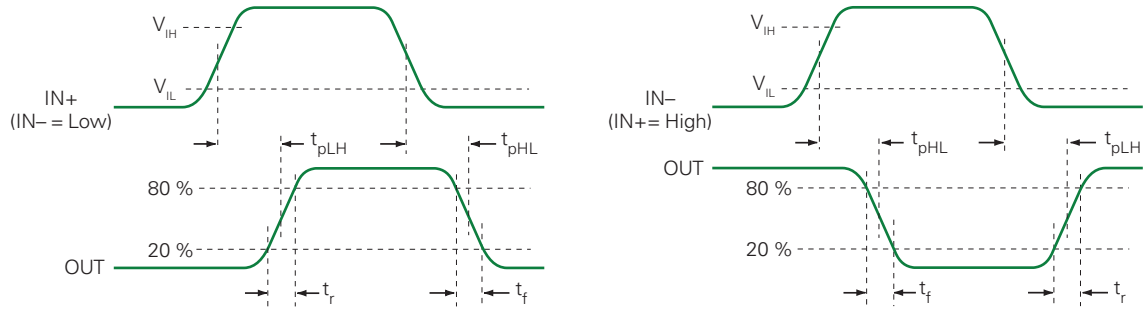
Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Active shut down voltage [1]	V_{DD} = Open, I_{OUT-} = 0.7 A	$V_{OUT-\_ASD\_th}$	—	2.6	3.35	V

[1] Referenced to V_{SS}.

1.6 Timing Characteristics

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Propagation delay time						
Turn-on	C_{OUT} = 1 nF	t_{pLH}	—	154	247	ns
Turn-off		t_{pHL}	—	162	261	
Turn-on rise time (20 % to 80 %)	C_{OUT} = 1 nF	t_r	—	10	20	
Turn-off fall time (20 % to 80 %)		t_f	—	10	20	
Output pulse width distortion $\lvert t_{pLH} - t_{pHL} \rvert$	C_{OUT} = 1 nF, T_A = 25 °C	PWD	—	7.5	27	
Input pulse width suppression	OUT = Open	PW_{min}	—	—	130	

Figure 1 Timing Waveforms



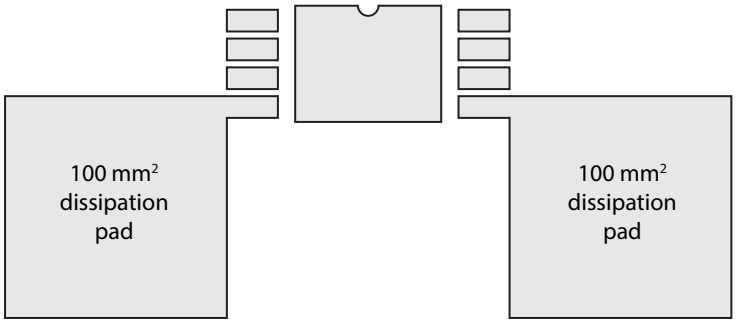
1.7 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal impedance			
Junction to Ambient	θ_{JA}	100	K/W

1.8 Power Ratings

Parameter	Test Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Max. Power Dissipation	V_{CC} = 5V, V_{DD} = 15V, IN– = 0V, IN+ = 50 % duty cycle, 440 kHz, C_L = 10 nF, T_A = 25 °C	P_{tot}	—	—	1250	mW
Max. Power Dissipation by Input Side		P_{IN}	—	—	65.25	
Max. Power Dissipation by Output Side		P_{OUT}	—	—	1184.75	

Figure 2 Thermal Characterization PCB Layout



Standard FR4 PCB with 1 oz (35 µm) copper after plating. Pin 4 and pin 5 thermal heat spreading pads are 100 mm².

1.9 Safety and Insulation Rating

1.9.1 Safety Related Certifications

UL
Recognized under UL 1577 Component Recognition Program, CSA Component Acceptance Notice 5A
Basic insulaton, 2500V_{RMS}
File number: E546287

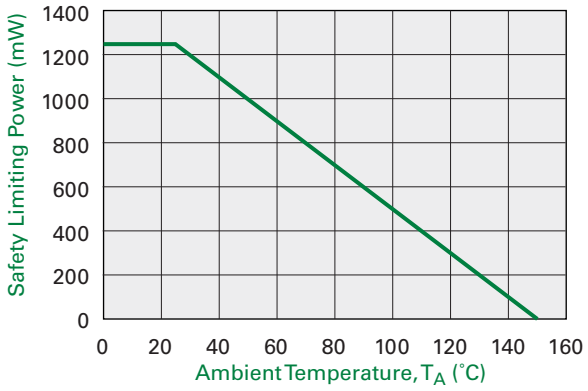
1.9.2 Insulation Specifications

Parameter	Test Conditions	Symbol	Rating	Unit
UL 1577				
Withstand isolation voltage	t = 60 s, RH < 50%, T_A = 25 °C (Qualification)	V_{ISO}	2500	V_{RMS}
	t = 1 s, T_A=25 °C (Production)	$V_{ISO(1s)}$	3000	

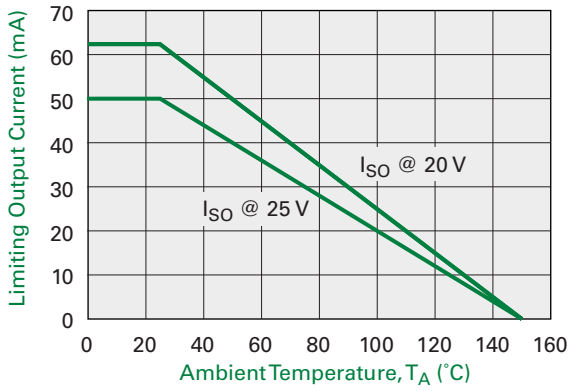
1.9.3 Safety Limiting Values

Parameter	Test Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Safety output	θ_{JA} = 100 °C/W, V_{DD} = 15V, V_{SS} = –5 V, T_J = 150 °C, T_A = 25 °C	I_{SO}	—	—	62.5	mA
	θ_{JA} = 100 °C/W, V_{DD} = 20V, V_{SS} = –5 V, T_J = 150 °C, T_A = 25 °C		—	—	50	
Safety input, output, or total power	θ_{JA} = 100 °C/W, V_{DD} = 15V, V_{SS} = –5 V, T_J = 150 °C, T_A = 25 °C	P_S	—	—	1250	mW
Safety temperature	—	T_S	—	—	150	°C

Safety Limiting Power vs. Ambient Temperature

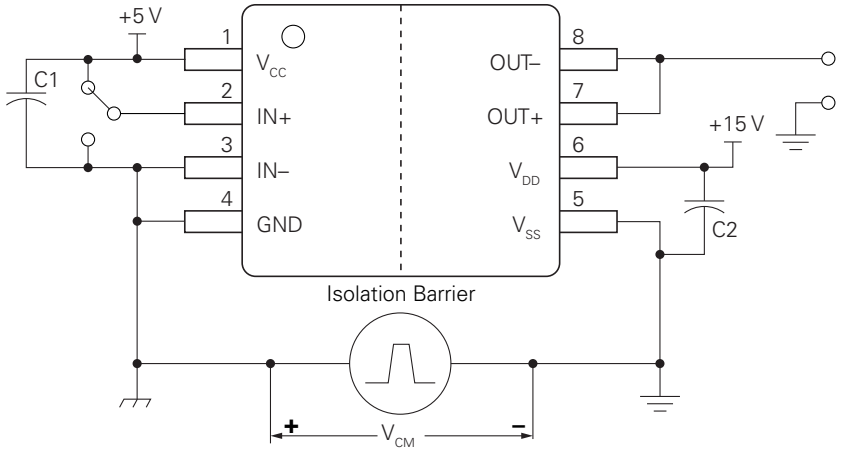


Limiting Output Current vs. Ambient Temperature



1.10 Test Diagrams

Figure 3 Common Mode Transient Immunity Test Circuit

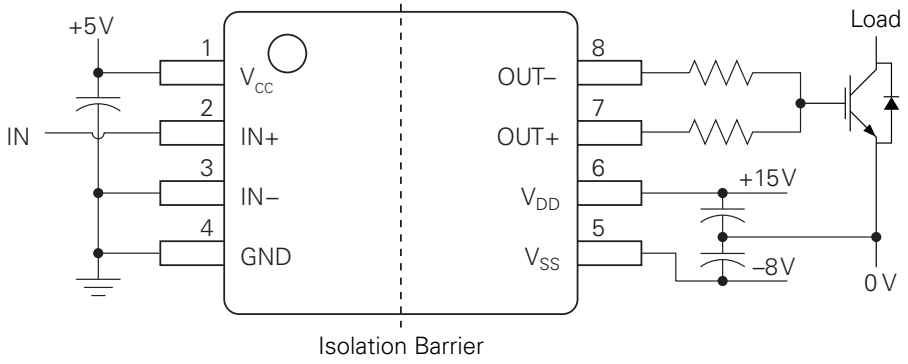


Note: C1 = 1 nF, C2 = 1 µF ceramic capacitors. The values of decoupling capacitors depend on application.

2 Functional Description

Designed to provide gate drive for high power IGBTs, the IX3407B is well suited for also driving MOSFET and SiC MOSFET gates. Supplying essential protection and control functionality enables straightforward designs, while minimizing design times of low-cost, highly-reliable systems. The proprietary capacitive isolation technique provides 2500V_{RMS} of input control logic side to output gate driver side isolation, thereby ensuring driver safe and reliable operation.

Figure 4 IX3407B Typical Application Circuit



2.1 Power Supplies

As the IX3407B input side is isolated from the driver output side, each side has independent voltage supply and returns (grounds). On the input side, power is supplied by V_{CC} and is grounded by the GND pin, while the output side power is supplied by V_{DD}; with V_{SS} being the return. V_{SS} can be biased to either a 0V ground rail, or a negative voltage supply for IGBT applications. These two output side biasing styles are commonly referred to as unipolar and bipolar respectively. In unipolar mode, V_{SS} is at the same potential as V_{EE}; the IGBT emitter. For MOSFET applications, V_{SS} would be at the same potential as the source voltage.

With bipolar supplies, the driver is operated with a positive supply voltage at the V_{DD} pin and a negative supply voltage on the V_{SS} pin, both with respect to V_{EE}; the supply voltage of the IGBT emitter. Typically, applications are operated with V_{DD} = 15V and V_{SS} = –8V relative to V_{EE}, as shown above in Figure 4, the "IX3407B Typical Application Circuit." Using a negative supply can help prevent dynamic turn-on due to the current flowing from the IGBT collector, through the Miller capacitor, to the gate driver OUT– output.

To assure proper startup and behavior when a supply voltage is lost or drops below a preset threshold, each side is equipped with Under Voltage Lockout circuitry.

2.2 Logic Inputs (IN+, IN–)

In order to simplify circuit design, the IX3407B provides both non-inverting and inverting inputs using TTL voltage level thresholds and are input voltage tolerant up to the V_{CC} supply voltage level. This flexibility allows designing to a wide range of predetermined conditions, or upgrading a preexisting product model with minimal, or no modification to the control logic hardware, or firmware.

The IN+ and IN– logic inputs control the state of the high-current source and sink driver outputs, OUT+ and OUT– respectively. These TTL voltage level threshold inputs are high-speed Schmitt trigger buffers with a typical 300 mV of hysteresis. To ensure a defined start up behavior, internal resistors pull the non-inverting input IN+ to GND, while the inverting input IN– is pulled up to V_{CC}, thereby ensuring the power device is off by pulling its gate down to V_{SS}.

Before being passed across the isolation barrier to the output control circuitry, the input side control signal is filtered to ensure high and low logic pulses shorter than the minimum PW_{min} specification are rejected. This enables the circuit to operate reliably with very large, or small input signal duty cycles, or when operating in a noisy environment.

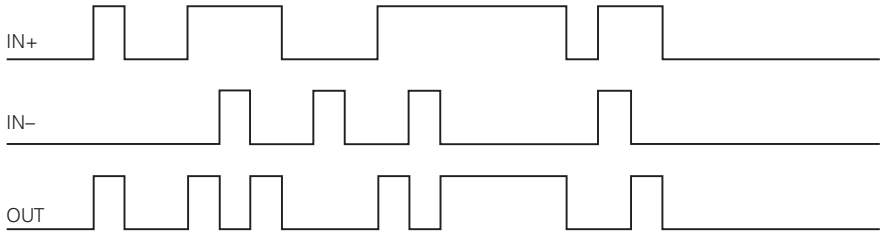
Although the IX3407B has two inputs, the gate driver is easily controlled using only one. To configure the driver as non-inverting, tie the IN– input to GND and apply the control signal to IN+. For an inverting driver tie IN+ to V_{CC} and apply the control signal to IN–. If using an external resistor to condition the IN+, or IN– high, or low, care must be taken to account for the voltage drop across the internal pull down (IN+) and pull up (IN–) resistors. The resistor values can be calculated with V_{CC} = 5V and typical leakage currents listed in 1.5.3 Logic Inputs table. The IN– pull-up resistor is 31.25 kΩ and IN+ pull-down resistor is 20 kΩ.

Table 1: Function Table

IN+	IN–	UVLO [3]		OUT+	OUT–	OUT [1]
		V_{CC}	V_{DD}			
X	X	X	1	Hi-Z	Low	V_{SS}
X	X	1	X	Hi-Z	Low	V_{SS}
0 [2]	X	X	X	Hi-Z	Low	V_{SS}
X	1 [2]	X	X	Hi-Z	Low	V_{SS}
1	0	0	0	High	Hi-Z	V_{DD}

[1] *OUT = OUT+ tied to OUT–.*
[2] *Or floating.*
[3] *UVLO = 0: Sufficient supply voltage.*
UVLO = 1: Insufficient supply voltage.

Figure 5 Logic Diagram



Note: V_{CC} and V_{DD} power supply UVLO must be off.

2.3 Gate Drive Outputs (OUT+ and OUT–)

The IX3407B gate drive outputs are rated for a minimum peak current of 4A, with a typical peak current of 7A. Independent source (OUT+) and sink (OUT–) outputs enable implementation of low-cost asymmetrical charge and discharge rates of the power device gate, through separate resistors between the driver outputs and the gate. To minimize power losses, an internal dead time prevents output cross conduction.

2.4 Short Circuit Clamping

Under conditions where the current through an IGBT begins to rapidly increase, such as when the load short circuits, charge may be transferred from the collector to the gate via the Miller capacitor, causing the gate voltage and subsequently the gate driver output voltage to increase. When the gate driver output voltage exceeds V_{DD}, the driver's positive voltage supply, an internal circuit clamps the rising voltage. The IX3407B is capable of passing 500mA for 10µs. For greater current or durations, an auxiliary external clamp should be provided.

2.5 Protection

The IX3407B provides two forms of protection: Under Voltage Lockout (UVLO), where the driver outputs are held low when either one of the positive voltage supplies is too low, and an Active Shutdown circuit that drives the power transistor off, whenever the output side positive supply is lost and sufficient gate charge persists.

2.5.1 Under Voltage Lockout (UVLO)

As a safety feature, the IX3407B contains UVLO circuitry on both the input-side and the driver (output) side, which monitors the supply voltage of their respective section. They prevent both intentional and false turn-on of the driver output, until the input and output-side supply voltages have attained their minimum required potentials for proper operation. As determined by internally set thresholds. Input control signals are permitted to manage the load only after both UVLO circuits have cleared; until then, output conditioning is independent of the input-control signal and the outputs are held in the off state, which clamps the power transistor gate to the V_{SS} level. During the off state, the driver is reset forcing OUT+ to a high impedance and OUT– to V_{SS}. The Function Table illustrates this aspect of the driver's behavior.

Under voltage lockout prevents the driver from unintended biasing of the power transistor gate, thereby preventing the power transistor from being fully or partially turned on. Without UVLO, a partial turn-on can occur whenever the driver side supply voltage is sufficient to initiate conductance through the power transistor, but less than the voltage required to fully turn the power transistor on.

Under voltage lockout will occur during start-up, prior to the power supplies reaching an acceptable operating level, during normal operation, anytime either supply drops below the internally set minimum threshold level and on power-down. Hysteresis is provided to separate the supply

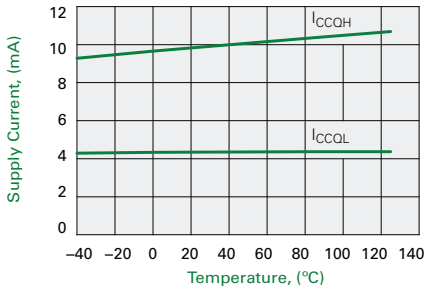
rising and falling thresholds, in order to provide continuous operation in the presence of noise and voltage drops in the supplies. While the UVLO hysteresis provides partial immunity to power supply transients, it does not mask large voltage changes in the supplies.

2.5.2 Active Shut Down

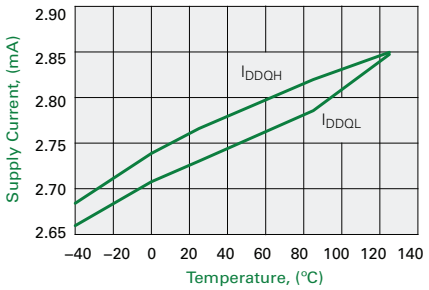
As a complement to the Under Voltage Lockout feature, the IX3407B offers an Active-Shut-Down (ASD) mechanism, to drain the IGBT/MOSFET gate charge whenever the driver-side-supply voltage is insufficient to operate the OUT– pull down FET, and excessive gate bias and charge is present at the OUT– pin.

3 Performance Data

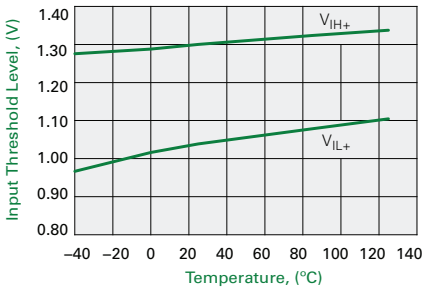
Input Quiescent Current vs. Temperature (V_{IN+} = V_{CC}, I_{CCQH} and V_{IN+} = GND or Open, I_{CCQL})



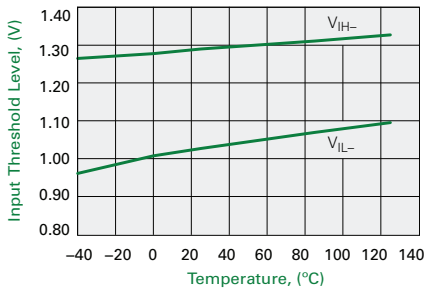
Output Quiescent Current vs. Temperature (V_{IN+} = V_{CC}, I_{DDQH} and V_{IN+} = GND or Open, I_{CCQL})



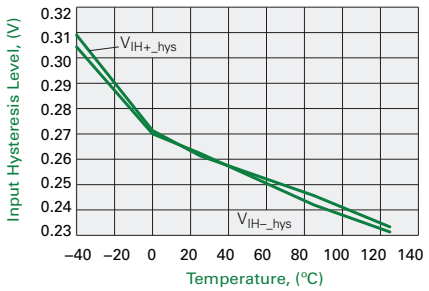
Input Threshold IN+ vs. Temperature



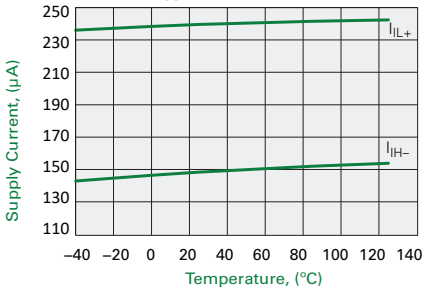
Input Threshold IN- vs. Temperature



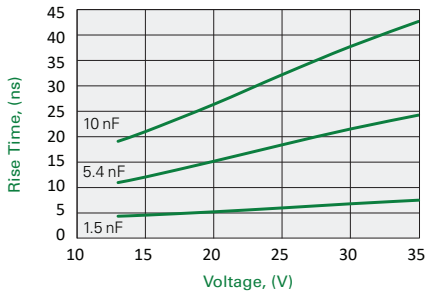
Logic Input Hysteresis vs. Temperature



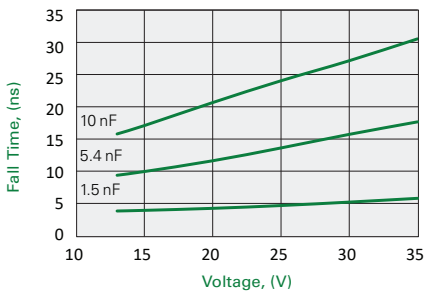
Logic Input Currents vs. Temperature (V_{IN+} =V_{CC}, I_{IH+} and $V_{IN–}$ = GND, $I_{IL–}$)



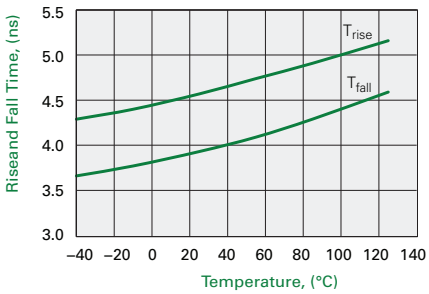
Rise Time vs. Supply Voltage (V_{DD}, T_A = 25 °C)



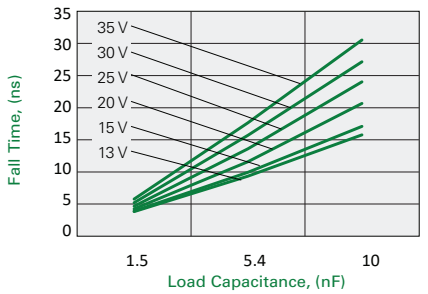
Fall Time vs. Supply Voltage (V_{DD}, T_A = 25 °C)



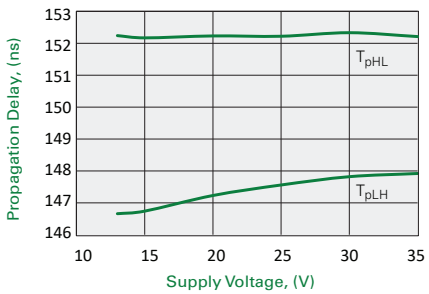
Rise and Fall Time vs. Temperature (V_{DD} = 15 V, C_{OUT} = 1.5 nF)



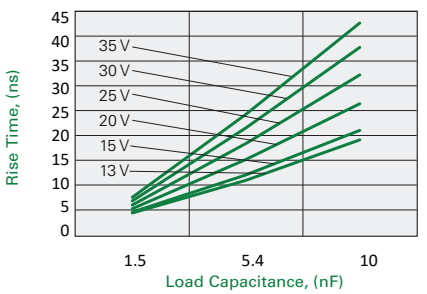
Fall Time vs. Load Capacitance at Various V_{DD} Levels



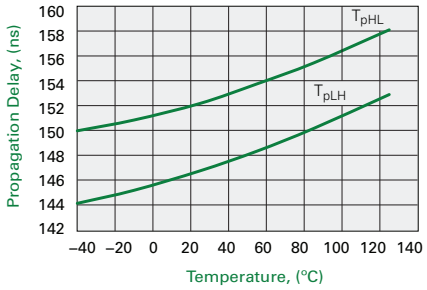
Propagation Delay vs. (V_{DD}, C_{OUT} = 1.5 nF, T_A = 25 °C)



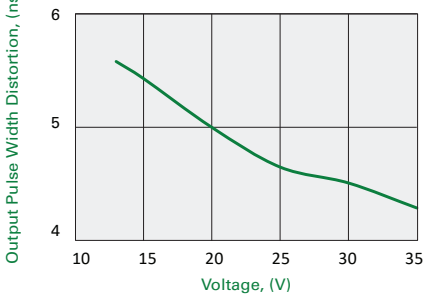
Rise Time vs. Load Capacitance at Various V_{DD} Levels



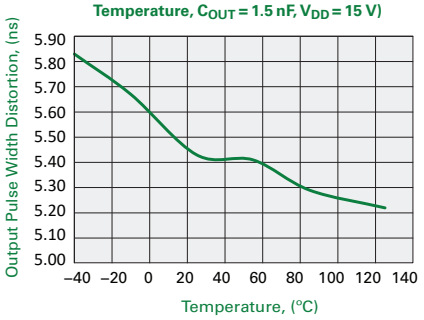
Propagation Delay vs. Temperature (C_{OUT} = 1.5 nF, V_{DD} = 15 V)



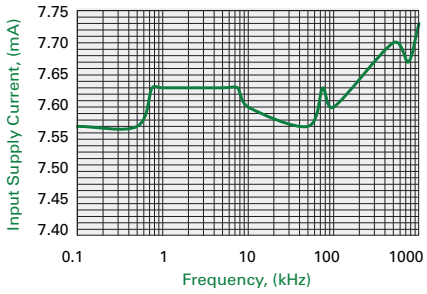
Output Pulse Width Distortion | tpLH-tpHL | C_{OUT} = 1.5 nF, T_A = 25 °C



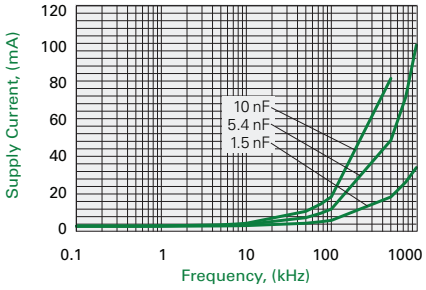
Output Pulse Width Distortion | tpLH-tpHL | vs. Temperature, C_{OUT} = 1.5 nF, V_{DD} = 15 V)



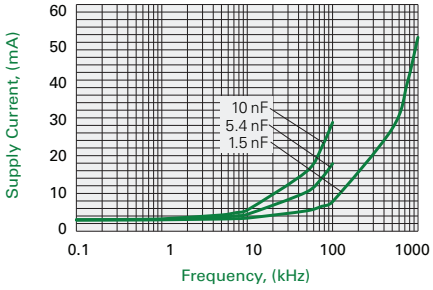
Input Supply Current vs. Frequency (V_{CC} = 5 V, V_{DD} = 15 V, T_A = 25 °C)



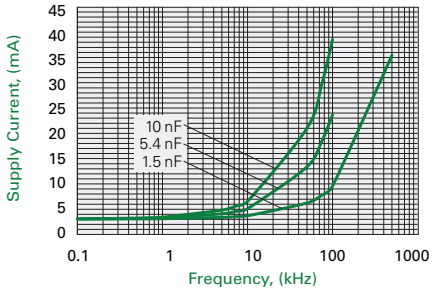
Supply Current vs. Frequency, V_{DD} = 15 V



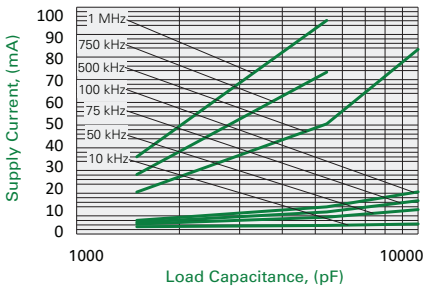
Supply Current vs. Frequency, V_{DD} = 25 V



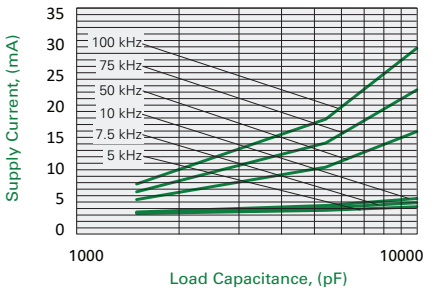
Supply Current vs. Frequency, V_{DD} = 35 V



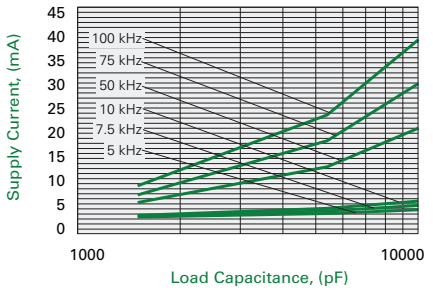
Supply Current vs. Load Capacitance (V_{DD} = 15 V, T_A = 25 °C)



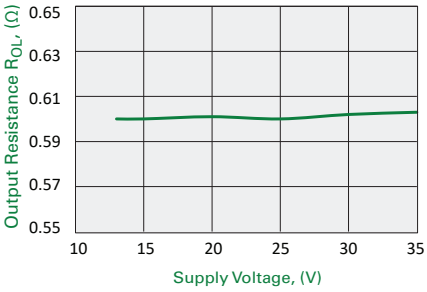
Supply Current vs. Load Capacitance (V_{DD} = 25 V, T_A = 25 °C)



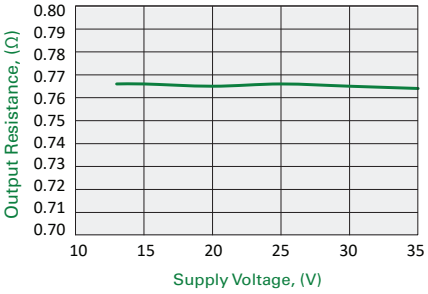
Supply Current vs. Load Capacitance (V_{DD} = 35 V, T_A = 25 °C)



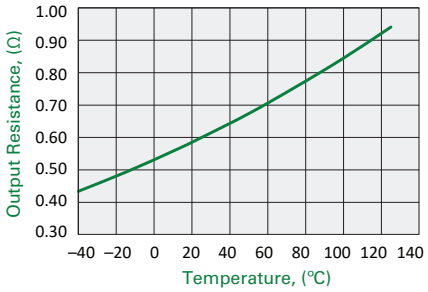
Low State Output Resistance vs. Supply Voltage (V_{IN+} = GND, I_{OUT} = +100 mA)



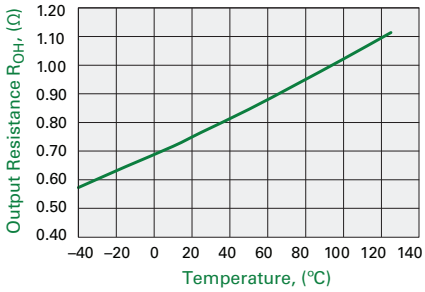
High State Output Resistance vs. Supply Voltage (V_{DD}, I_{OUT} = –100 mA)



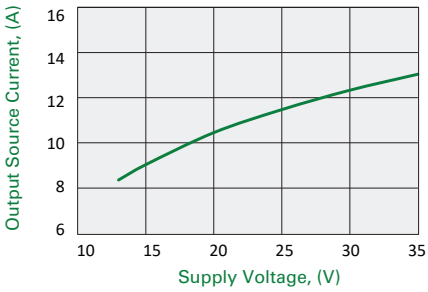
Low State Output Resistance vs. Temperature (V_{DD} = 15 V, I_{OUT} = 100 mA)



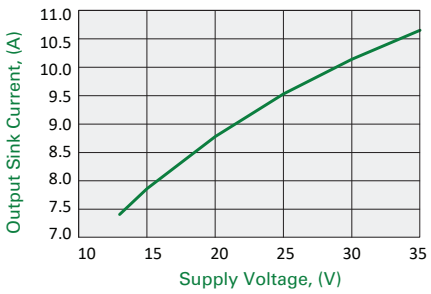
High State Output Resistance vs. Temperature (V_{DD} = 15 V, I_{OUT} = –100 mA, V_{IN+} = V_{CC})



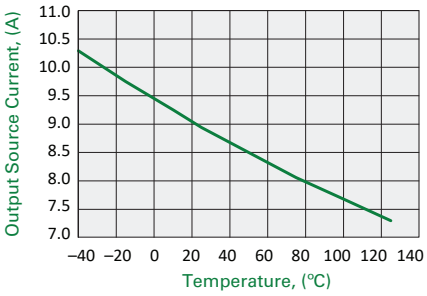
Output Source Current vs. Supply Voltage (V_{DD}, C_L = 1 µF, T_A = 25 °C)



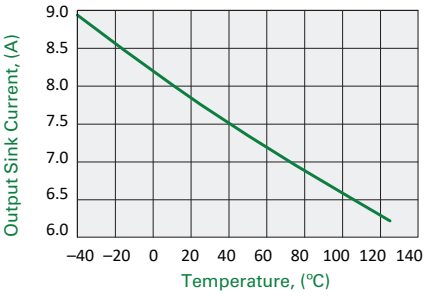
Output Sink Current vs. Supply Voltage (V_{DD}, C_L = 1 µF, T_A = 25 °C)



Output Source Current vs. Temperature (V_{DD} = 15 V, C_L = 1 µF)



Output Sink Current vs. Temperature (V_{DD} = 15 V, C_L = 1 µF)



4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest revision of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest revision of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX3407B	MSL 3

4.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time (T_C–5 °C). The Classification Temperature sets the Maximum Body Temperature allowed for these devices, during reflow soldering processes.

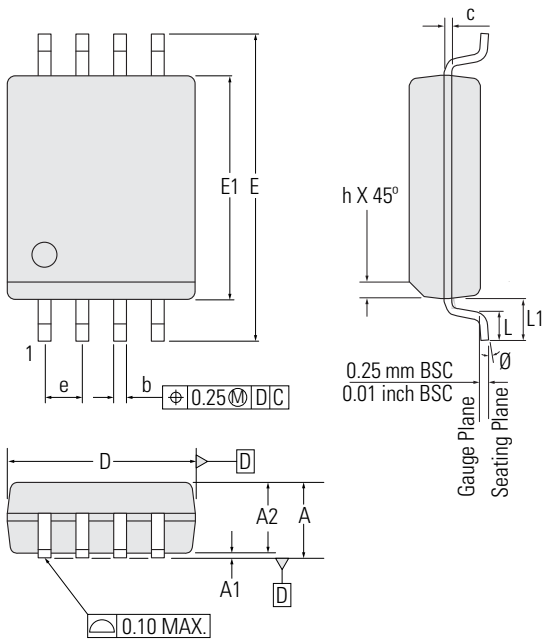
Device	Classification Temperature (T_C)	Dwell Time (T_P)	Max Reflow Cycles
IX3407B	260 °C	30 seconds	3

4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce, or remove flux residue following the solder reflow process is acceptable, provided proper precautions are taken to prevent damage to the device. These precautions include, but are not limited to: Using a low pressure wash and providing a follow-up bake cycle sufficient to remove any moisture trapped within the device, due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning, or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

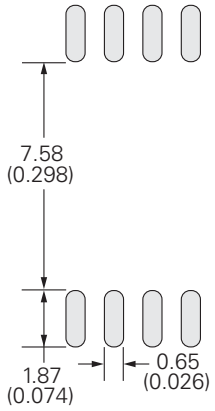
4.5 Mechanical Dimensions

4.5.1 SOIC-8



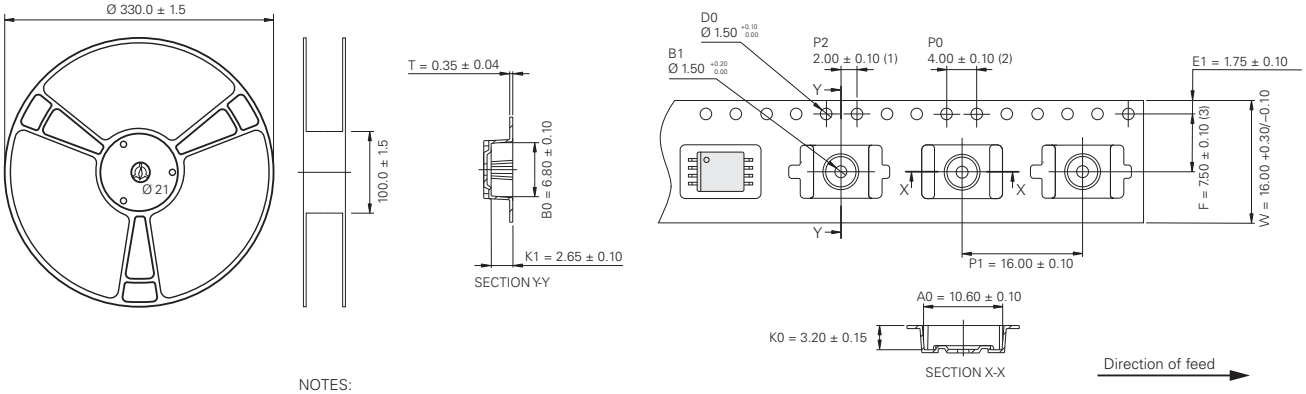
SYMBOL	mm		inch	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.20	0.004	0.008
A2	2.25	2.45	0.089	0.096
b	0.30	0.50	0.012	0.020
c	0.23	0.33	0.009	0.013
D	6.30 BSC		0.248 BSC	
E	10.30 BSC		0.406 BSC	
E1	7.50 BSC		0.295 BSC	
e	1.27 BSC		0.050 BSC	
L	0.50	0.90	0.020	0.035
L1	1.40 REF		0.055 REF	
h	0.25	0.75	0.010	0.030
Ø	0°	8°	0°	8°

Recommended PCB Land Pattern



NOTES:
1. Controlling dimension: millimeter
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
   Mold flash, protrusions and gate burrs shall not exceed 0.15 mm per side.
3. Dimension "E1" does not include inter-lead flash or protrusions.
   Inter-lead flash and protrusions shall not exceed 0.25 mm per side.

4.5.2 Tape and Reel Packaging



NOTES:
(1) Measured from centreline of sprocket hole to centreline of pocket.
(2) Cumulative tolerance of 10 sprocket holes is ±0.20.
(3) Measured from centreline of sprocket hole to centreline of pocket.
(4) Other material available.
(5) Dimension with ( ) is used for dessgin reference purposes,
NO measurement required.