knowles
DLI•Novacap•Syfer•Voltronics

SPECIFICATION

1. SCOPE

This specification covers the characteristics of the “ST” series size 4040, COG/NP0 dielectric, 1.1 nF capacitance, +/- 5% tolerance, 10000 VDC rated stacked ceramic chip capacitor with “J” shaped tab leads. RoHs compliant.

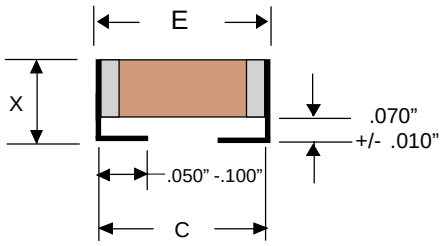
2. DIELECTRIC CHARACTERISTICS - COG/NP0

Operating Temperature Range:	-55°C to +125°C
Temperature Coefficient:	0 +/- 30 ppm/°C
Dissipation Factor:	0.1% Max. @ 25°C
Insulation Resistance, 25°C:	>100 Giga-Ohms or >1000 Ohm-Farads, whichever is less
Insulation Resistance, 125°C:	>10 Giga-Ohms or >100 Ohm-Farads, whichever is less
Dielectric Withstanding Voltage:	12000 VDC
Aging Rate:	0% per decade
Test Parameters:	1KHz, 1.0 Volts +/- 0.2 Vrms, 25°C
Lead Material:	Solder Coated Copper

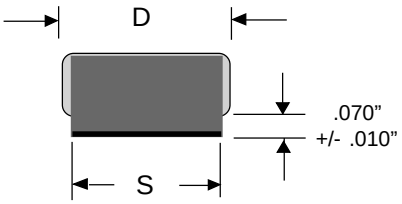
3. PHYSICAL DIMENSIONS (NOT SCALED)

TOP VIEW

FRONT VIEW



SIDE VIEW



dimensions	E	D	X	S	C
inches (mm)	.480 (12.2)	.400 (10.2)	.380 (9.65)	.400 (10.2)	.430 (10.9)
+/- in (mm)	Max	.025 (.635)	Max	.025 (.635)	.025 (.635)

4. PART NUMBER DESCRIPTION

ST 4040 N 112 J 103 TJ X W - 1 R

ST	= Stacked Capacitors Assembly
4040	= Size
N	= COG/NP0 Dielectric
112	= Capacitance Code (pF): First two digits are significant, third digit denotes number of zeros
J	= Capacitance tolerance: J = +/- 5%
103	= DC Voltage Rating: First two digits are significant, third digit denotes number of zeros
TJ	= Tab Leaded, “J” Shaped Configuration
X	= Overall Height: .380” Max. (9.65mm Max.)
W	= Packaging: Waffle Pack
- 1	= Quantity of stacked capacitors in the assembly
R	= RoHS compliant with exemptions 7a and 7cII.

REVISION: A

NOVACAP P/N: ST4040N112J103TJXW-1R
CUSTOMER:
CUST. P/N:

SPEC DESIGNER	MK 7/6/2016
SPEC MANAGER	BN 7/6/2016
ENGINEERING	BN 7/6/2016