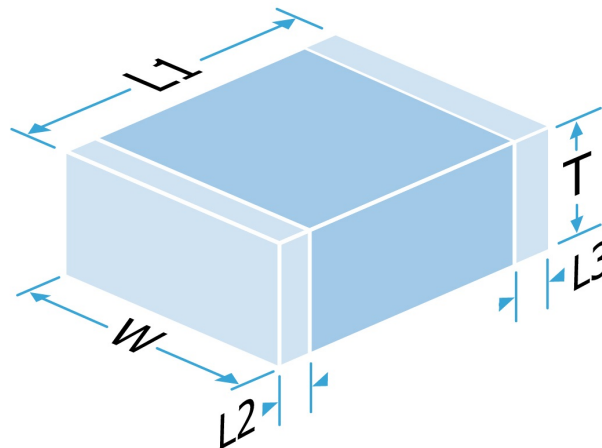


Multilayer Ceramic Chip Capacitor

Part Number: C11AH130G-9UN-X1T

Description: C11 250Vdc 13pF $\pm 2\%$ P90 Porcelain - Hi Q
Single-side marked

A range of high frequency, High Q capacitors for multiple challenging applications such as DC Blocking, Impedance Matching, Coupling, Bypass and Frequency Discrimination (Filtering). The AH range is targeted at temperature compensation applications.



Mechanical Specification

Size Code	C11 (0505 package)
Length (L1) in mm (")	1.477 \pm 0.391 (0.059 \pm 0.016)
Width (W) in mm (")	1.416 \pm 0.451 (0.056 \pm 0.018)
Thickness (T) in mm (")	1.334 Max (0.053 Max)
Minimum Termination Band (L2,L3) in mm (")	0.193 (0.008)
Maximum Termination Band (L2,L3) in mm (")	0.733 (0.029)
Termination Material	Nickel Barrier, Sn/Pb Plated Solder (Min 10% Lead, non RoHS)
Solderability	Per MIL-STD-202, Method 208
Packaging	7" Reel Horizontal Orientation, 3500 per reel

General Electrical Specification

Rated Voltage	250Vdc
Nominal Capacitance Value	13pF
Capacitance Tolerance	$\pm 2\%$
Tangent of Loss Angle (Tan δ)	≤ 0.0005
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current)	625Vdc (375Vdc if marked)
Min Insulation Resistance (IR)	1000.00GOhm @ 250Vdc
Dielectric Classification	P90 Porcelain - Hi Q
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage +90 \pm 20ppm/°C Rated DC Voltage -
Climatic Category (IEC)	-
Ageing Characteristic	Zero

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Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Monday, October 18, 2021

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Multilayer Ceramic Chip Capacitor

Part Number: C11AH130G-9UN-X1T

Description: C11 250Vdc 13pF $\pm 2\%$ P90 Porcelain - Hi Q Single-side marked

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU

Non Compliant

REACH Compliant

Contains 0.1 to 1.0% w/w Lead (CAS 7439-92-1)

California Proposition 65

Risk of exposure to lead (CAS 7439-92-1)

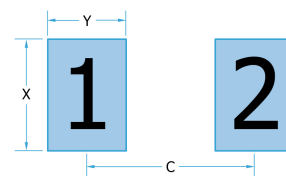
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

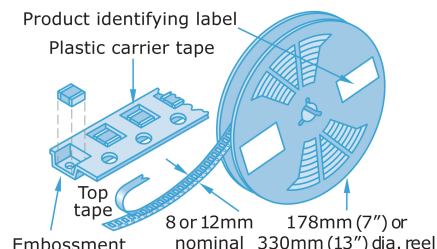
	C11 (0505 package)	
C	1.25mm	0.049"
Y	1.04mm	0.041"
X	1.88mm	0.074"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

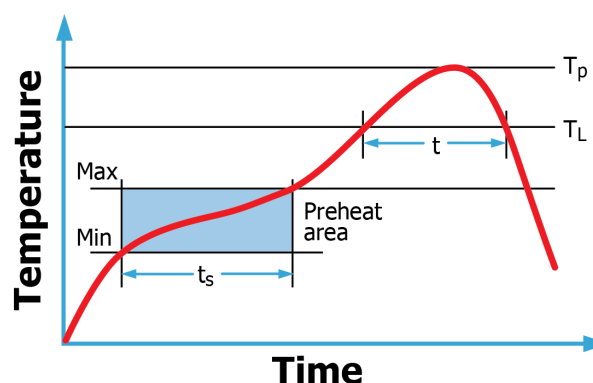
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Compex

DLI

Johanson MFG

Novacap

Syfer

Voltronics

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