SDIT/8GB
SDIT/16GB
SDIT/32GB
SDIT/64GB

Specification

Version: A

Revision History

Date	Revision	Description	Notes
04/13/23	A	Preliminary	

Introduction

SDHC/SDXC cards offer large volume data storage and optimized recording performance with support for FAT32/exFAT file formats. In addition, SD cards use new speed rating known as Ultra High Speed(UHS) performance, which delivers a minimum data transfer rate for optimum performance with respective host devices.

1. Part Number

Class	UHS-I	VSC	App Class	Capacity	Part Number(s)
Class 10	U3	V30	A1	8GB	**SDIT/8GB**
Class 10	U3	V30	A1	16GB	**SDIT/16GB**
Class 10	U3	V30	A1	32GB	**SDIT/32GB**
Class 10	U3	V30	A1	64GB	**SDIT/64GB**

2. SDHC/SDXC memory Card Features

Table 1: SD Card Features

Label Design, Contents, Media Format

Design	Standard	
Contents	None (OEM Design Available)	ID. MKB Programmed
Security Functions	SD Security Specification Ver. 4.00 Compliant (Non-CPRM based) *CPRM: Contents Protection for Recording Media Specification	
Logical Format	SD File System Specification Ver. 3.00 Compliant SDHC Card – FAT32 SDXC Card – exFAT.	

Physical, Electrical

Electrical	Operating Voltage: 2.7V to 3.6V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible DS/HS: Signaling Voltage 3.3V UHS104: Signaling Voltage 1.8V SD Physical Layer Specification Version 6.10 Compliant	
Physical	L: 32, W: 24, T: 2.1 (mm), Weight: 3g (Max) 2g (Typ) SD Physical Layer Specification Version 6.10 Compliant	
Durability	Comply to SD Physical Layer Specification Version 6.10	
ROHS	ROHS Compliant	

3. Compatibility

Compliant Specifications

SD Memory Card Specifications

- Compliant with PHYSICAL LAYER SPECIFICATION Ver.6.10. (Part1)
- Compliant with FILE SYSTEM SPECIFICATION Ver.3.00. (Part2)
- Compliant with SECURITY SPECIFICATION Ver.4.00. (Part3)

4. Physical Characteristics

4.1 Temperature

1) Operation Conditions Temperature Range: Ta = -40 °C to +85 °C

2) Storage Conditions Temperature Range: Tstg = -40 °C to +85 °C

4.2 Moisture (Reliability)

1) Operation Conditions Temperature 25 °C / 95% rel. humidity

2) Storage Conditions Temperature 40 °C / 93% rel. humidity / 500h

4.5. Physical Characteristics

Mechanical Write Protect Switch

A mechanical sliding tablet on the side of the card can be used to enable write protection. The host system shall be responsible for this function.

The card is in a "Write Protected" status when the tablet is located on the "Lock" position. The host system shall not write nor format the card in this status.

The card is in "Write Enabled" status when the tablet is moved to the opposite position (Un-Lock). (Please refer the figures below for the tablet position.)

Please slide the tablet till the dead end (stopped position).
The tablet is set on the "Write Enabled" position when it is shipped.

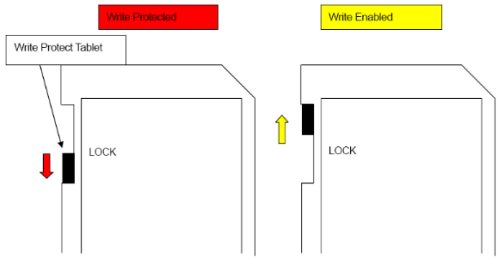

Figure 1: Write Protect Tablet Polarity (Front View)

5. Electrical Interface Outlines

5.1. SD Card Pins

Table 4 describes the pin assignment of the SD card.

Fig.2 describes the pin assignment of the SD card.

Please refer the details descriptions by SD Card Physical Layer Specification.

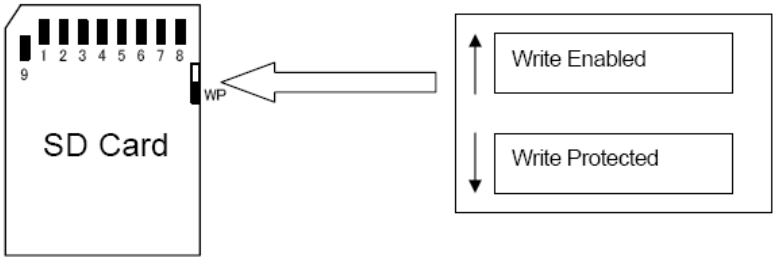

Figure 2: SD Card Pin Assignments (back view of the card)

Pins	SD Mode			SPI Mode		
	Name	IO Type	Description	Name	IO Type	Description
1	CD/ DAT3	I/O/ PP	Card Detect/ Data Line[Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Ground	V_{SS}	S	Ground
4	V_{DD}	S	Supply Voltage	V_{DD}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O/PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[Bit1]	RSV	—	Reserved(*)
9	DAT2	I/O/PP	Data Line[Bit2]	RSV	—	Reserved(*)

Table 4: SD Card Pin Assignment

S : power supply;
I : input;
O : output using push-pull drivers;
PP: I/O using push-pull drivers
(*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

5.2 SD Card Bus Topology

The device supports two alternative communication protocols: SD and SPI Bus Mode. It is as same as standard SD memory card. Host System can choose either one of modes. Same Data of the device can read and write by both modes. SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage of SPI Mode is loss of performance, relatively to the SD Mode.

5.2.1 SD Bus Mode Protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the Device will use only DAT0. After initialization, host can change the bus width. Multiplied SD cards connections are available to the host. Common VDD, VSS and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.
This feature allows easy trade-off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

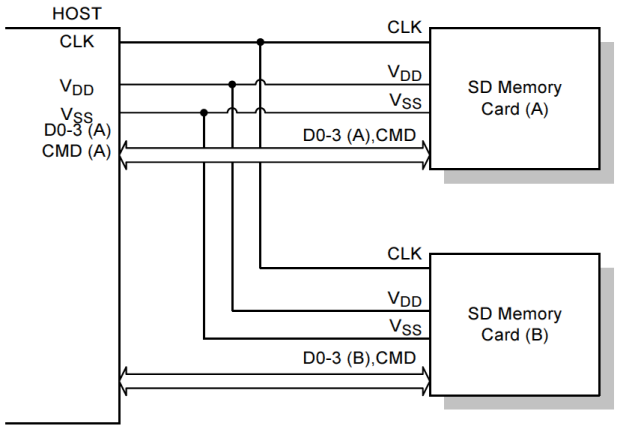

Figure.3: Bus Connection Diagram (SD Mode)

CLK : Host card Clock signal
CMD : Bi-directional Command/ Response Signal
DAT0 - DAT3 : 4 Bi-directional data signal
V_{DD} : Power supply
V_{SS} : GND

Table.5: SD Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD11	VOLTAGE_SWITCH	+	UHS-I Mode
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD19	SEND_TUNING_PATTERN	+	UHS-I Mode
CMD20	SPEED_CLASS_CONTROL	+	
CMD23	SET_BLOCK_COUNT	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD26	Reserved for Manufacturer	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
CMD60	Reserved for Manufacturer	+	
CMD61	Reserved for Manufacturer	+	
CMD62	Reserved for Manufacturer	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	1.8V Signaling and XPC (SDXC Power Control) support
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD44	GET_MID	+	

- CMD28, 29 and CMD30 are Optional Commands.
- CMD4 is not implemented because DSR Register(Optional Register)
- CMD56 is for vendor specific command. Which is not defined in the standard card.

5.2.2 SPI Bus Mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).
The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.
All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design-in effort.
Especially, MMC host can be modified with little change.
The disadvantage of the SPI mode is the loss of performance versus SD mode.
Caution: Please use SD Card Specification. DO NOT use MMC Specification.
For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

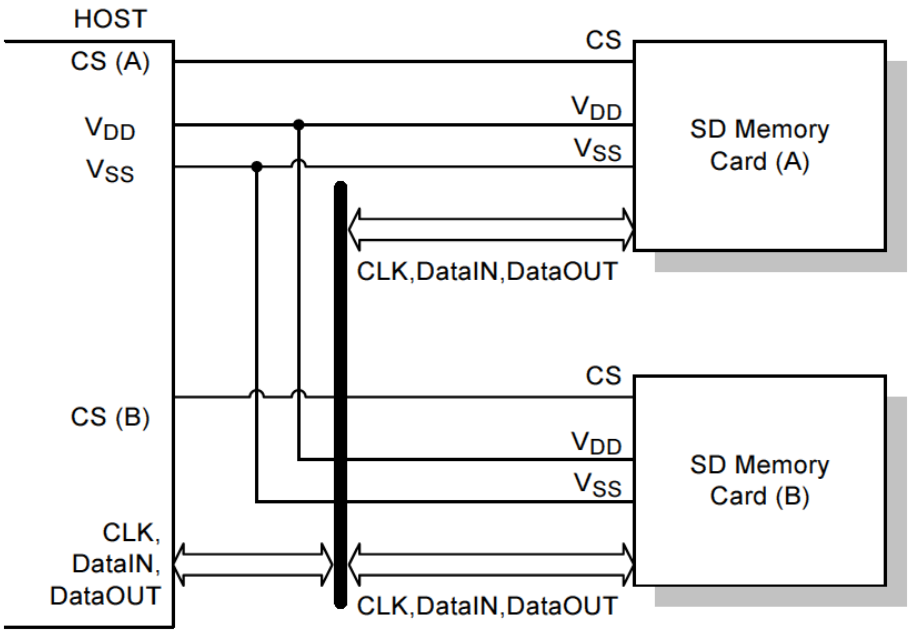

Figure.4: Bus connection Diagram (SPI Mode)

CS : Card Select Signal
CLK : Host card Clock signal
DataIN : Host to card data line
DataOUT : Host to card data line
V_{DD} : Power supply
V_{SS} : GND

Table.6: SPI Mode Command set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 and 9.2)
CMD6	SWITCH_FUNC	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	-	
ACMD25	SECURE_WRITE_MULTI_BLOCK	-	
ACMD26	SECURE_WRITE_MKB	-	
ACMD38	SECURE_ERASE	-	
ACMD43	GET_MKB	-	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	-	
ACMD46	SET_CER_RN2	-	
ACMD47	SET_CER_RES2	-	
ACMD48	SET_CER_RES1	-	
ACMD49	CHANGE_SECURE_AREA	-	

- CMD28, 29 and CMD30 are Optional Commands.
- CMD56 is for vendor specific command. Which is not defined in the standard card.

5.3 Initialization

Fig.5 shows initialization flow chart for UHS-I hosts and Fig.6 shows sequence of commands to perform signal voltage switch. Red and yellow boxes are new procedure to initialize UHS-I card.

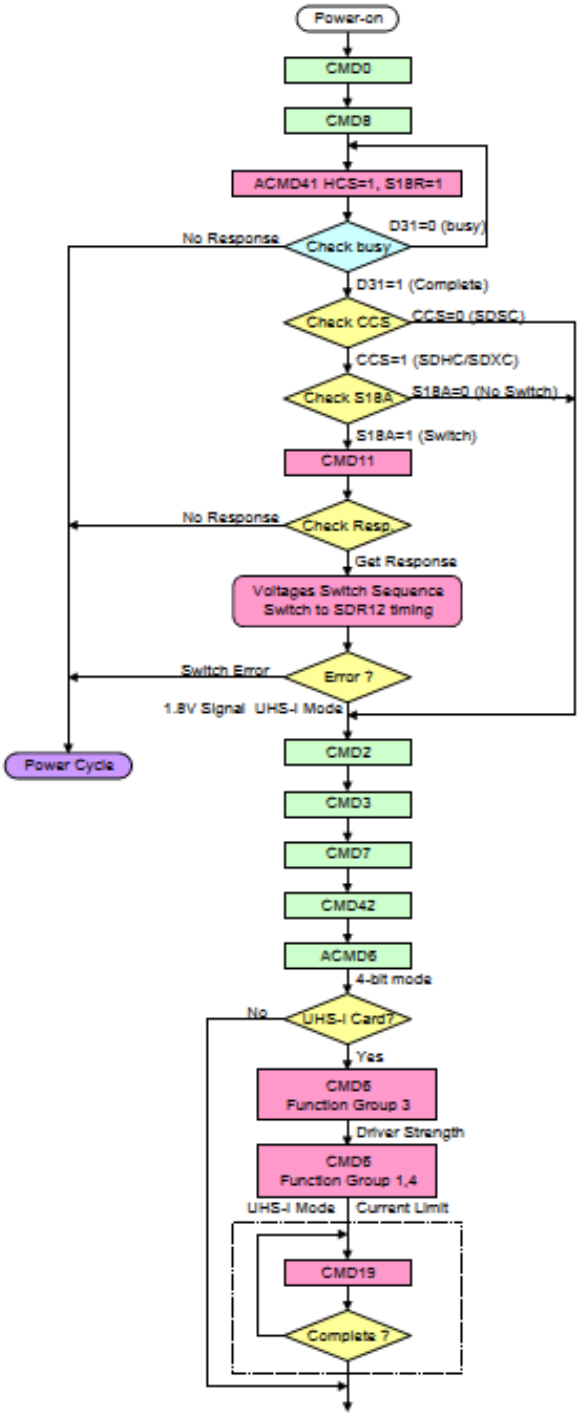

Figure 5: UHS-I Host Initialization Flow Diagram

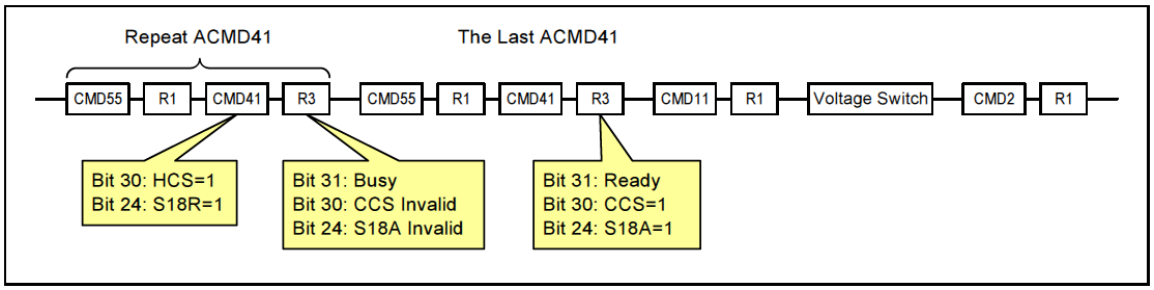

Figure 6: ACMD41 Timing Followed by Signal Voltage Switch Sequence

1) POWER ON: Supply Voltage for initialization.

Host System applies the Operating Voltage to the card.
Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to "Low" level. Then, issue CMD0.
In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to "High" normally).
Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send Interface condition command (CMD8).

When the card is in Idle state, the host shall issue CMD8 before ACMD41. In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument. If the card does not support the host supply voltage, it shall not return response and stays in Idle state.

4) Send initialization command (ACMD41).

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument. If Bit 31 indicates ready, host needs to check CCS and S18A.
The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 7: S18R and S18A Combination

Current Signal Level	S18R	S18A	Comments
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

5) Send voltage switch command (CMD11).

S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence. By receiving CMD11, the card returns R1 response and start voltage switch sequence. No response of CMD11 means that S18A was 0 and therefore host should not have sent CMD11. Completion of voltage switch sequence is checked by high level of DAT[3:0]. Any bit of DAT[3:0] can be checked depends on ability of the host. The card enters UHS-I mode and card input and output timings are

changed (SDR12 in default) when the voltage switch sequence is completed successfully.

6) Send ALL_SEND_CID command (CMD2) and get the Card ID (CID).

7) Send SEND_RELATIVE_ADDR (CMD3) and get the RCA.

RCA value is randomly changed by access, not equal zero.

8) Send SELECT / DESELECT_CARD command (CMD7) and move to the transfer state.

When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7).
If the CARD_IS_LOCKED status is set to 1 in the response of CMD7, CMD42 is required before ACMD6 to unlock the card. (If the card is locked, CMD42 is required to unlock the card.) If the card is unlocked, CMD42 can be skipped.

9) Send SET_BUS_WIDTH command (ACMD6).

UHS-I supports only 4-bit mode. Host shall select 4-bit mode by ACMD6.
If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.

10) Set driver strength.

CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current consumption of the card under the selected functions.
In case of UHS-I card, appropriate driver strength (default is Type-B buffer) is selected by CMD6 Function Group 3.

11) Set UHS-I mode current limit.

UHS-I modes (Bus Speed Mode) is selected by CMD6 Function Group 1.
Current Limit is selected by CMD6 Function Group 4.
Maximum access settings:
SDR104 = (CMD6 Function Group 1 = 3-h, CMD6 Function Group 4 = 0-h(*))
SDR50 = (CMD6 Function Group 1 = 2-h, CMD6 Function Group 4 = 0-h(*))
DDR50 = (CMD6 Function Group 1 = 4-h, CMD6 Function Group 4 = 0-h(*))
(*) The Current Limit is default value (200mA).

Note:

Function Group 4 is defined as Current Limit switch for SDR50, SDR104.
The Current Limit does not act on the card in SDR12 and SDR25.
The default value of the Current Limit is 200mA (minimum setting).
Then after selecting one of SDR50, SDR104 mode by Function Group 1, host needs to change the Current Limit to enable the card to operate in higher performance.
This value is determined by a host power supply capability to the card, heat release method taken by a host and the maximum current of a connector.

12) Tuning of sampling point

CMD19 sends a tuning block to the host to determine sampling point.
In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed
Then the Host can access the Data between the SD card as a storage device.

Application Notes:

1. The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.
2. Once signal voltage is switched to 1.8V, the card continues 1.8V signaling regardless of CMD0. Power cycle resets the signal voltage to 3.3V. After switching 1.8V singling, the card cannot be changed to SPI mode.
3. Timing to Switch Signal Voltage

To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Fig.8. CMD11 is issued only when S18A=1 in the response of ACMD41.

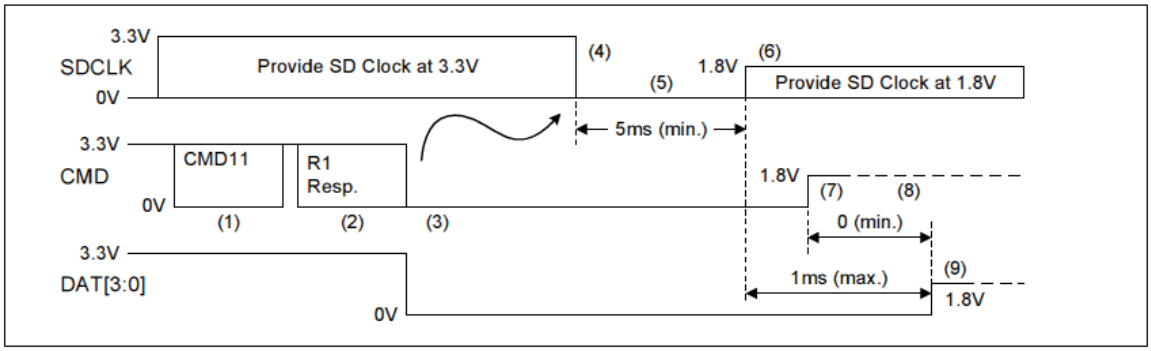

Figure 7: Signal Voltage Switch Sequence

(1) Host issues CMD11 to start voltage switch sequence.
(2) The card returns R1 response.
(3) The card drives CMD and DAT[3:0] to low immediately after the response.
(4) The host stops supplying SDCLK. The card shall start switching voltage after host stops SDCLK. The time to stop SDCLK is not specified. The host can detect whether the sequence starts by checking signal level of either one of CMD, DAT[3:0]. Which signal should be checked depends on ability of the host. If low level is not detected, the host should abort the sequence and execute power cycle.
(5) 1.8V output of voltage regulator in card shall be stable within 5ms. Host keeps SDCLK low at least 5ms. This means that 5ms is the maximum for the card and the minimum for the host.
(6) After 5ms from (4) and host voltage regulator is stable, the host starts providing SDCLK at 1.8V. The card can check whether SDCLK voltage is 1.8V.
(7) By detecting SDCLK, the card drives CMD to high at 1.8V at least one clock and then stop driving (tri-state).
CMD is triggered by rising edge of SDCLK (SDR timing).
(8) The card can check whether host drives CMD to 1.8V through the host pull-up resister.
(9) If switching to 1.8V signaling is completed successfully, the card drives DAT[3:0] to high at 1.8V at least one clock and then stop driving (tri-state). DAT[3:0] is triggered by rising edge of SDCLK (SDR timing). DAT[3:0] shall be high within 1ms from start of providing SDCLK. Host check whether DAT[3:0] is high after 1ms from supplying SDCLK. This means that 1ms is the maximum for the card and the minimum for the host.

5.4. SD Card Electrical Characteristics

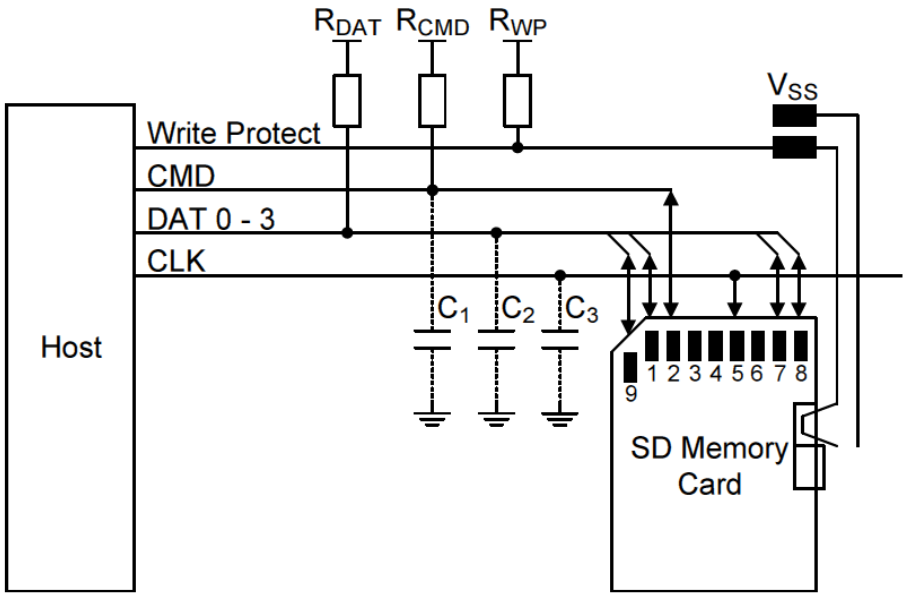

Figure 8: SD Card Connection Diagram

5.4.1 Bus Operating Conditions

Table 8: Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}	-	V	I_{OH}= -2mA V_{DD} min
Output Low Voltage	V_{OL}	-	0.125* V_{DD}	V	I_{OL}= 2mA V_{DD} min
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD} +0.3	V	
Input Low Voltage	V_{IL}	V_{IL}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

5.4.2 Peak Voltage and Leakage Current

Table 9: Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak Voltage on All Lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	µA	
All Outputs					
Output Leakage Current		-10	10	µA	

5.4.3 Current Consumption

The Current consumption is measured by averaging over 1 second.

- Before first command: Maximum 15mA
- During initialization: Maximum 100mA
- Operation in Default Speed Mode: Maximum 100 mA for SDSC and SDHC 100mA(XPC=0) or 150mA(XPC=1) for SDXC
- Operation in High Speed Mode: Maximum 200mA
- Operation in UHS-I Mode: Maximum 400mA(UHS50, DDR50) or 800mA(UHS104)
- Operation with other functions: Maximum 500mA.

Some functions can be added by CMD6 and SDIO(ex. McEX, ASSD and Combo Card). Host needs to select functions so that the total current of selected functions shall be up to 500mA. In case of UHS-I card, host should not select UHS-I mode and the other functions at the same time.

Table 10: Bus Operating Conditions – Signal Line's Load

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L	-	40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card capacitance for each signal pin	C_{CARD}	-	10	pF	
Maximum signal line inductance		-	16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KΩ	May be used for card detection
Capacity Connected to Power Line	C_C	-	5	µF	To prevent inrush current

5.4.4 AC Characteristics (Default)

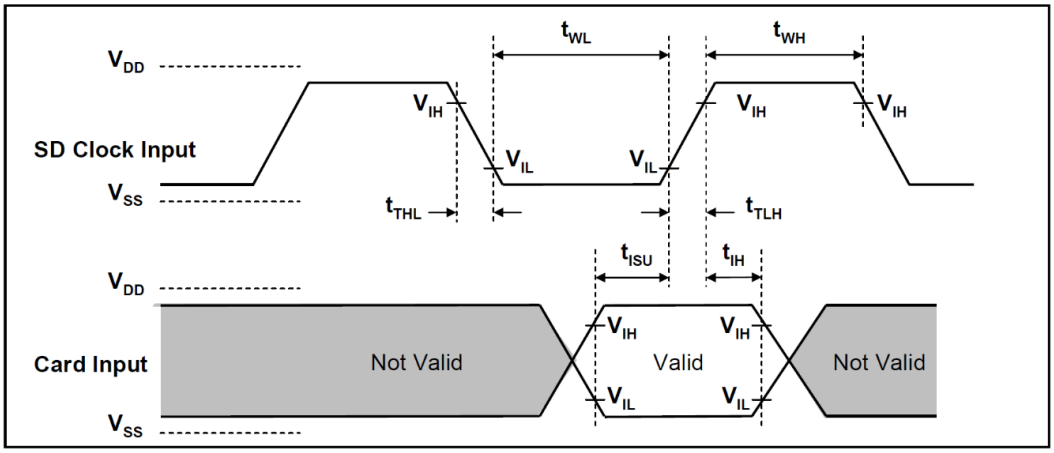

Figure 9: Card Input Timing (Default Speed Card)

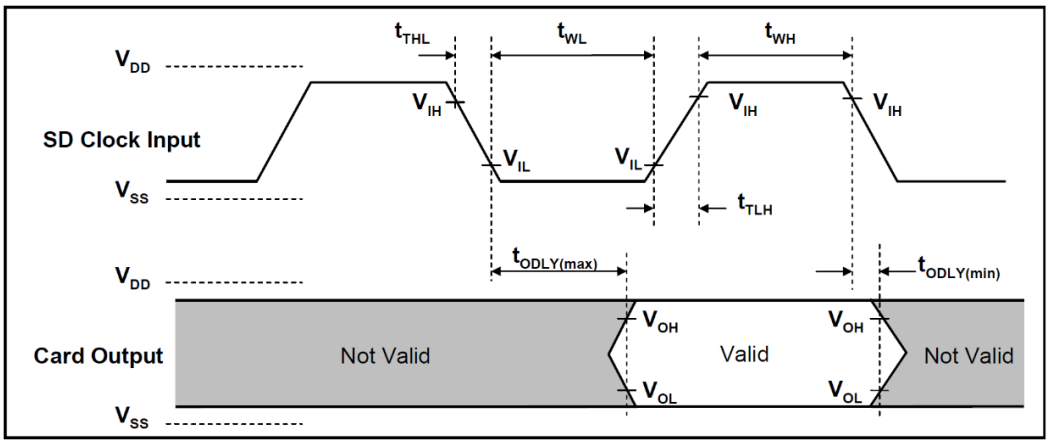

Figure 10: Card Output Timing (Default Speed Mode)

Table 11: AC Characteristics (Default Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_{CARD} \leq 10$ pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	$C_{CARD} \leq 10$ pF (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH}	5		ns	$C_{CARD} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 40$ pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leq 40$ pF (1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required (refer to Chapter 4.4- Clock Control).

5.4.5 AC Characteristics (High-Speed)

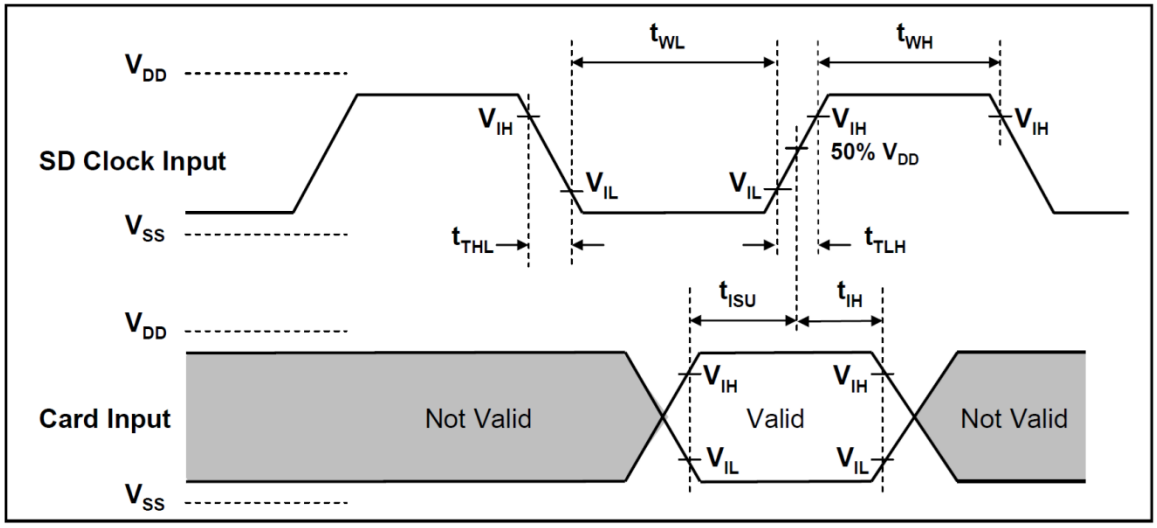

Figure 11: Card Input Timing (High Speed Mode)

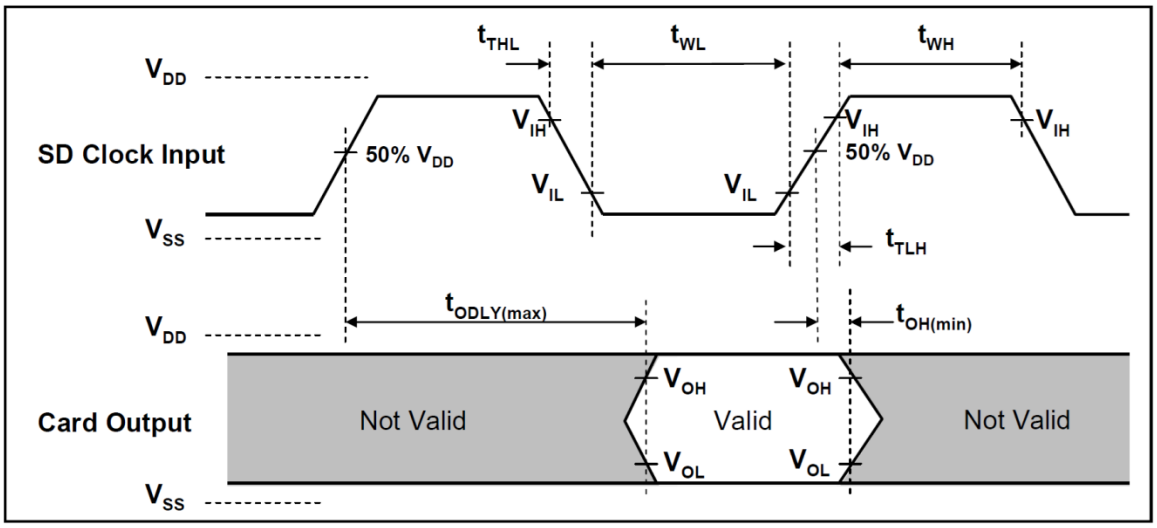

Figure 12: Card Output Timing (High Speed Mode)

Table 12: AC Characteristics (High Speed Mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L ≥ 15pF (1 card)
Total System capacitance for each line[1]	C_L		40	pF	1 card

1) In order to satisfy severe timing, host shall drive only one card.

5.4.6 AC Characteristics (Ultra High Speed; UHS104)

Bus Timing Specification <SDR104,SDR50,SDR25,SDR12>

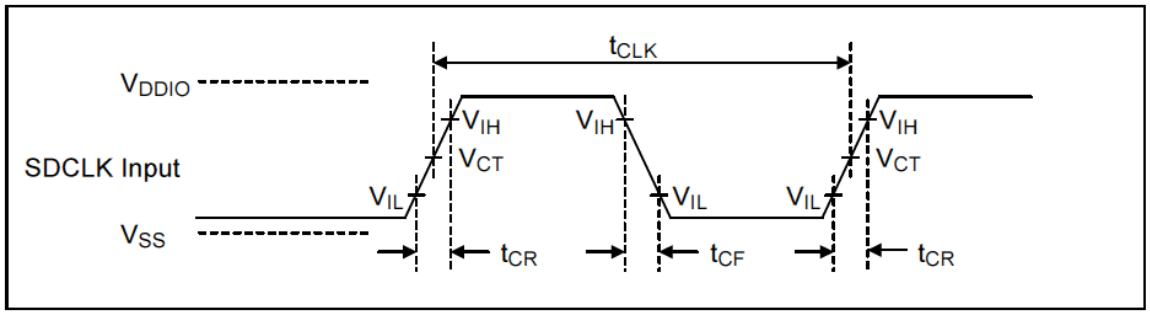

Figure 13: Clock Signal Timing

Table 13: Clock Signal Timing of SDR104, SDR50, SDR25, SDR12

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* tCLK	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF}, < 2.00ns (max.) at 100MHz, C_{CARD}=10pF
Clock Duty	30	70	%	

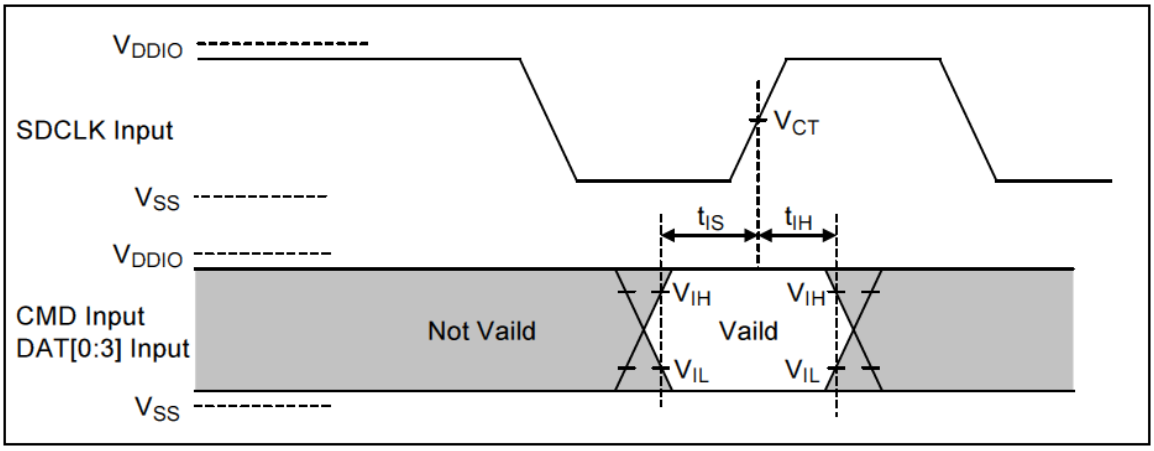

Figure 14: Card Input Timing

Table 14: SDR12, SDR25, SDR50 and SDR104 Input Timing

Symbol	Min.	Max.	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} =5pF, V_{CT}= 0.975V
Symbol	**Min.**	**Max.**	**Unit**	**SDR12, SDR25 and SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} =5pF, V_{CT}= 0.975V

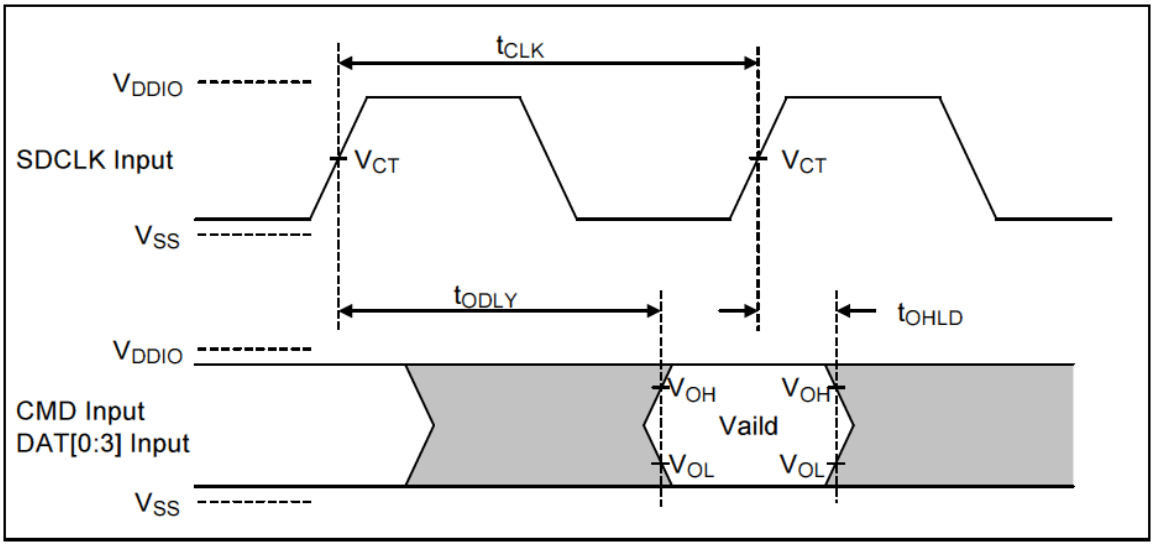

Figure 15: Output Timing of Fixed Data Window

Table 15: Output Timing of Fixed Data Window (SDR50, SDR25, SDR12)

Symbol	Min.	Max.	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}		14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
t_{OH}	1.5	-	ns	Hold time at the $t_{ODLY\ (min.)}$, C_L=15pF

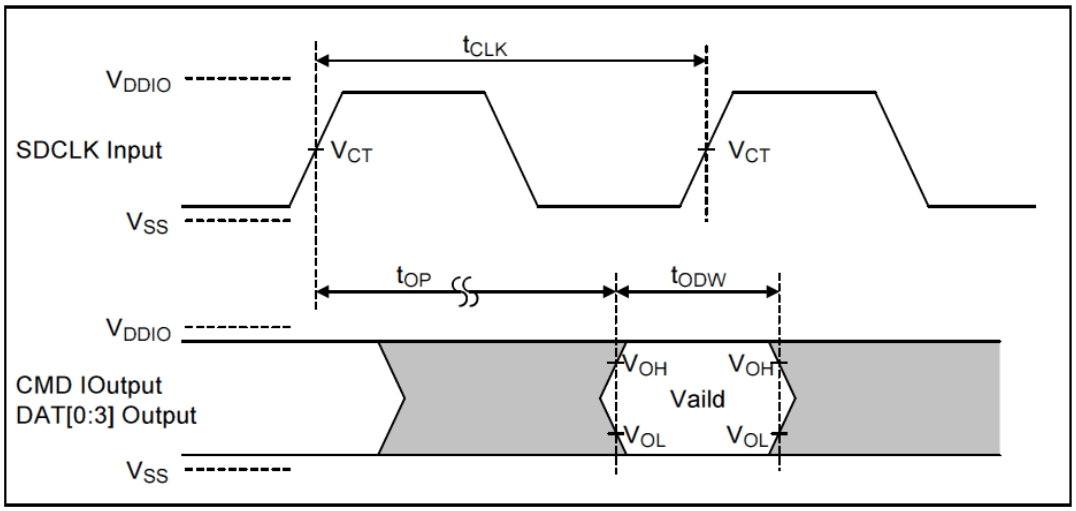

Figure 16: Output Timing of Variable Data Window

Table 16: Output Timing of Variable Data Window (SDR104)

Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW}=2.88ns at 208MHz

Card Δt_{OP} is the total allowable shift of output valid window (t_{ODW}) from last system Tuning procedure.
Card Δt_{OP} =1550pS for junction temperature of ΔT= 90°C during operation.
Card Δt_{OP} =-350pS for junction temperature of ΔT= -20°C during operation.

Bus Timing Specification <DDR50>

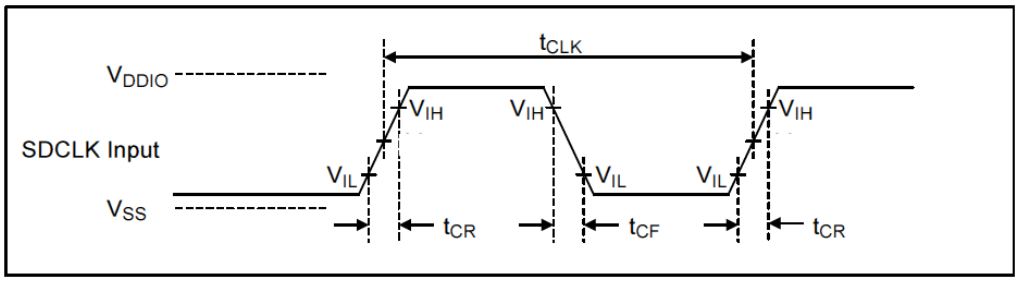

Fig.17: Clock Signal Timing

Table 17: Clock Signal Timing of DDR50

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF}, < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

CMD signal timings are not shown in Figure 17. For CMD signal timing refers to Figure 14 and Figure 15 (Timing Diagram of SDR mode).

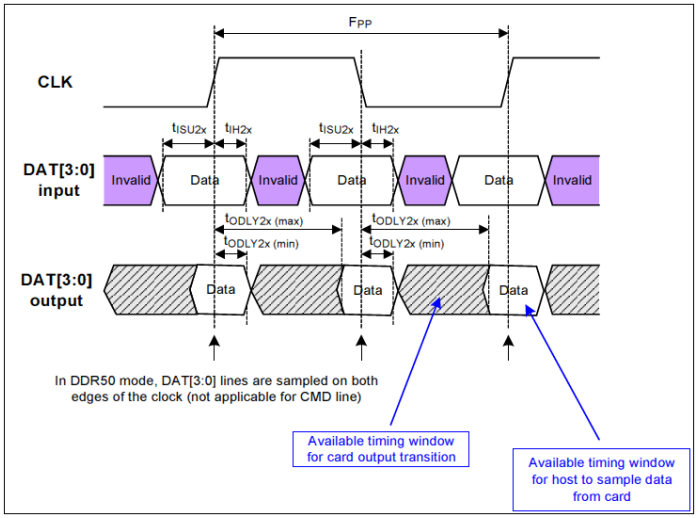

Fig.18 Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 18: BUS Timings – Parameters Values (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time (*)	t_{ISU}	3	-	ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} ≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L ≤ 30 pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L ≥ 15pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} ≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L ≤ 25 pF (1 card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_L ≥ 15pF (1 card)

(*) Input set-up time : t_{ISU}(min) is 6ns in PHYSICAL LAYER SPECIFICATION Ver.6.10

Appendix: SD Card Mechanical Dimensions (Unit: mm)